bq40z50 1-Series, 2-Series, 3-Series, and 4-Series Li-Ion Battery Pack Manager

1 Features

- Fully Integrated 1-Series, 2-Series, 3-Series, and 4-Series Li-Ion or Li-Polymer Cell Battery Pack Manager and Protection
- Next-Generation Patented Impedance Track™ Technology Accurately Measures Available Charge in Li-Ion and Li-Polymer Batteries
- High Side N-CH Protection FET Drive
- Integrated Cell Balancing While Charging or At Rest
- Full Array of Programmable Protection Features
  - Voltage
  - Current
  - Temperature
  - Charge Timeout
  - CHG/DSG FETs
  - AFE
- Sophisticated Charge Algorithms
  - JEITA
  - Enhanced Charging
  - Adaptive Charging
  - Cell Balancing
- Supports TURBO BOOST Mode
- Supports Battery Trip Point (BTP)
- Diagnostic Lifetime Data Monitor and Black Box Recorder
- LED Display
- Supports Two-Wire SMBus v1.1 Interface
- SHA-1 Authentication
- Compact Package: 32-Lead QFN (RSM)

2 Applications

- Notebook/Netbook PCs
- Medical and Test Equipment
- Portable Instrumentation

3 Description

The bq40z50 device, incorporating patented Impedance Track™ technology, is a fully integrated, single-chip, pack-based solution that provides a rich array of features for gas gauging, protection, and authentication for 1-series, 2-series, 3-series, and 4-series cell Li-Ion and Li-Polymer battery packs.

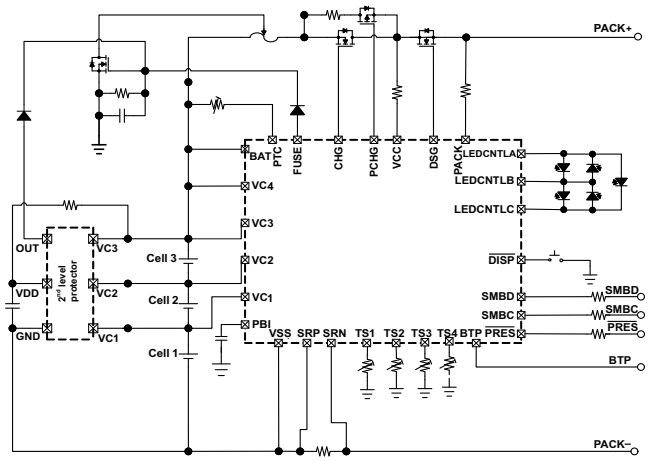
Using its integrated high-performance analog peripherals, the bq40z50 device measures and maintains an accurate record of available capacity, voltage, current, temperature, and other critical parameters in Li-Ion or Li-Polymer batteries, and reports this information to the system host controller over an SMBus v1.1 compatible interface.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
bq40z50	VQFN (32)	4.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic



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4 Revision History

Changes from Original (December 2013) to Revision A **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Added Feature: Supports TURBO BOOST Mode ... 1
- Added Feature: Supports Battery Trip Point (BTP) ... 1
- Changed a Feature bullet from "Diagnostic Lifetime Data Monitor" to "Diagnostic Lifetime Data Monitor and Black Box Recorder" ... 1
- Updated second paragraph of the Description. Added text "The bq40z50 device supports TURBO BOOST mode . . . "... 3

5 Description (continued)

The bq40z50 device supports TURBO BOOST mode by providing the available max power and max current to the host system. The device also supports Battery Trip Point to send a BTP interrupt signal to the host system at the pre-set state of charge thresholds.

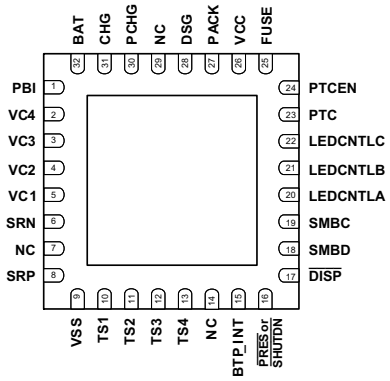
The bq40z50 provides software-based 1st- and 2nd-level safety protection against overvoltage, undervoltage, overcurrent, short-circuit current, overload, and overtemperature conditions, as well as other pack- and cell-related faults.

SHA-1 authentication, with secure memory for authentication keys, enables identification of genuine battery packs.

The compact 32-lead QFN package minimizes solution cost and size for smart batteries while providing maximum functionality and safety for battery gauging applications.

6 Pin Configuration and Functions

RSM Package
32-Pin VQFN with Exposed Thermal Pad
Top View



Pin Functions

PIN NAME	PIN NUMBER	TYPE(1)	DESCRIPTION
PBI	1	P	Power supply backup input pin
VC4	2	IA	Sense voltage input pin for most positive cell, and balance current input for most positive cell
VC3	3	IA	Sense voltage input pin for second most positive cell, balance current input for second most positive cell, and return balance current for most positive cell
VC2	4	IA	Sense voltage input pin for third most positive cell, balance current input for third most positive cell, and return balance current for second most positive cell
VC1	5	IA	Sense voltage input pin for least positive cell, balance current input for least positive cell, and return balance current for third most positive cell
SRN	6	I	Analog input pin connected to the internal coulomb counter peripheral for integrating a small voltage between SRP and SRN where SRP is the top of the sense resistor.
NC	7	—	Not internally connected. Connect to VSS.
SRP	8	I	Analog input pin connected to the internal coulomb counter peripheral for integrating a small voltage between SRP and SRN where SRP is the top of the sense resistor.
VSS	9	P	Device ground
TS1	10	IA	Temperature sensor 1 thermistor input pin
TS2	11	IA	Temperature sensor 2 thermistor input pin
TS3	12	IA	Temperature sensor 3 thermistor input pin
TS4	13	IA	Temperature sensor 4 thermistor input pin
NC	14	—	Not internally connected

(1) P = Power Connection, O = Digital Output, AI = Analog Input, I = Digital Input, I/OD = Digital Input/Output

Pin Functions (continued)

PIN NAME	PIN NUMBER	TYPE(1)	DESCRIPTION
BTP_INT	15	O	Battery Trip Point (BTP) interrupt output
$\overline{\text{PRES}}$ or $\overline{\text{SHUTDN}}$	16	I	Host system present input for removable battery pack or emergency system shutdown input for embedded pack
$\overline{\text{DISP}}$	17	—	Display control for LEDs
SMBD	18	I/OD	SMBus data pin
SMBC	19	I/OD	SMBus clock pin
LEDCNTLA	20	—	LED display segment that drives the external LEDs depending on the firmware configuration
LEDCNTLB	21	—	LED display segment that drives the external LEDs depending on the firmware configuration
LEDCNTLC	22	—	LED display segment that drives the external LEDs depending on the firmware configuration
PTC	23	IA	Safety PTC thermistor input pin. To disable, connect both PTC and PTCEN to VSS.
PTCEN	24	IA	Safety PTC thermistor enable input pin. Connect to BAT. To disable, connect both PTC and PTCEN to VSS.
FUSE	25	O	Fuse drive output pin
VCC	26	P	Secondary power supply input
PACK	27	IA	Pack sense input pin
DSG	28	O	NMOS Discharge FET drive output pin
NC	29	—	Not internally connected
PCHG	30	O	PMOS Precharge FET drive output pin
CHG	31	O	NMOS Charge FET drive output pin
BAT	32	P	Primary power supply input pin

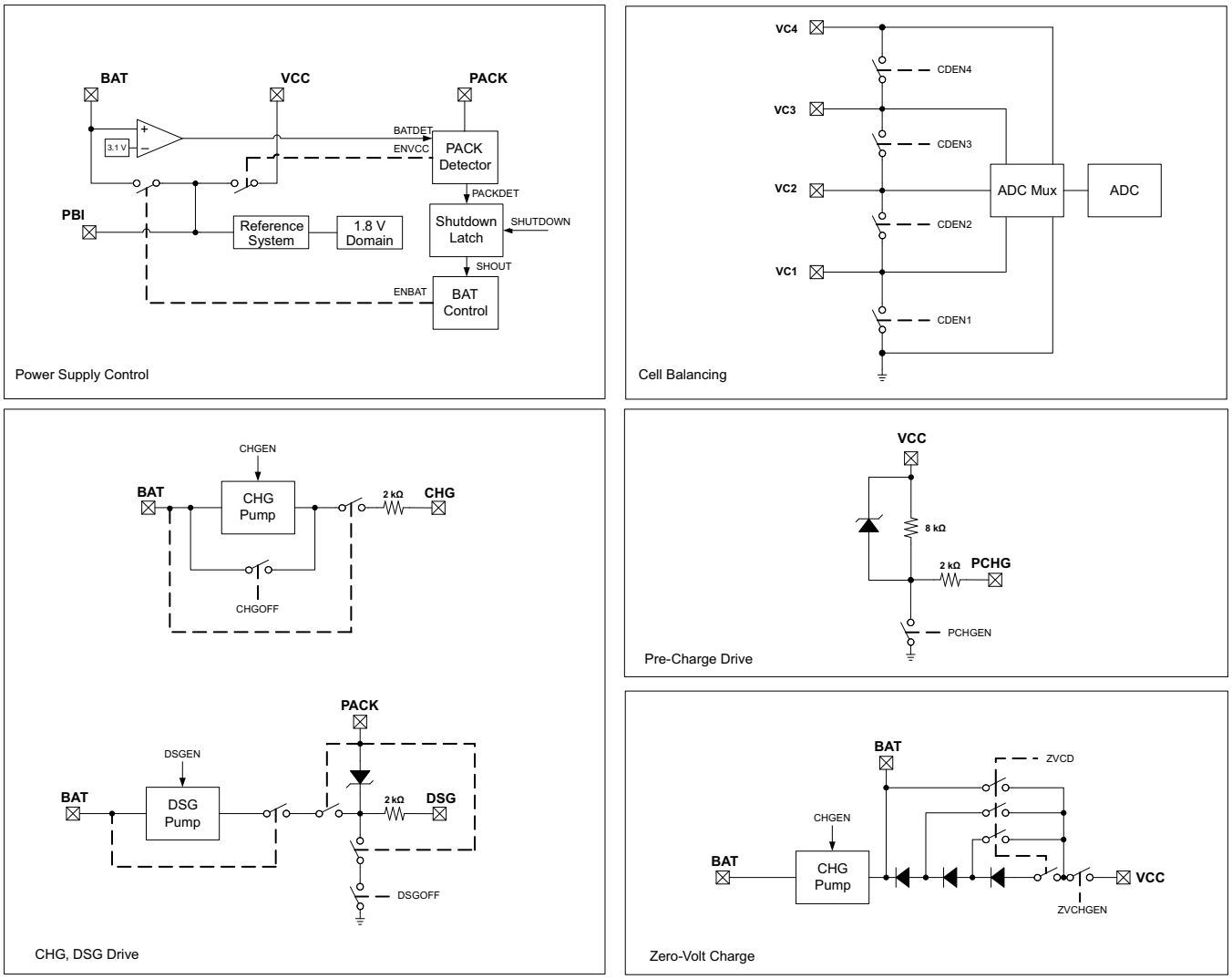


Figure 1. Pin Equivalent Diagram 1

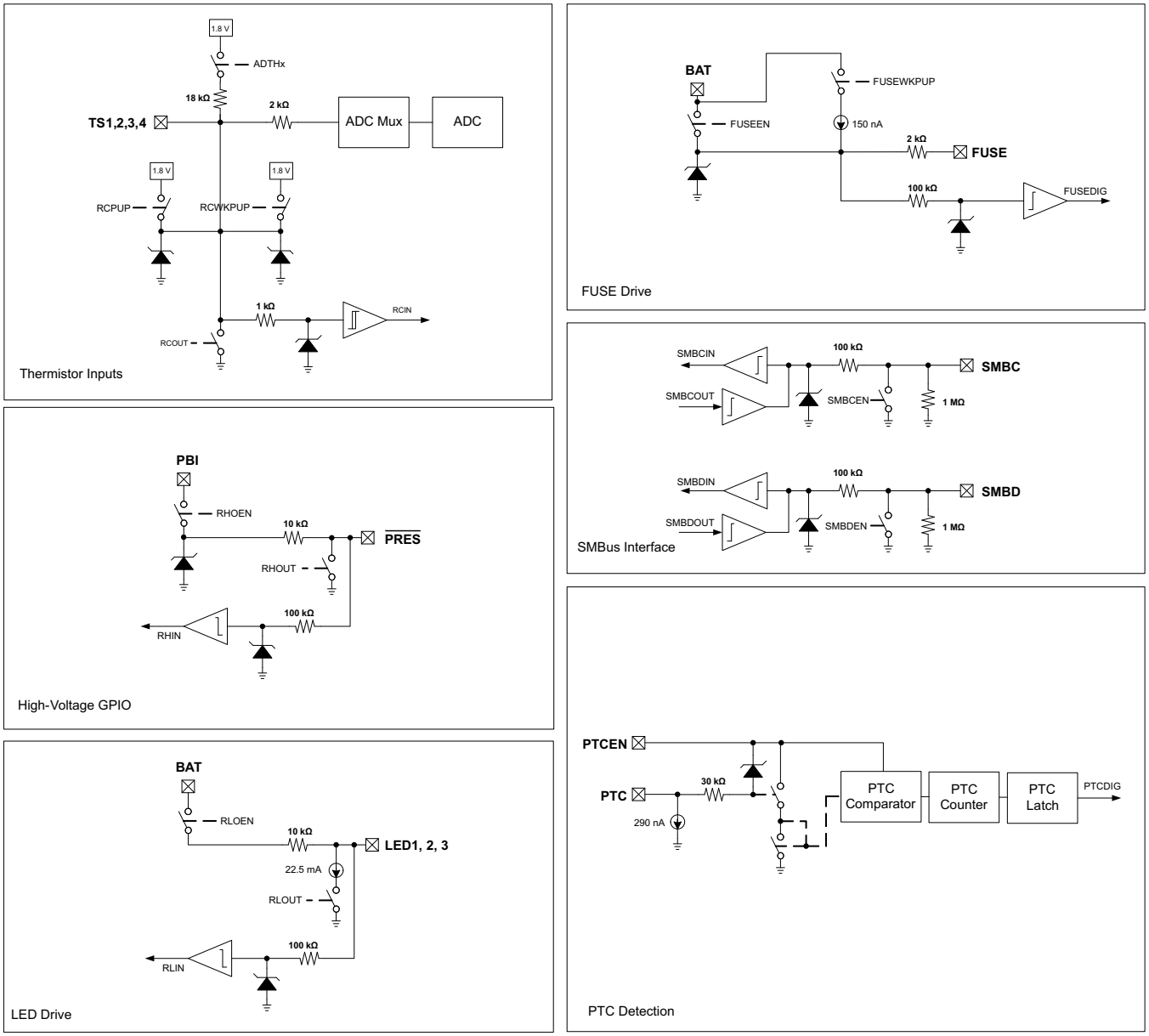


Figure 2. Pin Equivalent Diagram 2

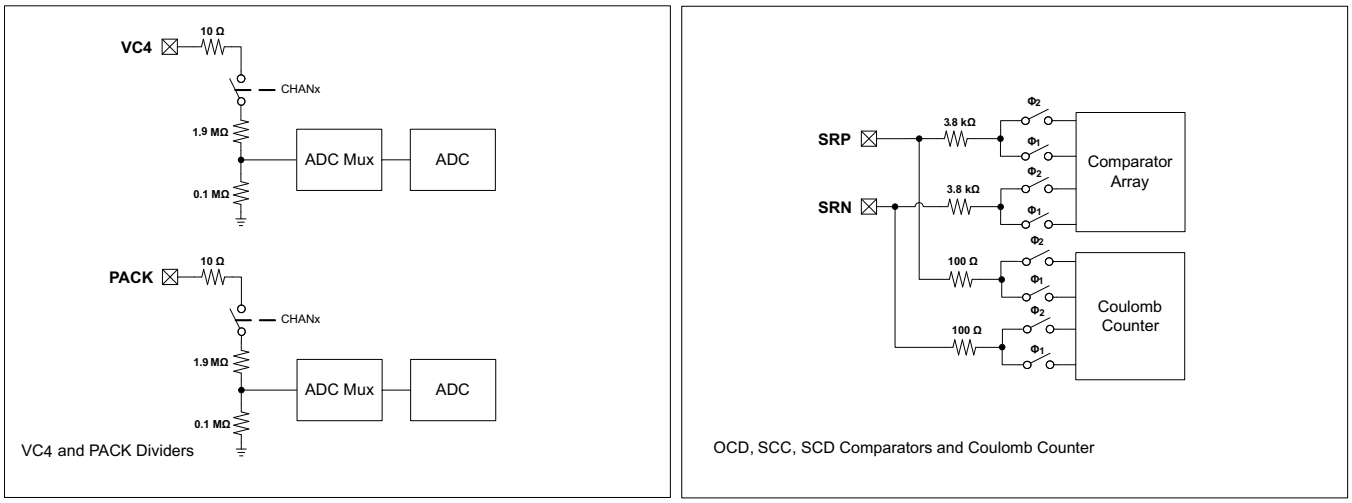


Figure 3. Pin Equivalent Diagram 3

7 Specifications

7.1 Absolute Maximum Ratings

Over-operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage range, V_{CC}	BAT, VCC, PBI	–0.3	30	V
Input voltage range, V_{IN}	PACK, SMBC, SMBD, $\overline{PRES}$ or $\overline{SHUTDN}$, BTP_INT, $\overline{DISP}$	–0.3	30	V
	TS1, TS2, TS3, TS4	–0.3	V_{REG} + 0.3	V
	PTC, PTCEN, LEDCNTLA, LEDCNTLB, LEDCNTLC	–0.3	V_{BAT} + 0.3	V
	SRP, SRN	–0.3	0.3	V
	VC4	VC3 – 0.3	VC3 + 8.5 V, or VSS + 30	V
	VC3	VC2 – 0.3	VC2 + 8.5 V, or VSS + 30	V
	VC2	VC1 – 0.3	VC1 + 8.5 V, or VSS + 30	V
	VC1	VSS – 0.3	VSS + 8.5 V, or VSS + 30 V	V
Output voltage range, V_O	CHG, DSG	–0.3	32	
	PCHG, FUSE	–0.3	30	V
Maximum VSS current, I_{SS}			50	mA
T_{STG}	Storage temperature	–65	150	°C
Lead temperature (soldering, 10 s), T_{SOLDER}			300	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Typical values stated where T_A = 25°C and VCC = 14.4 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	BAT, VCC, PBI	2.2		26	V
$V_{SHUTDOWN-}$	Shutdown voltage	$V_{PACK} < V_{SHUTDOWN-}$	1.8	2.0	2.2	V
$V_{SHUTDOWN+}$	Start-up voltage	$V_{PACK} > V_{SHUTDOWN-} + V_{HYS}$	2.05	2.25	2.45	V
V_{HYS}	Shutdown voltage hysteresis	$V_{SHUTDOWN+} – V_{SHUTDOWN-}$		250		mV
V_{IN}	Input voltage range	PACK, SMBC, SMBD , $\overline{PRES}$, BTP_IN, $\overline{DISP}$			26	V
		TS1, TS2, TS3, TS4			V_{REG}	
		PTC, PTCEN, LEDCNTLA, LEDCNTLB, LEDCNTLC			V_{BAT}	
		SRP, SRN	–0.2		0.2	
		VC4	V_{VC3}		V_{VC3} + 5	
		VC3	V_{VC2}		V_{VC2} + 5	
		VC2	V_{VC1}		V_{VC1} + 5	
		VC1	V_{VSS}		V_{VSS} + 5	
V_O	Output voltage range	CHG, DSG, PCHG, FUSE			26	V
C_{PBI}	External PBI capacitor		2.2			µF
T_{OPR}	Operating temperature		–40		85	°C

7.4 Thermal Information

THERMAL METRIC(1)		RSM (QFN) 32 PINS	UNIT
$R_{\theta JA, High K}$	Junction-to-ambient thermal resistance(2)	47.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance(3)	40.3	
$R_{\theta JB}$	Junction-to-board thermal resistance(4)	14.7	
ψ_{JT}	Junction-to-top characterization parameter(5)	0.8	
ψ_{JB}	Junction-to-board characterization parameter(6)	14.4	
$R_{\theta JC(bottom)}$	Junction-to-case(bottom) thermal resistance(7)	3.8	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

7.5 Electrical Characteristics: Supply Current

Typical values stated where T_A = 25°C and VCC = 14.4 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 20 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{NORMAL}	NORMAL mode	CHG on. DSG on, no Flash write		336		µA
I_{SLEEP}	SLEEP mode	CHG off, DSG on, no SBS communication		75		µA
		CHG off, DSG off, no SBS communication		52		
$I_{SHUTDOWN}$	SHUTDOWN mode			1.6		µA

7.6 Electrical Characteristics: Power Supply Control

Typical values stated where T_A = 25°C and VCC = 14.4 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{SWITCHOVER-}$	BAT to V_{CC} switchover voltage	$V_{BAT} < V_{SWITCHOVER-}$	1.95	2.1	2.2	V
$V_{SWITCHOVER+}$	V_{CC} to BAT switchover voltage	$V_{BAT} > V_{SWITCHOVER-} + V_{HYS}$	2.9	3.1	3.25	V
V_{HYS}	Switchover voltage hysteresis	$V_{SWITCHOVER+} – V_{SWITCHOVER-}$		1000		mV
I_{LKG}	Input Leakage current	BAT pin, BAT = 0 V, VCC = 25 V, PACK = 25 V			1	µA
		PACK pin, BAT = 25 V, VCC = 0 V, PACK = 0 V			1	
		BAT and PACK terminals, BAT = 0 V, VCC = 0 V, PACK = 0 V, PBI = 25 V			1	
R_{PD}	Internal pulldown resistance	PACK	30	40	50	kΩ

7.7 Electrical Characteristics: AFE Power-On Reset

Typical values stated where T_A = 25°C and VCC = 14.4 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{REGIT-}	Negative-going voltage input	V_{REG}	1.51	1.55	1.59	V
V_{HYS}	Power-on reset hysteresis	$V_{REGIT+} – V_{REGIT-}$	70	100	130	mV
t_{RST}	Power-on reset time		200	300	400	µs

7.8 Electrical Characteristics: AFE Watchdog Reset and Wake Timer

Typical values stated where T_A = 25°C and VCC = 14.4 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{WDT}	AFE watchdog timeout	t_{WDT} = 500	372	500	628	ms
		t_{WDT} = 1000	744	1000	1256	
		t_{WDT} = 2000	1488	2000	2512	
		t_{WDT} = 4000	2976	4000	5024	
t_{WAKE}	AFE wake timer	t_{WAKE} = 250	186	250	314	ms
		t_{WAKE} = 500	372	500	628	
		t_{WAKE} = 1000	744	1000	1256	
		t_{WAKE} = 512	1488	2000	2512	
t_{FETOFF}	FET off delay after reset	t_{FETOFF} = 512	409	512	614	ms

7.9 Electrical Characteristics: Current Wake Comparator

Typical values stated where T_A = 25°C and VCC = 14.4 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{WAKE}	Wake voltage threshold	V_{WAKE} = ±0.625 mV	±0.3	±0.625	±0.9	mV
		V_{WAKE} = ±1.25 mV	±0.6	±1.25	±1.8	
		V_{WAKE} = ±2.5 mV	±1.2	±2.5	±3.6	
		V_{WAKE} = ±5 mV	±2.4	±5.0	±7.2	
$V_{WAKE(DRIFT)}$	Temperature drift of V_{WAKE} accuracy			0.5%		°C
t_{WAKE}	Time from application of current to wake interrupt				700	µs
$t_{WAKE(SU)}$	Wake comparator startup time			500	1000	µs

7.10 Electrical Characteristics: VC1, VC2, VC3, VC4, BAT, PACK

Typical values stated where T_A = 25°C and VCC = 14.4 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
K	Scaling factor	VC1–VSS, VC2–VC1, VC3–VC2, VC4–VC3	0.1980	0.2000	0.2020	—
		BAT–VSS, PACK–VSS	0.049	0.050	0.051	
		V_{REF2}	0.490	0.500	0.510	
V_{IN}	Input voltage range	VC1–VSS, VC2–VC1, VC3–VC2, VC4–VC3	–0.2		5	V
		BAT–VSS, PACK–VSS	–0.2		20	
I_{LKG}	Input leakage current	VC1, VC2, VC3, VC4, cell balancing off, cell detach detection off, ADC multiplexer off			1	µA
R_{CB}	Internal cell balance resistance	$R_{DS(ON)}$ for internal FET switch at 2 V < V_{DS} < 4 V			200	Ω
I_{CD}	Internal cell detach check current	VCx > VSS + 0.8 V	30	50	70	µA

7.11 Electrical Characteristics: SMBD, SMBC

Typical values stated where T_A = 25°C and VCC = 14.4 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	Input voltage high	SMBC, SMBD, V_{REG} = 1.8 V	1.3			V
V_{IL}	Input voltage low	SMBC, SMBD, V_{REG} = 1.8 V			0.8	V
V_{OL}	Output low voltage	SMBC, SMBD, V_{REG} = 1.8 V, I_{OL} = 1.5 mA			0.4	V
C_{IN}	Input capacitance			5		pF
I_{LKG}	Input leakage current				1	µA
R_{PD}	Pulldown resistance		0.7	1.0	1.3	MΩ

7.12 Electrical Characteristics: $\overline{PRES}$, BTP_INT, $\overline{DISP}$

Typical values stated where T_A = 25°C and VCC = 14.4 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input		1.3			V
V_{IL}	Low-level input				0.55	V
V_{OH}	Output voltage high	V_{BAT} > 5.5 V, I_{OH} = –0 µA	3.5			V
		V_{BAT} > 5.5 V, I_{OH} = –10 µA	1.8			

Electrical Characteristics: $\overline{PRES}$, BTP_INT, $\overline{DISP}$ (continued)

Typical values stated where T_A = 25°C and VCC = 14.4 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OL}	Output voltage low	I_{OL} = 1.5 mA			0.4	V
C_{IN}	Input capacitance			5		pF
I_{LKG}	Input leakage current				1	µA
R_O	Output reverse resistance	Between $\overline{PRES}$ or BTP_INT or $\overline{DISP}$ and PBI	8			kΩ

7.13 Electrical Characteristics: LEDCNTLA, LEDCNTLB, LEDCNTLC

Typical values stated where T_A = 25°C and VCC = 14.4 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input		1.45			V
V_{IL}	Low-level input				0.55	V
V_{OH}	Output voltage high	V_{BAT} > 3.0 V, I_{OH} = –22.5 mA	V_{BAT} – 1.6			V
V_{OL}	Output voltage low	I_{OL} = 1.5 mA			0.4	V
I_{SC}	High level output current protection		–30	–45	–6 0	mA
I_{OL}	Low level output current	V_{BAT} > 3.0 V, V_{OH} = 0.4 V	15.75	22.5	29.25	mA
$I_{LEDCNTLx}$	Current matching between LEDCNTLx	V_{BAT} = $V_{LEDCNTLx}$ + 2.5 V		±1%		
C_{IN}	Input capacitance			20		pF
I_{LKG}	Input leakage current				1	µA
$f_{LEDCNTLx}$	Frequency of LED pattern			124		Hz

7.14 Electrical Characteristics: Coulomb Counter

Typical values stated where T_A = 25°C and VCC = 14.4 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage range		–0.1		0.1	V
Full scale range		$–V_{REF1}/10$		$V_{REF1}/10$	V
Integral nonlinearity(1)	16-bit, best fit over input voltage range		±5.2	±22.3	LSB
Offset error	16-bit, Post-calibration		±5	±10	µV
Offset error drift	15-bit + sign, Post-calibration		0.2	0.3	µV/°C
Gain error	15-bit + sign, over input voltage range		±0.2%	±0.8%	FSR
Gain error drift	15-bit + sign, over input voltage range			150	PPM/°C
Effective input resistance		2.5			MΩ

(1) 1 LSB = $V_{REF1}/(10 \times 2^N)$ = 1.215/(10 × 2^{15}) = 3.71 µV

7.15 Electrical Characteristics: CC Digital Filter

Typical values stated where T_A = 25°C and VCC = 14.4 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Conversion time	Single conversion		250		ms
Effective resolution	Single conversion	15			Bits

7.16 Electrical Characteristics: ADC

Typical values stated where T_A = 25°C and VCC = 14.4 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage range	Internal reference (V_{REF1})	–0.2		1	V
	External reference (V_{REG})	–0.2		0.8 x V_{REG}	
Full scale range	V_{FS} = V_{REF1} or V_{REG}	–V_{FS}		V_{FS}	V
Integral nonlinearity(1)	16-bit, best fit, –0.1 V to 0.8 x V_{REF1}			±6.6	LSB
	16-bit, best fit, –0.2 V to –0.1 V			±13.1	
Offset error(2)	16-bit, Post-calibration, V_{FS} = V_{REF1}		±67	±157	µV
Offset error drift	16-bit, Post-calibration, V_{FS} = V_{REF1}		0.6	3	µV/°C
Gain error	16-bit, –0.1 V to 0.8 x V_{FS}		±0.2%	±0.8%	FSR
Gain error drift	16-bit, –0.1 V to 0.8 x V_{FS}			150	PPM/°C
Effective input resistance		8			MΩ

(1) 1 LSB = $V_{REF1}/(2^N)$ = 1.225/(2^{15}) = 37.4 µV (when t_{CONV} = 31.25 ms)
(2) For VC1–VSS, VC2–VC1, VC3–VC2, VC4–VC3, VC4–VSS, PACK–VSS, and V_{REF1}/2, the offset error is multiplied by (1/ADC multiplexer scaling factor (K)).

7.17 Electrical Characteristics: ADC Digital Filter

Typical values stated where T_A = 25°C and VCC = 14.4 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Conversion time	Single conversion		31.25		ms
	Single conversion		15.63		
	Single conversion		7.81		
	Single conversion		1.95		
Resolution	No missing codes	16			Bits
Effective resolution	With sign, t_{CONV} = 31.25 ms	14	15		Bits
	With sign, t_{CONV} = 15.63 ms	13	14		
	With sign, t_{CONV} = 7.81 ms	11	12		
	With sign, t_{CONV} = 1.95 ms	9	10		

7.18 Electrical Characteristics: CHG, DSG FET Drive

Typical values stated where T_A = 25°C and VCC = 14.4 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Output voltage ratio	$Ratio_{DSG}$ = (V_{DSG} – V_{BAT})/V_{BAT}, 2.2 V < V_{BAT} < 4.92 V, 10 MΩ between PACK and DSG	2.133	2.333	2.433	—
		$Ratio_{CHG}$ = (V_{CHG} – V_{BAT})/V_{BAT}, 2.2 V < V_{BAT} < 4.92 V, 10 MΩ between BAT and CHG	2.133	2.333	2.433	
$V_{(FETON)}$	Output voltage, CHG and DSG on	$V_{DSG(ON)}$ = V_{DSG} – V_{BAT}, V_{BAT} ≥ 4.92 V, 10 MΩ between PACK and DSG, V_{BAT} = 18 V	10.5	11.5	12	V
		$V_{CHG(ON)}$ = V_{CHG} – V_{BAT}, V_{BAT} ≥ 4.92 V, 10 MΩ between BAT and CHG, V_{BAT} = 18 V	10.5	11.5	12	
$V_{(FETOFF)}$	Output voltage, CHG and DSG off	$V_{DSG(OFF)}$ = V_{DSG} – V_{PACK}, 10 MΩ between PACK and DSG	–0.4		0.4	V
		$V_{CHG(OFF)}$ = V_{CHG} – V_{BAT}, 10 MΩ between BAT and CHG	–0.4		0.4	
t_R	Rise time	V_{DSG} from 0% to 35% $V_{DSG(ON)(TYP)}$, V_{BAT} ≥ 2.2 V, C_L = 4.7 nF between DSG and PACK, 5.1 kΩ between DSG and C_L, 10 MΩ between PACK and DSG		200	500	µs
		V_{CHG} from 0% to 35% $V_{CHG(ON)(TYP)}$, V_{BAT} ≥ 2.2 V, C_L = 4.7 nF between CHG and BAT, 5.1 kΩ between CHG and C_L, 10 MΩ between BAT and CHG		200	500	

Electrical Characteristics: CHG, DSG FET Drive (continued)

Typical values stated where T_A = 25°C and VCC = 14.4 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_F	Fall time	V_{DSG} from $V_{DSG(ON)(TYP)}$ to 1 V, V_{BAT} ≥ 2.2 V, C_L = 4.7 nF between DSG and PACK, 5.1 kΩ between DSG and C_L, 10 MΩ between PACK and DSG		40	300	µs
		V_{CHG} from $V_{CHG(ON)(TYP)}$ to 1 V, V_{BAT} ≥ 2.2 V, C_L = 4.7 nF between CHG and BAT, 5.1 kΩ between CHG and C_L, 10 MΩ between BAT and CHG		40	200	

7.19 Electrical Characteristics: PCHG FET Drive

Typical values stated where T_A = 25°C and VCC = 14.4 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(FETON)}$	Output voltage, PCHG on	$V_{PCHG(ON)}$ = VV_{CC} – V_{PCHG}, 10 MΩ between V_{CC} and PCHG	6	7	8	V
$V_{(FETOFF)}$	Output voltage, PCHG off	$V_{PCHG(OFF)}$ = VV_{CC} – V_{PCHG}, 10 MΩ between V_{CC} and PCHG	–0.4		0.4	V
t_R	Rise time	V_{PCHG} from 10% to 90% $V_{PCHG(ON)(TYP)}$, VV_{CC} ≥ 8 V, C_L = 4.7 nF between PCHG and V_{CC}, 5.1 kΩ between PCHG and C_L, 10 MΩ between V_{CC} and CHG		40	200	µs
t_F	Fall time	V_{PCHG} from 90% to 10% $V_{PCHG(ON)(TYP)}$, V_{CC} ≥ 8 V, C_L = 4.7 nF between PCHG and V_{CC}, 5.1 kΩ between PCHG and C_L, 10 MΩ between V_{CC} and CHG		40	200	µs

7.20 Electrical Characteristics: FUSE Drive

Typical values stated where T_A = 25°C and VCC = 14.4 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	Output voltage high	V_{BAT} ≥ 8 V, C_L = 1 nF, $I_{AFEFUSE}$ = 0 µA	6	7	8.65	V
		V_{BAT} < 8 V, C_L = 1 nF, $I_{AFEFUSE}$ = 0 µA	V_{BAT} – 0.1		V_{BAT}	
V_{IH}	High-level input		1.5	2.0	2.5	V
$I_{AFEFUSE(PU)}$	Internal pullup current	V_{BAT} ≥ 8 V, $V_{AFEFUSE}$ = VSS		150	330	nA
$R_{AFEFUSE}$	Output impedance		2	2.6	3.2	kΩ
C_{IN}	Input capacitance			5		pF
t_{DELAY}	Fuse trip detection delay		128		256	µs
t_{RISE}	Fuse output rise time	V_{BAT} ≥ 8 V, C_L = 1 nF, V_{OH} = 0 V to 5 V		5	20	µs

7.21 Electrical Characteristics: Internal Temperature Sensor

Typical values stated where T_A = 25°C and VCC = 14.4 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{TEMP}	Internal temperature sensor voltage drift	V_{TEMPP}	–1.9	–2.0	–2.1	mV/°C
		V_{TEMPP} – V_{TEMPN}, assured by design	0.177	0.178	0.179	

7.22 Electrical Characteristics: TS1, TS2, TS3, TS4

Typical values stated where T_A = 25°C and VCC = 14.4 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range	TS1, TS2, TS3, TS4, V_{BIAS} = V_{REF1}	–0.2		0.8 x V_{REF1}	V
		TS1, TS2, TS3, TS4, V_{BIAS} = V_{REG}	–0.2		0.8 x V_{REG}	
$R_{NTC(PU)}$	Internal pullup resistance	TS1, TS2, TS3, TS4	14.4	18	21.6	kΩ
$R_{NTC(DRIFT)}$	Resistance drift over temperature	TS1, TS2, TS3, TS4	–360	–280	–200	PPM/°C

7.23 Electrical Characteristics: PTC, PTCEN

Typical values stated where T_A = 25°C and VCC = 14.4 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{PTC(TRIP)}$	PTC trip resistance		1.2	2.5	3.95	MΩ
$V_{PTC(TRIP)}$	PTC trip voltage	$V_{PTC(TRIP)}$ = V_{PTCEN} – V_{PTC}	200	500	890	mV
I_{PTC}	Internal PTC current bias	T_A = –40°C to 110°C	200	290	350	nA
$t_{PTC(DELAY)}$	PTC delay time	T_A = –40°C to 110°C	40	80	145	ms

7.24 Electrical Characteristics: Internal 1.8-V LDO

Typical values stated where T_A = 25°C and VCC = 14.4 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{REG}	Regulator voltage		1.6	1.8	2.0	V
$\Delta V_{O(TEMP)}$	Regulator output over temperature	$\Delta V_{REG}/\Delta T_A$, I_{REG} = 10 mA		±0.25%		
$\Delta V_{O(LINE)}$	Line regulation	$\Delta V_{REG}/\Delta V_{BAT}$, V_{BAT} = 10 mA	–0 .6%		0.5%	
$\Delta V_{O(LOAD)}$	Load regulation	$\Delta V_{REG}/\Delta I_{REG}$, I_{REG} = 0 mA to 10 mA	–1.5%		1.5%	
I_{REG}	Regulator output current limit	V_{REG} = 0.9 x $V_{REG(NOM)}$, V_{IN} > 2.2 V	20			mA
I_{SC}	Regulator short-circuit current limit	V_{REG} = 0 x $V_{REG(NOM)}$	25	40	55	mA
$PSRR_{REG}$	Power supply rejection ratio	$\Delta V_{BAT}/\Delta V_{REG}$, I_{REG} = 10 mA ,V_{IN} > 2.5 V, f = 10 Hz		40		dB
V_{SLEW}	Slew rate enhancement voltage threshold	V_{REG}	1.58	1.65		V

7.25 Electrical Characteristics: High-Frequency Oscillator

Typical values stated where T_A = 25°C and VCC = 14.4 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{HFO}	Operating frequency			16.78		MHz
$f_{HFO(ERR)}$	Frequency error	T_A = –20°C to 70°C, includes frequency drift	–2.5%	±0.25%	2.5%	
		T_A = –40°C to 85°C, includes frequency drift	–3.5%	±0.25%	3.5%	
$t_{HFO(SU)}$	Start-up time	T_A = –20°C to 85°C, oscillator frequency within +/–3% of nominal			4	ms
		oscillator frequency within +/–3% of nominal			100	µs

7.26 Electrical Characteristics: Low-Frequency Oscillator

Typical values stated where T_A = 25°C and VCC = 14.4 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{LFO}	Operating frequency			262.144		kHz
$f_{LFO(ERR)}$	Frequency error	T_A = –20°C to 70°C, includes frequency drift	–1.5%	±0.25%	1.5%	
		T_A = –40°C to 85°C, includes frequency drift	–2.5	±0.25	2.5	
$f_{LFO(FAIL)}$	Failure detection frequency		30	80	100	kHz

7.27 Electrical Characteristics: Voltage Reference 1

Typical values stated where T_A = 25°C and VCC = 14.4 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{REF1}	Internal reference voltage	T_A = 25°C, after trim	1.21	1.215	1.22	V
$V_{REF1(DRIFT)}$	Internal reference voltage drift	T_A = 0°C to 60°C, after trim		±50		PPM/°C
		T_A = –40°C to 85°C, after trim		±80		

7.28 Electrical Characteristics: Voltage Reference 2

Typical values stated where T_A = 25°C and VCC = 14.4 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{REF2}	Internal reference voltage	T_A = 25°C, after trim	1.22	1.225	1.23	V
$V_{REF2(DRIFT)}$	Internal reference voltage drift	T_A = 0°C to 60°C, after trim		±50		PPM/°C
		T_A = –40°C to 85°C, after trim		±80		

7.29 Electrical Characteristics: Instruction Flash

Typical values stated where T_A = 25°C and VCC = 14.4 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Data retention		10			Years
	Flash programming write cycles		1000			Cycles
$t_{PROGWORD}$	Word programming time	T_A = –40°C to 85°C			40	µs
$t_{MASSERASE}$	Mass-erase time	T_A = –40°C to 85°C			40	ms
$t_{PAGEERASE}$	Page-erase time	T_A = –40°C to 85°C			40	ms
$I_{FLASHREAD}$	Flash-read current	T_A = –40°C to 85°C			2	mA
$I_{FLASHWRITE}$	Flash-write current	T_A = –40°C to 85°C			5	mA
$I_{FLASHERASE}$	Flash-erase current	T_A = –40°C to 85°C			15	mA

7.30 Electrical Characteristics: Data Flash

Typical values stated where T_A = 25°C and VCC = 14.4 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Data retention		10			Years
	Flash programming write cycles		20000			Cycles
$t_{PROGWORD}$	Word programming time	T_A = –40°C to 85°C			40	µs

Electrical Characteristics: Data Flash (continued)

Typical values stated where T_A = 25°C and VCC = 14.4 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{MASSERASE}$	Mass-erase time	T_A = –40°C to 85°C			40	ms
$t_{PAGEERASE}$	Page-erase time	T_A = –40°C to 85°C			40	ms
$I_{FLASHREAD}$	Flash-read current	T_A = –40°C to 85°C			1	mA
$I_{FLASHWRITE}$	Flash-write current	T_A = –40°C to 85°C			5	mA
$I_{FLASHERASE}$	Flash-erase current	T_A = –40°C to 85°C			15	mA

7.31 Electrical Characteristics: OCD, SCC, SCD1, SCD2 Current Protection Thresholds

Typical values stated where T_A = 25°C and VCC = 14.4 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OCD}	OCD detection threshold voltage range	$V_{OCD} = V_{SRP} – V_{SRN}$, AFE PROTECTION CONTROL[RSNS] = 1	–16.6		–100	mV
		$V_{OCD} = V_{SRP} – V_{SRN}$, AFE PROTECTION CONTROL[RSNS] = 0	–8.3		–50	
ΔV_{OCD}	OCD detection threshold voltage program step	$V_{OCD} = V_{SRP} – V_{SRN}$, AFE PROTECTION CONTROL[RSNS] = 1		–5.56		mV
		$V_{OCD} = V_{SRP} – V_{SRN}$, AFE PROTECTION CONTROL[RSNS] = 0		–2.78		
V_{SCC}	SCC detection threshold voltage range	$V_{SCC} = V_{SRP} – V_{SRN}$, AFE PROTECTION CONTROL[RSNS] = 1	44.4		200	mV
		$V_{SCC} = V_{SRP} – V_{SRN}$, AFE PROTECTION CONTROL[RSNS] = 0	22.2		100	
ΔV_{SCC}	SCC detection threshold voltage program step	$V_{SCC} = V_{SRP} – V_{SRN}$, AFE PROTECTION CONTROL[RSNS] = 1		22.2		mV
		$V_{SCC} = V_{SRP} – V_{SRN}$, AFE PROTECTION CONTROL[RSNS] = 0		11.1		
V_{SCD1}	SCD1 detection threshold voltage range	$V_{SCD1} = V_{SRP} – V_{SRN}$, AFE PROTECTION CONTROL[RSNS] = 1	–44.4		–200	mV
		$V_{SCD1} = V_{SRP} – V_{SRN}$, AFE PROTECTION CONTROL[RSNS] = 0	–22.2		–100	
ΔV_{SCD1}	SCD1 detection threshold voltage program step	$V_{SCD1} = V_{SRP} – V_{SRN}$, AFE PROTECTION CONTROL[RSNS] = 1		–22.2		mV
		$V_{SCD1} = V_{SRP} – V_{SRN}$, AFE PROTECTION CONTROL[RSNS] = 0		–11.1		
V_{SCD2}	SCD2 detection threshold voltage range	$V_{SCD2} = V_{SRP} – V_{SRN}$, AFE PROTECTION CONTROL[RSNS] = 1	–44.4		–200	mV
		$V_{SCD2} = V_{SRP} – V_{SRN}$, AFE PROTECTION CONTROL[RSNS] = 0	–22.2		–100	
ΔV_{SCD2}	SCD2 detection threshold voltage program step	$V_{SCD2} = V_{SRP} – V_{SRN}$, AFE PROTECTION CONTROL[RSNS] = 1		–22.2		mV
		$V_{SCD2} = V_{SRP} – V_{SRN}$, AFE PROTECTION CONTROL[RSNS] = 0		–11.1		
V_{OFFSET}	OCD, SCC, and SCDx offset error	Post-trim	–2.5		2.5	mV
V_{SCALE}	OCD, SCC, and SCDx scale error	No trim	–10%		10%	
		Post-trim	–5%		5%	

7.32 Timing Requirements: OCD, SCC, SCD1, SCD2 Current Protection Timing

Typical values stated where T_A = 25°C and VCC = 14.4 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

			MIN	NOM	MAX	UNIT
t_{OCD}	OCD detection delay time		1		31	ms
Δt_{OCD}	OCD detection delay time program step			2		ms
t_{SCC}	SCC detection delay time		0		915	µs
Δt_{SCC}	SCC detection delay time program step			61		µs
t_{SCD1}	SCD1 detection delay time	AFE PROTECTION CONTROL[SCDDx2] = 0	0		915	µs
		AFE PROTECTION CONTROL[SCDDx2] = 1	0		1850	
Δt_{SCD1}	SCD1 detection delay time program step	AFE PROTECTION CONTROL[SCDDx2] = 0		61		µs
		AFE PROTECTION CONTROL[SCDDx2] = 1		121		
t_{SCD2}	SCD2 detection delay time	AFE PROTECTION CONTROL[SCDDx2] = 0	0		458	µs
		AFE PROTECTION CONTROL[SCDDx2] = 1	0		915	
Δt_{SCD2}	SCD2 detection delay time program step	AFE PROTECTION CONTROL[SCDDx2] = 0		30.5		µs
		AFE PROTECTION CONTROL[SCDDx2] = 1		61		
t_{DETECT}	Current fault detect time	$V_{SRP} – V_{SRN} = V_T – 3$ mV for OCD, SCD1, and SC2, $V_{SRP} – V_{SRN} = V_T + 3$ mV for SCC			160	µs
t_{ACC}	Current fault delay time accuracy	Max delay setting	–10%		10%	

7.33 Timing Requirements: SMBus

Typical values stated where T_A = 25°C and VCC = 14.4 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

			MIN	NOM	MAX	UNIT
f_{SMB}	SMBus operating frequency	SLAVE mode, SMBC 50% duty cycle	10		100	kHz
f_{MAS}	SMBus master clock frequency	MASTER mode, no clock low slave extend		51.2		kHz
t_{BUF}	Bus free time between start and stop		4.7			µs
$t_{HD(START)}$	Hold time after (repeated) start		4.0			µs
$t_{SU(START)}$	Repeated start setup time		4.7			µs
$t_{SU(STOP)}$	Stop setup time		4.0			µs
$t_{HD(DATA)}$	Data hold time		300			ns
$t_{SU(DATA)}$	Data setup time		250			ns
$t_{TIMEOUT}$	Error signal detect time		25		35	ms
t_{LOW}	Clock low period		4.7			µs
t_{HIGH}	Clock high period		4.0		50	µs
t_R	Clock rise time	10% to 90%			1000	ns
t_F	Clock fall time	90% to 10%			300	ns
$t_{LOW(SEXT)}$	Cumulative clock low slave extend time				25	ms
$t_{LOW(MEXT)}$	Cumulative clock low master extend time				10	ms

7.34 Timing Requirements: SMBus XL

Typical values stated where T_A = 25°C and VCC = 14.4 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

			MIN	NOM	MAX	UNIT
f_{SMBXL}	SMBus XL operating frequency	SLAVE mode	40		400	kHz
t_{BUF}	Bus free time between start and stop		4.7			µs
$t_{HD(START)}$	Hold time after (repeated) start		4.0			µs
$t_{SU(START)}$	Repeated start setup time		4.7			µs
$t_{SU(STOP)}$	Stop setup time		4.0			µs
$t_{TIMEOUT}$	Error signal detect time		5		20	ms
t_{LOW}	Clock low period				20	µs
t_{HIGH}	Clock high period				20	µs

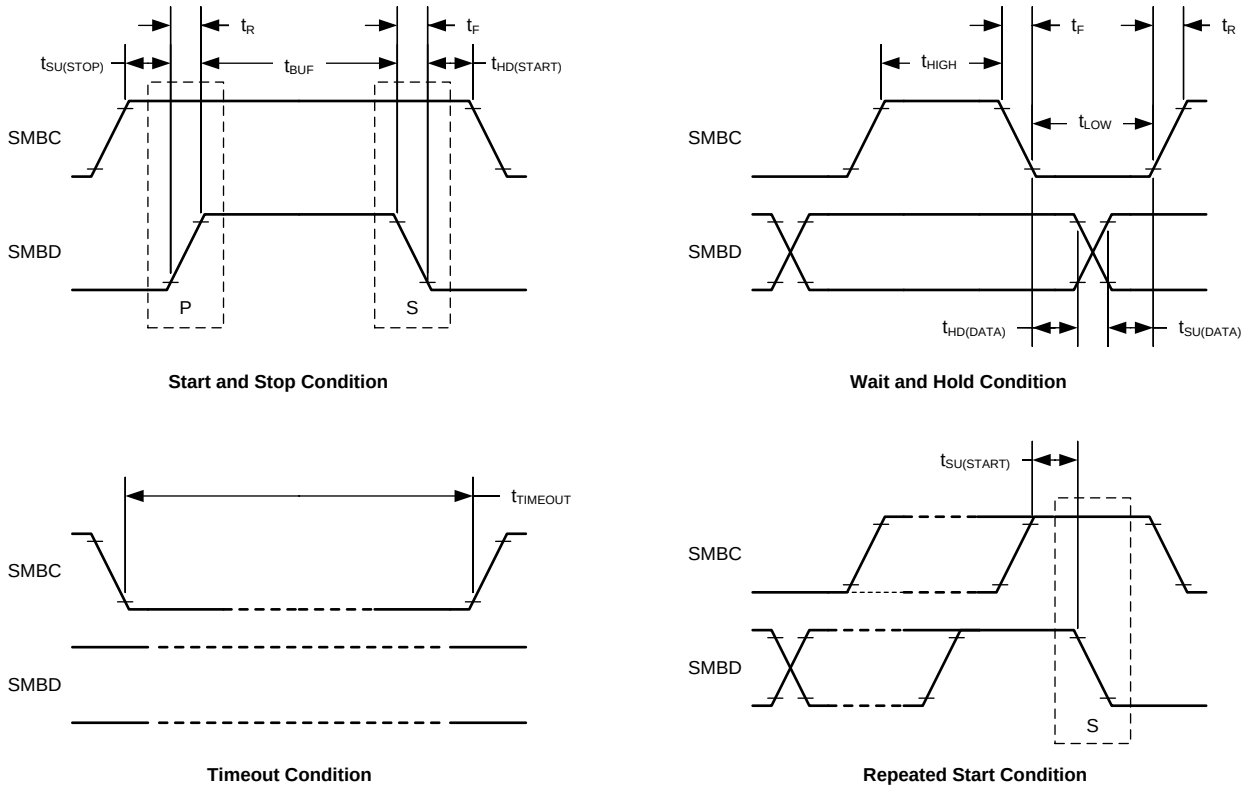


Figure 4. SMBus Timing Diagram

7.35 Typical Characteristics

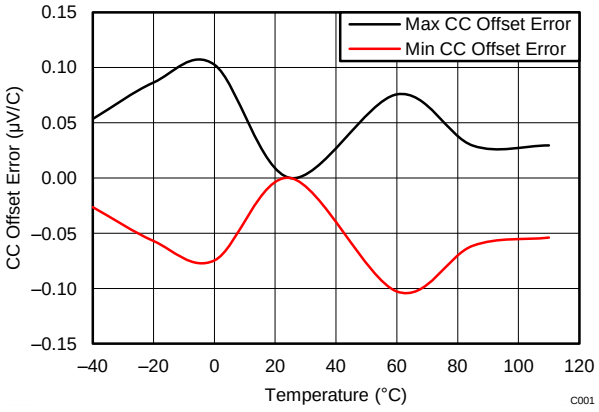


Figure 5. CC Offset Error vs. Temperature

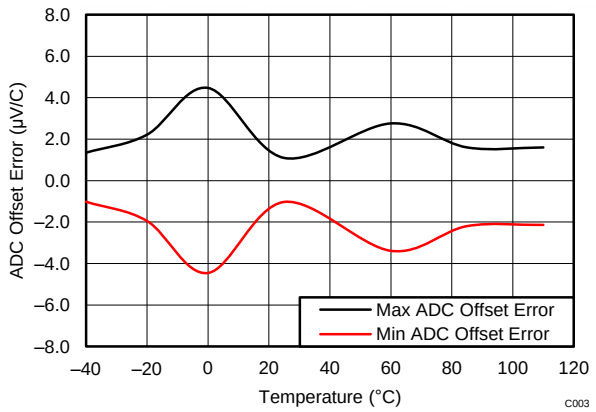


Figure 6. ADC Offset Error vs. Temperature

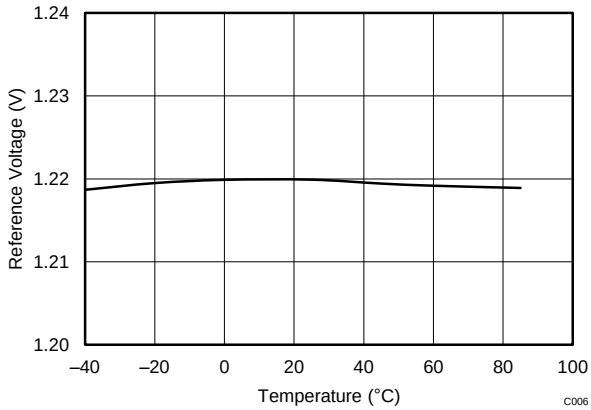


Figure 7. Reference Voltage vs. Temperature

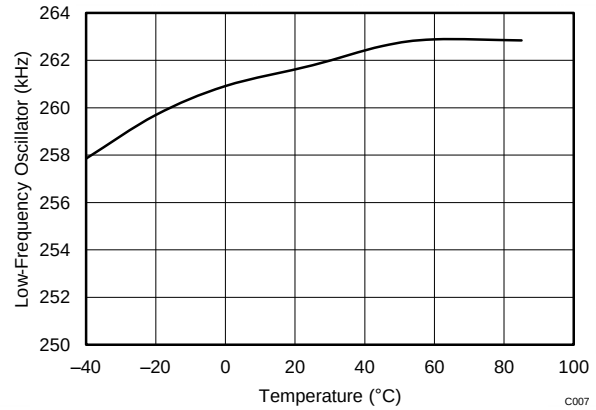


Figure 8. Low-Frequency Oscillator vs. Temperature

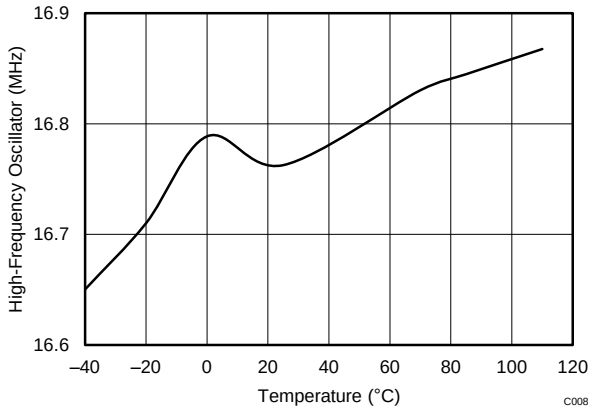
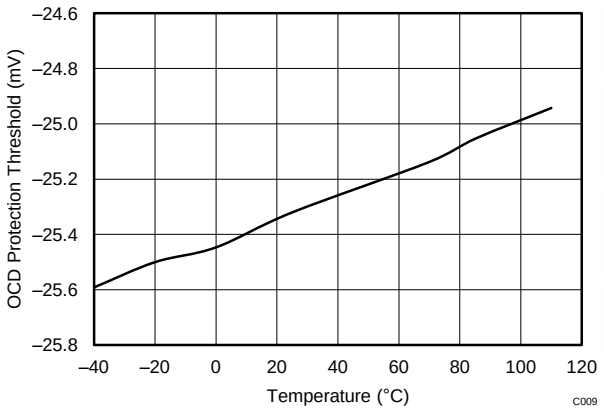


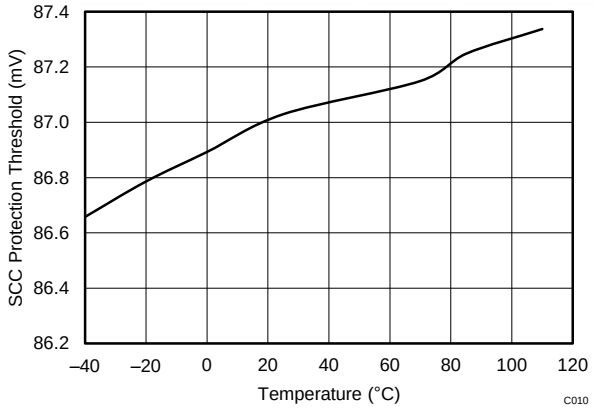
Figure 9. High-Frequency Oscillator vs. Temperature



Threshold setting is 25 mV.

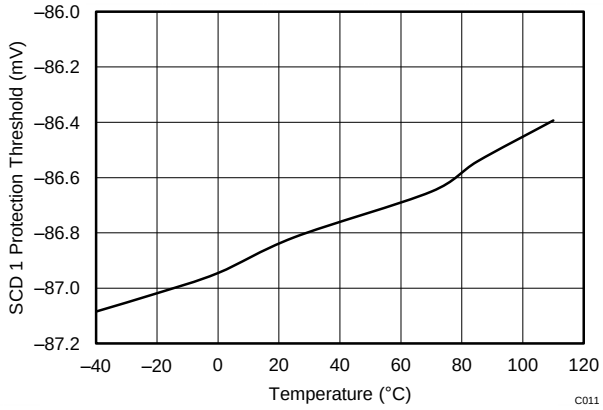
Figure 10. Overcurrent Discharge Protection Threshold vs. Temperature

Typical Characteristics (continued)



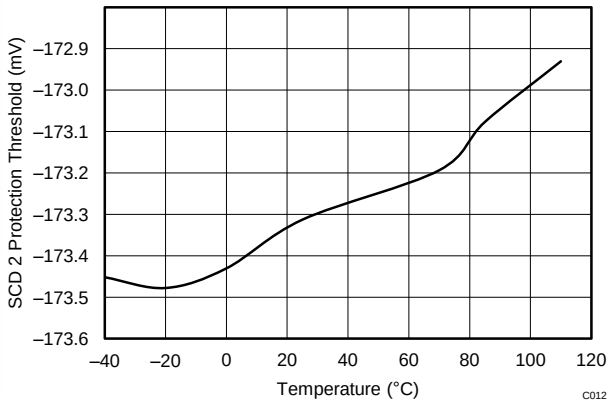
Threshold setting is 25 mV.

Figure 11. Short Circuit Charge Protection Threshold vs. Temperature



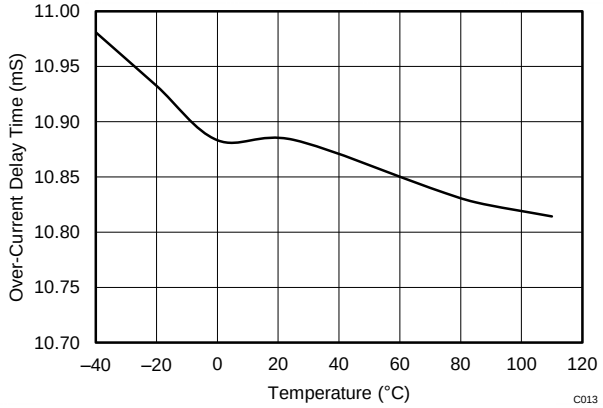
Threshold setting is –88.85 mV.

Figure 12. Short Circuit Discharge 1 Protection Threshold vs. Temperature



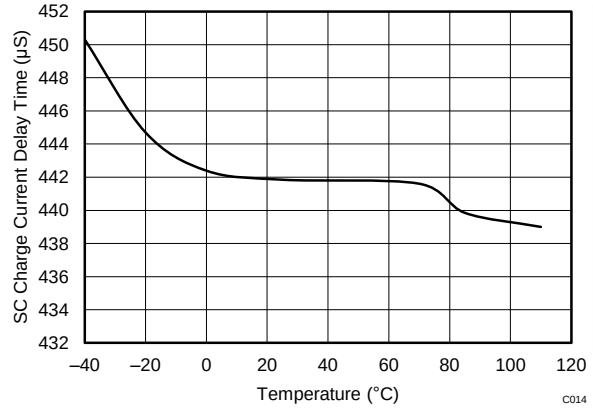
Threshold setting is –177.7 mV.

Figure 13. Short Circuit Discharge 2 Protection Threshold vs. Temperature



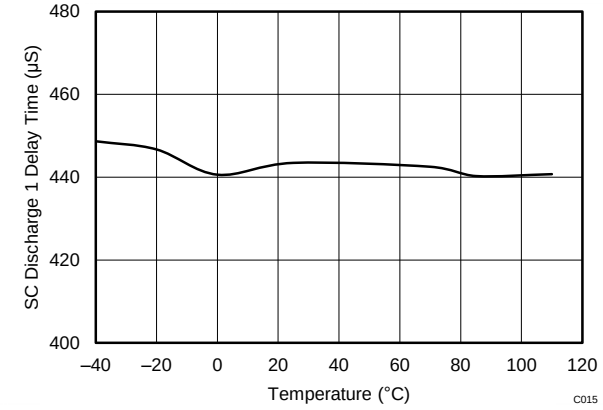
Threshold setting is 11 ms.

Figure 14. Overcurrent Delay Time vs. Temperature



Threshold setting is 465 µs.

Figure 15. Short Circuit Charge Current Delay Time vs. Temperature



Threshold setting is 465 µs (including internal delay).

Figure 16. Short Circuit Discharge 1 Delay Time vs. Temperature

Typical Characteristics (continued)

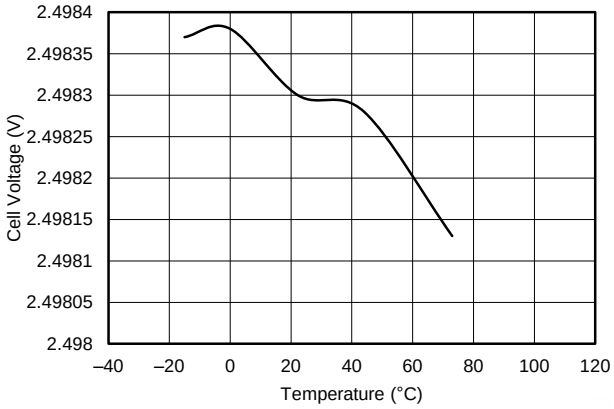
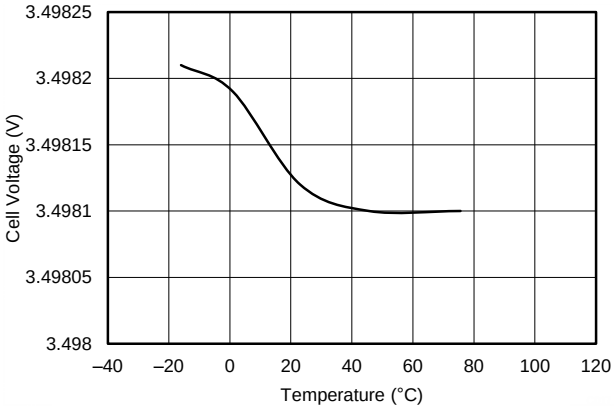
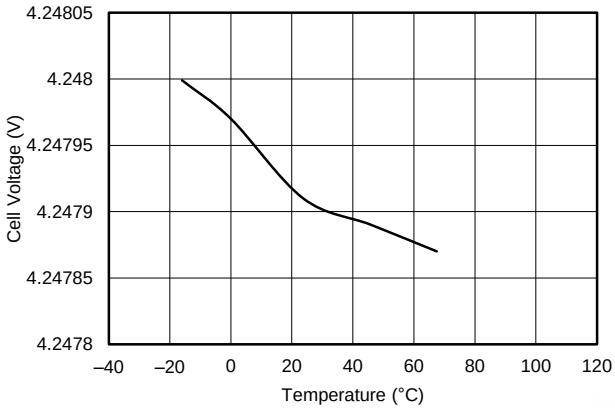


Figure 17. V_{CELL} Measurement at 2.5-V vs. Temperature



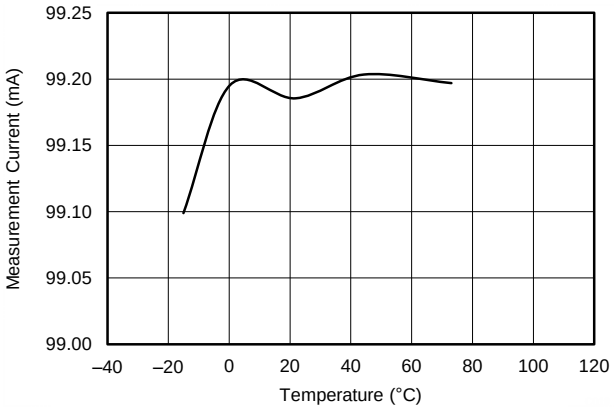
This is the V_{CELL} average for single cell.

Figure 18. V_{CELL} Measurement at 3.5-V vs. Temperature



This is the V_{CELL} average for single cell.

Figure 19. V_{CELL} Measurement at 4.25-V vs. Temperature



I_{SET} = 100 mA

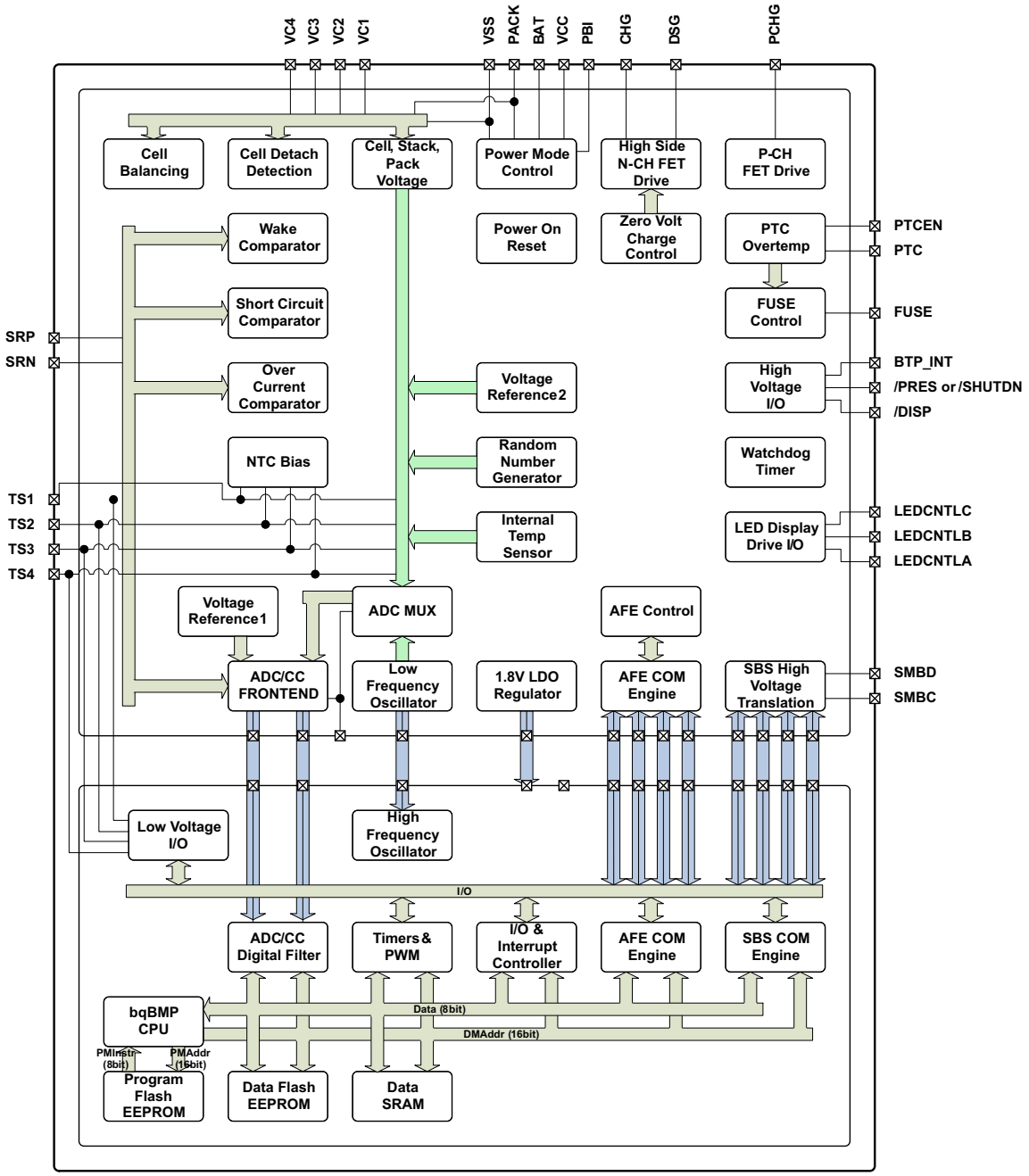
Figure 20. I measured vs. Temperature

8 Detailed Description

8.1 Overview

The bq40z50 device, incorporating patented Impedance Track™ technology, provides cell balancing while charging or at rest. This fully integrated, single-chip, pack-based solution provides a rich array of features for gas gauging, protection, and authentication for 1-series, 2-series, 3-series, and 4-series cell Li-Ion and Li-Polymer battery packs, including a diagnostic lifetime data monitor and black box recorder.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Primary (1st Level) Safety Features

The bq40z50 supports a wide range of battery and system protection features that can easily be configured. See the *bq40z50 Technical Reference Manual* (SLUUA43) for detailed descriptions of each protection function.

The primary safety features include:

- Cell Overvoltage Protection
- Cell Undervoltage Protection
- Cell Undervoltage Protection Compensated
- Overcurrent in Charge Protection
- Overcurrent in Discharge Protection
- Overload in Discharge Protection
- Short Circuit in Charge Protection
- Short Circuit in Discharge Protection
- Overtemperature in Charge Protection
- Overtemperature in Discharge Protection
- Undertemperature in Charge Protection
- Undertemperature in Discharge Protection
- Overtemperature FET protection
- Precharge Timeout Protection
- Host Watchdog Timeout Protection
- Fast Charge Timeout Protection
- Overcharge Protection
- Overcharging Voltage Protection
- Overcharging Current Protection
- Over Precharge Current Protection

8.3.2 Secondary (2nd Level) Safety Features

The secondary safety features of the bq40z50 can be used to indicate more serious faults via the FUSE pin. This pin can be used to blow an in-line fuse to permanently disable the battery pack from charging or discharging. See the *bq40z50 Technical Reference Manual* (SLUUA43) for detailed descriptions of each protection function.

The secondary safety features provide protection against:

- Safety Overvoltage Permanent Failure
- Safety Undervoltage Permanent Failure
- Safety Overtemperature Permanent Failure
- Safety FET Overtemperature Permanent Failure
- Qmax Imbalance Permanent Failure
- Impedance Imbalance Permanent Failure
- Capacity Degradation Permanent Failure
- Cell Balancing Permanent Failure
- Fuse Failure Permanent Failure
- PTC Permanent Failure
- Voltage Imbalance at Rest Permanent Failure
- Voltage Imbalance Active Permanent Failure
- Charge FET Permanent Failure
- Discharge FET Permanent Failure
- AFE Register Permanent Failure
- AFE Communication Permanent Failure
- Second Level Protector Permanent Failure

Feature Description (continued)

- Instruction Flash Checksum Permanent Failure
- Open Cell Connection Permanent Failure
- Data Flash Permanent Failure
- Open Thermistor Permanent Failure

8.3.3 Charge Control Features

The bq40z50 charge control features include:

- Supports JEITA temperature ranges. Reports charging voltage and charging current according to the active temperature range
- Handles more complex charging profiles. Allows for splitting the standard temperature range into two sub-ranges and allows for varying the charging current according to the cell voltage
- Reports the appropriate charging current needed for constant current charging and the appropriate charging voltage needed for constant voltage charging to a smart charger using SMBus broadcasts
- Reduces the charge difference of the battery cells in fully charged state of the battery pack gradually using a voltage-based cell balancing algorithm during charging. A voltage threshold can be set up for cell balancing to be active. This prevents fully charged cells from overcharging and causing excessive degradation and also increases the usable pack energy by preventing premature charge termination.
- Supports pre-charging/zero-volt charging
- Supports charge inhibit and charge suspend if battery pack temperature is out of temperature range
- Reports charging fault and also indicates charge status via charge and discharge alarms

8.3.4 Gas Gauging

The bq40z50 uses the Impedance Track algorithm to measure and calculate the available capacity in battery cells. The bq40z50 accumulates a measure of charge and discharge currents and compensates the charge current measurement for the temperature and state-of-charge of the battery. The bq40z50 estimates self-discharge of the battery and also adjusts the self-discharge estimation based on temperature. The device also has TURBO BOOST mode support, which enables the bq40z50 to provide the necessary data for the MCU to determine what level of peak power consumption can be applied without causing a system reset or transient battery voltage level spike to trigger termination flags. See the *bq40z50 Technical Reference Manual* (SLUUA43) for further details.

8.3.5 Configuration

8.3.5.1 Oscillator Function

The bq40z50 fully integrates the system oscillators and does not require any external components to support this feature.

8.3.5.2 System Present Operation

The bq40z50 checks the $\overline{\text{PRES}}$ pin periodically (1 s). If $\overline{\text{PRES}}$ input is pulled to ground by the external system, the bq40z50 detects this as system present.

8.3.5.3 Emergency Shutdown

For battery maintenance, the emergency shutdown feature enables a push button action connecting the $\overline{\text{SHUTDN}}$ pin to shutdown an embedded battery pack system before removing the battery. A high-to-low transition of the $\overline{\text{SHUTDN}}$ pin signals the bq40z50 to turn off both CHG and DSG FETs, disconnecting the power from the system to safely remove the battery pack. The CHG and DSG FETs can be turned on again by another high-to-low transition detected by the $\overline{\text{SHUTDN}}$ pin or when a data flash configurable timeout is reached.

8.3.5.4 1-Series, 2-Series, 3-Series, or 4-Series Cell Configuration

In a 1-series cell configuration, VC4 is shorted to VC, VC2 and VC1. In a 2-series cell configuration, VC4 is shorted to VC3 and VC2. In a 3-series cell configuration, VC4 is shorted to VC3.

Feature Description (continued)

8.3.5.5 Cell Balancing

The device supports cell balancing by bypassing the current of each cell during charging or at rest. If the device's internal bypass is used, up to 10 mA can be bypassed and multiple cells can be bypassed at the same time. Higher cell balance current can be achieved by using an external cell balancing circuit. In external cell balancing mode, only one cell at a time can be balanced.

The cell balancing algorithm determines the amount of charge needed to be bypassed to balance the capacity of all cells.

8.3.6 Battery Parameter Measurements

8.3.6.1 Charge and Discharge Counting

The bq40z50 uses an integrating delta-sigma analog-to-digital converter (ADC) for current measurement, and a second delta-sigma ADC for individual cell and battery voltage and temperature measurement.

The integrating delta-sigma ADC measures the charge/discharge flow of the battery by measuring the voltage drop across a small-value sense resistor between the SRP and SRN terminals. The integrating ADC measures bipolar signals from –0.1 V to 0.1 V. The bq40z50 detects charge activity when $V_{SR} = V_{(SRP)} – V_{(SRN)}$ is positive, and discharge activity when $V_{SR} = V_{(SRP)} – V_{(SRN)}$ is negative. The bq40z50 continuously integrates the signal over time, using an internal counter. The fundamental rate of the counter is 0.26 nVh.

8.3.7 Battery Trip Point (BTP)

Required for WIN8 OS, the battery trip point (BTP) feature indicates when the RSOC of a battery pack has depleted to a certain value set in a DF register. This feature allows a host to program two capacity-based thresholds that govern the triggering of a BTP interrupt on the BTP_INT pin and the setting or clearing of the *OperationStatus[BTP_INT]* on the basis of *RemainingCapacity()*.

An internal weak pull-up is applied when the BTP feature is active. Depending on the system design, an external pull-up may required to put on the BTP_INT pin. See *Electrical Characteristics: PRES, BTP_INT, DISP* for details.

8.3.8 Lifetime Data Logging Features

The bq40z50 offers lifetime data logging for several critical battery parameters. The following parameters are updated every 10 hours if a difference is detected between values in RAM and data flash:

- Maximum and Minimum Cell Voltages
- Maximum Delta Cell Voltage
- Maximum Charge Current
- Maximum Discharge Current
- Maximum Average Discharge Current
- Maximum Average Discharge Power
- Maximum and Minimum Cell Temperature
- Maximum Delta Cell Temperature
- Maximum and Minimum Internal Sensor Temperature
- Maximum FET Temperature
- Number of Safety Events Occurrences and the Last Cycle of the Occurrence
- Number of Valid Charge Termination and the Last Cycle of the Valid Charge Termination
- Number of Qmax and Ra Updates and the Last Cycle of the Qmax and Ra Updates
- Number of Shutdown Events
- Cell Balancing Time for Each Cell
  (This data is updated every 2 hours if a difference is detected.)
- Total FW Runtime and Time Spent in Each Temperature Range
  (This data is updated every 2 hours if a difference is detected.)

Feature Description (continued)

8.3.9 Authentication

The bq40z50 supports authentication by the host using SHA-1.

8.3.10 LED Display

The bq40z50 can drive a 3-, 4-, or 5- segment LED display for remaining capacity indication and/or a permanent fail (PF) error code indication.

8.3.11 Voltage

The bq40z50 updates the individual series cell voltages at 0.25-second intervals. The internal ADC of the bq40z50 measures the voltage, and scales and calibrates it appropriately. This data is also used to calculate the impedance of the cell for the Impedance Track gas gauging.

8.3.12 Current

The bq40z50 uses the SRP and SRN inputs to measure and calculate the battery charge and discharge current using a 1-mΩ to 3-mΩ typ. sense resistor.

8.3.13 Temperature

The bq40z50 has an internal temperature sensor and inputs for four external temperature sensors. All five temperature sensor options can be individually enabled and configured for cell or FET temperature usage. Two configurable thermistor models are provided to allow the monitoring of cell temperature in addition to FET temperature, which use a different thermistor profile.

8.3.14 Communications

The bq40z50 uses SMBus v1.1 with MASTER mode and packet error checking (PEC) options per the SBS specification.

8.3.14.1 SMBus On and Off State

The bq40z50 detects an SMBus off state when SMBC and SMBD are low for two or more seconds. Clearing this state requires that either SMBC or SMBD transition high. The communication bus will resume activity within 1 ms.

8.3.14.2 SBS Commands

See the *bq40z50 Technical Reference Manual* (SLUUA43) for further details.

8.4 Device Functional Modes

The bq40z50 supports three power modes to reduce power consumption:

- In NORMAL mode, the bq40z50 performs measurements, calculations, protection decisions, and data updates in 250-ms intervals. Between these intervals, the bq40z50 is in a reduced power stage.
- In SLEEP mode, the bq40z50 performs measurements, calculations, protection decisions, and data updates in adjustable time intervals. Between these intervals, the bq40z50 is in a reduced power stage. The bq40z50 has a wake function that enables exit from SLEEP mode when current flow or failure is detected.
- In SHUTDOWN mode, the bq40z50 is completely disabled.

9 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The bq40z50 is a gas gauge with primary protection support, and that can be used with a 1-series to 4-series Li-Ion/Li Polymer battery pack. To implement and design a comprehensive set of parameters for a specific battery pack, users need the Battery Management Studio (bqSTUDIO) graphical user-interface tool installed on a PC during development. The firmware installed on the bqSTUDIO tool has default values for this product, which are summarized in the *bq40z50 Technical Reference Manual* (SLUUA43). Using the bqSTUDIO tool, these default values can be changed to cater to specific application requirements during development once the system parameters, such as fault trigger thresholds for protection, enable/disable of certain features for operation, configuration of cells, chemistry that best matches the cell used, and more are known. This data is referred to as the "golden image."

9.2 Typical Applications

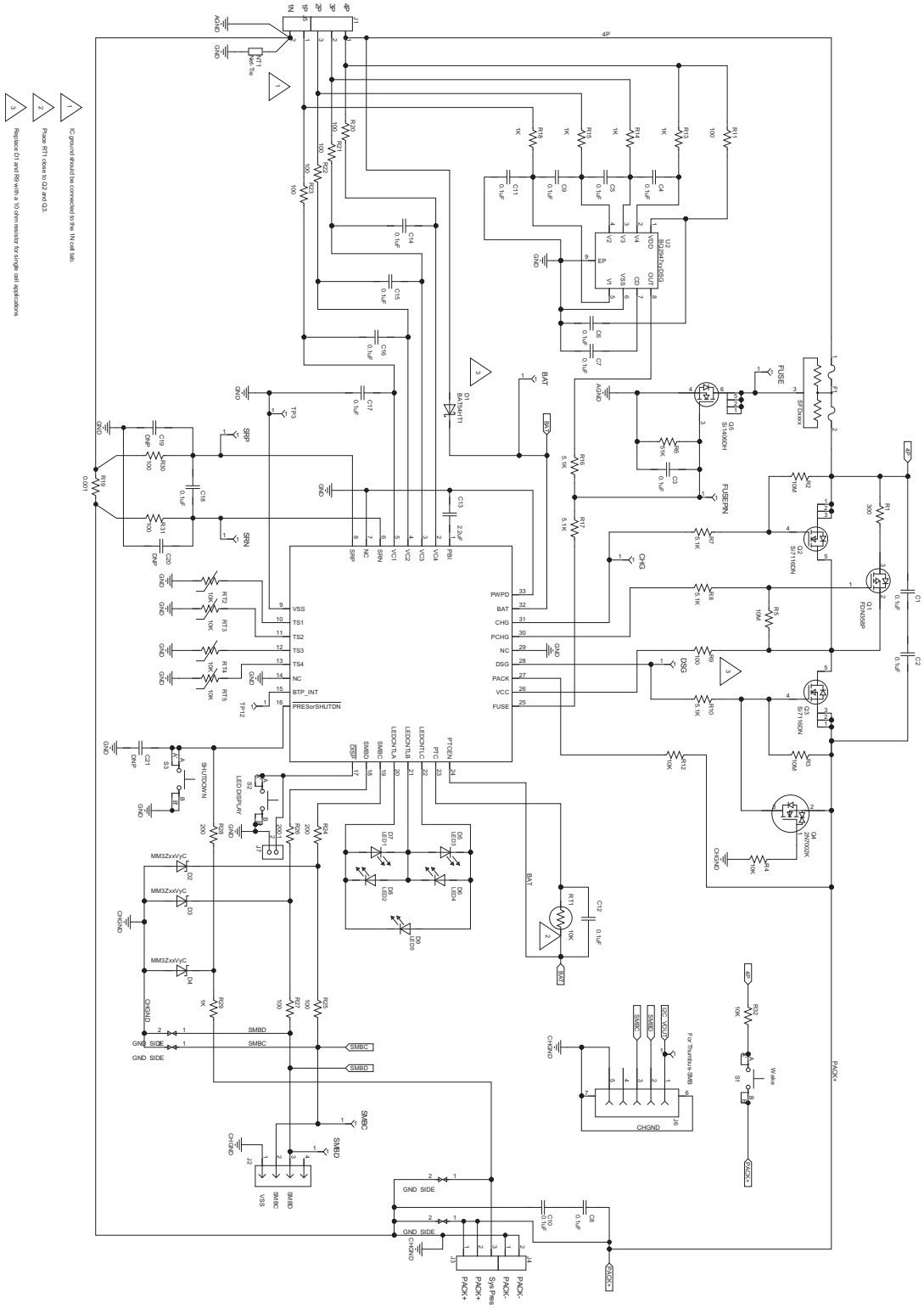


Figure 21. Application Schematic

Typical Applications (continued)

9.2.1 Design Requirements

Table 1 shows the default settings for the main parameters. Use the bqSTUDIO tool to update the settings to meet the specific application or battery pack configuration requirements.

The device should be calibrated before any gauging test. Follow the bqSTUDIO **Calibration** page to calibrate the device, and use the bqSTUDIO **Chemistry** page to update the match chemistry profile to the device.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE
Cell Configuration	3s1p (3-series with 1 Parallel)(1)
Design Capacity	4400 mAH
Device Chemistry	1210 (LiCoO2/graphitized carbon)
Cell Overvoltage at Standard Temperature	4300 mV
Cell Undervoltage	2500 mV
Shutdown Voltage	2300 mV
Overcurrent in CHARGE Mode	6000 mA
Overcurrent in DISCHARGE Mode	–6000 mA
Short Circuit in CHARGE Mode	0.1 V/Rsense across SRP, SRN
Short Circuit in DISCHARGE Mode	0.1 V/Rsense across SRP, SRN
Safety Over Voltage	4500 mV
Cell Balancing	Disabled
Internal and External Temperature Sensor	External Temperature Sensor is used.
Under Temperature Charging	0°C
Under Temperature Discharging	0°C
BROADCAST Mode	Disabled
Battery Trip Point (BTP) with active high interrupt	Disabled

(1) When using the device the first time, if the a 1-S or 2-S battery pack is used, then a charger or power supply should be connected to the PACK+ terminal to prevent device shutdown. Then update the cell configuration (see the *bq40z50 Technical Reference Manual* (SLUUA43) for details) before removing the charger connection.

9.2.2 Detailed Design Procedure

9.2.2.1 High-Current Path

The high-current path begins at the PACK+ terminal of the battery pack. As charge current travels through the pack, it finds its way through protection FETs, a chemical fuse, the lithium-ion cells and cell connections, and the sense resistor, and then returns to the PACK– terminal (see Figure 22). In addition, some components are placed across the PACK+ and PACK– terminals to reduce effects from electrostatic discharge.

9.2.2.1.1 Protection FETs

Select the N-channel charge and discharge FETs for a given application. Most portable battery applications are a good match for the CSD17308Q3. The TI CSD17308Q3 is a 47A, 30-V device with Rds(on) of 8.2 mΩ when the gate drive voltage is 8 V.

If a precharge FET is used, R1 is calculated to limit the precharge current to the desired rate. Be sure to account for the power dissipation of the series resistor. The precharge current is limited to $(V_{CHARGER} – V_{BAT})/R1$ and maximum power dissipation is $(V_{charger} – V_{bat})^2/R1$.

The gates of all protection FETs are pulled to the source with a high-value resistor between the gate and source to ensure they are turned off if the gate drive is open.

Capacitors C1 and C2 help protect the FETs during an ESD event. Using two devices ensures normal operation if one becomes shorted. To have good ESD protection, the copper trace inductance of the capacitor leads must be designed to be as short and wide as possible. Ensure that the voltage rating of both C1 and C2 are adequate to hold off the applied voltage if one of the capacitors becomes shorted.

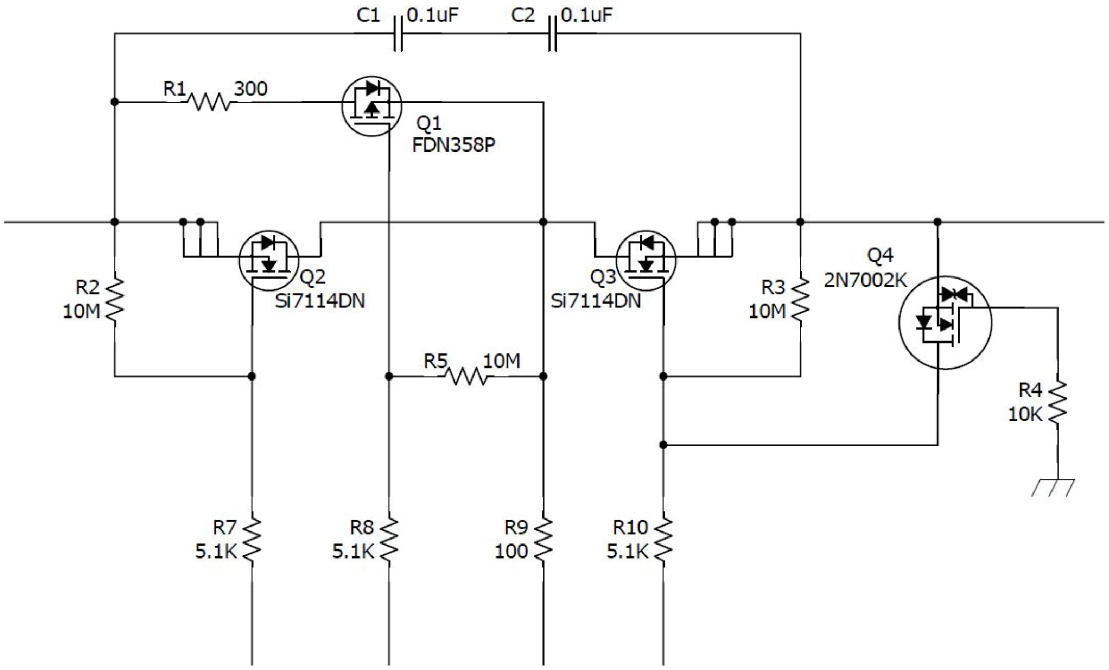


Figure 22. bq40z50 Protection FETs

9.2.2.1.2 Chemical Fuse

The chemical fuse (Dexerials, Uchihashi, and so forth) is ignited under command from either the bq294700 secondary voltage protection IC or from the FUSE pin of the gas gauge. Either of these events applies a positive voltage to the gate of Q5, shown in Figure 23, which then sinks current from the third terminal of the fuse, causing it to ignite and open permanently.

It is important to carefully review the fuse specifications and match the required ignition current to that available from the N-channel FET. Ensure that the proper voltage, current, and Rds(on) ratings are used for this device. The fuse control circuit is discussed in detail in *FUSE Circuitry*.

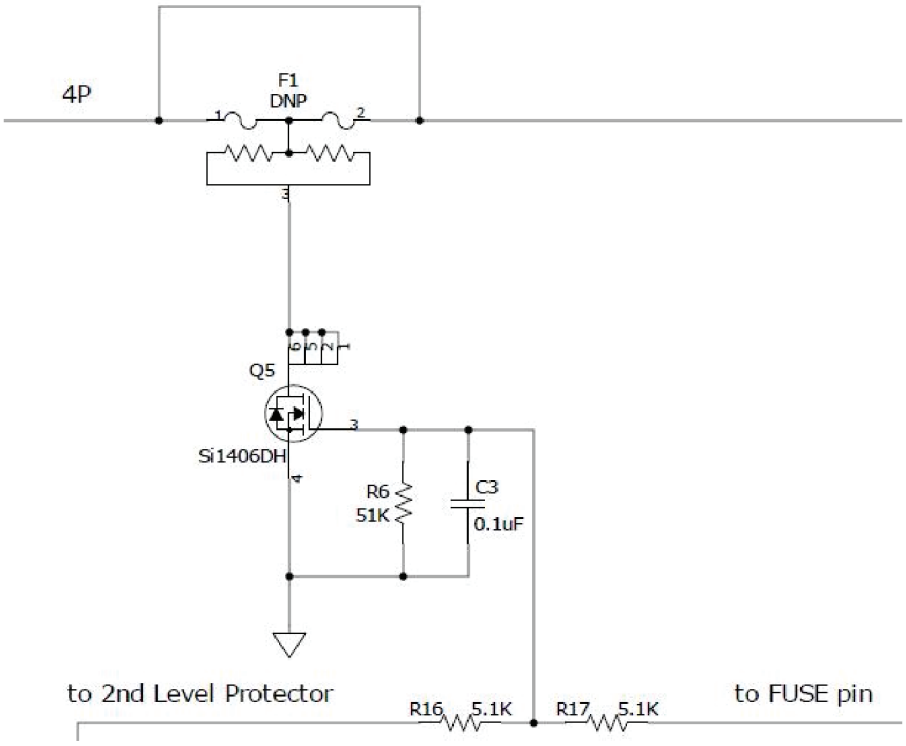


Figure 23. FUSE Circuit

9.2.2.1.3 Lithium-Ion Cell Connections

The important part to remember about the cell connections is that high current flows through the top and bottom connections; therefore, the voltage sense leads at these points must be made with a Kelvin connection to avoid any errors due to a drop in the high-current copper trace. The location marked 4P in Figure 24 indicates the Kelvin connection of the most positive battery node. The connection marked 1N is equally important. The VC5 pin (a ground reference for cell voltage measurement), which is in the older generation devices, is not in the bq40z50 device. Therefore, the single-point connection at 1N to the low-current ground is needed to avoid an undesired voltage drop through long traces while the gas gauge is measuring the bottom cell voltage.

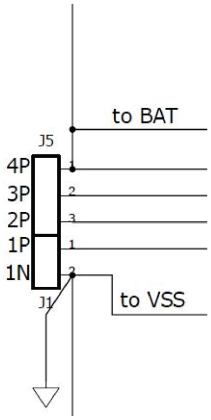


Figure 24. Lithium-Ion Cell Connections

9.2.2.1.4 Sense Resistor

As with the cell connections, the quality of the Kelvin connections at the sense resistor is critical. The sense resistor must have a temperature coefficient no greater than 50 ppm in order to minimize current measurement drift with temperature. Choose the value of the sense resistor to correspond to the available overcurrent and short-circuit ranges of the bq40z50. Select the smallest value possible to minimize the negative voltage generated on the bq40z50 V_{SS} node(s) during a short circuit. This pin has an absolute minimum of –0.3 V. Parallel resistors can be used as long as good Kelvin sensing is ensured. The device is designed to support a 1-mΩ to 3-mΩ sense resistor.

The ground scheme of bq40z50 is different from the older generation devices. In previous devices, the device ground (or low current ground) is connected to the SRN side of the Rsense resistor pad. The bq40z50, however, connects the low-current ground on the SRP side of the Rsense resistor pad, close to the battery 1N terminal (see *Lithium-Ion Cell Connections*). This is because the bq40z50 has one less VC pin (a ground reference pin VC5) compared to the previous devices. The pin was removed and was internally combined to SRP.

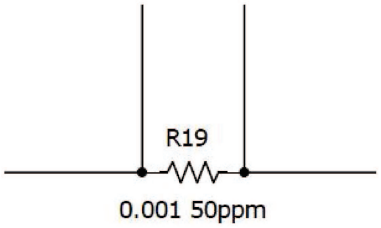


Figure 25. Sense Resistor

9.2.2.1.5 ESD Mitigation

A pair of series 0.1-µF ceramic capacitors is placed across the PACK+ and PACK– terminals to help in the mitigation of external electrostatic discharges. The two devices in series ensure continued operation of the pack if one of the capacitors becomes shorted.

Optionally, a tranzorb such as the SMBJ2A can be placed across the terminals to further improve ESD immunity.

9.2.2.2 Gas Gauge Circuit

The Gas Gauge Circuit includes the bq40z50 and its peripheral components. These components are divided into the following groups: Differential Low-Pass Filter, PBI, System Present, SMBus Communication, FUSE circuit, and LED.

9.2.2.2.1 Coulomb-Counting Interface

The bq40z50 uses an integrating delta-sigma ADC for current measurements. Add a 100-Ω resistor from the sense resistor to the SRP and SRN inputs of the device. Place a 0.1-µF (C18) filter capacitor across the SRP and SRN inputs. Optional 0.1-µF filter capacitors (C19 and C20) can be added for additional noise filtering, if required for your circuit.

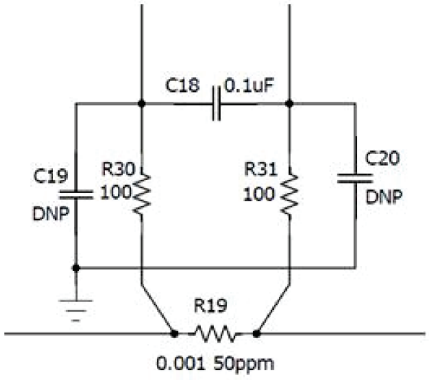


Figure 26. Differential Filter

9.2.2.2.2 Power Supply Decoupling and PBI

The bq40z50 has an internal LDO that is internally compensated and does not require an external decoupling capacitor.

The PBI pin is used as a power supply backup input pin providing power during brief transient power outages. A standard 2.2-µF ceramic capacitor is connected from the PBI pin to ground as shown in Figure 27.

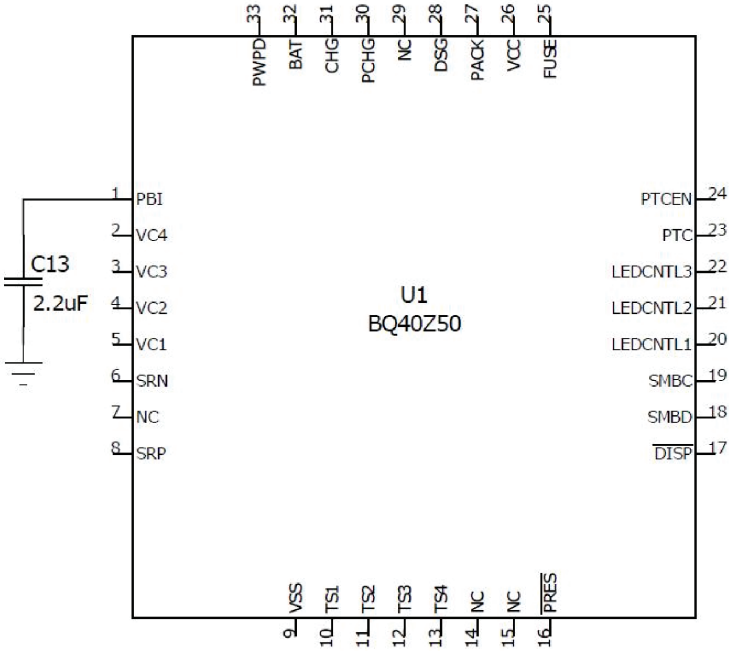


Figure 27. Power Supply Decoupling

9.2.2.2.3 System Present

The System Present signal is used to inform the gas gauge whether the pack is installed into or removed from the system. In the host system, this pin is grounded. The $\overline{\text{PRES}}$ pin of the bq40z50 is occasionally sampled to test for system present. To save power, an internal pullup is provided by the gas gauge during a brief 4-µs sampling pulse once per second. A resistor can be used to pull the signal low and the resistance must be 20 kΩ or lower to insure that the test pulse is lower than the VIL limit. The pull-up current source is typically 10 µA to 20 µA.

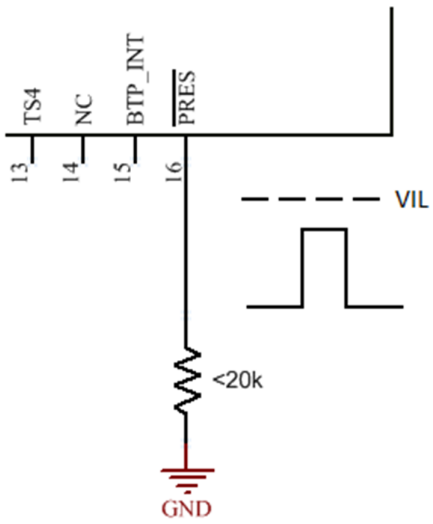


Figure 28. System Present Pull-Down Resistor

Because the System Present signal is part of the pack connector interface to the outside world, it must be protected from external electrostatic discharge events. An integrated ESD protection on the PRES device pin reduces the external protection requirement to just R29 for an 8-kV ESD contact rating. However, if it is possible that the System Present signal may short to PACK+, then R28 and D4 must be included for high-voltage protection.

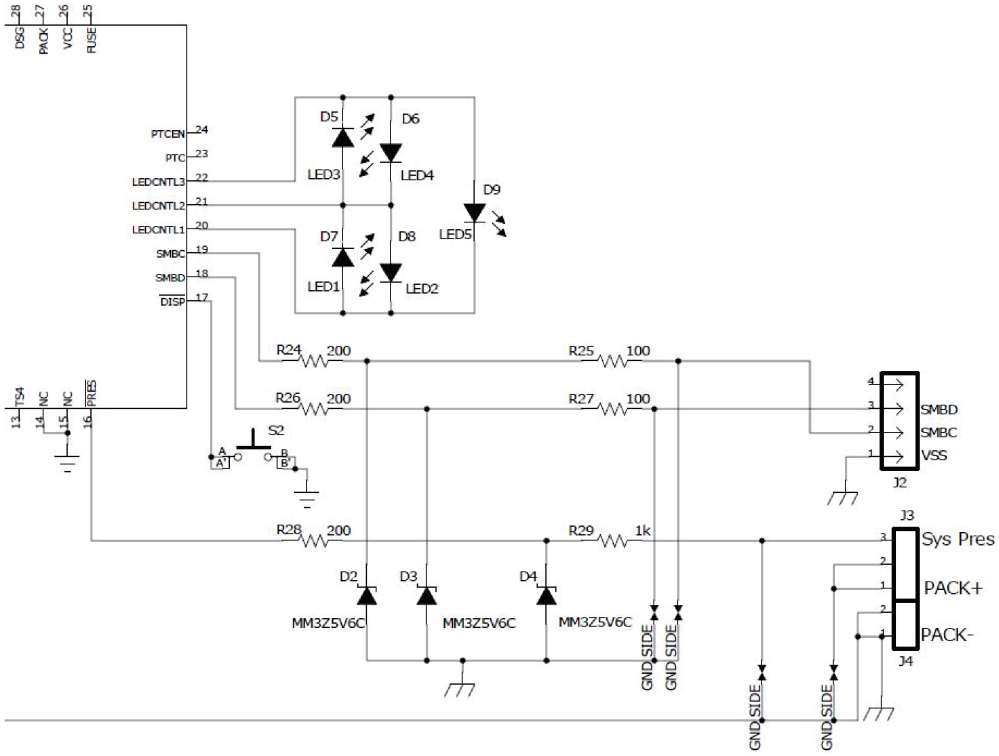


Figure 29. System Present ESD and Short Protection

9.2.2.2.4 SMBus Communication

The SMBus clock and data pins have integrated high-voltage ESD protection circuits, however, adding a Zener diode (D2 and D3) and series resistor (R24 and R26) provides more robust ESD performance.

The SMbus clock and data lines have internal pulldown. When the gas gauge senses that both lines are low (such as during removal of the pack), the device performs auto-offset calibration and then goes into SLEEP mode to conserve power.

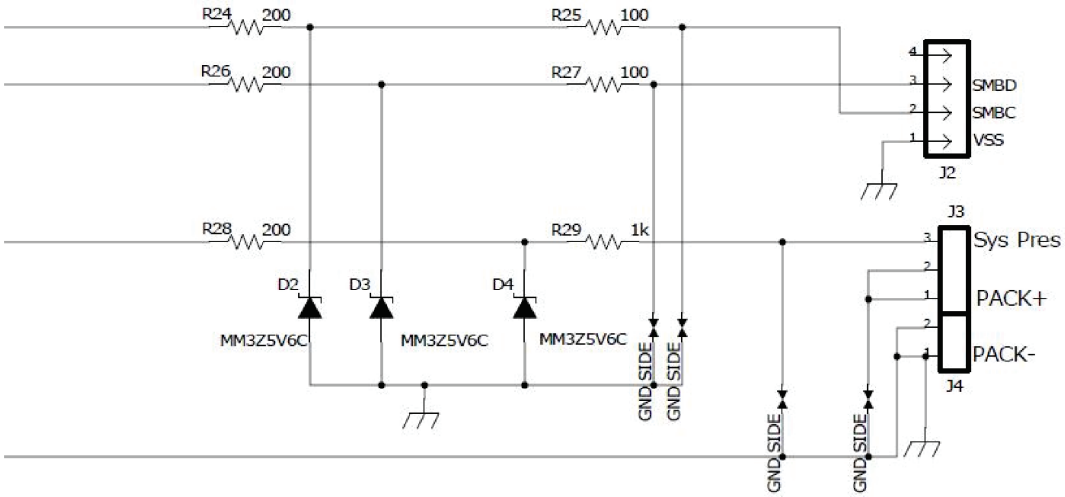


Figure 30. ESD Protection for SMB Communication

9.2.2.2.5 FUSE Circuitry

The FUSE pin of the bq40z50 is designed to ignite the chemical fuse if one of the various safety criteria is violated. The FUSE pin also monitors the state of the secondary-voltage protection IC. Q5 ignites the chemical fuse when its gate is high. The 7-V output of the bq294700 is divided by R16 and R6, which provides adequate gate drive for Q5 while guarding against excessive back current into the bq294700 if the FUSE signal is high.

Using C3 is generally a good practice, especially for RFI immunity. C3 may be removed, if desired, because the chemical fuse is a comparatively slow device and is not affected by any sub-microsecond glitches that come from the FUSE output during the cell connection process.

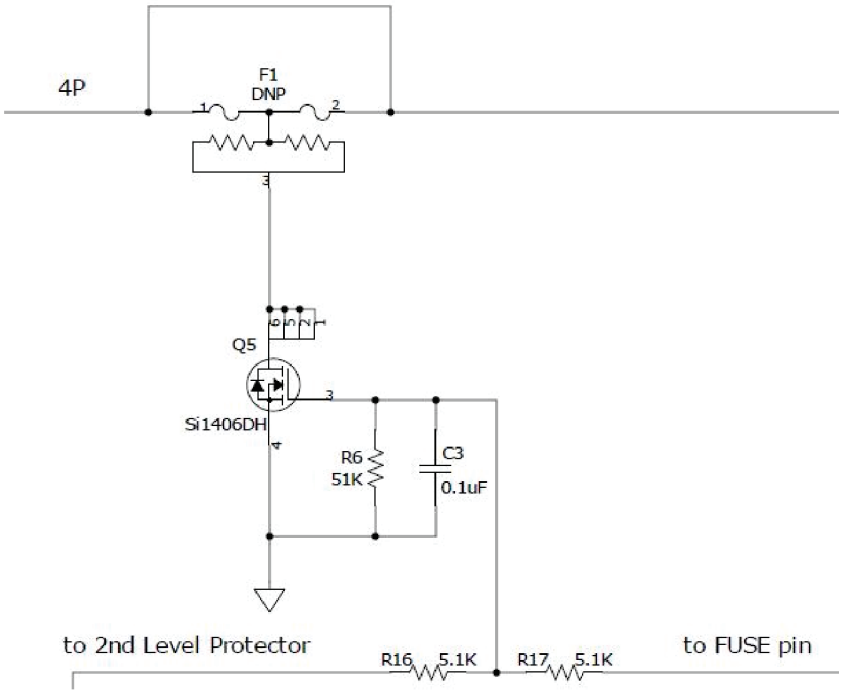


Figure 31. FUSE Circuit

When the bq40z50 is commanded to ignite the chemical fuse, the FUSE pin activates to give a typical 8-V output. The new design makes it possible to use a higher Vgs FET for Q5. This improves the robustness of the system, as well as widens the choices for Q5.

9.2.2.3 Secondary-Current Protection

The bq40z50 provides secondary overcurrent and short-circuit protection, cell balancing, cell voltage multiplexing, and voltage translation. The following discussion examines Cell and Battery Inputs, Pack and FET Control, Temperature Output, and Cell Balancing.

9.2.2.3.1 Cell and Battery Inputs

Each cell input is conditioned with a simple RC filter, which provides ESD protection during cell connect and acts to filter unwanted voltage transients. The resistor value allows some trade-off for cell balancing versus safety protection.

The integrated cell balancing FETs allow the AFE to bypass cell current around a given cell or numerous cells, effectively balancing the entire battery stack. External series resistors placed between the cell connections and the VCx I/O pins set the balancing current magnitude. The internal FETs provide a 200-Ω resistance (2 V < VDS < 4 V). Series input resistors between 100 Ω and 1 kΩ are recommended for effective cell balancing.

The BAT input uses a diode (D1) to isolate and decouple it from the cells in the event of a transient dip in voltage caused by a short-circuit event.

Also, as described in *High-Current Path*, the top and bottom nodes of the cells must be sensed at the battery connections with a Kelvin connection to prevent voltage sensing errors caused by a drop in the high-current PCB copper.

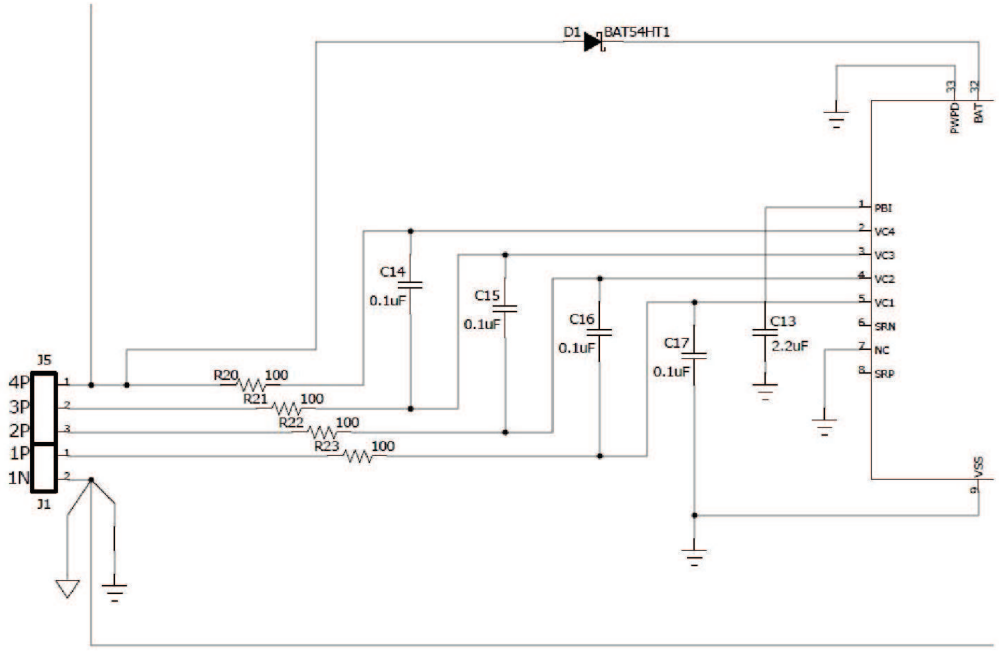


Figure 32. Cell and BAT Inputs

9.2.2.3.2 External Cell Balancing

Internal cell balancing can only support up to 10 mA. External cell balancing provide as another option for faster cell balancing. For details, refer to the application note, *Fast Cell Balancing Using External MOSFET* (SLUA420).

9.2.2.3.3 PACK and FET Control

The PACK and V_{CC} inputs provide power to the bq40z50 from the charger. The PACK input also provides a method to measure and detect the presence of a charger. The PACK input uses a 100-Ω resistor, whereas the V_{CC} input uses a diode to guard against input transients and prevents misoperation of the date driver during short-circuit events.

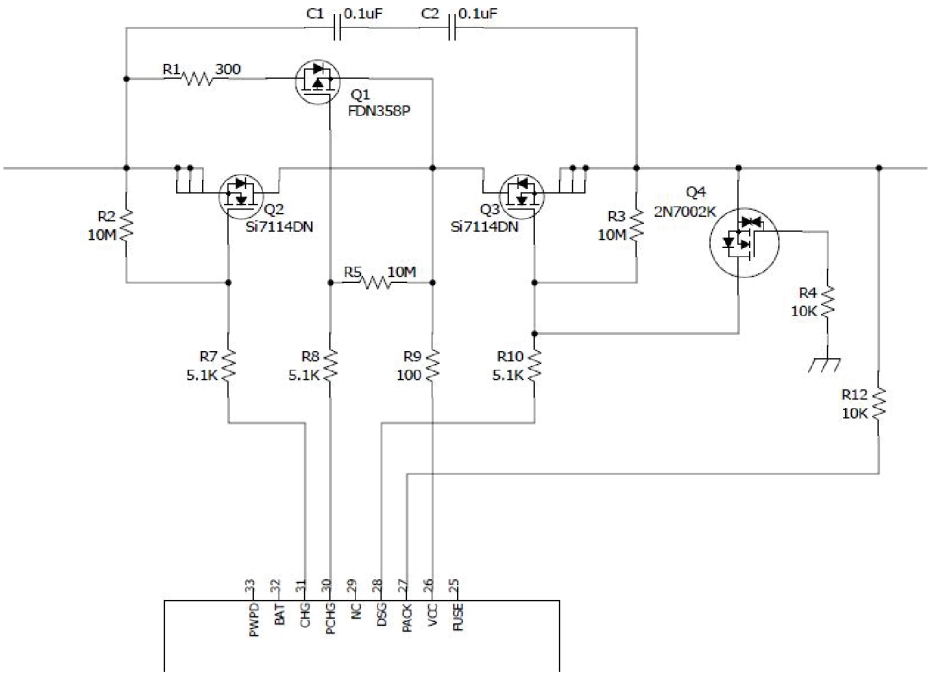


Figure 33. bq40z50 PACK and FET Control

The N-channel charge and discharge FETs are controlled with 5.1-kΩ series gate resistors, which provide a switching time constant of a few microseconds. The 10-MΩ resistors ensure that the FETs are off in the event of an open connection to the FET drivers. Q4 is provided to protect the discharge FET (Q3) in the event of a reverse-connected charger. Without Q4, Q3 can be driven into its linear region and suffer severe damage if the PACK+ input becomes slightly negative.

Q4 turns on in that case to protect Q3 by shorting its gate to source. To use the simple ground gate circuit, the FET must have a low gate turn-on threshold. If it is desired to use a more standard device, such as the 2N7002 as the reference schematic, the gate should be biased up to 3.3 V with a high-value resistor. The bq40z50 device has the capability to provide a current-limited charging path typically used for low battery voltage or low temperature charging. The bq40z50 device uses an external P-channel, pre-charge FET controlled by PCHG.

9.2.2.3.4 Temperature Output

For the bq40z50 device, TS1, TS2, TS3, and TS4 provide thermistor drive-under program control. Each pin can be enabled with an integrated 18-kΩ (typical) linearization pullup resistor to support the use of a 10-kΩ at 25°C (103) NTC external thermistor such as a Mitsubishi BN35-3H103. The reference design includes four 10-kΩ thermistors: RT1, RT2, RT3, and RT4. The bq40z50 device supports up to four external thermistors. Connect unused thermistor pins to V_{SS}.

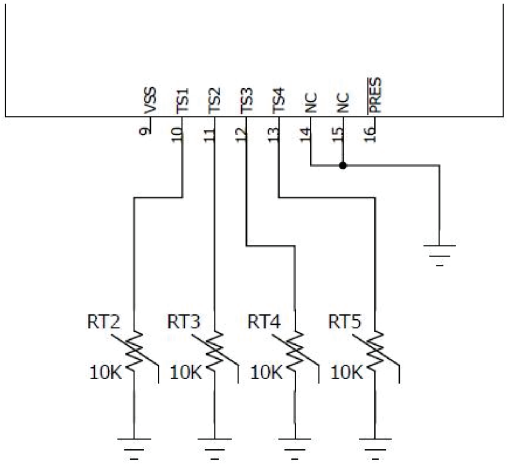


Figure 34. Thermistor Drive

9.2.2.3.5 LEDs

Three LED control outputs provide constant current sinks for the driving external LEDs. These outputs are configured to provide voltage and control for up to 5 LEDs. No external bias voltage is required. Unused LEDCNTL pins can remain open or they can be connected to V_{SS}. The DISP pin should be connected to V_{SS}, if the LED feature is not used.

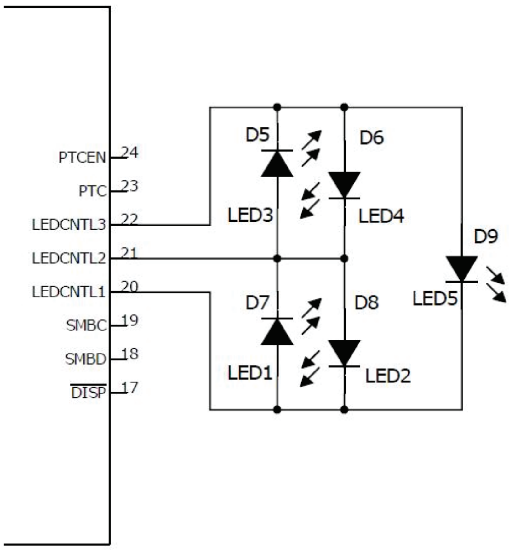


Figure 35. LEDs

9.2.2.3.6 Safety PTC Thermistor

The bq40z50 device provides support for a safety PTC thermistor. The PTC thermistor is connected between the PTC pin and V_{SS}. It can be placed close to the CHG/DSG FETs to monitor the temperature. The PTC pin outputs a very small current, typical ~370 nA, and the PTC fault will be triggered at ~0.7 V typical. A PTC fault is one of the permanent failure modes. It can only be cleared by a POR.

To disable this feature, connect a 10-kΩ resistor between PTC and V_{SS}.

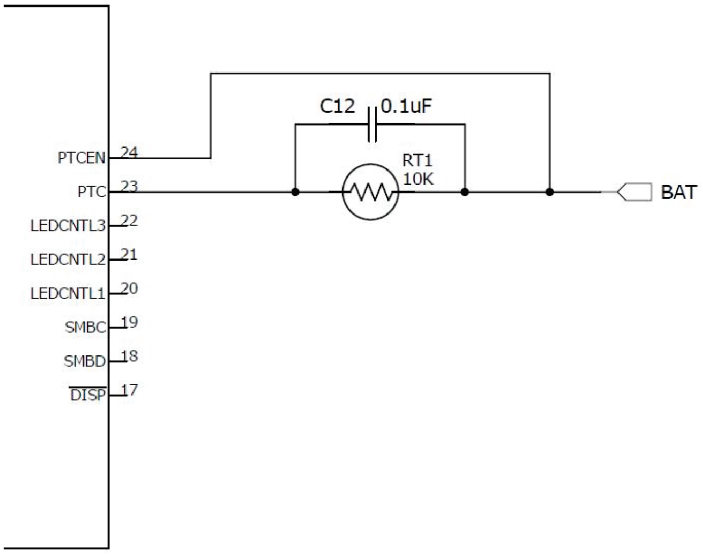
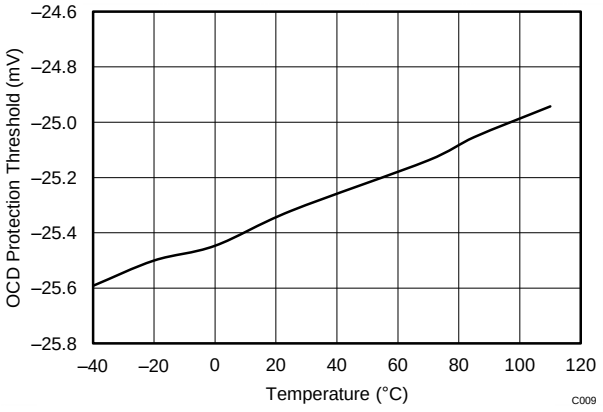


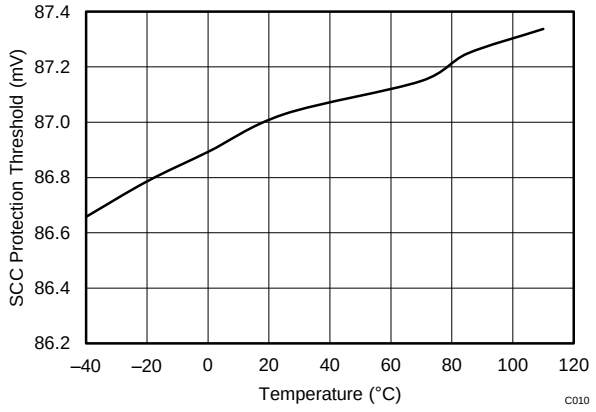
Figure 36. PTC Thermistor

9.2.3 Application Curves



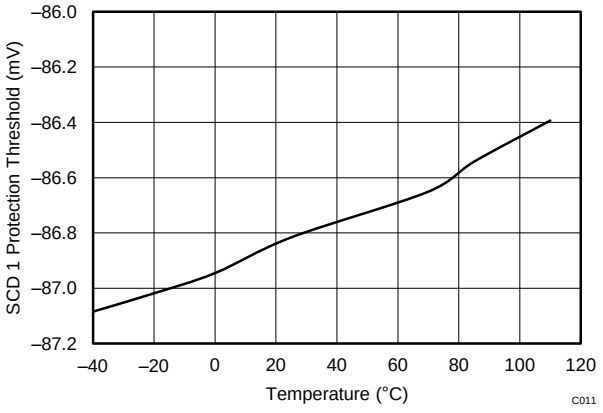
Threshold setting is 25 mV.

Figure 37. Overcurrent Discharge Protection Threshold Vs. Temperature



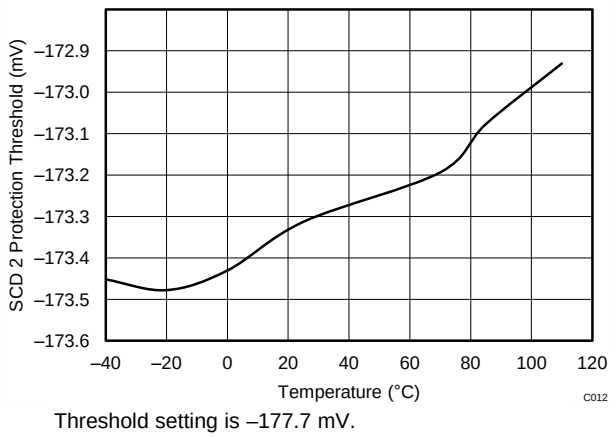
Threshold setting is 25 mV.

Figure 38. Short Circuit Charge Protection Threshold Vs. Temperature



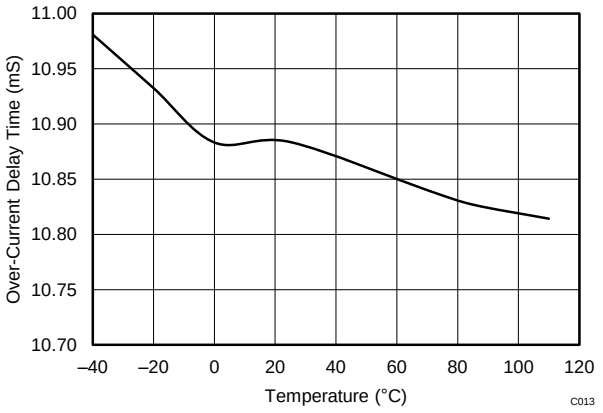
Threshold setting is –88.85 mV.

Figure 39. Short Circuit Discharge 1 Protection Threshold Vs. Temperature



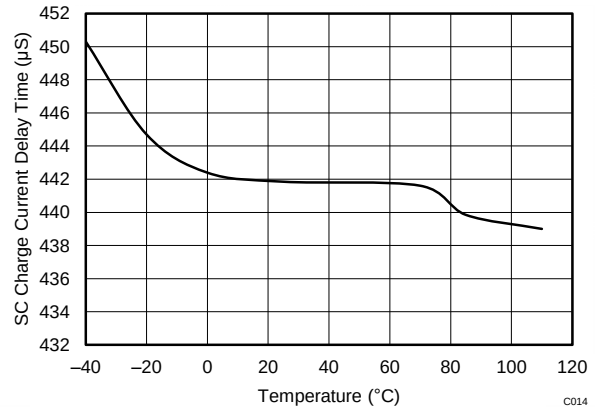
Threshold setting is –177.7 mV.

Figure 40. Short Circuit Discharge 2 Protection Threshold Vs. Temperature



Threshold setting is 11 ms.

Figure 41. Overcurrent Delay Time Vs. Temperature



Threshold setting is 465 µs.

Figure 42. Short Circuit Charge Current Delay Time Vs. Temperature

10 Power Supply Recommendations

The device manages its supply voltage dynamically according to the operation conditions. Normally, the BAT input is the primary power source to the device. The BAT pin should be connected to the positive termination of the battery stack. The input voltage for the BAT pin ranges from 2.2 V to 26 V.

The VCC pin is the secondary power input, which activates when the BAT voltage falls below minimum Vcc. This allows the device to source power from a charger (if present) connected to the PACK pin. The VCC pin should be connected to the common drain of the CHG and DSG FETs. The charger input should be connected to the PACK pin.

11 Layout

11.1 Layout Guidelines

A battery fuel gauge circuit board is a challenging environment due to the fundamental incompatibility of high-current traces and ultra-low current semiconductor devices. The best way to protect against unwanted trace-to-trace coupling is with a component placement, such as that shown in Figure 43, where the high-current section is on the opposite side of the board from the electronic devices. Clearly this is not possible in many situations due to mechanical constraints. Still, every attempt should be made to route high-current traces away from signal traces, which enter the bq40z50 directly. IC references and registers can be disturbed and in rare cases damaged due to magnetic and capacitive coupling from the high-current path. Note that during surge current and ESD events, the high-current traces appear inductive and can couple unwanted noise into sensitive nodes of the gas gauge electronics, as illustrated in Figure 44.

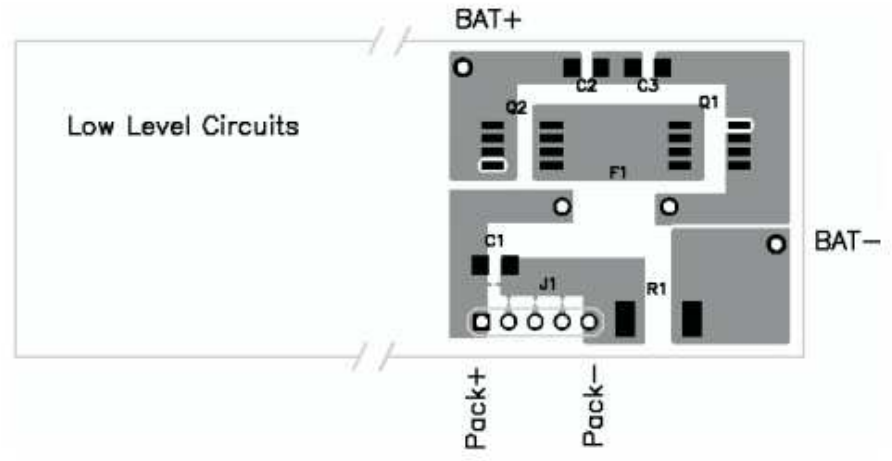


Figure 43. Separating High- and Low-Current Sections Provides an Advantage in Noise Immunity

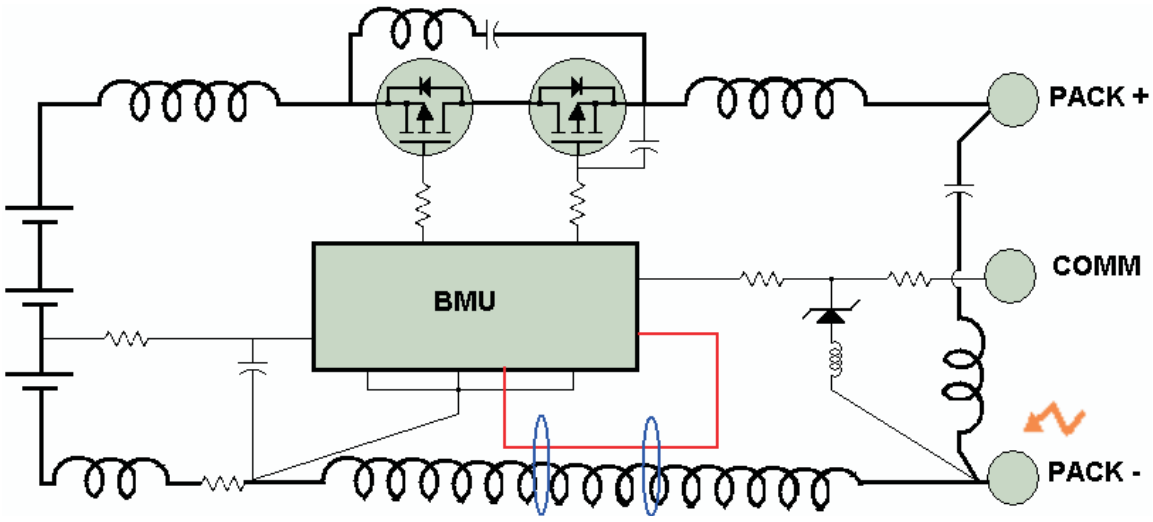


Figure 44. Avoid Close Spacing Between High-Current and Low-Level Signal Lines

Kelvin voltage sensing is extremely important in order to accurately measure current and top and bottom cell voltages. Place all filter components as close as possible to the device. Route the traces from the sense resistor in parallel to the filter circuit. Adding a ground plane around the filter network can add additional noise immunity. Figure 45 and Figure 46 demonstrates correct kelvin current sensing.

Layout Guidelines (continued)

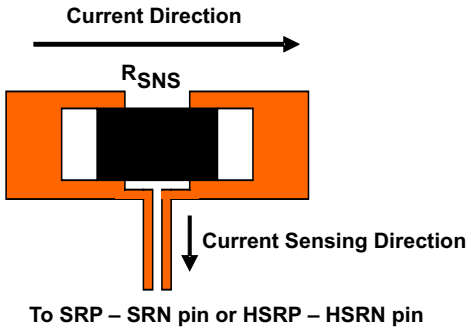


Figure 45. Sensing Resistor PCB Layout

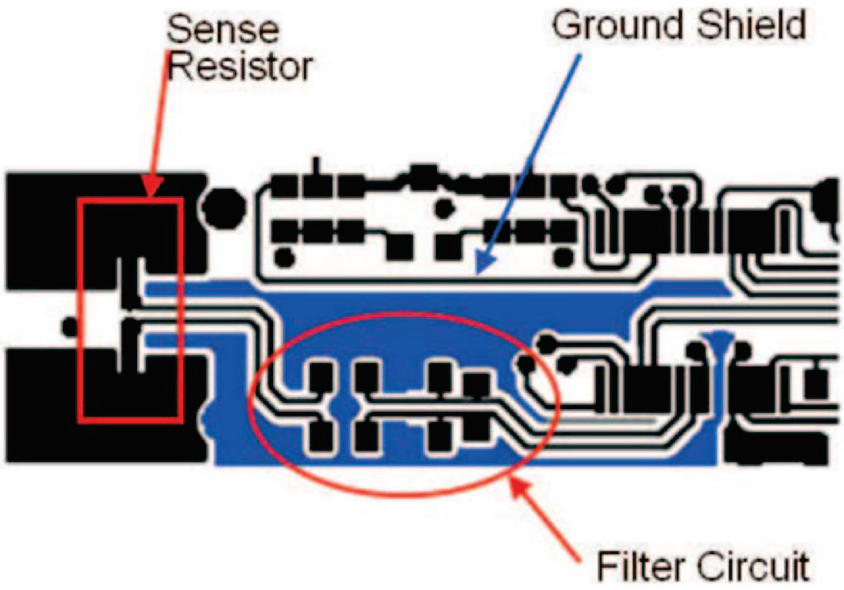


Figure 46. Sense Resistor, Ground Shield, and Filter Circuit Layout

11.1.1 Protector FET Bypass and Pack Terminal Bypass Capacitors

The general principle is to use wide copper traces to lower the inductance of the bypass capacitor circuit. In Figure 47, an example layout demonstrates this technique.

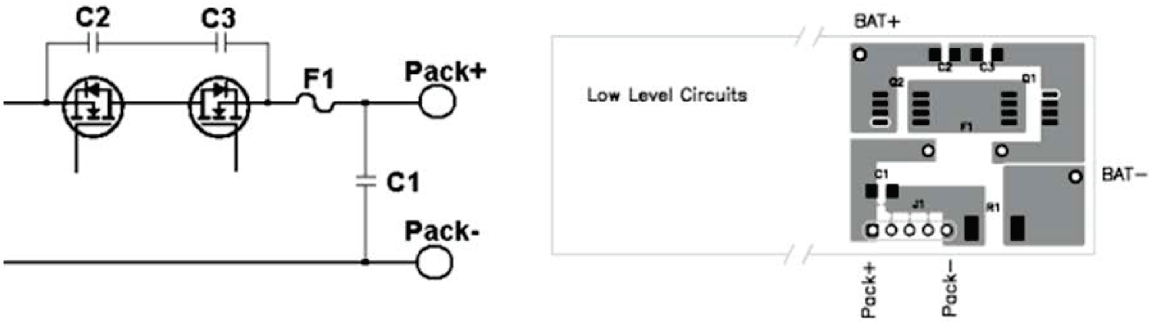


Figure 47. Use Wide Copper Traces to Lower the Inductance of Bypass Capacitors C1, C2, and C3

Layout Guidelines (continued)

11.1.2 ESD Spark Gap

Protect SMBus Clock, Data, and other communication lines from ESD with a spark gap at the connector. The pattern in Figure 48 recommended, with 0.2-mm spacing between the points.

Figure 48. Recommended Spark-Gap Pattern Helps Protect Communication Lines From ESD

11.2 Layout Example

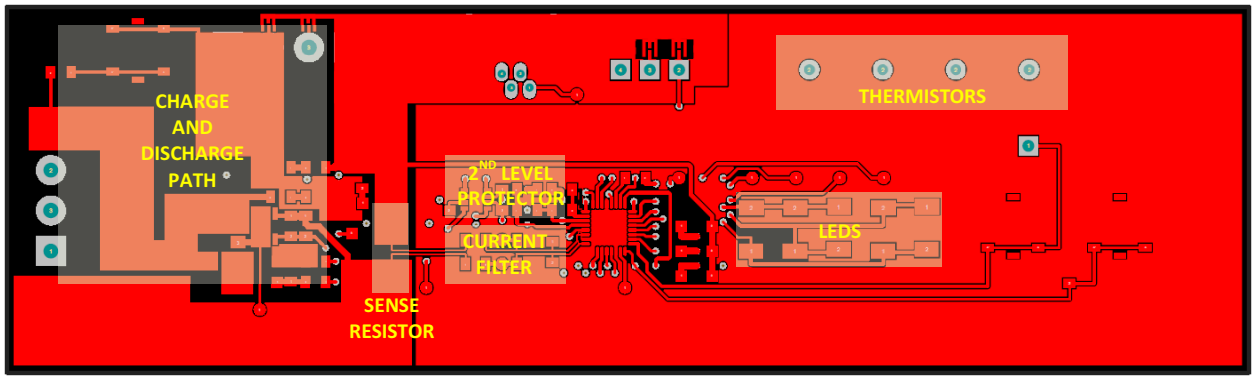


Figure 49. Top Layer

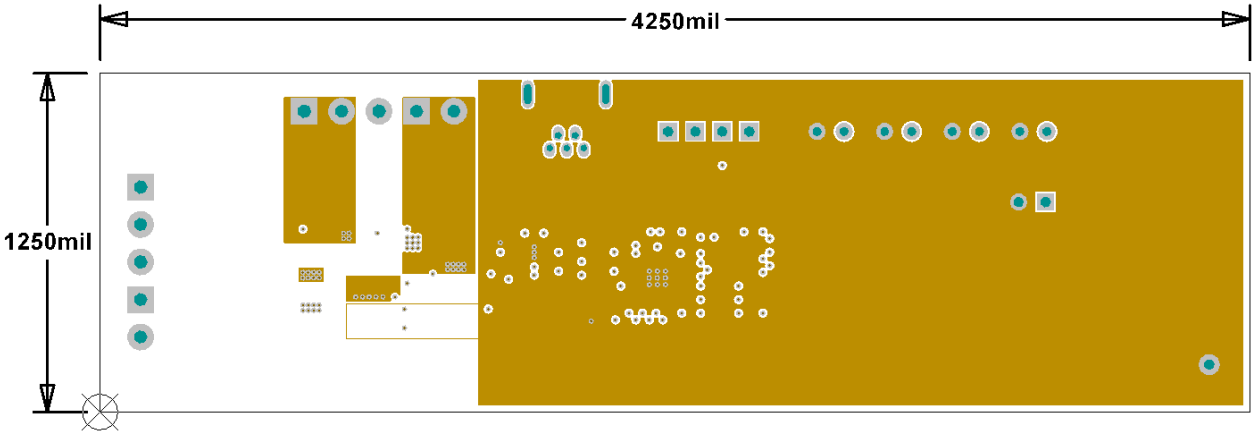


Figure 50. Internal Layer 1

Layout Example (continued)

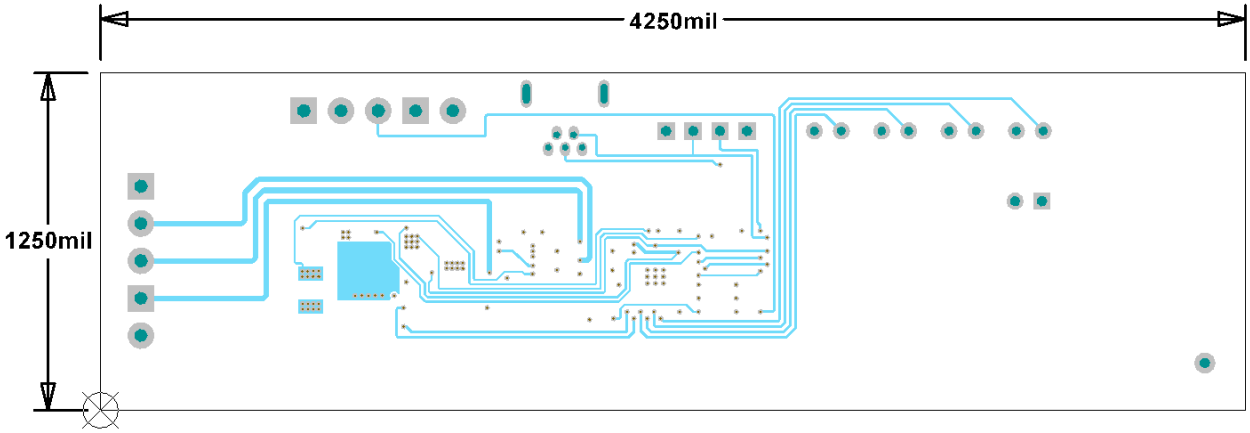


Figure 51. Internal Layer 2

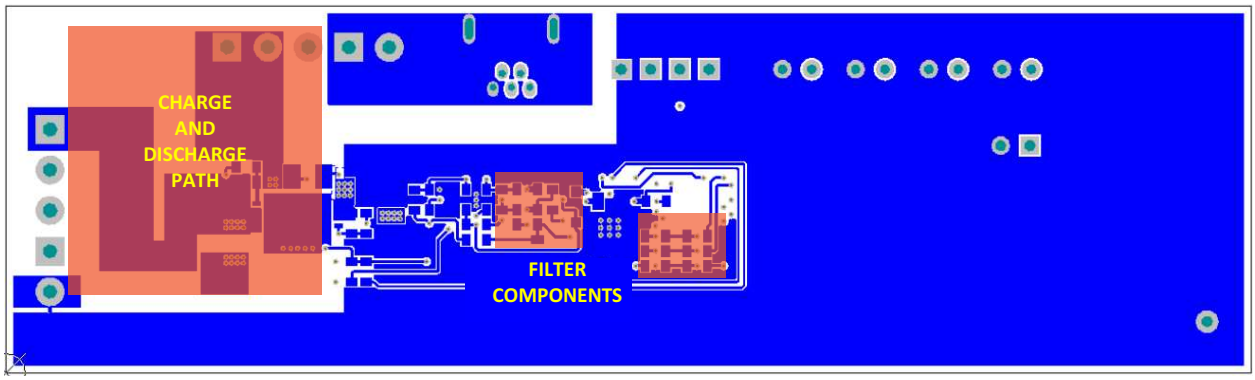


Figure 52. Bottom Layer

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the *bq40z50 Technical Reference Manual* (SLUUA43).

12.2 Trademarks

Impedance Track is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ40Z50RSMR	ACTIVE	VQFN	RSM	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ40Z50	Samples
BQ40Z50RSMT	ACTIVE	VQFN	RSM	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ40Z50	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

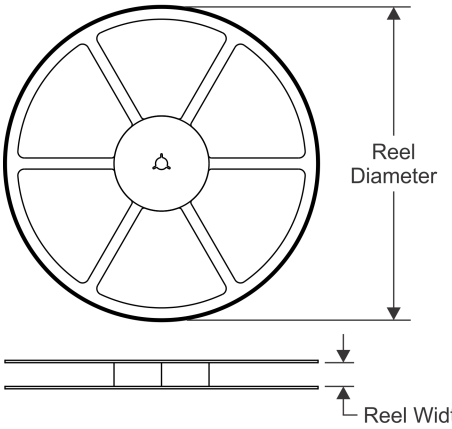
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

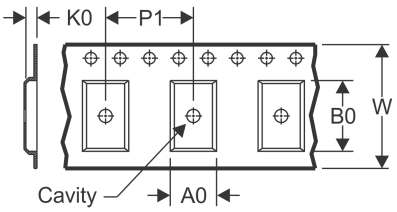
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

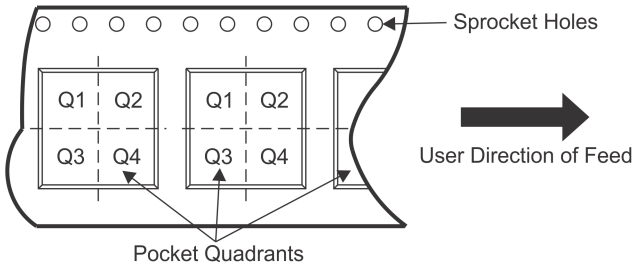


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

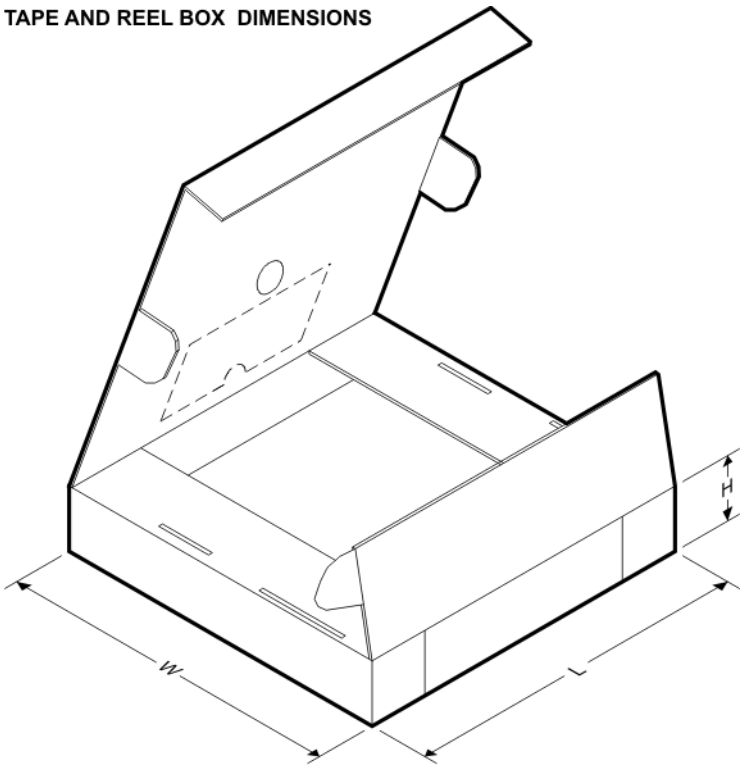
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ40Z50RSMR	VQFN	RSM	32	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
BQ40Z50RSMT	VQFN	RSM	32	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
BQ40Z50RSMT	VQFN	RSM	32	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

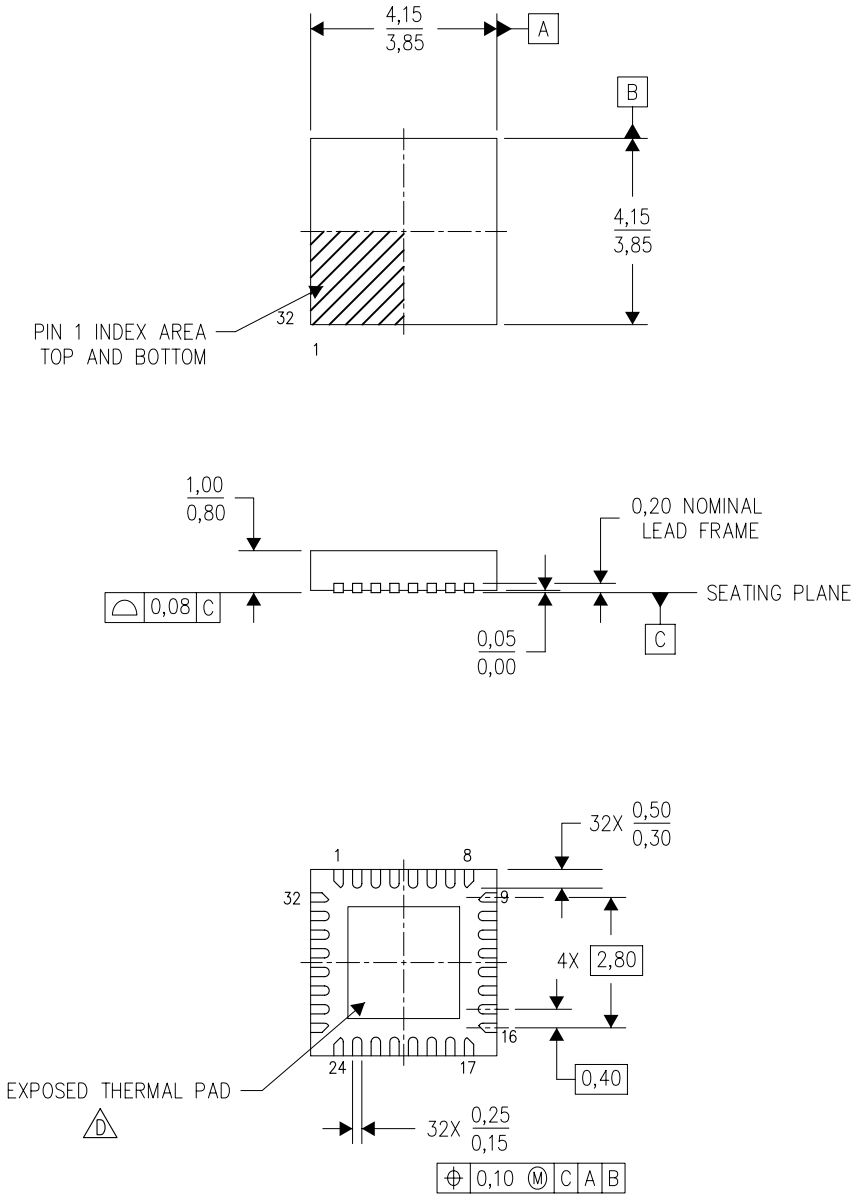
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ40Z50RSMR	VQFN	RSM	32	3000	367.0	367.0	35.0
BQ40Z50RSMT	VQFN	RSM	32	250	210.0	185.0	35.0
BQ40Z50RSMT	VQFN	RSM	32	250	210.0	185.0	35.0

RSM (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



4207560/B 03/10

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

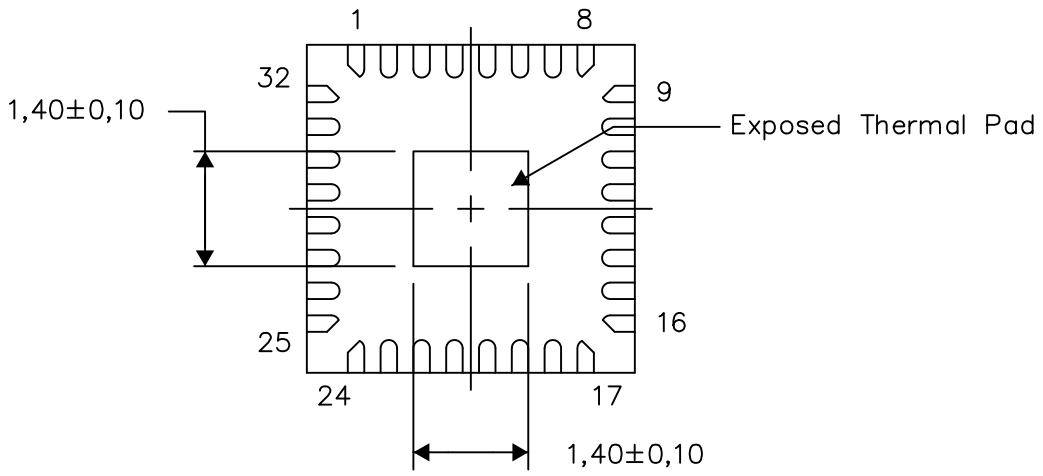
RSM (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

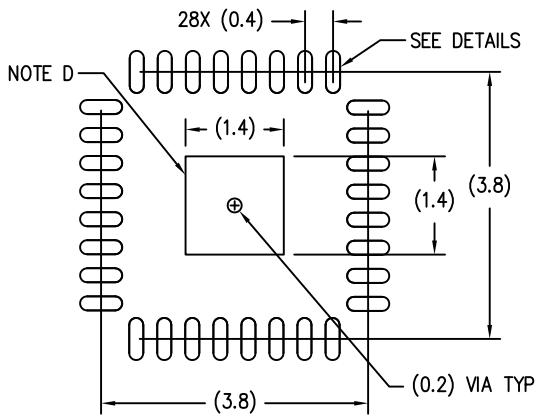
Exposed Thermal Pad Dimensions

4207868–3/I 07/14

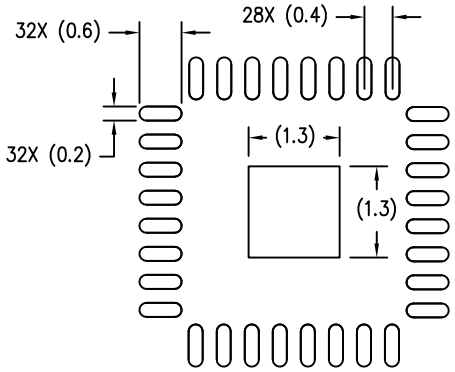
NOTE: All linear dimensions are in millimeters

RSM (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD

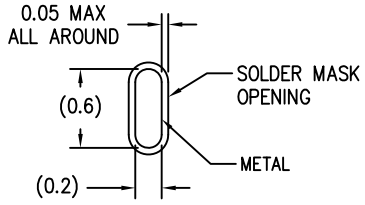
EXAMPLE BOARD LAYOUT



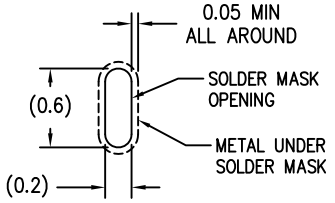
EXAMPLE STENCIL DESIGN
BASED ON 0.1 mm THICK STENCIL
(NOTE E)



86% PRINTED SOLDER COVERAGE BY AREA



NON SOLDER MASK DEFINED



SOLDER MASK DEFINED

SOLDER MASK DETAILS

4207134–4/J 11/14

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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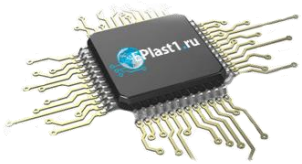
- Защита от снятия компонента с производства.



Как с нами связаться

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