VND600SP

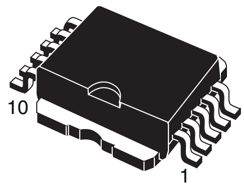
Double channel high-side solid state relay

Features

Type	$R_{DS(on)}$	I_{OUT}	V_{CC}
VND600SP	30mΩ(1)	25A(1)	36V

1. Per each channel.

- DC short circuit current: 25A
- CMOS compatible inputs
- Proportional load current sense
- Under-voltage and over-voltage shutdown
- Over-voltage clamp
- Thermal shutdown
- Current limitation
- Very low standby power consumption
- Protection against loss of ground and loss of V_{CC}
- Reverse battery protection



PowerSO-10

Description

The VND600SP is a monolithic device made using STMicroelectronics VIPower M0-3 technology. It is intended for driving resistive or inductive loads with one side connected to ground.

Active V_{CC} pin voltage clamp protects the device against low energy spikes (see ISO7637 transient compatibility table). This device has two channels in high-side configuration; each channel has an analog sense output on which the sensing current is proportional (according to a known ratio) to the corresponding load current.

Built-in thermal shutdown and outputs current limitation protect the chip from over-temperature and short circuit. Device turns-off in case of ground pin disconnection.

Table 1. Device summary

Package	Order codes	
	Tube	Tape and reel
PowerSO-10	VND600SP	VND600SP13TR

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1 Block diagram and pin description

Figure 1. Block diagram

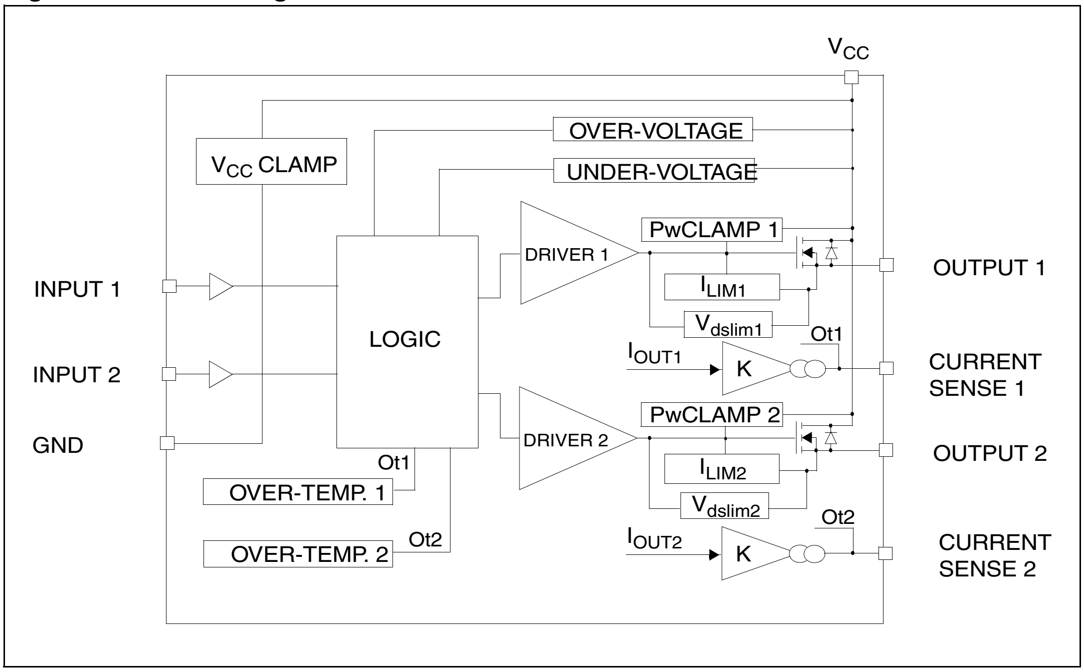


Figure 2. Configuration diagram (top view)

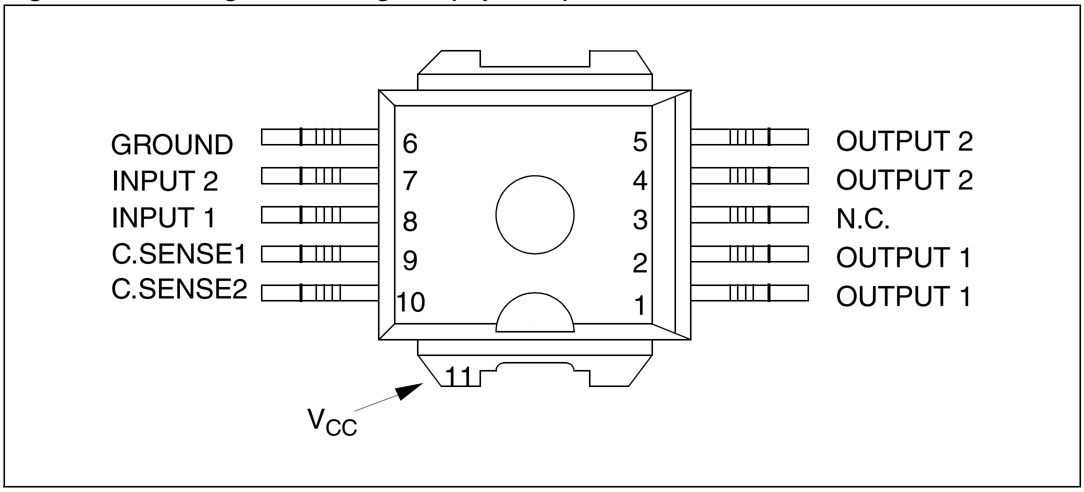
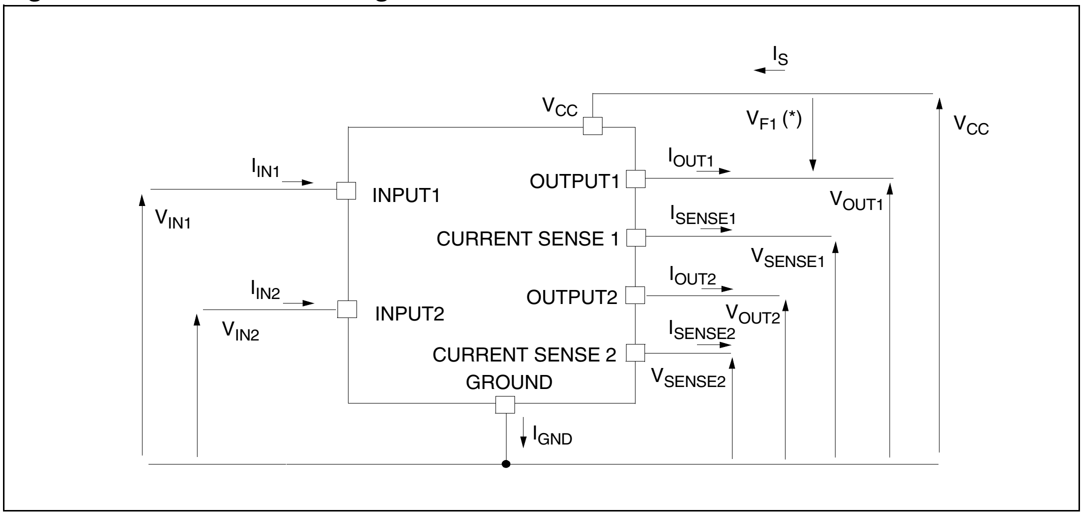


Table 2. Suggested connections for unused and not connected pins

Connection / pin	Current sense	N.C.	Output	Input
Floating		X	X	X
To ground	Through 10KΩ resistor	X		Through 10KΩ resistor

2 Electrical specifications

Figure 3. Current and voltage conventions



2.1 Absolute maximum ratings

Stressing the device above the rating listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality document.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	41	V
$-V_{CC}$	Reverse supply voltage	- 0.3	V
$- I_{GND}$	DC reverse ground pin current	- 200	mA
I_{OUT}	Output current	Internally limited	A
I_R	Reverse output current	- 21	A
I_{IN}	Input current	+/- 10	mA
V_{CSENSE}	Current sense maximum voltage	- 3 + 15	V V
V_{ESD}	Electrostatic discharge (human body model: R = 1.5KΩ; C = 100pF) - INPUT - CURRENT SENSE - OUTPUT - V_{CC}	 4000 2000 5000 5000	 V V V V

Table 3. Absolute maximum ratings (continued)

Symbol	Parameter	Value	Unit
E_{MAX}	Maximum switching energy ($L = 0.13mH$; $R_L = 0\Omega$; $V_{bat} = 13.5V$; $T_{jstart} = 150ºC$; $I_L = 40A$)	145	mJ
P_{tot}	Power dissipation at $T_c = 25°C$	96.1	W
T_j	Junction operating temperature	Internally limited	°C
T_c	Case operating temperature	-40 to 150	°C
T_{STG}	Storage temperature	-55 to 150	°C

2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Max. value		Unit
$R_{thj-case}$	Thermal resistance junction-case	1.3		°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient	51.3(1)	37(2)	°C/W

1. When mounted on a standard single-sided FR-4 board with $0.5cm^2$ of Cu (at least 35 µm thick).
2. When mounted on a standard single-sided FR-4 board with $6\ cm^2$ of Cu (at least 35 µm thick).

2.3 Electrical characteristics

Values specified in this section are for $8V < V_{CC} < 36V$; $-40°C < T_j < 150°C$, unless otherwise stated.

Table 5. Power

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}(1)	Operating supply voltage		5.5	13	36	V
V_{USD}(1)	Under-voltage shutdown		3	4	5.5	V
V_{OV}(1)	Over-voltage shutdown		36			V
R_{ON}	On-state resistance	$I_{OUT} = 5A$; $T_j = 25°C$ $I_{OUT} = 5A$; $T_j = 150°C$ $I_{OUT} = 3A$; $V_{CC} = 6V$			30 60 100	mΩ mΩ mΩ
V_{clamp}	Clamp voltage	$I_{CC} = 20mA$(2)	41	48	55	V
I_S(1)	Supply current	Off-state; $V_{CC}=13V$; $V_{IN}=V_{OUT}=0V$ Off-state; $V_{CC}=13V$; $V_{IN}=V_{OUT}=0V$; $T_j=25°C$ On-state; $V_{IN} = 5V$; $V_{CC} = 13V$; $I_{OUT} = 0A$; $R_{SENSE} = 3.9k\Omega$		12 12 	40 25 6	µA mA mA
$I_{L(off1)}$	Off-state output current	$V_{IN} = V_{OUT} = 0V$	0		50	µA

Table 5. Power (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{L(off2)}$	Off-state output current	V_{IN} = 0V; V_{OUT} = 3.5V	-75		0	μA
$I_{L(off3)}$	Off-state output current	V_{IN} = V_{OUT}=0V; V_{CC}=13V; T_j =125°C			5	μA
$I_{L(off4)}$	Off-state output current	V_{IN} =V_{OUT} = 0V; V_{CC} = 13V; T_j = 25°C			3	μA

1. Per device.
2. V_{clamp} and V_{OV} are correlated. Typical difference is 5V.

Table 6. Protections

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{lim}	DC short circuit current	V_{CC} = 13V 5.5V < V_{CC} < 36V	25	40	70 70	A A
T_{TSD}	Thermal shutdown temperature		150	175	200	°C
T_R	Thermal reset temperature		135			°C
T_{HYST}	Thermal hysteresis		7	15		°C
V_{demag}	Turn-off output voltage clamp	I_{OUT} = 2A; V_{IN} = 0V; L = 6mH	V_{CC}-41	V_{CC}-48	V_{CC}-55	V
V_{ON}	Output voltage drop limitation	I_{OUT} = 0.5A T_j = -40°C...+150°C		50		mV

Note: To ensure long term reliability under heavy over-load or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles.

Table 7. V_{CC} - output diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_F	Forward on voltage	- I_{OUT} = 2.6A; T_j = 150°C			0.6	V

Table 8. Current sense (9V $\leq V_{CC} \leq$16V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
K_1	I_{OUT}/I_{SENSE}	I_{OUT1} or I_{OUT2} = 0.5A; V_{SENSE} = 0.5V; other channels open; T_j = -40°C...150°C	3300	4400	6000	
dK_1/K_1	Current sense ratio drift	I_{OUT1} or I_{OUT2} = 0.5A; V_{SENSE} = 0.5V; other channels open; T_j= - 40°C...150°C	-10		+10	%
K_2	I_{OUT}/I_{SENSE}	I_{OUT1} or I_{OUT2} = 5A; V_{SENSE} = 4V; other channels open; T_j = - 40°C T_j= 25°C...150°C	 4200 4400	 4900 4900	 6000 5750	
dK_2/K_2	Current sense ratio drift	I_{OUT1} or I_{OUT2} = 5A; V_{SENSE} = 4V; other channels open; T_j = -40°C...150°C	-6		+6	%
K_3	I_{OUT}/I_{SENSE}	I_{OUT1} or I_{OUT2} = 15A; V_{SENSE} = 4V; other channels open; T_j = -40°C T_j = 25°C...150°C	 4200 4400	 4900 4900	 5500 5250	
dK_3/K_3	Current sense ratio drift	I_{OUT1} or I_{OUT2} = 15A; V_{SENSE} = 4V; other channels open; T_j = -40°C...150°C	-6		+6	%
$V_{SENSE1,2}$	Max analog sense output voltage	V_{CC} = 5.5V; $I_{OUT1,2}$ = 2.5A; R_{SENSE} = 10kΩ V_{CC} > 8V, $I_{OUT1,2}$ = 5A; R_{SENSE} = 10kΩ	2 4			V V
V_{SENSEH}	Analog sense output voltage in over-temperature condition	V_{CC} = 13V; R_{SENSE} = 3.9kΩ		5.5		V
$R_{VSENSEH}$	Analog sense output impedance in over-temperature condition	V_{CC} = 13V; T_j > T_{TSD}; all channels open		400		Ω
t_{DSENSE}	Current sense delay response	To 90% I_{SENSE} [1]			500	µs

1. Current sense signal delay after positive input slope.

Table 9. Logic inputs

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input low level voltage				1.25	V
I_{IL}	Low level input current	V_{IN} = 1.25V	1			µA
V_{IH}	Input high level voltage		3.25			V
I_{IH}	High level input current	V_{IN} = 3.25V			10	µA
$V_{I(hyst)}$	Input hysteresis voltage		0.5			V
V_{ICL}	Input clamp voltage	I_{IN} = 1mA I_{IN} = - 1mA	6	6.8 -0.7	8	V V

Table 10. Switching (V_{CC} = 13V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	R_L= 2.6Ω (see *Figure 4.*)		30		µs
$t_{d(off)}$	Turn-on delay time	R_L = 2.6Ω (see *Figure 4.*)		30		µs
$(dV_{OUT}/dt)_{on}$	Turn-on voltage slope	R_L = 2.6Ω (see *Figure 4.*)		See *Figure 10.*		V/ µs
$(dV_{OUT}/dt)_{off}$	Turn-off voltage slope	R_L = 2.6Ω (see *Figure 4.*)		See *Figure 12.*		V/ µs

Table 11. Truth table

Conditions	Input	Output	Sense
Normal operation	L H	L H	0 Nominal
Over-temperature	L H	L L	0 V_{SENSEH}
Under-voltage	L H	L L	0 0
Over-voltage	L H	L L	0 0
Short circuit to GND	L H H	L L L	0 (T_j<T_{TSD}) 0 (T_j>T_{TSD}) V_{SENSEH}
Short circuit to V_{CC}	L H	H H	0 < Nominal
Negative output voltage clamp	L	L	0

Table 12. Electrical transient requirements

ISO T/R 7637/1 Test pulse	Test level				
	I	II	III	IV	Delays and impedance
1	- 25V(1)	- 50V(1)	- 75V(1)	- 100V(1)	2ms, 10Ω
2	+ 25V(1)	+ 50V(1)	+ 75V(1)	+ 100V(1)	0.2ms, 10Ω
3a	- 25V(1)	- 50V(1)	- 100V(1)	- 150V(1)	0.1µs, 50Ω
3b	+ 25V(1)	+ 50V(1)	+ 75V(1)	+ 100V(1)	0.1µs, 50Ω
4	- 4V(1)	- 5V(1)	- 6V(1)	- 7V(1)	100ms, 0.01Ω
5	+ 26.5V(1)	+ 46.5V(2)	+ 66.5V(2)	+ 86.5V(2)	400ms, 2Ω

1. All functions of the device are performed as designed after exposure to disturbance.
2. One or more functions of the device is not performed as designed after exposure and cannot be returned to proper operation without replacing the device.

Figure 4. Switching characteristics

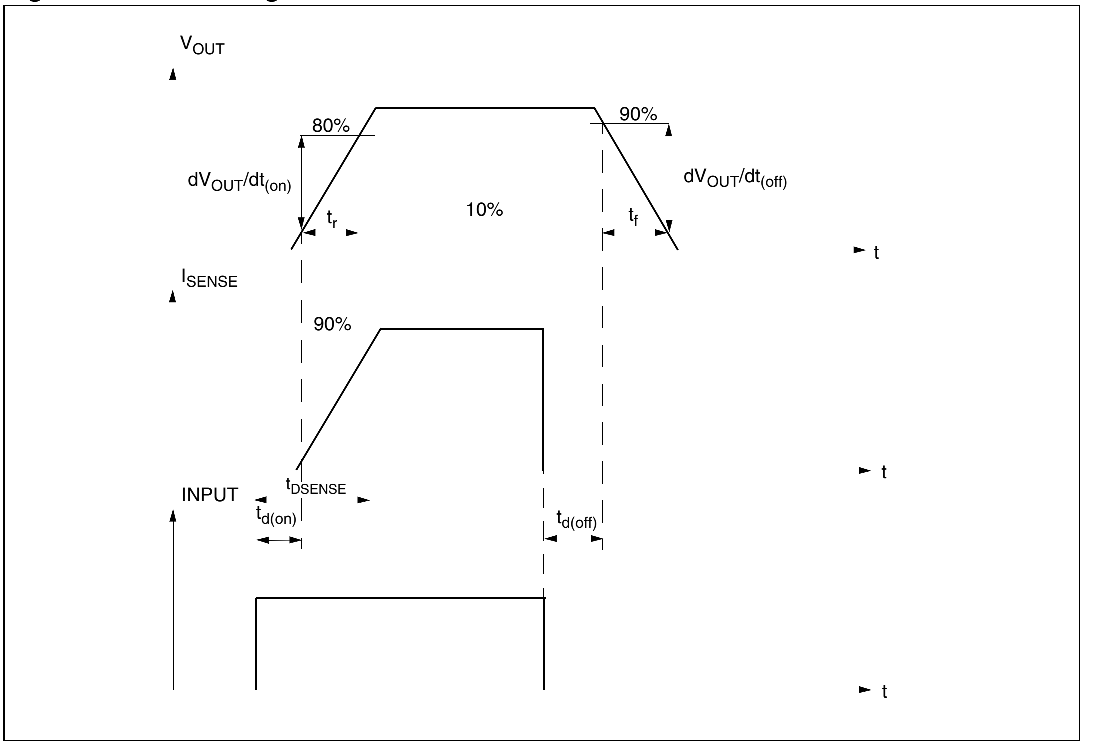


Figure 5. I_{OUT}/I_{SENSE} versus I_{OUT}

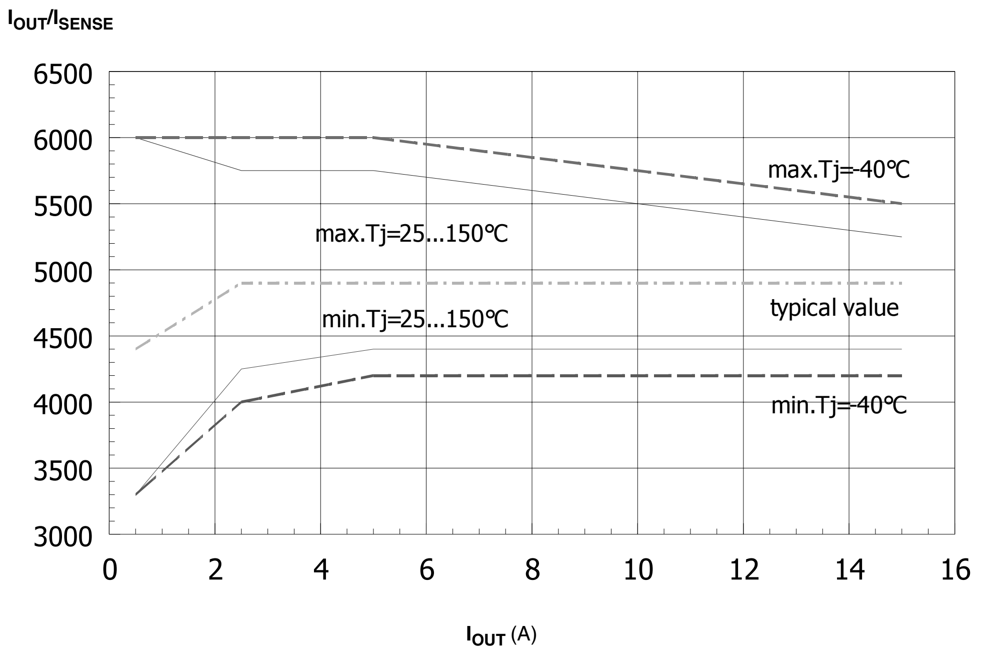
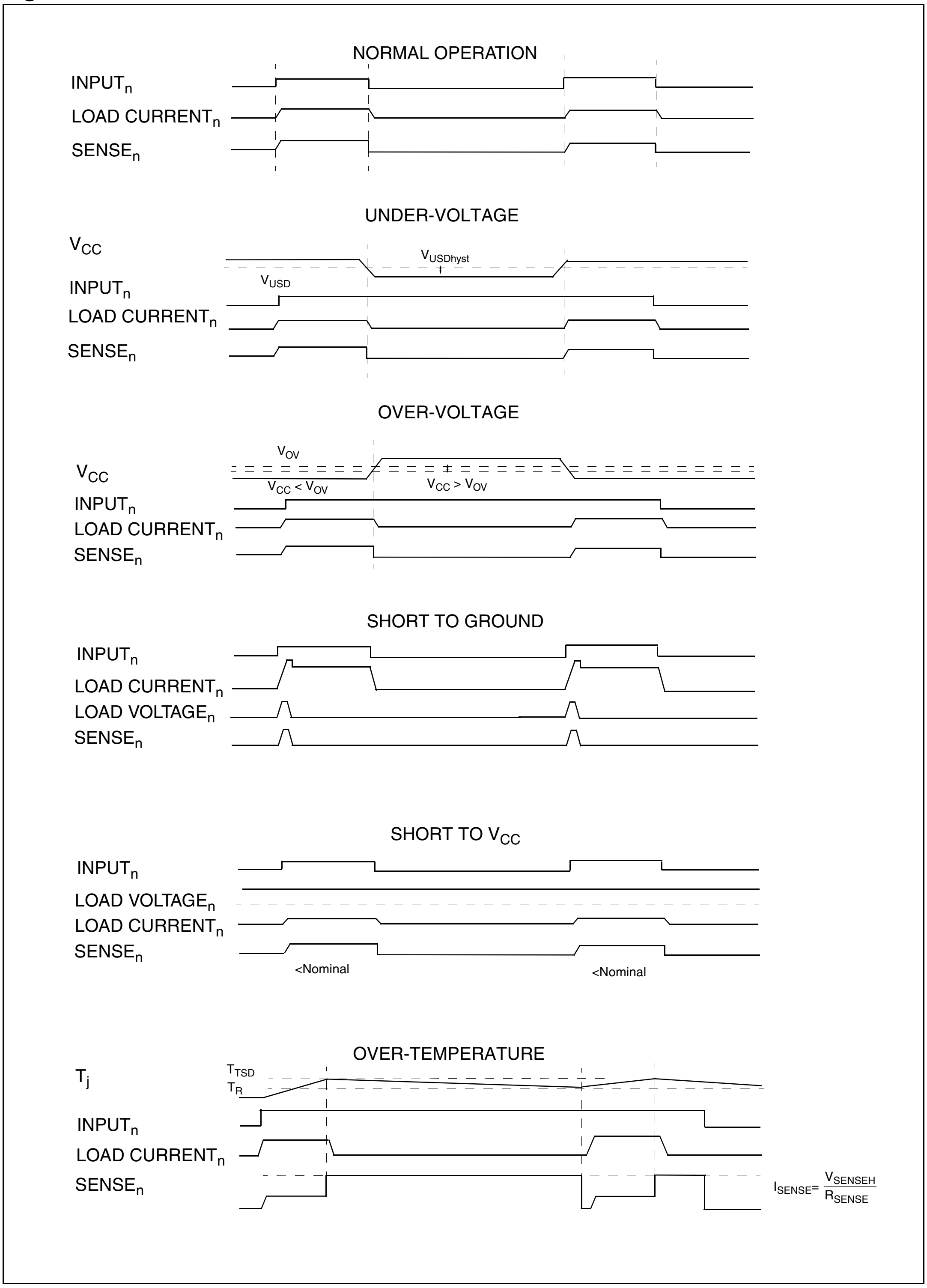


Figure 6. Waveforms



2.4 Electrical characteristics curves

Figure 7. Off-state output current

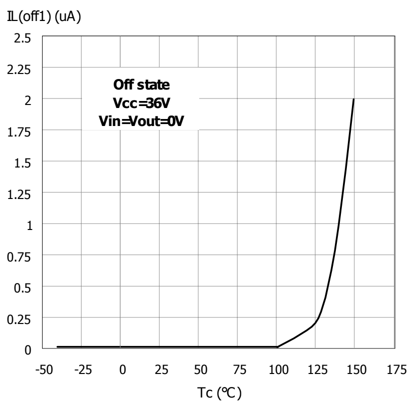


Figure 8. High level input current

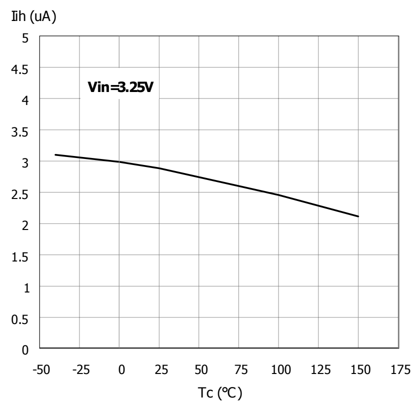


Figure 9. Input clamp voltage

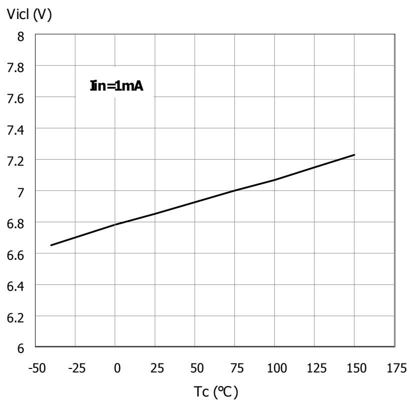


Figure 10. Turn-on voltage slope

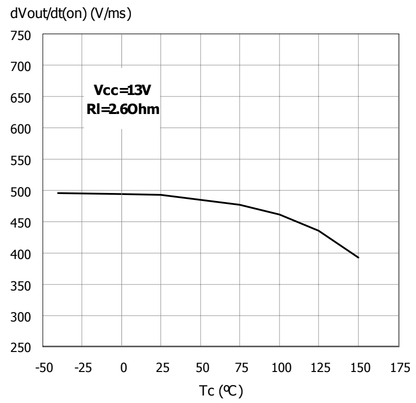


Figure 11. Over-voltage shutdown

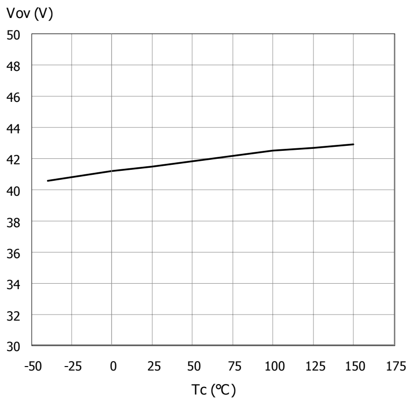


Figure 12. Turn-off voltage slope

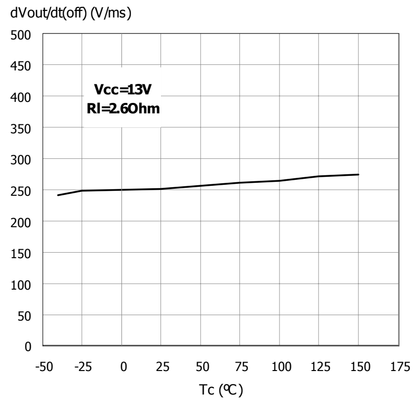


Figure 13. I_{LIM} vs T_{case}

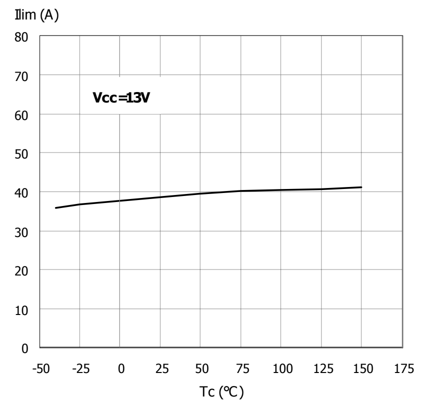


Figure 14. On-state resistance vs V_{CC}

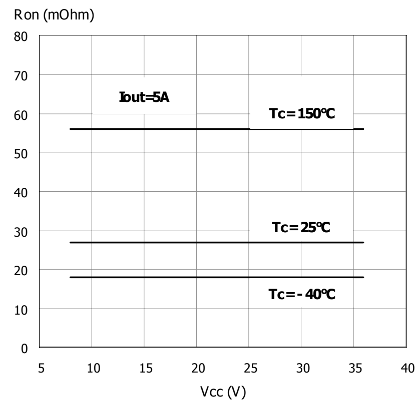


Figure 15. Input high level

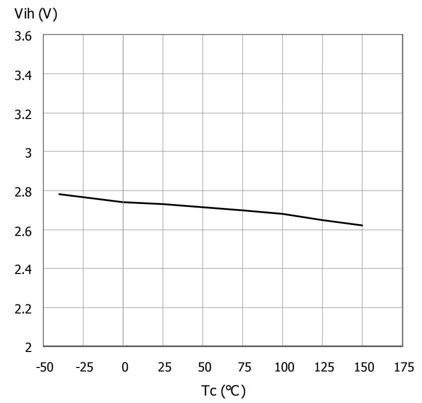


Figure 16. Input hysteresis voltage

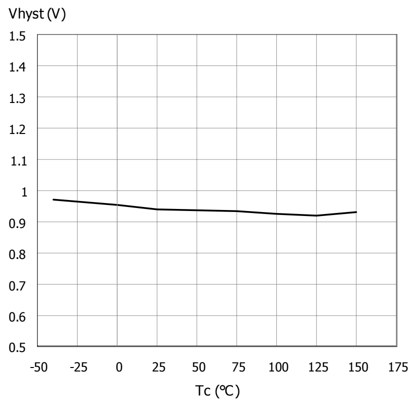


Figure 17. On-state resistance vs Tcase

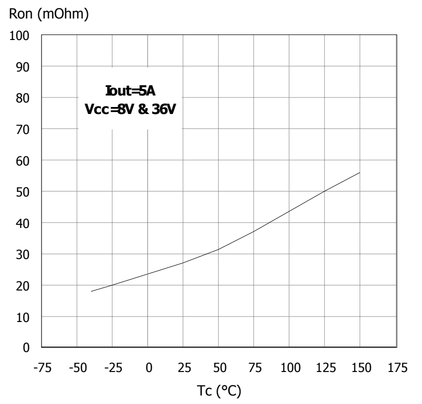
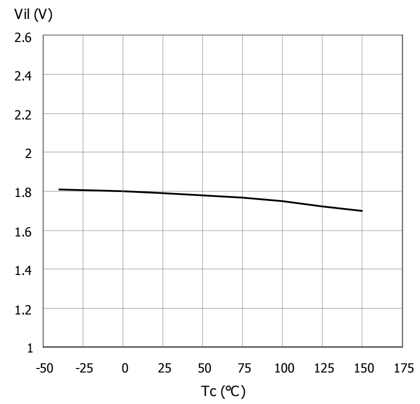
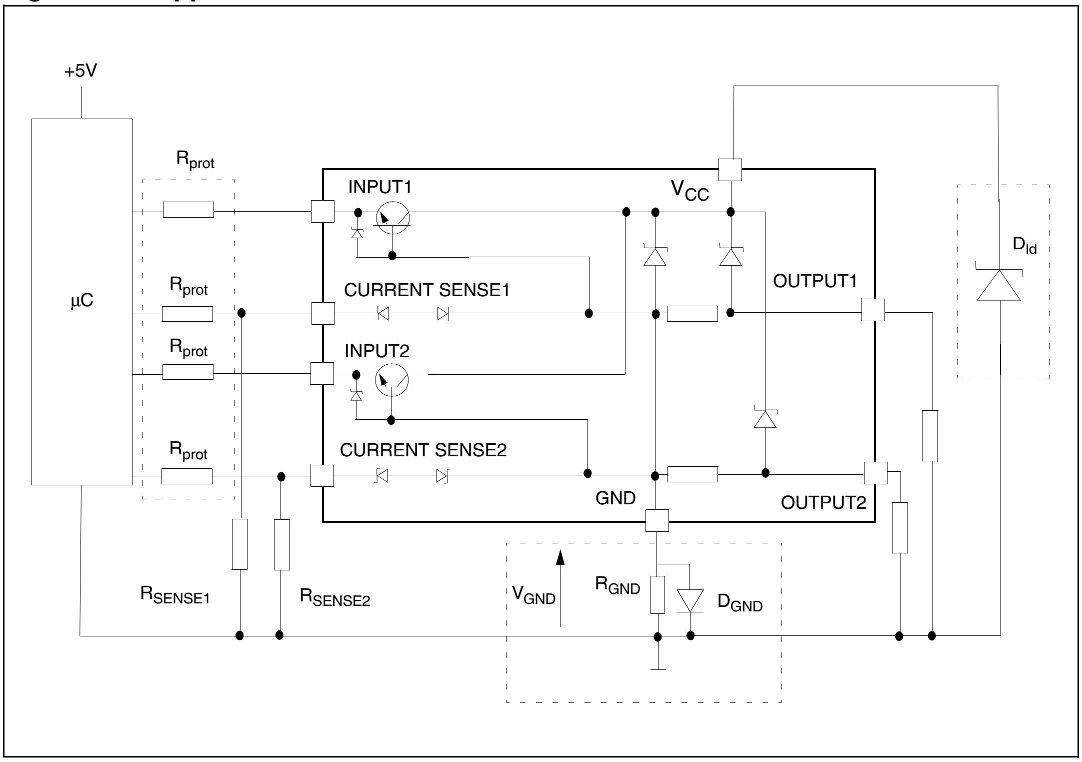


Figure 18. Input low level



3 Application information

Figure 19. Application schematic



3.1 GND protection network against reverse battery

This section provides two solutions for implementing a ground protection network against reverse battery.

3.1.1 Solution 1: a resistor in the ground line (R_{GND} only)

This can be used with any type of load.

The following show how to dimension the R_{GND} resistor:

1. $R_{GND} \leq 600mV / 2 (I_{S(on)max})$
2. $R_{GND} \geq (- V_{CC}) / (- I_{GND})$

where - I_{GND} is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device datasheet.

Power dissipation in R_{GND} (when $V_{CC} < 0$ during reverse battery situations) is:

$$P_D = (- V_{CC})^2 / R_{GND}$$

This resistor can be shared amongst several different HSDs. Please note that the value of this resistor should be calculated with formula (1) where $I_{S(on)max}$ becomes the sum of the maximum on-state currents of the different devices.

Please note that, if the microprocessor ground is not shared by the device ground, then the R_{GND} will produce a shift ($I_{S(on)max}$ * R_{GND}) in the input thresholds and the status output values. This shift will vary depending on how many devices are ON in the case of several high-side drivers sharing the same R_{GND} .

If the calculated power dissipation requires the use of a large resistor, or several devices have to share the same resistor, then ST suggests using solution 2 below.

3.1.2 Solution 2: a diode (D_{GND}) in the ground line

A resistor (R_{GND} = 1kΩ) should be inserted in parallel to D_{GND} if the device will be driving an inductive load. This small signal diode can be safely shared amongst several different HSD. Also in this case, the presence of the ground network will produce a shift (j600mV) in the input threshold and the status output values if the microprocessor ground is not common with the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network. Series resistor in INPUT and STATUS lines are also required to prevent that, during battery voltage transient, the current exceeds the Absolute Maximum Rating. Safest configuration for unused INPUT and STATUS pin is to leave them unconnected.

3.2 Load dump protection

D_{ld} is necessary (voltage transient suppressor) if the load dump peak voltage exceeds the V_{CC} maximum DC rating. The same applies if the device is subject to transients on the V_{CC} line that are greater than those shown in the ISO T/R 7637/1 table.

3.3 MCU I/O protection

If a ground protection network is used and negative transients are present on the V_{CC} line, the control pins will be pulled negative. ST suggests to insert a resistor (R_{prot}) in line to prevent the µC I/O pins from latching up.

The value of these resistors is a compromise between the leakage current of µC and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of µC I/Os:

$-V_{CCpeak} / I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$

Example

For the following conditions:

$V_{CCpeak} = -100V$

$I_{latchup} \geq 20mA$

$V_{OH\mu C} \geq 4.5V$

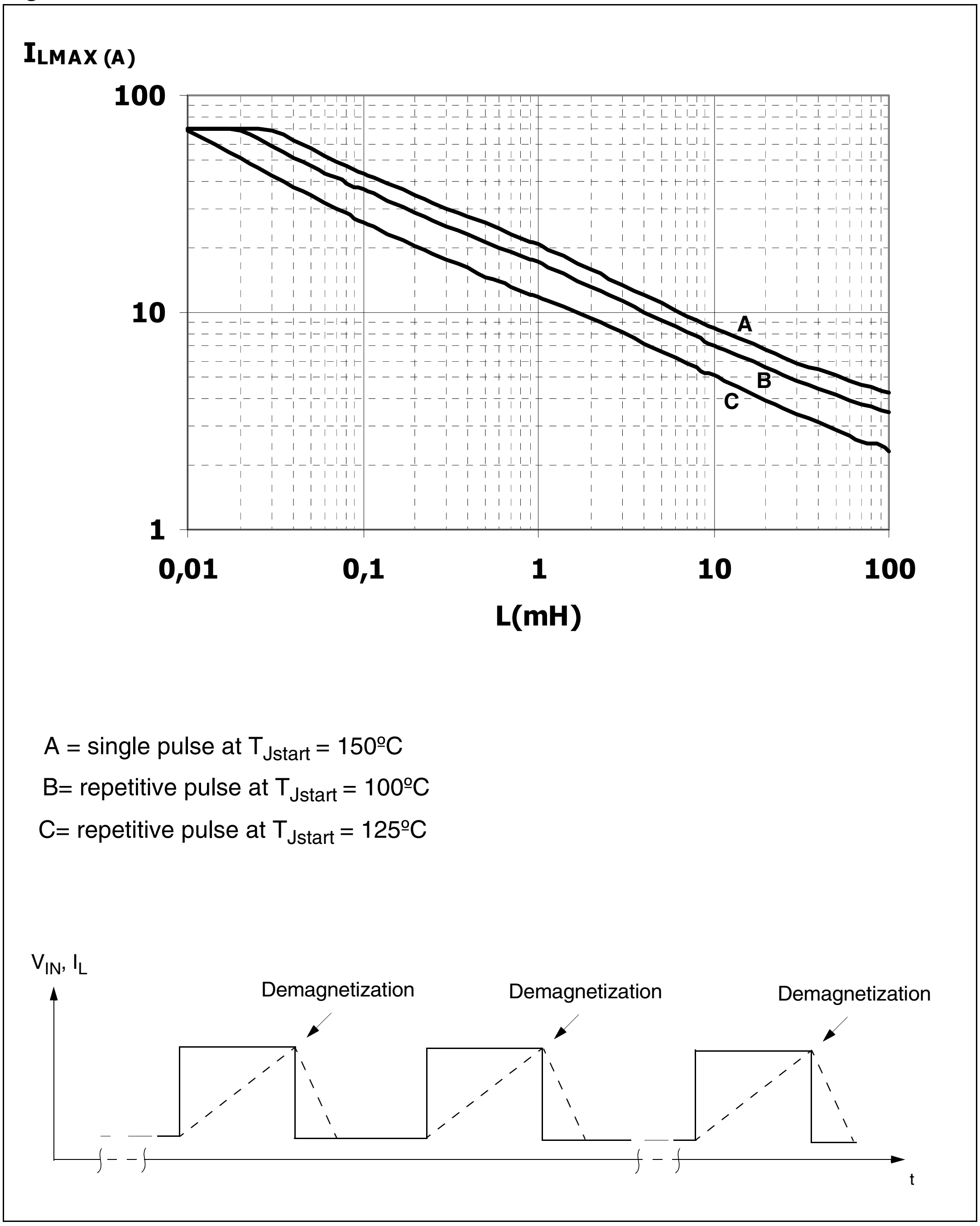
$5k\Omega \leq R_{prot} \leq 65k\Omega$

Recommended values are:

$R_{prot} = 10k\Omega$

3.4 Maximum demagnetization energy (V_{CC} = 13.5V)

Figure 20. Maximum turn-off current versus load inductance



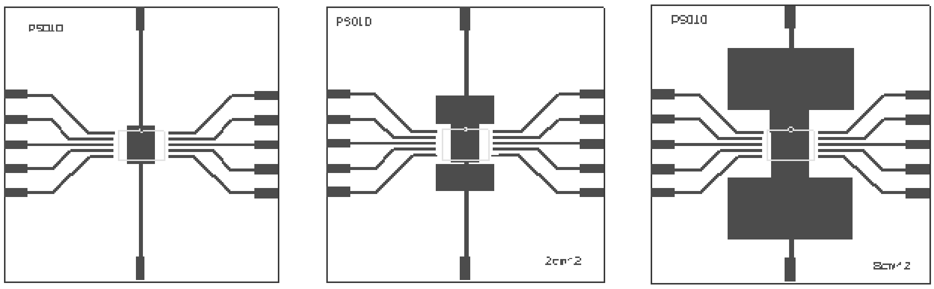
Note: *Values are generated with $R_L = 0\Omega$.*

In case of repetitive pulses, T_{jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves B and C.

4 Package and PCB thermal data

4.1 PowerSO-10 thermal data

Figure 21. PowerSO-10 PC board



Note: *Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area = 58mm x 58mm, PCB thickness = 2mm, Cu thickness = 35µm, Copper areas: from minimum pad-lay-out to 8cm^2).*

Figure 22. $R_{thj-amb}$ Vs PCB copper area in open box free air condition

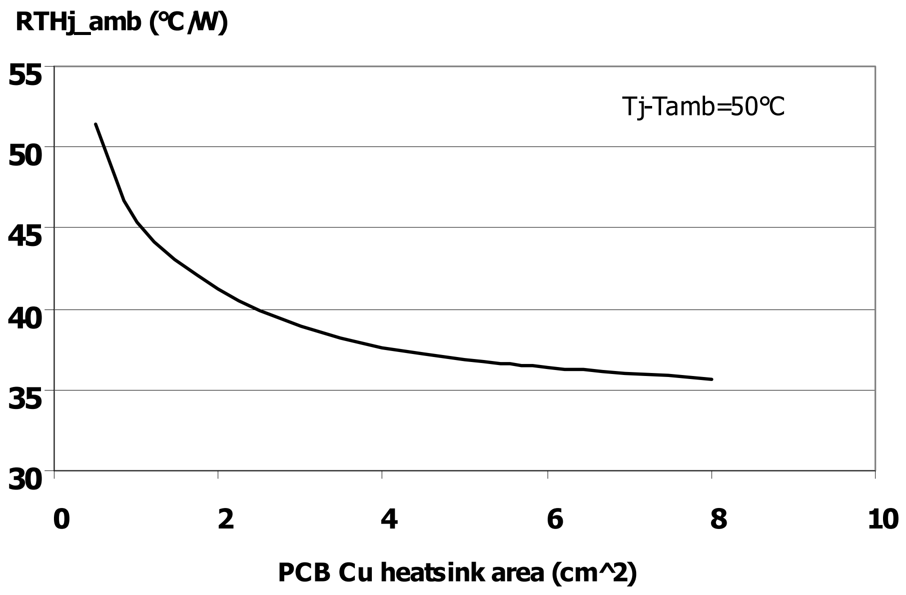
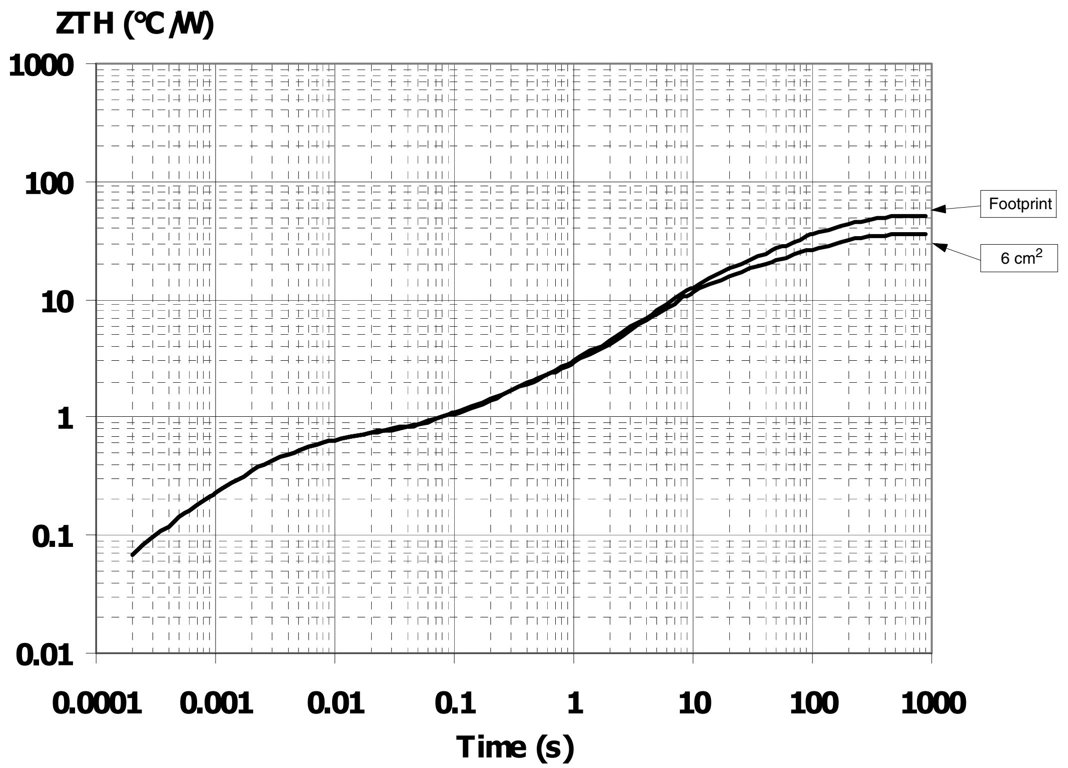


Figure 23. Thermal impedance junction ambient single pulse



Equation 1: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p / T$

Figure 24. Thermal fitting model of a quad channel HSD in PowerSO-10

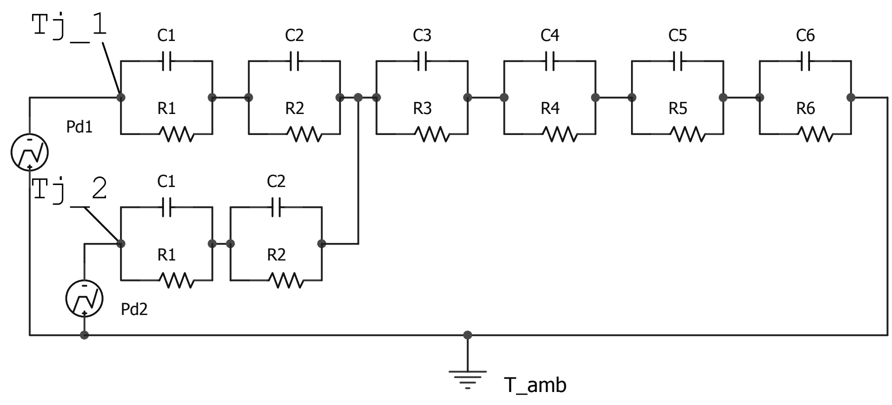


Table 13. Thermal parameters

Area / island (cm^2)	Footprint	6
R1 (°C/W)	0.05	
R2 (°C/W)	0.3	
R3 (°C/W)	0.3	
R4 (°C/W)	0.8	
R5 (°C/W)	12	
R6 (°C/W)	37	22
C1 (W.s/°C)	0.001	
C2 (W.s/°C)	5E-03	
C3 (W.s/°C)	0.02	
C4 (W.s/°C)	0.3	
C5 (W.s/°C)	0.75	
C6 (W.s/°C)	3	5

5 Package and packing information

5.1 ECOPACK® packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

5.2 PowerSO-10 mechanical data

Figure 25. PowerSO-10 package dimensions

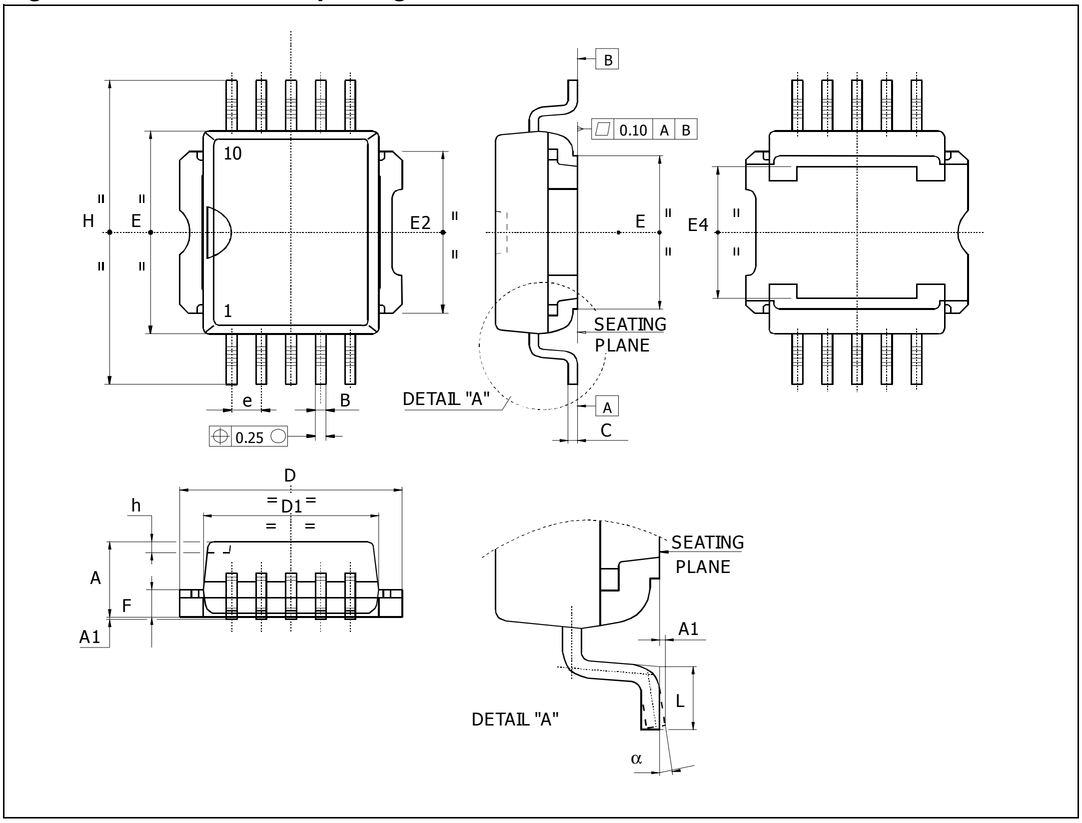


Table 14. PowerSO-10 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	3.35		3.65
A(1)	3.4		3.6
A1	0		0.10
B	0.40		0.60
B(1)	0.37		0.53
C	0.35		0.55
C(1)	0.23		0.32
D	9.40		9.60
D1	7.40		7.60
E	9.30		9.50
E2	7.20		7.60
E2(1)	7.30		7.50
E4	5.90		6.10
E4(1)	5.90		6.30
e		1.27	
F	1.25		1.35
F(1)	1.20		1.40
H	13.80		14.40
H(1)	13.85		14.35
h		0.50	
L	1.20		1.80
L(1)	0.80		1.10
α	0°		8°
α(1)	2°		8°

1. Muar only POA P013P.

5.3 PowerSO-10 packing information

Figure 26. PowerSO-10 suggested pad layout

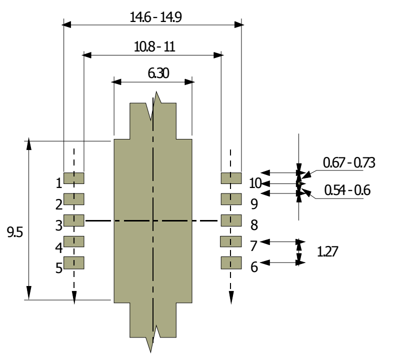
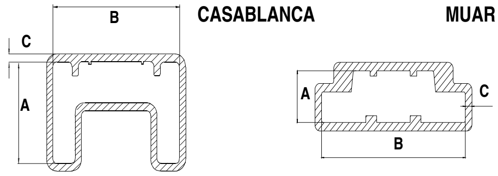


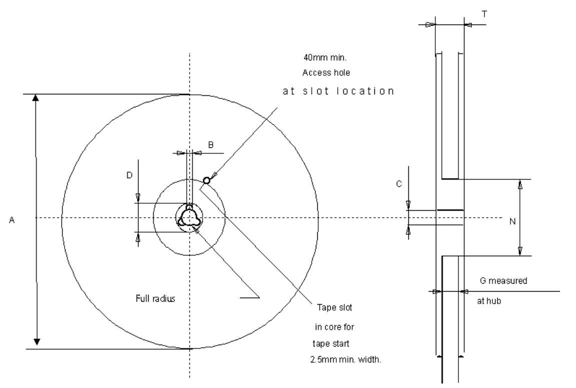
Figure 27. PowerSO-10 tube shipment (no suffix)



All dimensions are in mm.

	Base Q.ty	Bulk Q.ty	Tube length (± 0.5)	A	B	C (± 0.1)
Casablanca	50	1000	532	10.4	16.4	0.8
Muar	50	1000	532	4.9	17.2	0.8

Figure 28. PowerSO-10 tape and reel shipment (suffix "TR")



Reel dimensions

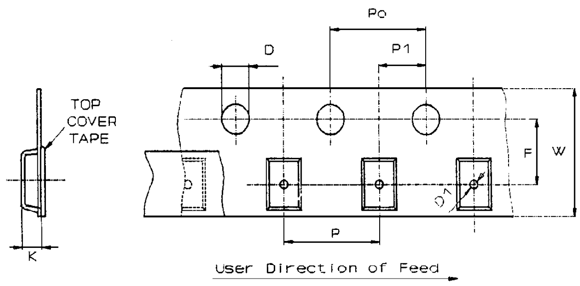
Base Q.ty	600
Bulk Q.ty	600
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	24.4
N (min)	60
T (max)	30.4

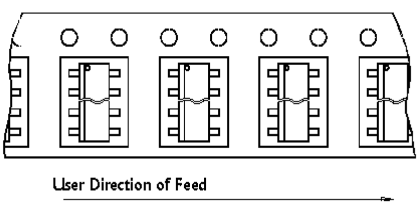
Tape dimensions

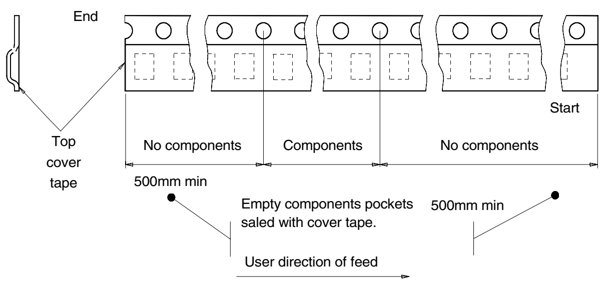
According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb. 1986

Tape width	W	24
Tape Hole Spacing	P0 (± 0.1)	4
Component Spacing	P	24
Hole Diameter	D (± 0.1/-0)	1.5
Hole Diameter	D1 (min)	1.5
Hole Position	F (± 0.05)	11.5
Compartment Depth	K (max)	6.5
Hole Spacing	P1 (± 0.1)	2

All dimensions are in mm.







6 Revision history

Table 15. Document revision history

Date	Revision	Changes
07-Jul-2004	1	Initial release.
09-Sep-2004	2	Current and voltage convention update (page 2). Configuration diagram (top view) & suggested connections for unused and n.c. pins insertion (page 2). 6 cm2 Cu condition insertion in thermal data table (page 3). V_{CC} - output diode section update (page 3). Revision history table insertion (page 17). Disclaimers update (page 18).
03-May-2006	3	Suggested connections for unused and n.c. pins correction.
15-Dec-2008	4	Document reformatted and restructured. Added contents, list of tables and figures. Added *ECOPACK® packages* information.

Please Read Carefully:

Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits,General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.

Как с нами связаться

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