



BUK7K18-40E

Dual N-channel 40 V, 19 mΩ standard level MOSFET

10 December 2013

Product data sheet

1. General description

Dual standard level N-channel MOSFET in an LPAK56D (Dual Power-SO8) package using TrenchMOS technology. This product has been designed and qualified to AEC Q101 standard for use in high performance automotive applications.

2. Features and benefits

- Dual MOSFET
- Q101 compliant
- Repetitive avalanche rated
- Suitable for thermally demanding environments due to 175 °C rating
- True standard level gate with $V_{GS(th)}$ of greater than 1 V at 175 °C

3. Applications

- 12 V Automotive systems
- Motors, lamps and solenoid control
- Transmission control
- Ultra high performance power switching

4. Quick reference data

Table 1. Quick reference data

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--|----------------------------------|--|-----|------|------|------|
| V_{DS} | drain-source voltage | $T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$ | - | - | 40 | V |
| I_D | drain current | $V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 1 | - | - | 24.2 | A |
| P_{tot} | total power dissipation | $T_{mb} = 25\text{ °C}$; Fig. 2 | - | - | 38 | W |
| Static characteristics FET1 and FET2 | | | | | | |
| $R_{DS(on)}$ | drain-source on-state resistance | $V_{GS} = 10\text{ V}$; $I_D = 10\text{ A}$; $T_j = 25\text{ °C}$; Fig. 11 | - | 15.5 | 19 | mΩ |
| Dynamic characteristics FET1 and FET2 | | | | | | |
| Q_{GD} | gate-drain charge | $I_D = 10\text{ A}$; $V_{DS} = 32\text{ V}$; $V_{GS} = 10\text{ V}$; $T_j = 25\text{ °C}$; Fig. 13 ; Fig. 14 | - | 4.3 | - | nC |

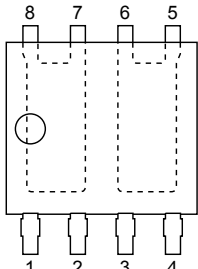
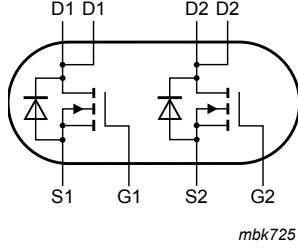


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5. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|-----|--------|-------------|---|---|
| 1 | S1 | source1 |  <p>LFPAK56D (SOT1205)</p> |  <p>mbk725</p> |
| 2 | G1 | gate1 | | |
| 3 | S2 | source2 | | |
| 4 | G2 | gate2 | | |
| 5 | D2 | drain2 | | |
| 6 | D2 | drain2 | | |
| 7 | D1 | drain1 | | |
| 8 | D1 | drain1 | | |

6. Ordering information

Table 3. Ordering information

| Type number | Package | | |
|-------------|----------|--|---------|
| | Name | Description | Version |
| BUK7K18-40E | LFPAK56D | Plastic single ended surface mounted package (LFPAK56D); 8 leads | SOT1205 |

7. Marking

Table 4. Marking codes

| Type number | Marking code |
|-------------|--------------|
| BUK7K18-40E | 71840E |

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------|-------------------------|---|-----|------|------|
| V_{DS} | drain-source voltage | $T_j \geq 25\text{ }^\circ\text{C}$; $T_j \leq 175\text{ }^\circ\text{C}$ | - | 40 | V |
| V_{DGR} | drain-gate voltage | $R_{GS} = 20\text{ k}\Omega$ | - | 40 | V |
| V_{GS} | gate-source voltage | $T_j \leq 175\text{ }^\circ\text{C}$; DC | -20 | 20 | V |
| I_D | drain current | $T_{mb} = 25\text{ }^\circ\text{C}$; $V_{GS} = 10\text{ V}$; Fig. 1 | - | 24.2 | A |
| | | $T_{mb} = 100\text{ }^\circ\text{C}$; $V_{GS} = 10\text{ V}$; Fig. 1 | - | 22 | A |
| I_{DM} | peak drain current | $T_{mb} = 25\text{ }^\circ\text{C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$; Fig. 4 | - | 127 | A |
| P_{tot} | total power dissipation | $T_{mb} = 25\text{ }^\circ\text{C}$; Fig. 2 | - | 38 | W |

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|--|---|---|-----|------|------|
| T_{stg} | storage temperature | | | -55 | 175 | °C |
| T_j | junction temperature | | | -55 | 175 | °C |
| Source-drain diode FET1 and FET2 | | | | | | |
| I_S | source current | $T_{\text{mb}} = 25\text{ °C}$ | | - | 24.2 | A |
| I_{SM} | peak source current | pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{\text{mb}} = 25\text{ °C}$ | | - | 127 | A |
| Avalanche Ruggedness FET1 and FET2 | | | | | | |
| $E_{\text{DS(AL)S}}$ | non-repetitive drain-source avalanche energy | $I_D = 24.2\text{ A}$; $V_{\text{sup}} \leq 40\text{ V}$; $V_{\text{GS}} = 10\text{ V}$; $T_{j(\text{init})} = 25\text{ °C}$; Fig. 3 | [1] [2] | - | 26.3 | mJ |

[1] Refer to application note AN10273 for further information

[2] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C

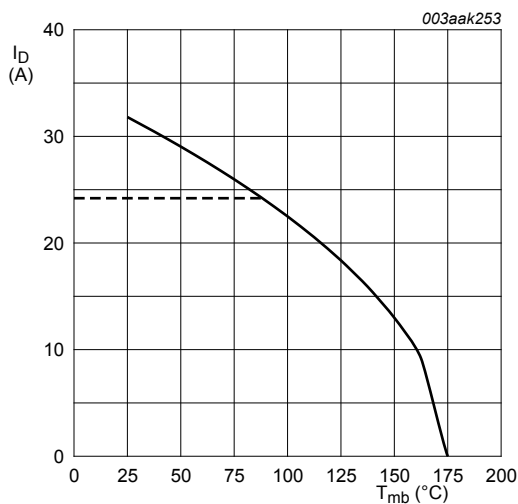


Fig. 1. Continuous drain current as a function of mounting base temperature

$$V_{\text{GS}} \geq 10\text{ V}$$

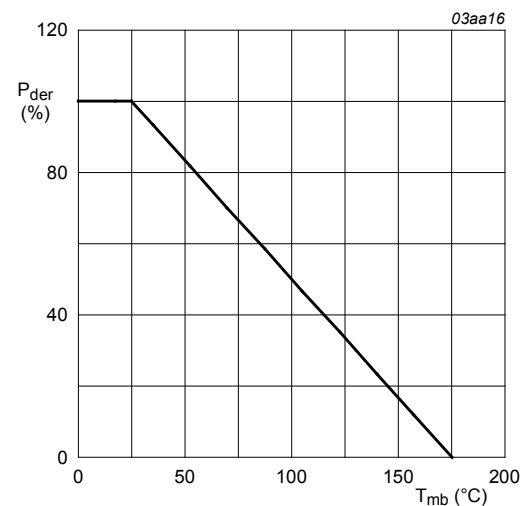


Fig. 2. Normalized total power dissipation as a function of mounting base temperature

$$P_{\text{der}} = \frac{P_{\text{tot}}}{P_{\text{tot}(25^\circ\text{C})}} \times 100\%$$

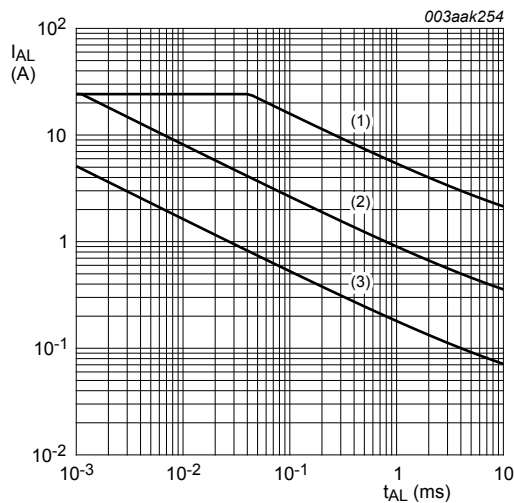


Fig. 3. Avalanche rating; avalanche current as a function of avalanche time

(1) $T_{j(jnt)} = 25^{\circ}\text{C}$; (2) $T_{j(jnt)} = 150^{\circ}\text{C}$; (3) Repetitive Avalanche

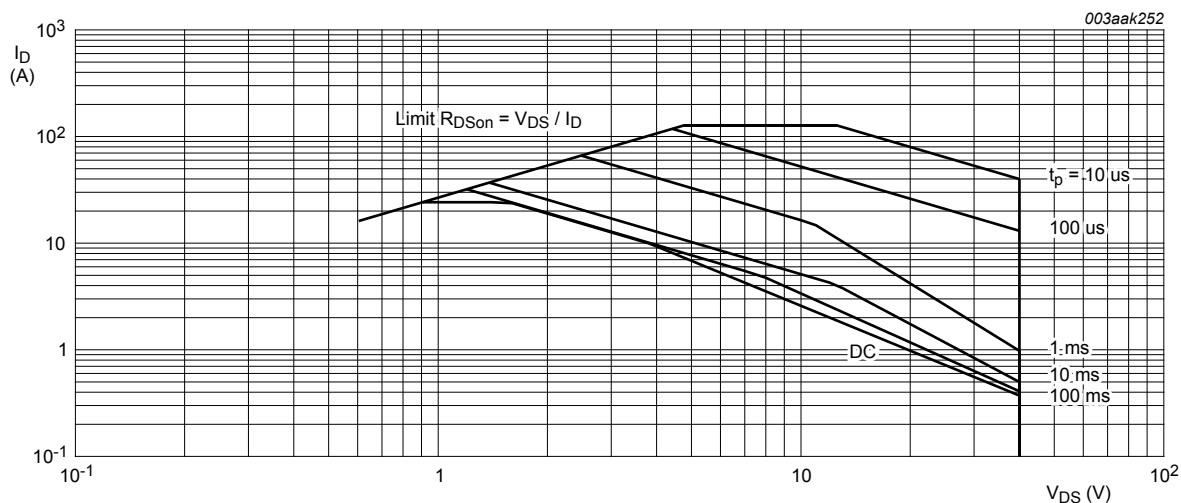


Fig. 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$T_{mb} = 25^{\circ}\text{C}$; I_{DM} is a single pulse

9. Thermal characteristics

Table 6. Thermal characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------|---|---|-----|-----|------|------|
| $R_{th(j-mb)}$ | thermal resistance from junction to mounting base | Fig. 5 | - | - | 3.96 | K/W |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | Minimum footprint; mounted on a printed circuit board | - | 95 | - | K/W |

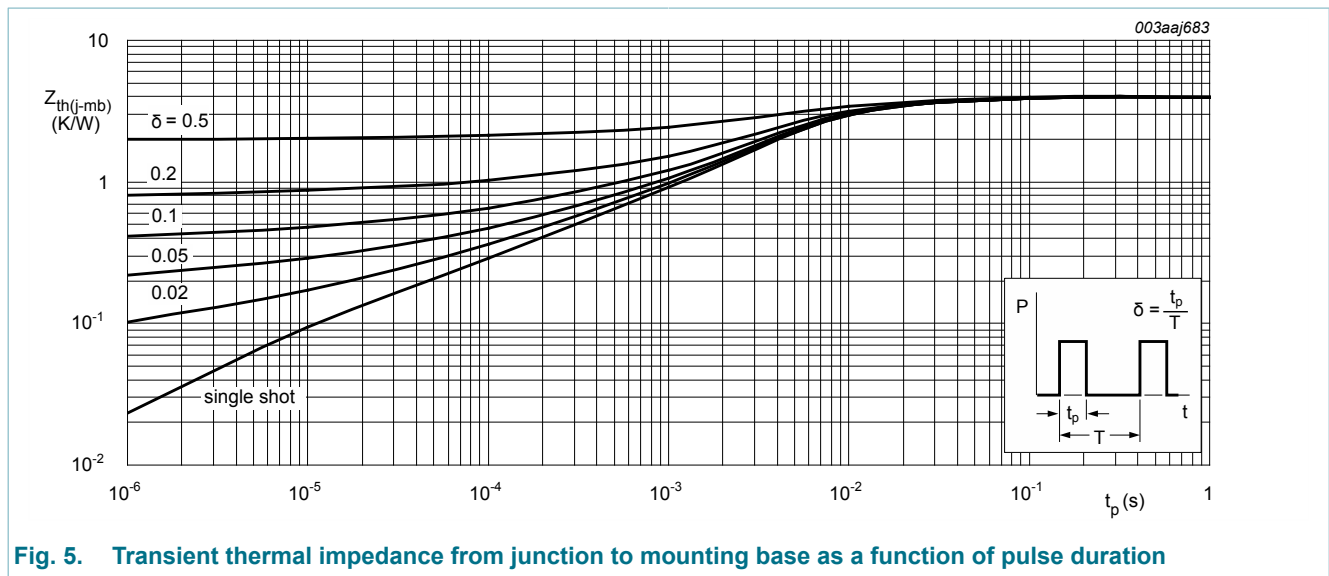


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

10. Characteristics

Table 7. Characteristics

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---------------------------------------|----------------------------------|--|--|-----|------|------|---------------|
| Static characteristics FET1 and FET2 | | | | | | | |
| $V_{(BR)DSS}$ | drain-source breakdown voltage | $I_D = 250\text{ }\mu\text{A}$; $V_{GS} = 0\text{ V}$; $T_j = -55\text{ }^\circ\text{C}$ | | 36 | - | - | V |
| | | $I_D = 250\text{ }\mu\text{A}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$ | | 40 | - | - | V |
| $V_{GS(th)}$ | gate-source threshold voltage | $I_D = 1\text{ mA}$; $V_{DS} = V_{GS}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 9 ; Fig. 10 | | 2.4 | 3 | 4 | V |
| | | $I_D = 1\text{ mA}$; $V_{DS} = V_{GS}$; $T_j = 175\text{ }^\circ\text{C}$; Fig. 9 ; Fig. 10 | | 1 | - | - | V |
| | | $I_D = 1\text{ mA}$; $V_{DS} = V_{GS}$; $T_j = -55\text{ }^\circ\text{C}$; Fig. 9 ; Fig. 10 | | - | - | 4.5 | V |
| I_{DSS} | drain leakage current | $V_{DS} = 40\text{ V}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$ | | - | 0.02 | 1 | μA |
| | | $V_{DS} = 40\text{ V}$; $V_{GS} = 0\text{ V}$; $T_j = 175\text{ }^\circ\text{C}$ | | - | - | 500 | μA |
| I_{GSS} | gate leakage current | $V_{GS} = -20\text{ V}$; $V_{DS} = 0\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$ | | - | 2 | 100 | nA |
| | | $V_{GS} = 20\text{ V}$; $V_{DS} = 0\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$ | | - | 2 | 100 | nA |
| R_{DSon} | drain-source on-state resistance | $V_{GS} = 10\text{ V}$; $I_D = 10\text{ A}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 11 | | - | 15.5 | 19 | m Ω |
| | | $V_{GS} = 10\text{ V}$; $I_D = 10\text{ A}$; $T_j = 175\text{ }^\circ\text{C}$; Fig. 11 ; Fig. 12 | | - | 30.5 | 37.4 | m Ω |
| Dynamic characteristics FET1 and FET2 | | | | | | | |
| $Q_{G(tot)}$ | total gate charge | $I_D = 10\text{ A}$; $V_{DS} = 32\text{ V}$; $V_{GS} = 10\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 13 ; Fig. 14 | | - | 11.8 | - | nC |
| Q_{GS} | gate-source charge | | | - | 3.6 | - | nC |
| Q_{GD} | gate-drain charge | | | - | 4.3 | - | nC |

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|----------------------------------|------------------------------|---|--|-----|------|-----|------|
| C _{iss} | input capacitance | V _{GS} = 0 V; V _{DS} = 25 V; f = 1 MHz; T _j = 25 °C; Fig. 15 | | - | 606 | 808 | pF |
| C _{oss} | output capacitance | | | - | 134 | 161 | pF |
| C _{rss} | reverse transfer capacitance | | | - | 87 | 119 | pF |
| t _{d(on)} | turn-on delay time | V _{DS} = 32 V; R _L = 3.3 Ω; V _{GS} = 10 V; R _{G(ext)} = 5 Ω; T _j = 25 °C; I _D = 10 A | | - | 6.2 | - | ns |
| t _r | rise time | | | - | 12.7 | - | ns |
| t _{d(off)} | turn-off delay time | | | - | 7.9 | - | ns |
| t _f | fall time | | | - | 10 | - | ns |
| Source-drain diode FET1 and FET2 | | | | | | | |
| V _{SD} | source-drain voltage | I _S = 10 A; V _{GS} = 0 V; T _j = 25 °C; Fig. 16 | | - | 0.83 | 1.2 | V |
| t _{rr} | reverse recovery time | I _S = 10 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V; V _{DS} = 20 V; T _j = 25 °C | | - | 16.8 | - | ns |
| Q _r | recovered charge | | | - | 9.1 | - | nC |

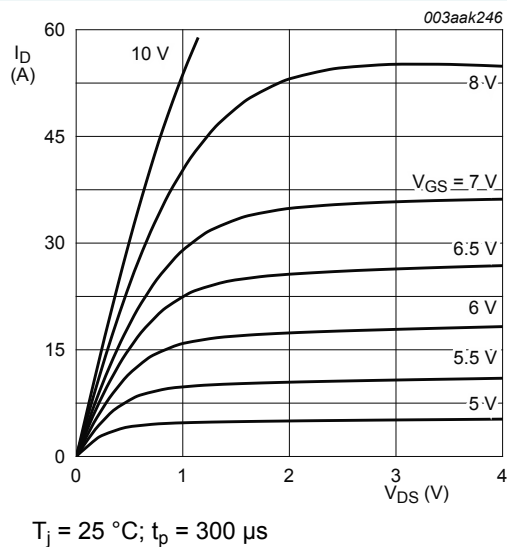


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

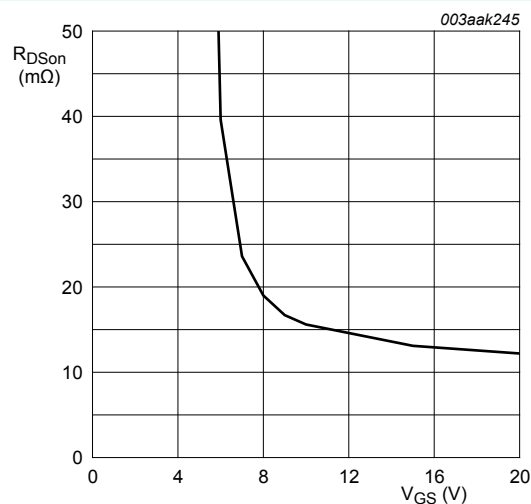


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

$T_j = 25\text{ }^{\circ}\text{C}; I_D = 10\text{ A}$

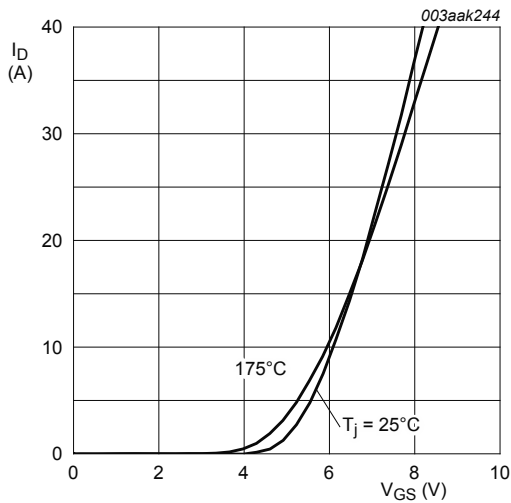


Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values

$V_{DS} = 10V$

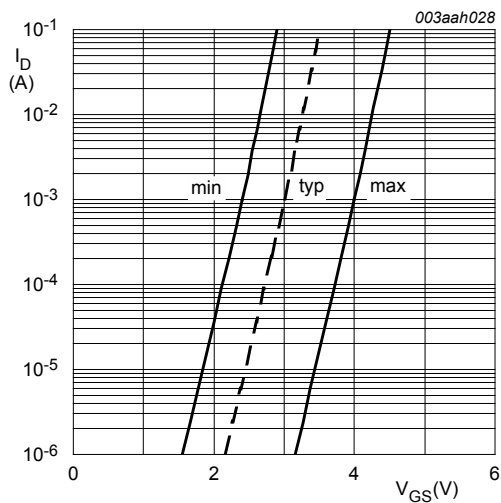


Fig. 9. Sub-threshold drain current as a function of gate-source voltage

$T_j = 25^\circ C; V_{DS} = 5V$

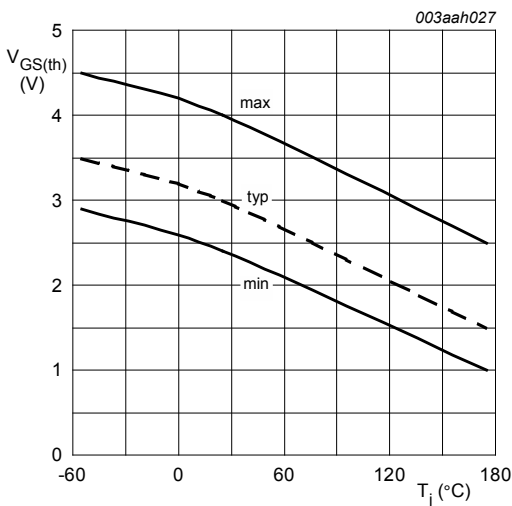


Fig. 10. Gate-source threshold voltage as a function of junction temperature

$I_D = 1\text{ mA}; V_{DS} = V_{GS}$

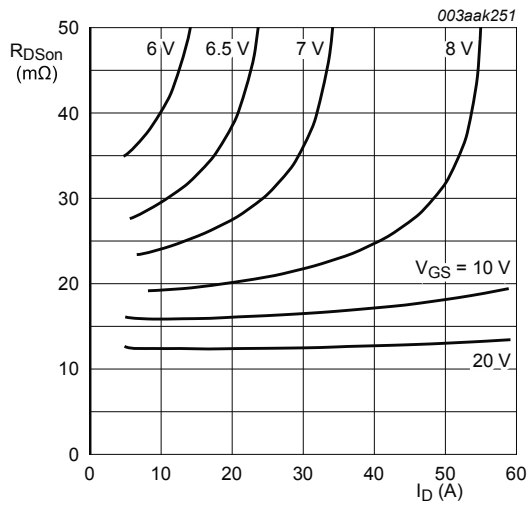


Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

$T_j = 25^\circ C; t_p = 300\text{ }\mu s$

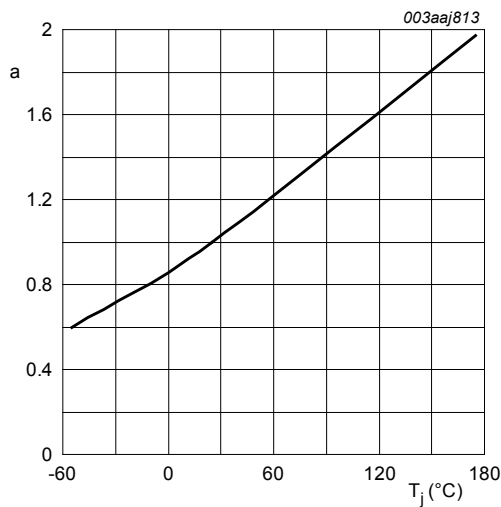


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DS(on)}}{R_{DS(on)}(25^{\circ}\text{C})}$$

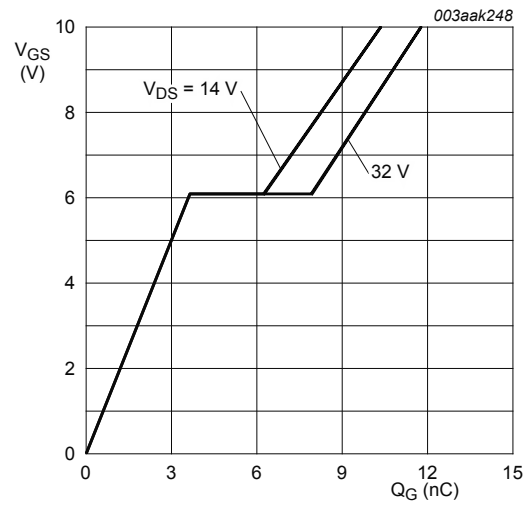


Fig. 13. Gate-source voltage as a function of gate charge; typical values

$$T_j = 25^{\circ}\text{C}; I_D = 10\text{ A}$$

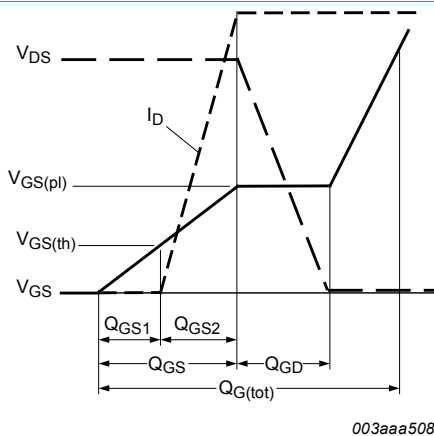


Fig. 14. Gate charge waveform definitions

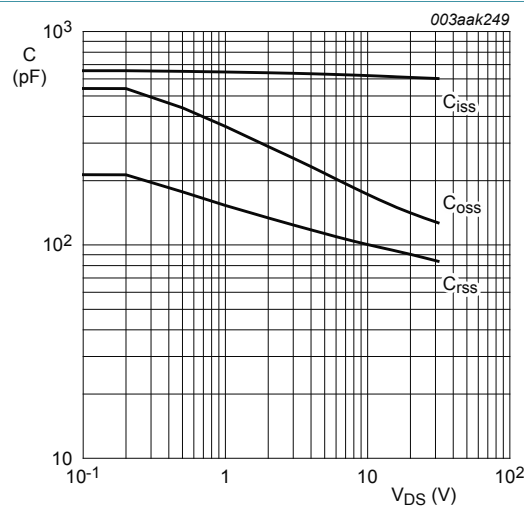


Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$$V_{GS} = 0\text{ V}; f = 1\text{ MHz}$$

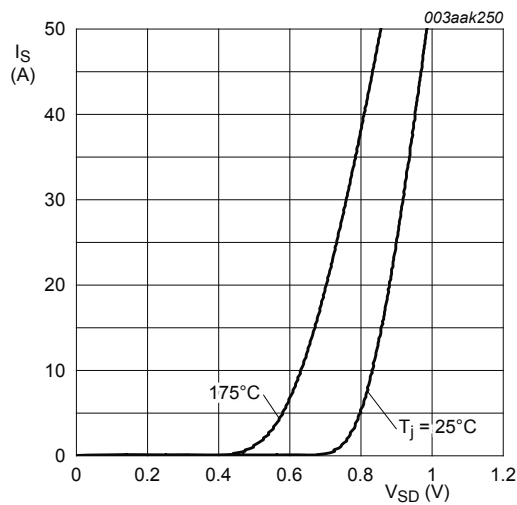


Fig. 16. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

$V_{GS} = 0V$

11. Package outline

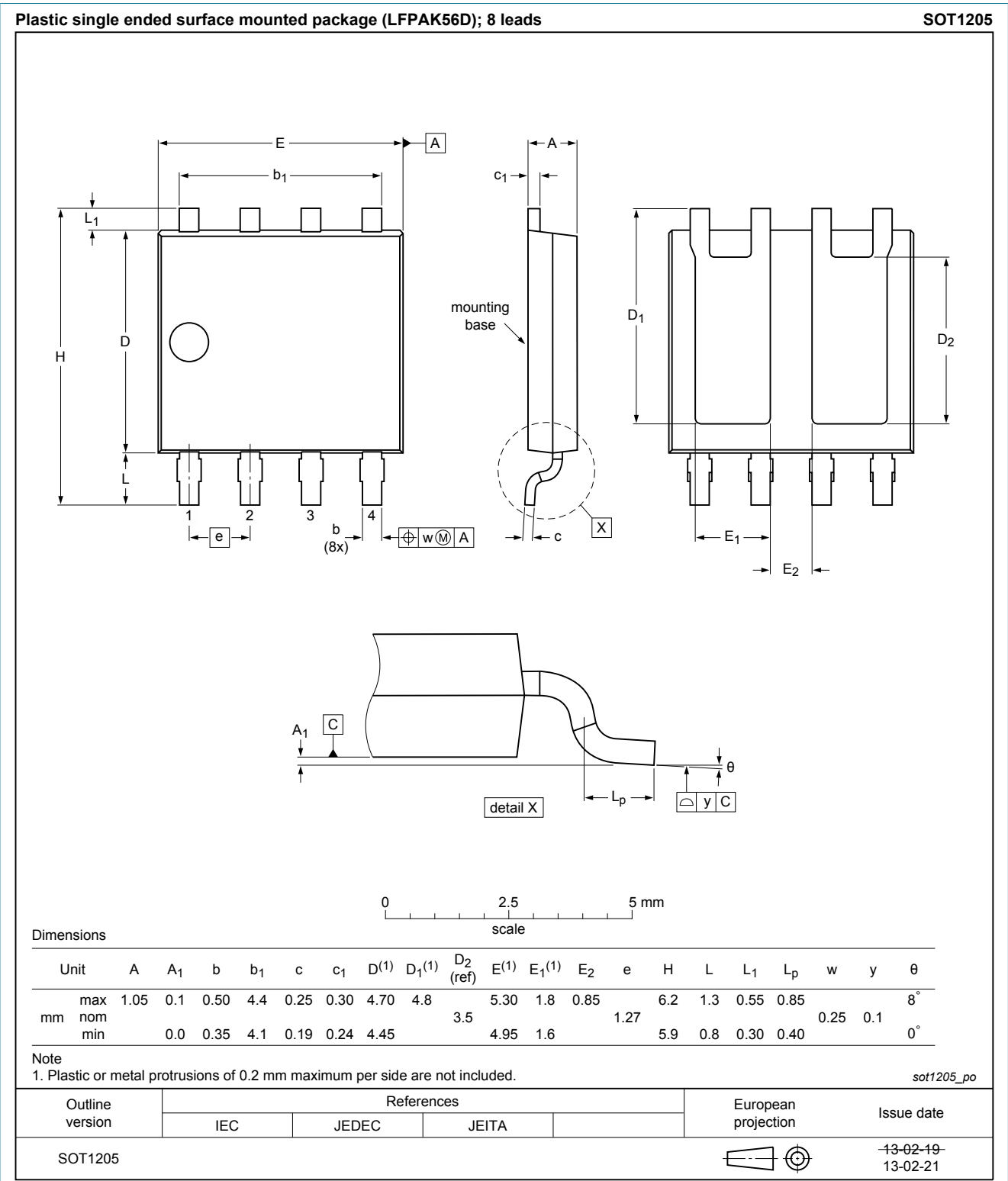


Fig. 17. Package outline LPAK56D (SOT1205)

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|--------------------------------|--------------------|---|
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13. Contents

| | | |
|------|-------------------------------|----|
| 1 | General description | 1 |
| 2 | Features and benefits | 1 |
| 3 | Applications | 1 |
| 4 | Quick reference data | 1 |
| 5 | Pinning information | 2 |
| 6 | Ordering information | 2 |
| 7 | Marking | 2 |
| 8 | Limiting values | 2 |
| 9 | Thermal characteristics | 4 |
| 10 | Characteristics | 5 |
| 11 | Package outline | 10 |
| 12 | Legal information | 11 |
| 12.1 | Data sheet status | 11 |
| 12.2 | Definitions | 11 |
| 12.3 | Disclaimers | 11 |
| 12.4 | Trademarks | 12 |

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Date of release: 10 December 2013



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- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

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