



# **PIC18F2458/2553/4458/4553**

## **Data Sheet**

28/40/44-Pin High-Performance,  
Enhanced Flash, USB Microcontrollers  
with 12-Bit A/D and nanoWatt Technology

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# MICROCHIP

# PIC18F2458/2553/4458/4553

## 28/40/44-Pin High-Performance, Enhanced Flash, USB Microcontrollers with 12-Bit A/D and nanoWatt Technology

### Universal Serial Bus Features:

- USB V2.0 Compliant
- Low Speed (1.5 Mb/s) and Full Speed (12 Mb/s)
- Supports Control, Interrupt, Isochronous and Bulk Transfers
- Supports up to 32 Endpoints (16 bidirectional)
- 1-Kbyte Dual Access RAM for USB
- On-Chip USB Transceiver with On-Chip Voltage Regulator
- Interface for Off-Chip USB Transceiver
- Streaming Parallel Port (SPP) for USB Streaming Transfers (40/44-pin devices only)

### Power-Managed Modes:

- Run: CPU On, Peripherals On
- Idle: CPU Off, Peripherals On
- Sleep: CPU Off, Peripherals Off
- Idle mode Currents Down to 5.8  $\mu$ A Typical
- Sleep mode Currents Down to 0.1  $\mu$ A Typical
- Timer1 Oscillator: 1.1  $\mu$ A Typical, 32 kHz, 2V
- Watchdog Timer: 2.1  $\mu$ A Typical
- Two-Speed Oscillator Start-up

### Special Microcontroller Features:

- C Compiler Optimized Architecture with Optional Extended Instruction Set
- 100,000 Erase/Write Cycle Enhanced Flash Program Memory Typical
- 1,000,000 Erase/Write Cycle Data EEPROM Memory Typical
- Flash/Data EEPROM Retention: > 40 Years
- Self-Programmable under Software Control
- Priority Levels for Interrupts
- 8 x 8 Single-Cycle Hardware Multiplier
- Extended Watchdog Timer (WDT):
  - Programmable period from 41 ms to 131s
- Programmable Code Protection
- Single-Supply 5V In-Circuit Serial Programming™ (ICSP™) via Two Pins
- In-Circuit Debug (ICD) via Two Pins
- Optional Dedicated ICD/ICSP Port (44-pin TQFP package only)
- Wide Operating Voltage Range (2.0V to 5.5V)

### Flexible Oscillator Structure:

- Four Crystal modes, Including High-Precision PLL for USB
- Two External Clock modes, up to 48 MHz
- Internal Oscillator Block:
  - 8 user-selectable frequencies, from 31 kHz to 8 MHz
  - User-tunable to compensate for frequency drift
- Secondary Oscillator using Timer1 @ 32 kHz
- Dual Oscillator Options allow Microcontroller and USB module to Run at Different Clock Speeds
- Fail-Safe Clock Monitor:
  - Allows for safe shutdown if any clock stops

### Peripheral Highlights:

- High-Current Sink/Source: 25 mA/25 mA
- Three External Interrupts
- Four Timer modules (Timer0 to Timer3)
- Up to 2 Capture/Compare/PWM (CCP) modules:
  - Capture is 16-bit, max. resolution 5.2 ns ( $T_{CY}/16$ )
  - Compare is 16-bit, max. resolution 83.3 ns ( $T_{CY}$ )
  - PWM output: PWM resolution is 1 to 10-bits
- Enhanced Capture/Compare/PWM (ECCP) module:
  - Multiple output modes
  - Selectable polarity
  - Programmable dead time
  - Auto-shutdown and auto-restart
- Enhanced USART module:
  - LIN bus support
- Master Synchronous Serial Port (MSSP) module supporting 3-wire SPI (all 4 modes) and I<sup>2</sup>C™ Master and Slave modes
- 12-Bit, up to 13-Channel Analog-to-Digital Converter module (A/D) with Programmable Acquisition Time
- Dual Analog Comparators with Input Multiplexing

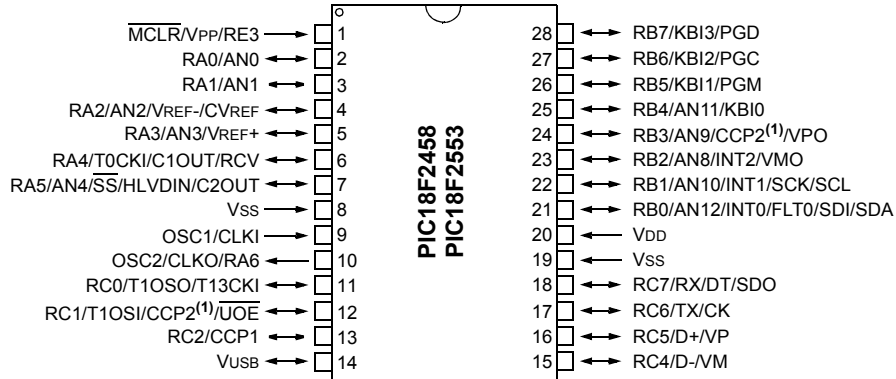
**Note:** This document is supplemented by the "PIC18F2455/2550/4455/4550 Data Sheet" (DS39632). See **Section 1.0 "Device Overview"**.

| Device     | Program Memory |                            | Data Memory  |                | I/O | 12-Bit A/D (ch) | CCP/ECCP (PWM) | SPP | MSSP |                          | EUSART | Comp. | Timers 8/16-Bit |
|------------|----------------|----------------------------|--------------|----------------|-----|-----------------|----------------|-----|------|--------------------------|--------|-------|-----------------|
|            | Flash (bytes)  | # Single-Word Instructions | SRAM (bytes) | EEPROM (bytes) |     |                 |                |     | SPI  | Master I <sup>2</sup> C™ |        |       |                 |
| PIC18F2458 | 24K            | 12288                      | 2048         | 256            | 24  | 10              | 2/0            | No  | Y    | Y                        | 1      | 2     | 1/3             |
| PIC18F2553 | 32K            | 16384                      |              |                | 35  | 13              | 1/1            | Yes |      |                          |        |       |                 |
| PIC18F4458 | 24K            | 12288                      |              |                |     |                 |                |     |      |                          |        |       |                 |
| PIC18F4553 | 32K            | 16384                      |              |                |     |                 |                |     |      |                          |        |       |                 |

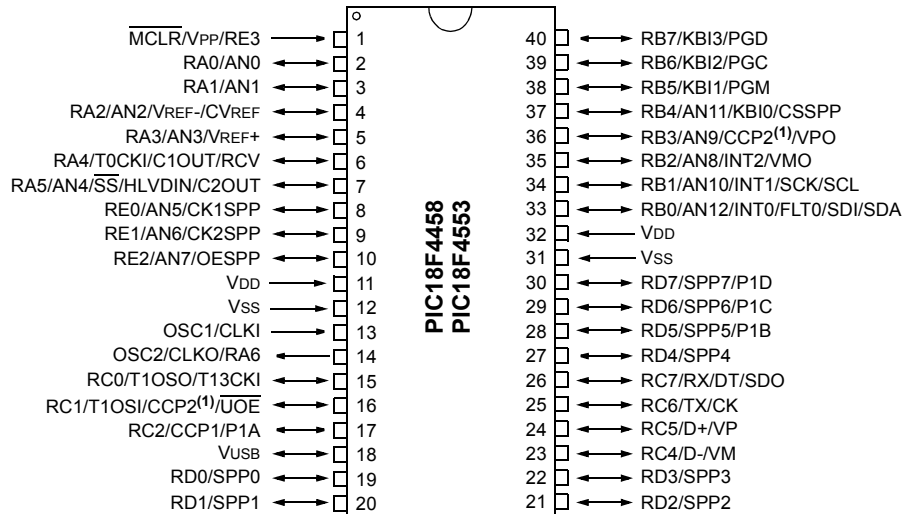
# PIC18F2458/2553/4458/4553

## Pin Diagrams

### 28-Pin SPDIP, SOIC



### 40-Pin PDIP

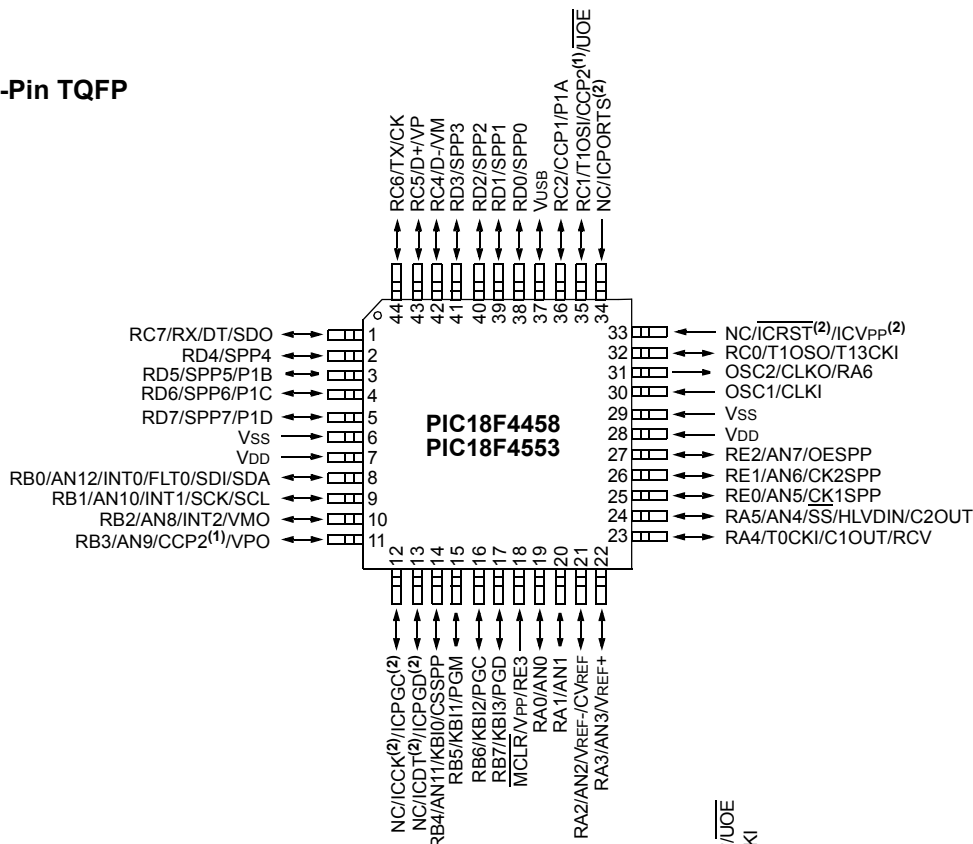


**Note 1:** RB3 is the alternate pin for CCP2 multiplexing.

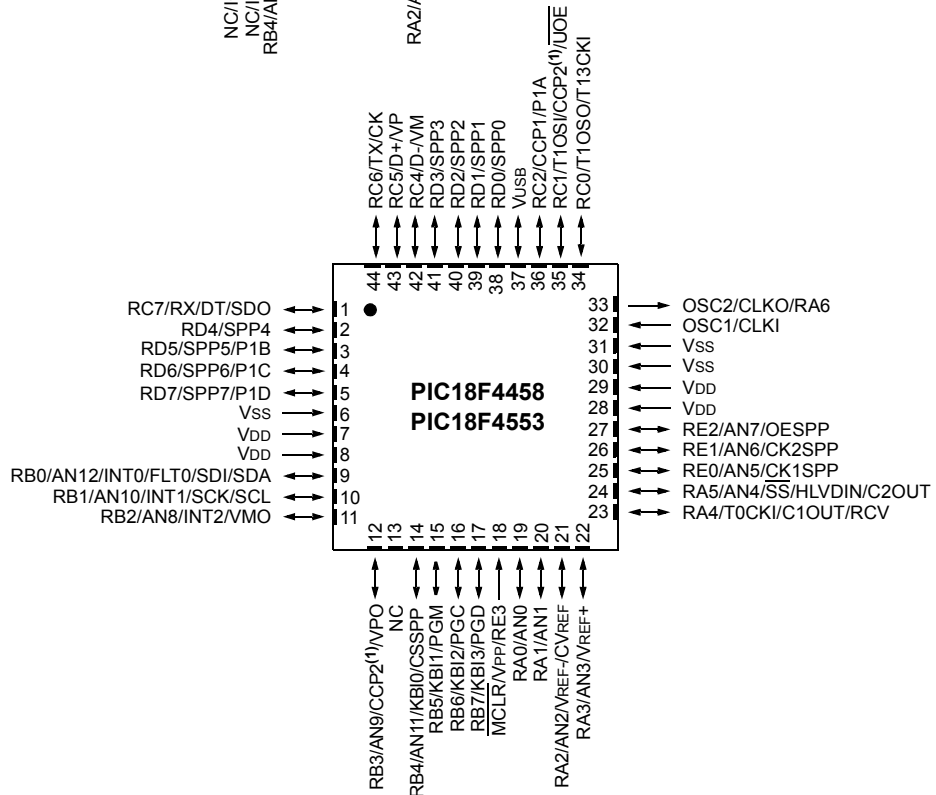
# PIC18F2458/2553/4458/4553

## Pin Diagrams (Continued)

### 44-Pin TQFP



### 44-Pin QFN



- Note** 1: RB3 is the alternate pin for CCP2 multiplexing.  
2: Special ICPORT features are available only in 44-pin TQFP packages. See Section 25.9 "Special ICPORT Features" in the "PIC18F2455/2550/4455/4550 Data Sheet".

# PIC18F2458/2553/4458/4553

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# PIC18F2458/2553/4458/4553

## 1.0 DEVICE OVERVIEW

This document contains device-specific information for the following devices:

- PIC18F2458
- PIC18F4458
- PIC18F2553
- PIC18F4553

**Note:** This data sheet documents only the devices' features and specifications that are in addition to the features and specifications of the PIC18F2455/2550/4455/4550 devices. For information on the features and specifications shared by the PIC18F2458/2553/4458/4553 and PIC18F2455/2550/4455/4550 devices, see the "PIC18F2455/2550/4455/4550 Data Sheet" (DS39632).

The PIC18F4553 family of devices offers the advantages of all PIC18 microcontrollers – namely, high computational performance at an economical price – with the addition of high-endurance, Enhanced Flash program memory. In addition to these features, the PIC18F4553 family introduces design enhancements that make these microcontrollers a logical choice for many high-performance, power sensitive applications.

### 1.1 Special Features

- **12-Bit A/D Converter:** The PIC18F4553 family implements a 12-bit A/D Converter. The A/D Converter incorporates programmable acquisition time. This allows for a channel to be selected and a conversion to be initiated, without waiting for a sampling period and thus, reducing code overhead.

## 1.2 Details on Individual Family Members

The PIC18F2458/2553/4458/4553 devices are available in 28-pin and 40/44-pin packages. Block diagrams for the two groups are shown in Figure 1-1 and Figure 1-2.

The devices are differentiated from each other in the following ways:

1. Flash program memory (24 Kbytes for PIC18FX458 devices, 32 Kbytes for PIC18FX553).
2. A/D channels (10 for 28-pin devices, 13 for 40-pin and 44-pin devices).
3. I/O ports (3 bidirectional ports and 1 input only port on 28-pin devices, 5 bidirectional ports on 40-pin and 44-pin devices).
4. CCP and Enhanced CCP implementation (28-pin devices have two standard CCP modules, 40-pin and 44-pin devices have one standard CCP module and one ECCP module).
5. Streaming Parallel Port (present only on 40/44-pin devices).

All other features for devices in this family are identical. These are summarized in Table 1-1.

The pinouts for all devices are listed in Table 1-2 and Table 1-3.

Members of the PIC18F4553 family are available as both standard and low-voltage devices. Standard devices with Enhanced Flash memory, designated with an "F" in the part number (such as PIC18F2458), accommodate an operating VDD range of 4.2V to 5.5V. Low-voltage parts, designated by "LF" (such as PIC18LF2458), function over an extended VDD range of 2.0V to 5.5V.

# PIC18F2458/2553/4458/4553

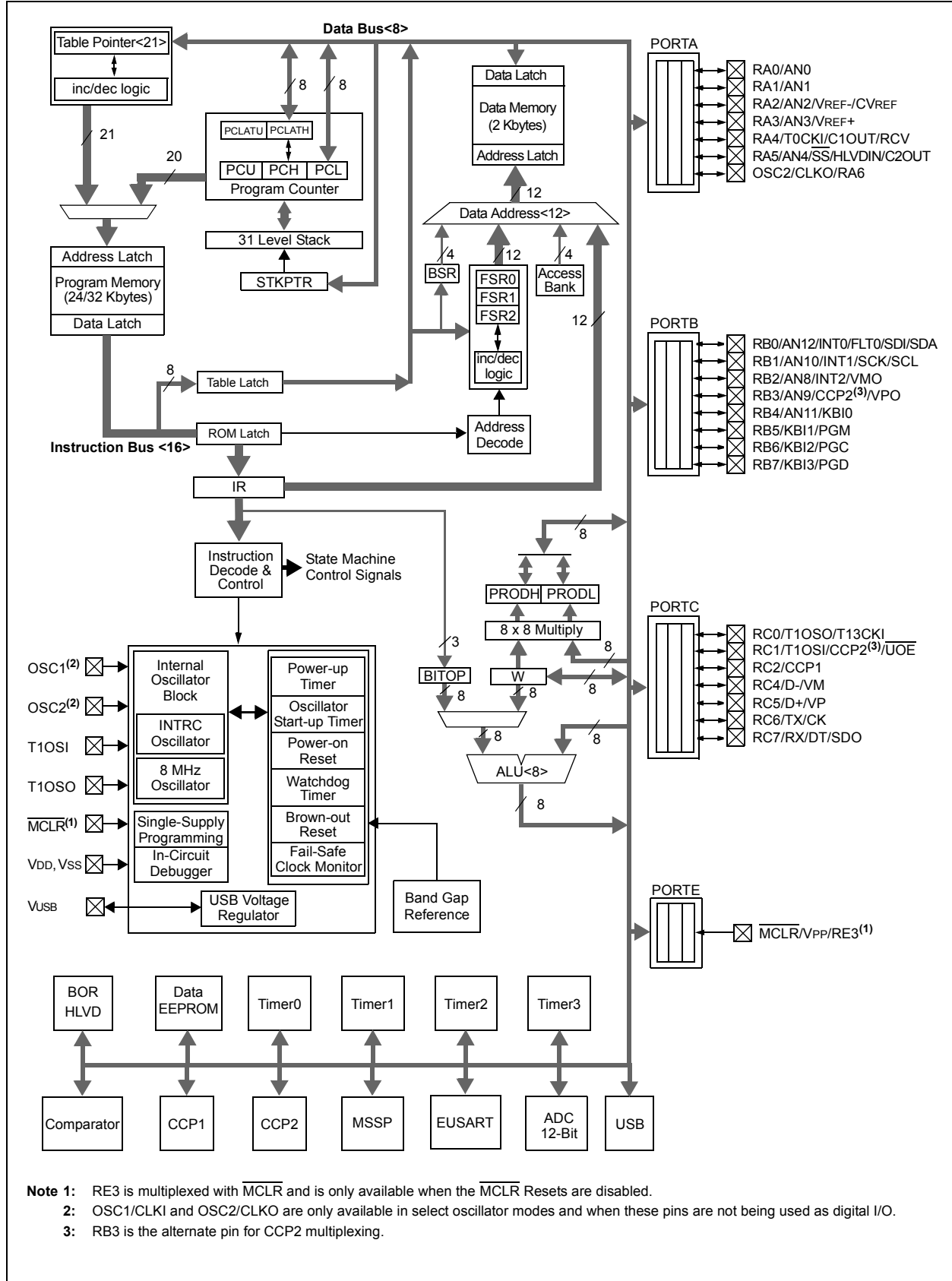
**TABLE 1-1: DEVICE FEATURES**

| Features                                  | PIC18F2458  | PIC18F2553  | PIC18F4458  | PIC18F4553  |
|---|---|---|---|---|
| Operating Frequency                       | DC – 48 MHz   | DC – 48 MHz   | DC – 48 MHz   | DC – 48 MHz   |
| Program Memory (Bytes)                    | 24576   | 32768   | 24576   | 32768   |
| Program Memory (Instructions)             | 12288   | 16384   | 12288   | 16384   |
| Data Memory (Bytes)                       | 2048  | 2048  | 2048  | 2048  |
| Data EEPROM Memory (Bytes)                | 256   | 256   | 256   | 256   |
| Interrupt Sources                         | 19  | 19  | 20  | 20  |
| I/O Ports                                 | Ports A, B, C, (E)  | Ports A, B, C, (E)  | Ports A, B, C, D, E   | Ports A, B, C, D, E   |
| Timers                                    | 4   | 4   | 4   | 4   |
| Capture/Compare/PWM Modules               | 2   | 2   | 1   | 1   |
| Enhanced Capture/Compare/PWM Modules      | 0   | 0   | 1   | 1   |
| Serial Communications                     | MSSP, Enhanced USART  | MSSP, Enhanced USART  | MSSP, Enhanced USART  | MSSP, Enhanced USART  |
| Universal Serial Bus (USB) Module         | 1   | 1   | 1   | 1   |
| Streaming Parallel Port (SPP)             | No  | No  | Yes   | Yes   |
| 12-Bit Analog-to-Digital Converter Module | 10 Input Channels   | 10 Input Channels   | 13 Input Channels   | 13 Input Channels   |
| Comparators                               | 2   | 2   | 2   | 2   |
| Resets (and Delays)                       | POR, BOR, WDT, RESET Instruction, Stack Full, Stack Underflow, MCLR (optional), (PWRT, OST) | POR, BOR, WDT, RESET Instruction, Stack Full, Stack Underflow, MCLR (optional), (PWRT, OST) | POR, BOR, WDT, RESET Instruction, Stack Full, Stack Underflow, MCLR (optional), (PWRT, OST) | POR, BOR, WDT, RESET Instruction, Stack Full, Stack Underflow, MCLR (optional), (PWRT, OST) |
| Programmable High/Low-Voltage Detect      | Yes   | Yes   | Yes   | Yes   |
| Programmable Brown-out Reset              | Yes   | Yes   | Yes   | Yes   |
| Instruction Set                           | 75 Instructions; 83 with Extended Instruction Set Enabled                                   | 75 Instructions; 83 with Extended Instruction Set Enabled                                   | 75 Instructions; 83 with Extended Instruction Set Enabled                                   | 75 Instructions; 83 with Extended Instruction Set Enabled                                   |
| Packages                                  | 28-Pin SPDIP<br>28-Pin SOIC   | 28-Pin SPDIP<br>28-Pin SOIC   | 40-Pin PDIP<br>44-Pin QFN<br>44-Pin TQFP  | 40-Pin PDIP<br>44-Pin QFN<br>44-Pin TQFP  |
| Corresponding Devices with 10-Bit A/D     | PIC18F2455  | PIC18F2550  | PIC18F4455  | PIC18F4550  |



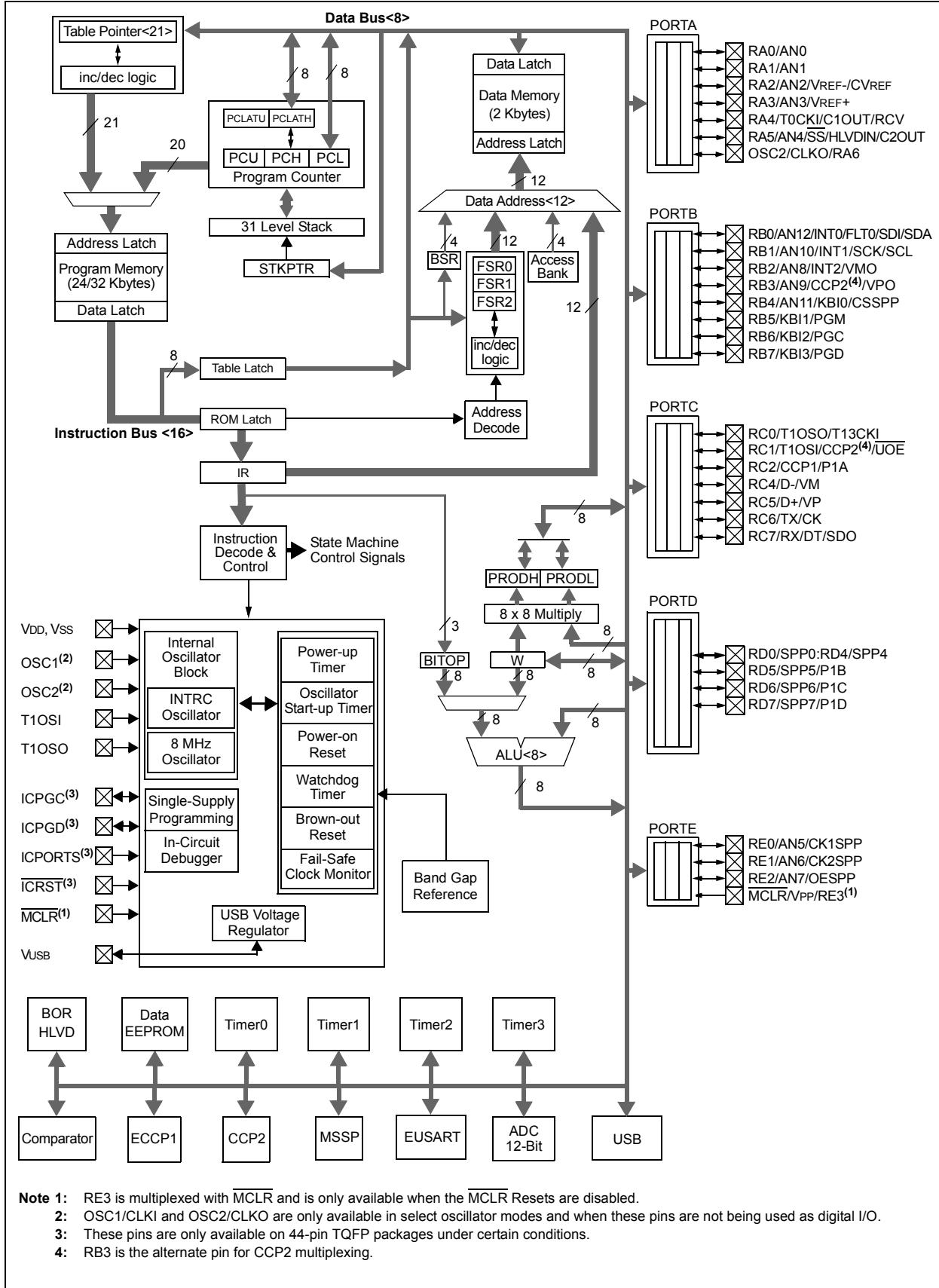
# PIC18F2458/2553/4458/4553

FIGURE 1-1: PIC18F2458/2553 (28-PIN) BLOCK DIAGRAM



# PIC18F2458/2553/4458/4553

**FIGURE 1-2: PIC18F4458/4553(40/44-PIN) BLOCK DIAGRAM**



- Note 1:** RE3 is multiplexed with MCLR and is only available when the MCLR Resets are disabled.  
**Note 2:** OSC1/CLKI and OSC2/CLKO are only available in select oscillator modes and when these pins are not being used as digital I/O.  
**Note 3:** These pins are only available on 44-pin TQFP packages under certain conditions.  
**Note 4:** RB3 is the alternate pin for CCP2 multiplexing.











# PIC18F2458/2553/4458/4553

**TABLE 1-3: PIC18F4458/4553 PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name                                   | Pin Number |     |      | Pin Type | Buffer Type | Description  |                                     |
|--|------------|-----|------|----------|-------------|--|-------------------------------------|
|  | PDIP       | QFN | TQFP |          |             |  |                                     |
| RA0/AN0                                    | 2          | 19  | 19   | I/O      | TTL         | PORTA is a bidirectional I/O port.<br>Digital I/O. |                                     |
| RA0<br>AN0                                 |            |     |      | I        | Analog      |  | Analog input 0.                     |
| RA1/AN1                                    | 3          | 20  | 20   | I/O      | TTL         | Digital I/O.                                       |                                     |
| RA1<br>AN1                                 |            |     |      | I        | Analog      |  | Analog input 1.                     |
| RA2/AN2/VREF-/<br>CVREF                    | 4          | 21  | 21   | I/O      | TTL         | Digital I/O.                                       |                                     |
| RA2  |            |     |      | I        | Analog      |  | Analog input 2.                     |
| AN2  |            |     |      | I        | Analog      |  | A/D reference voltage (low) input.  |
| VREF-<br>CVREF                             |            |     |      | O        | Analog      |  | Analog comparator reference output. |
| RA3/AN3/VREF+                              | 5          | 22  | 22   | I/O      | TTL         | Digital I/O.                                       |                                     |
| RA3  |            |     |      | I        | Analog      |  | Analog input 3.                     |
| AN3<br>VREF+                               |            |     |      | I        | Analog      |  | A/D reference voltage (high) input. |
| RA4/T0CKI/C1OUT/<br>RCV                    | 6          | 23  | 23   | I/O      | ST          | Digital I/O.                                       |                                     |
| RA4  |            |     |      | I        | ST          |  | Timer0 external clock input.        |
| T0CKI                                      |            |     |      | O        | —           |  | Comparator 1 output.                |
| C1OUT<br>RCV                               |            |     |      | I        | TTL         |  | External USB transceiver RCV input. |
| RA5/AN4/ $\overline{SS}$ /<br>HLVDIN/C2OUT | 7          | 24  | 24   | I/O      | TTL         | Digital I/O.                                       |                                     |
| RA5  |            |     |      | I        | Analog      |  | Analog input 4.                     |
| AN4  |            |     |      | I        | TTL         |  | SPI slave select input.             |
| $\overline{SS}$                            |            |     |      | I        | Analog      |  | High/Low-Voltage Detect input.      |
| HLVDIN<br>C2OUT                            |            |     |      | O        | —           |  | Comparator 2 output.                |
| RA6  | —          | —   | —    | —        | —           | See the OSC2/CLKO/RA6 pin.                         |                                     |

**Legend:** TTL = TTL compatible input      CMOS = CMOS compatible input or output  
 ST = Schmitt Trigger input with CMOS levels      I = Input  
 O = Output      P = Power

- Note 1:** Alternate assignment for CCP2 when CCP2MX Configuration bit is cleared.  
**Note 2:** Default assignment for CCP2 when CCP2MX Configuration bit is set.  
**Note 3:** These pins are No Connect unless the ICPRT Configuration bit is set. For NC/ICPORTS, the pin is No Connect unless ICPRT is set and the DEBUG Configuration bit is cleared.











# PIC18F2458/2553/4458/4553

## 2.0 12-BIT ANALOG-TO-DIGITAL CONVERTER (A/D) MODULE

The Analog-to-Digital (A/D) Converter module has 10 inputs for the 28-pin devices and 13 for the 40-pin and 44-pin devices. This module allows conversion of an analog input signal to a corresponding 12-bit digital number.

The module has five registers:

- A/D Result High Register (ADRESH)
- A/D Result Low Register (ADRESL)
- A/D Control Register 0 (ADCON0)
- A/D Control Register 1 (ADCON1)
- A/D Control Register 2 (ADCON2)

The ADCON0 register, shown in Register 2-1, controls the operation of the A/D module. The ADCON1 register, shown in Register 2-2, configures the functions of the port pins. The ADCON2 register, shown in Register 2-3, configures the A/D clock source, programmed acquisition time and justification.

### REGISTER 2-1: ADCON0: A/D CONTROL REGISTER 0

|       |     |       |       |       |       |         |       |
|-------|-----|-------|-------|-------|-------|---------|-------|
| U-0   | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0   | R/W-0 |
| —     | —   | CHS3  | CHS2  | CHS1  | CHS0  | GO/DONE | ADON  |
| bit 7 |     |       |       |       |       |         | bit 0 |

#### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5-2 **CHS3:CHS0:** Analog Channel Select bits

0000 = Channel 0 (AN0)

0001 = Channel 1 (AN1)

0010 = Channel 2 (AN2)

0011 = Channel 3 (AN3)

0100 = Channel 4 (AN4)

0101 = Channel 5 (AN5)<sup>(1,2)</sup>

0110 = Channel 6 (AN6)<sup>(1,2)</sup>

0111 = Channel 7 (AN7)<sup>(1,2)</sup>

1000 = Channel 8 (AN8)

1001 = Channel 9 (AN9)

1010 = Channel 10 (AN10)

1011 = Channel 11 (AN11)

1100 = Channel 12 (AN12)

1101 = Unimplemented<sup>(2)</sup>

1110 = Unimplemented<sup>(2)</sup>

1111 = Unimplemented<sup>(2)</sup>

bit 1 **GO/DONE:** A/D Conversion Status bit

When ADON = 1:

1 = A/D conversion in progress

0 = A/D Idle

bit 0 **ADON:** A/D On bit

1 = A/D Converter module is enabled

0 = A/D Converter module is disabled

**Note 1:** These channels are not implemented on 28-pin devices.

**2:** Performing a conversion on unimplemented channels will return a floating input measurement.

# PIC18F2458/2553/4458/4553

## REGISTER 2-2: ADCON1: A/D CONTROL REGISTER 1

|       |     |       |       |       |                    |                    |                    |
|-------|-----|-------|-------|-------|--------------------|--------------------|--------------------|
| U-0   | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W <sup>(1)</sup> | R/W <sup>(1)</sup> | R/W <sup>(1)</sup> |
| —     | —   | VCFG1 | VCFG0 | PCFG3 | PCFG2              | PCFG1              | PCFG0              |
| bit 7 |     |       |       |       |                    |                    | bit 0              |

### Legend:

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
 -n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

bit 7-6                      **Unimplemented:** Read as '0'

bit 5                      **VCFG1:** Voltage Reference Configuration bit (VREF- source)

1 = VREF- (AN2)  
 0 = VSS

bit 4                      **VCFG0:** Voltage Reference Configuration bit (VREF+ source)

1 = VREF+ (AN3)  
 0 = VDD

bit 3-0                      **PCFG3:PCFG0:** A/D Port Configuration Control bits:

| PCFG3:<br>PCFG0     | AN12 | AN11 | AN10 | AN9 | AN8 | AN7 <sup>(2)</sup> | AN6 <sup>(2)</sup> | AN5 <sup>(2)</sup> | AN4 | AN3 | AN2 | AN1 | AN0 |
|---------------------|------|------|------|-----|-----|--------------------|--------------------|--------------------|-----|-----|-----|-----|-----|
| 0000 <sup>(1)</sup> | A    | A    | A    | A   | A   | A                  | A                  | A                  | A   | A   | A   | A   | A   |
| 0001                | A    | A    | A    | A   | A   | A                  | A                  | A                  | A   | A   | A   | A   | A   |
| 0010                | A    | A    | A    | A   | A   | A                  | A                  | A                  | A   | A   | A   | A   | A   |
| 0011                | D    | A    | A    | A   | A   | A                  | A                  | A                  | A   | A   | A   | A   | A   |
| 0100                | D    | D    | A    | A   | A   | A                  | A                  | A                  | A   | A   | A   | A   | A   |
| 0101                | D    | D    | D    | A   | A   | A                  | A                  | A                  | A   | A   | A   | A   | A   |
| 0110                | D    | D    | D    | D   | A   | A                  | A                  | A                  | A   | A   | A   | A   | A   |
| 0111 <sup>(1)</sup> | D    | D    | D    | D   | D   | A                  | A                  | A                  | A   | A   | A   | A   | A   |
| 1000                | D    | D    | D    | D   | D   | D                  | A                  | A                  | A   | A   | A   | A   | A   |
| 1001                | D    | D    | D    | D   | D   | D                  | D                  | A                  | A   | A   | A   | A   | A   |
| 1010                | D    | D    | D    | D   | D   | D                  | D                  | D                  | A   | A   | A   | A   | A   |
| 1011                | D    | D    | D    | D   | D   | D                  | D                  | D                  | D   | A   | A   | A   | A   |
| 1100                | D    | D    | D    | D   | D   | D                  | D                  | D                  | D   | D   | A   | A   | A   |
| 1101                | D    | D    | D    | D   | D   | D                  | D                  | D                  | D   | D   | D   | A   | A   |
| 1110                | D    | D    | D    | D   | D   | D                  | D                  | D                  | D   | D   | D   | D   | A   |
| 1111                | D    | D    | D    | D   | D   | D                  | D                  | D                  | D   | D   | D   | D   | D   |

A = Analog input

D = Digital I/O

**Note 1:** The Reset value of the PCFG bits depends on the value of the PBDEN Configuration bit. When PBDEN = 1, PCFG<3:0> = 0000; when PBDEN = 0, PCFG<3:0> = 0111.

**2:** AN5 through AN7 are available only on 40-pin and 44-pin devices.

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## REGISTER 2-3: ADCON2: A/D CONTROL REGISTER 2

|       |     |       |       |       |       |       |       |
|-------|-----|-------|-------|-------|-------|-------|-------|
| R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| ADFM  | —   | ACQT2 | ACQT1 | ACQT0 | ADCS2 | ADCS1 | ADCS0 |
| bit 7 |     |       |       |       |       |       | bit 0 |

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 7      **ADFM:** A/D Result Format Select bit  
1 = Right justified  
0 = Left justified
- bit 6      **Unimplemented:** Read as '0'
- bit 5-3    **ACQT2:ACQT0:** A/D Acquisition Time Select bits  
111 = 20 TAD  
110 = 16 TAD  
101 = 12 TAD  
100 = 8 TAD  
011 = 6 TAD  
010 = 4 TAD  
001 = 2 TAD  
000 = 0 TAD<sup>(1)</sup>
- bit 2-0    **ADCS2:ADCS0:** A/D Conversion Clock Select bits  
111 = FRC (clock derived from A/D RC oscillator)<sup>(1)</sup>  
110 = FOSC/64  
101 = FOSC/16  
100 = FOSC/4  
011 = FRC (clock derived from A/D RC oscillator)<sup>(1)</sup>  
010 = FOSC/32  
001 = FOSC/8  
000 = FOSC/2

**Note 1:** If the A/D FRC clock source is selected, a delay of one T<sub>CY</sub> (instruction cycle) is added before the A/D clock starts. This allows the *SLEEP* instruction to be executed before starting a conversion.

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The analog reference voltage is software selectable to either the device's positive and negative supply voltage (VDD and VSS), or the voltage level on the RA3/AN3/VREF+ and RA2/AN2/VREF-/CVREF pins.

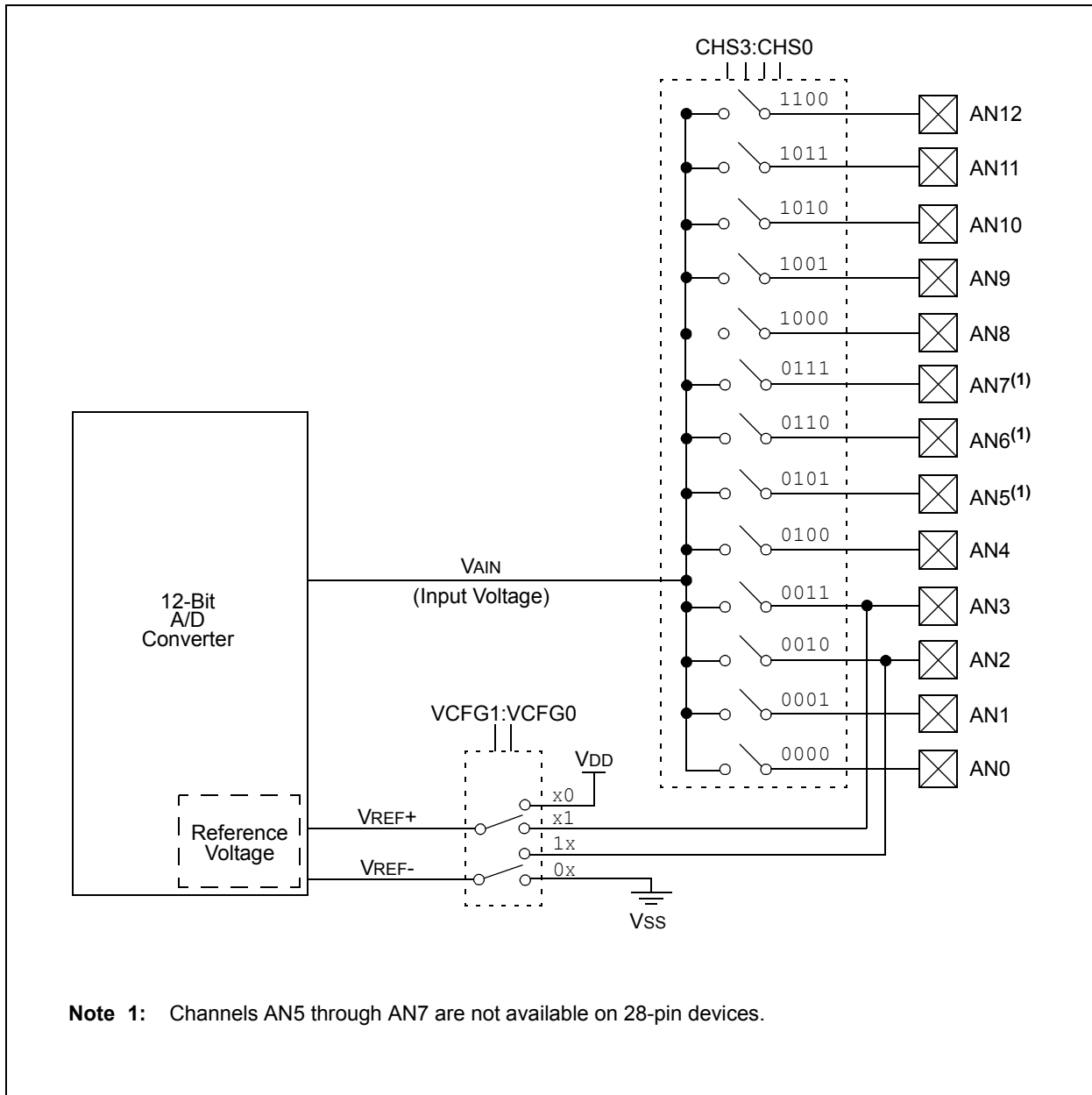
The A/D Converter has a unique feature of being able to operate while the device is in Sleep mode. To operate in Sleep, the A/D conversion clock must be derived from the A/D's internal RC oscillator.

The output of the sample and hold is the input into the Converter, which generates the result via successive approximation.

A device Reset forces all registers to their Reset state. This forces the A/D module to be turned off and any conversion in progress is aborted.

Each port pin associated with the A/D Converter can be configured as an analog input or as a digital I/O. The ADRESH and ADRESL registers contain the result of the A/D conversion. When the A/D conversion is complete, the result is loaded into the ADRESH:ADRESL register pair, the GO/DONE bit (ADCON0 register) is cleared and the A/D Interrupt Flag bit, ADIF, is set. The block diagram of the A/D module is shown in Figure 2-1.

**FIGURE 2-1: A/D BLOCK DIAGRAM**





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The value in the ADRESH:ADRESL registers is unknown following Power-on and Brown-out Resets, and is not affected by any other Reset.

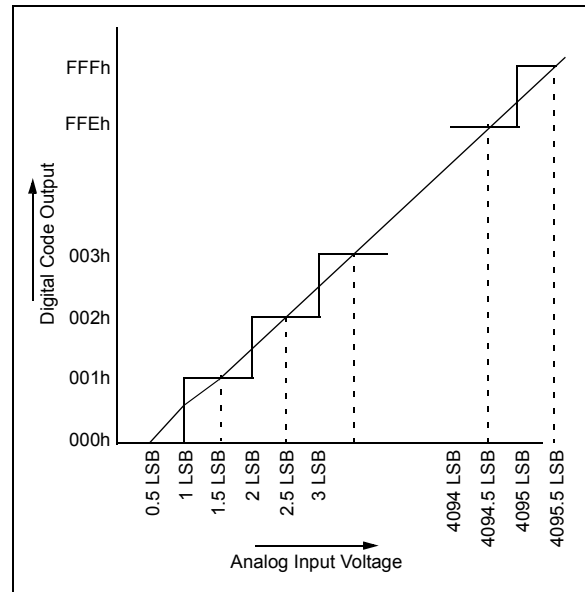
After the A/D module has been configured as desired, the selected channel must be acquired before the conversion is started. The analog input channels must have their corresponding TRIS bits selected as an input. To determine acquisition time, see **Section 2.1 “A/D Acquisition Requirements”**. After this acquisition time has elapsed, the A/D conversion can be started. An acquisition time can be programmed to occur between setting the GO/DONE bit and the actual start of the conversion.

The following steps should be followed to perform an A/D conversion:

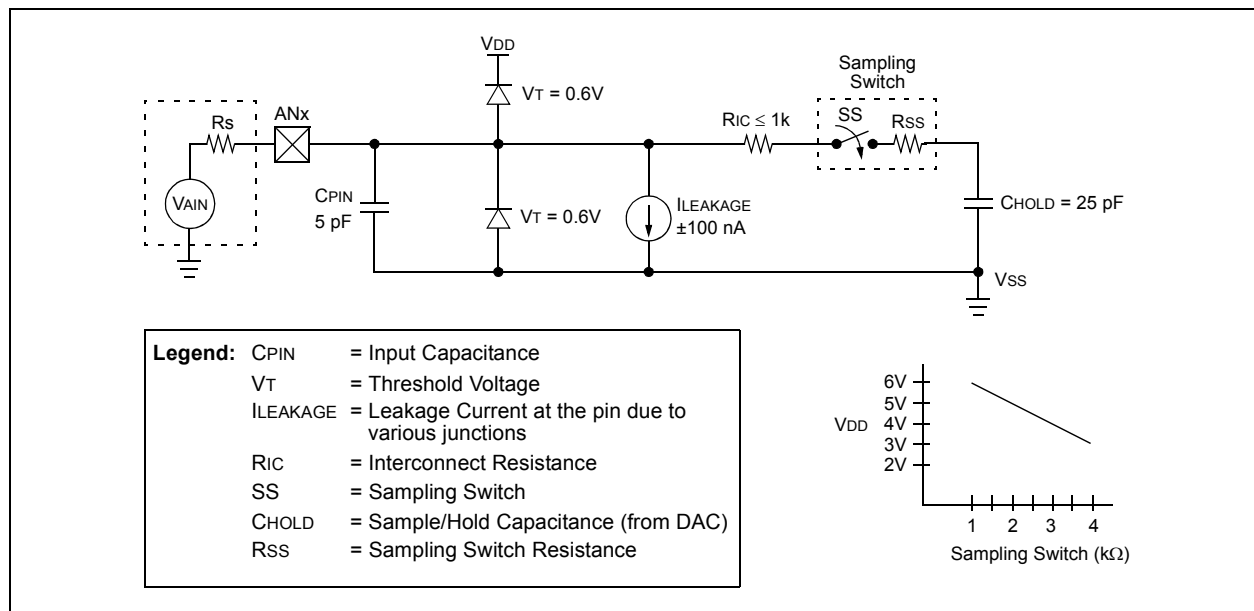
1. Configure the A/D module:
  - Configure analog pins, voltage reference and digital I/O (ADCON1)
  - Select A/D input channel (ADCON0)
  - Select A/D acquisition time (ADCON2)
  - Select A/D conversion clock (ADCON2)
  - Turn on A/D module (ADCON0)
2. Configure A/D interrupt (if desired):
  - Clear ADIF bit
  - Set ADIE bit
  - Set GIE bit
3. Wait the required acquisition time (if required).
4. Start conversion:
  - Set GO/DONE bit (ADCON0 register)

5. Wait for A/D conversion to complete, by either:
  - Polling for the GO/DONE bit to be cleared
 OR
  - Waiting for the A/D interrupt
6. Read A/D Result registers (ADRESH:ADRESL); clear bit ADIF, if required.
7. For next conversion, go to step 1 or step 2, as required. The A/D conversion time per bit is defined as T<sub>AD</sub>. A minimum wait of 2 T<sub>AD</sub> is required before the next acquisition starts.

**FIGURE 2-2: A/D TRANSFER FUNCTION**



**FIGURE 2-3: ANALOG INPUT MODEL**



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## 2.1 A/D Acquisition Requirements

For the A/D Converter to meet its specified accuracy, the charge holding capacitor (CHOLD) must be allowed to fully charge to the input channel voltage level. The analog input model is shown in Figure 2-3. The source impedance (Rs) and the internal sampling switch (Rss) impedance directly affect the time required to charge the capacitor CHOLD. The sampling switch (Rss) impedance varies over the device voltage (VDD). The source impedance affects the offset voltage at the analog input (due to pin leakage current). **The maximum recommended impedance for analog sources is 2.5 kΩ.** After the analog input channel is selected (changed), the channel must be sampled for at least the minimum acquisition time before starting a conversion.

**Note:** When the conversion is started, the holding capacitor is disconnected from the input pin.

To calculate the minimum acquisition time, Equation 2-1 may be used. This equation assumes that 1/2 LSB error is used (4096 steps for the 12-bit A/D). The 1/2 LSB error is the maximum error allowed for the A/D to meet its specified resolution.

Example 2-3 shows the calculation of the minimum required acquisition time, TACQ. This calculation is based on the following application system assumptions:

|                  |   |                    |
|------------------|---|--------------------|
| CHOLD            | = | 25 pF              |
| Rs               | = | 2.5 kΩ             |
| Conversion Error | ≤ | 1/2 LSB            |
| VDD              | = | 3V → Rss = 4 kΩ    |
| Temperature      | = | 85°C (system max.) |

### EQUATION 2-1: ACQUISITION TIME

$$\begin{aligned} TACQ &= \text{Amplifier Settling Time} + \text{Holding Capacitor Charging Time} + \text{Temperature Coefficient} \\ &= TAMP + TC + TCOFF \end{aligned}$$

### EQUATION 2-2: A/D MINIMUM CHARGING TIME

$$\begin{aligned} V_{HOLD} &= (V_{REF} - (V_{REF}/4096)) \cdot (1 - e^{-(Tc/CHOLD)(RIC + Rss + Rs)}) \\ \text{or} \\ Tc &= -(CHOLD)(RIC + Rss + Rs) \ln(1/4096) \end{aligned}$$

### EQUATION 2-3: CALCULATING THE MINIMUM REQUIRED ACQUISITION TIME

$$\begin{aligned} TACQ &= TAMP + TC + TCOFF \\ TAMP &= 0.2 \mu\text{s} \\ TCOFF &= (\text{Temp} - 25^\circ\text{C})(0.02 \mu\text{s}/^\circ\text{C}) \\ &\quad (85^\circ\text{C} - 25^\circ\text{C})(0.02 \mu\text{s}/^\circ\text{C}) \\ &\quad 1.2 \mu\text{s} \end{aligned}$$

Temperature coefficient is only required for temperatures > 25°C. Below 25°C, TCOFF = 0 μs.

$$\begin{aligned} TC &= -(CHOLD)(RIC + Rss + Rs) \ln(1/4096) \mu\text{s} \\ &\quad -(25 \text{ pF})(1 \text{ k}\Omega + 4 \text{ k}\Omega + 2.5 \text{ k}\Omega) \ln(0.0002441) \mu\text{s} \\ &\quad 1.56 \mu\text{s} \\ TACQ &= 0.2 \mu\text{s} + 1.56 \mu\text{s} + 1.2 \mu\text{s} \\ &\quad 2.96 \mu\text{s} \end{aligned}$$

## 2.2 Selecting and Configuring Acquisition Time

The ADCON2 register allows the user to select an acquisition time that occurs each time the GO/DONE bit is set. It also gives users the option to use an automatically determined acquisition time.

Acquisition time may be set with the ACQT2:ACQT0 bits (ADCON2<5:3>), which provides a range of 2 to 20 TAD. When the GO/DONE bit is set, the A/D module continues to sample the input for the selected acquisition time, then automatically begins a conversion. Since the acquisition time is programmed, there may be no need to wait for an acquisition time between selecting a channel and setting the GO/DONE bit.

Manual acquisition is selected when ACQT2:ACQT0 = 000. When the GO/DONE bit is set, sampling is stopped and a conversion begins. The user is responsible for ensuring the required acquisition time has passed between selecting the desired input channel and setting the GO/DONE bit. This option is also the default Reset state of the ACQT2:ACQT0 bits and is compatible with devices that do not offer programmable acquisition times.

In either case, when the conversion is completed, the GO/DONE bit is cleared, the ADIF flag is set and the A/D begins sampling the currently selected channel again. If an acquisition time is programmed, there is nothing to indicate if the acquisition time has ended or if the conversion has begun.

## 2.3 Selecting the A/D Conversion Clock

The A/D conversion time per bit is defined as TAD. The A/D conversion requires 13 TAD per 12-bit conversion. The source of the A/D conversion clock is software selectable. There are seven possible options for TAD:

- 2 TOSC
- 4 TOSC
- 8 TOSC
- 16 TOSC
- 32 TOSC
- 64 TOSC
- Internal RC Oscillator

For correct A/D conversions, the A/D conversion clock (TAD) must be as short as possible, but greater than the minimum TAD (see parameter 130 for more information).

Table 2-1 shows the resultant TAD times derived from the device operating frequencies and the A/D clock source selected.

**TABLE 2-1: TAD vs. DEVICE OPERATING FREQUENCIES**

| A/D Clock Source (TAD) |             | Assumes TAD Min. = 0.8 $\mu$ s |
|------------------------|-------------|--------------------------------|
| Operation              | ADCS2:ADCS0 | Maximum FOSC                   |
| 2 TOSC                 | 000         | 2.50 MHz                       |
| 4 TOSC                 | 100         | 5.00 MHz                       |
| 8 TOSC                 | 001         | 10.00 MHz                      |
| 16 TOSC                | 101         | 20.00 MHz                      |
| 32 TOSC                | 010         | 40.00 MHz                      |
| 64 TOSC                | 110         | 48.00 MHz                      |
| RC <sup>(1)</sup>      | x11         | 1.00 MHz <sup>(2)</sup>        |

**Note 1:** The RC source has a typical TAD time of 2.5  $\mu$ s.

- 2:** For device frequencies above 1 MHz, the device must be in Sleep for the entire conversion or a FOSC divider should be used instead; otherwise, the A/D accuracy specification may not be met.

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## 2.4 Operation in Power-Managed Modes

The selection of the automatic acquisition time and A/D conversion clock is determined in part by the clock source and frequency while in a power-managed mode.

If the A/D is expected to operate while the device is in a power-managed mode, the AD<sub>CS</sub>2:AD<sub>CS</sub>0 bits in AD<sub>CON</sub>2 should be updated in accordance with the clock source to be used. The AC<sub>QT</sub>2:AC<sub>QT</sub>0 bits do not need to be adjusted as the AD<sub>CS</sub>2:AD<sub>CS</sub>0 bits adjust the T<sub>AD</sub> time for the new clock speed. After entering the mode, an A/D acquisition or conversion may be started. Once started, the device should continue to be clocked by the same clock source until the conversion has been completed.

If desired, the device may be placed into the corresponding Idle mode during the conversion. If the device clock frequency is less than 1 MHz, the A/D RC clock source should be selected.

Operation in Sleep mode requires the A/D FRC clock to be selected. If bits AC<sub>QT</sub>2:AC<sub>QT</sub>0 are set to '000' and a conversion is started, the conversion will be delayed one instruction cycle to allow execution of the `SLEEP` instruction and entry to Sleep mode. The IDLEN bit (OSCCON<7>) must have already been cleared prior to starting the conversion.

## 2.5 Configuring Analog Port Pins

The AD<sub>CON</sub>1, TRISA, TRISB and TRISE registers all configure the A/D port pins. The port pins needed as analog inputs must have their corresponding TRIS bits set (input). If the TRIS bit is cleared (output), the digital output level (V<sub>OH</sub> or V<sub>OL</sub>) will be converted.

The A/D operation is independent of the state of the CHS3:CHS0 bits and the TRIS bits.

- |  |
|--|
| <p><b>Note 1:</b> When reading the PORT register, all pins configured as analog input channels will read as cleared (a low level). Analog conversion on pins configured as digital pins can be performed. The voltage on the pin will be accurately converted.</p> <p><b>2:</b> Analog levels on any pin defined as a digital input may cause the digital input buffer to consume current out of the device's specification limits.</p> <p><b>3:</b> The P<sub>BADEN</sub> bit in Configuration Register 3H configures PORTB pins to reset as analog or digital pins by controlling how the PCFG3:PCFG0 bits in AD<sub>CON</sub>1 are reset.</p> |
|--|

## 2.6 A/D Conversions

Figure 2-4 shows the operation of the A/D Converter after the  $\overline{\text{GO/DONE}}$  bit has been set and the ACQT2:ACQT0 bits are cleared. A conversion is started after the following instruction to allow entry into Sleep mode before the conversion begins.

Figure 2-5 shows the operation of the A/D Converter after the  $\overline{\text{GO/DONE}}$  bit has been set and the ACQT2:ACQT0 bits are set to '010', and selecting a 4 TAD acquisition time before the conversion starts.

Clearing the  $\overline{\text{GO/DONE}}$  bit during a conversion will abort the current conversion. The A/D Result register pair will NOT be updated with the partially completed A/D conversion sample. This means the ADRESH:ADRESL registers will continue to contain the value of the last completed conversion (or the last value written to the ADRESH:ADRESL registers).

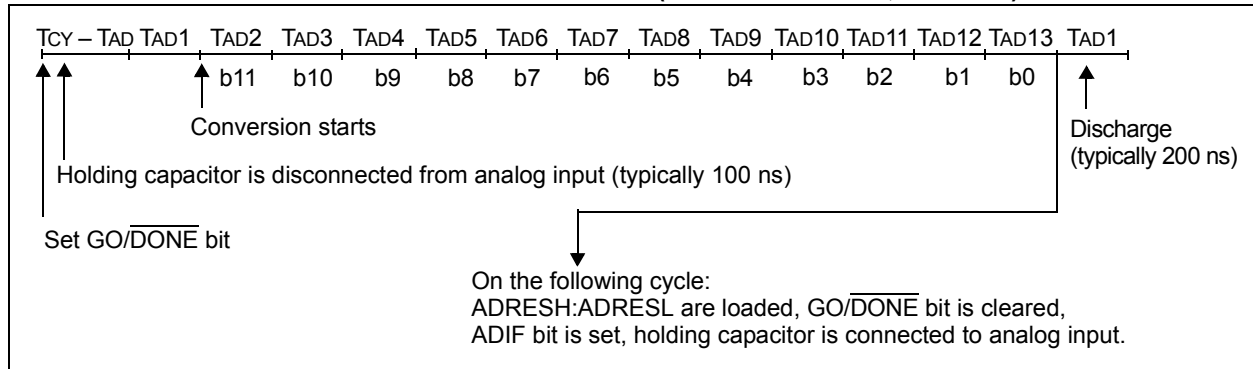
After the A/D conversion is completed or aborted, a  $2 T_{CY}$  wait is required before the next acquisition can be started. After this wait, acquisition on the selected channel is automatically started.

**Note:** The  $\overline{\text{GO/DONE}}$  bit should **NOT** be set in the same instruction that turns on the A/D. Code should wait at least  $2 \mu\text{s}$  after enabling the A/D before beginning an acquisition and conversion cycle.

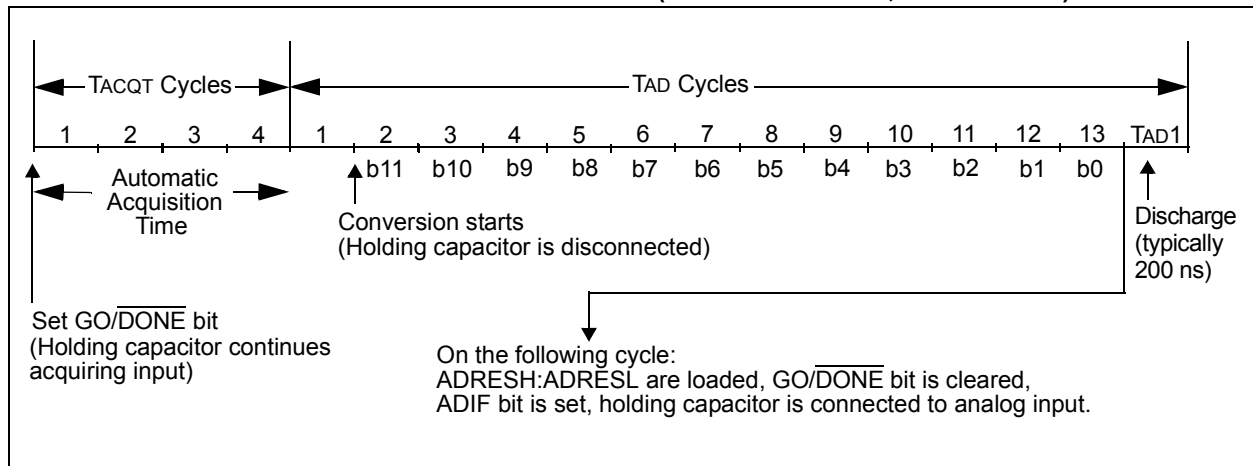
## 2.7 Discharge

The discharge phase is used to initialize the value of the holding capacitor. The array is discharged before every sample. This feature helps to optimize the unity gain amplifier, as the circuit always needs to charge the capacitor array, rather than charge/discharge based on previous measure values.

**FIGURE 2-4: A/D CONVERSION TAD CYCLES (ACQT<2:0> = 000, TACQ = 0)**



**FIGURE 2-5: A/D CONVERSION TAD CYCLES (ACQT<2:0> = 010, TACQ = 4 TAD)**



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## 2.8 Use of the CCP2 Trigger

An A/D conversion can be started by the Special Event Trigger of the CCP2 module. This requires that the CCP2M3:CCP2M0 bits (CCP2CON<3:0>) be programmed as '1011' and that the A/D module is enabled (ADON bit is set). When the trigger occurs, the GO/DONE bit will be set, starting the A/D acquisition and conversion, and the Timer1 (or Timer3) counter will be reset to zero. Timer1 (or Timer3) is reset to automatically repeat the A/D acquisition period with minimal software overhead (firmware must move ADRESH:ADRESL to

the desired location). The appropriate analog input channel must be selected and the minimum acquisition period is either timed by the user, or an appropriate TACQ time selected before the Special Event Trigger sets the GO/DONE bit (starts a conversion).

If the A/D module is not enabled (ADON is cleared), the Special Event Trigger will be ignored by the A/D module, but will still reset the Timer1 (or Timer3) counter.

**TABLE 2-2: REGISTERS ASSOCIATED WITH A/D OPERATION**

| Name                 | Bit 7  | Bit 6                 | Bit 5                                 | Bit 4  | Bit 3              | Bit 2                     | Bit 1              | Bit 0              | Reset Values on Page: |
|----------------------|--|-----------------------|---------------------------------------|--------|--------------------|---------------------------|--------------------|--------------------|-----------------------|
| INTCON               | GIE/GIEH   | PEIE/GIEL             | TMR0IE                                | INT0IE | RBIE               | TMR0IF                    | INT0IF             | RBIF               | (4)                   |
| PIR1                 | SPPIF <sup>(1)</sup>                                     | ADIF                  | RCIF                                  | TXIF   | SSPIF              | CCP1IF                    | TMR2IF             | TMR1IF             | (4)                   |
| PIE1                 | SPPIE <sup>(1)</sup>                                     | ADIE                  | RCIE                                  | TXIE   | SSPIE              | CCP1IE                    | TMR2IE             | TMR1IE             | (4)                   |
| IPR1                 | SPPIP <sup>(1)</sup>                                     | ADIP                  | RCIP                                  | TXIP   | SSPIP              | CCP1IP                    | TMR2IP             | TMR1IP             | (4)                   |
| PIR2                 | OSCFIF   | CMIF                  | USBIF                                 | EEIF   | BCLIF              | HLVDIF                    | TMR3IF             | CCP2IF             | (4)                   |
| PIE2                 | OSCFIE   | CMIE                  | USBIE                                 | EEIE   | BCLIE              | HLVDIE                    | TMR3IE             | CCP2IE             | (4)                   |
| IPR2                 | OSCFIP   | CMIP                  | USBIP                                 | EEIP   | BCLIP              | HLVDIP                    | TMR3IP             | CCP2IP             | (4)                   |
| ADRESH               | A/D Result Register High Byte                            |                       |                                       |        |                    |                           |                    |                    | (4)                   |
| ADRESL               | A/D Result Register Low Byte                             |                       |                                       |        |                    |                           |                    |                    | (4)                   |
| ADCON0               | —  | —                     | CHS3                                  | CHS2   | CHS1               | CHS0                      | GO/DONE            | ADON               | 21                    |
| ADCON1               | —  | —                     | VCFG1                                 | VCFG0  | PCFG3              | PCFG2                     | PCFG1              | PCFG0              | 22                    |
| ADCON2               | ADFM   | —                     | ACQT2                                 | ACQT1  | ACQT0              | ADCS2                     | ADCS1              | ADCS0              | 23                    |
| PORTA                | —  | RA6 <sup>(2)</sup>    | RA5                                   | RA4    | RA3                | RA2                       | RA1                | RA0                | (4)                   |
| TRISA                | —  | TRISA6 <sup>(2)</sup> | PORTA Data Direction Control Register |        |                    |                           |                    |                    | (4)                   |
| PORTB                | RB7  | RB6                   | RB5                                   | RB4    | RB3                | RB2                       | RB1                | RB0                | (4)                   |
| TRISB                | PORTB Data Direction Control Register                    |                       |                                       |        |                    |                           |                    |                    | (4)                   |
| LATB                 | PORTB Data Latch Register (Read and Write to Data Latch) |                       |                                       |        |                    |                           |                    |                    | (4)                   |
| PORTE <sup>(1)</sup> | RDPU   | —                     | —                                     | —      | RE3 <sup>(3)</sup> | RE2 <sup>(1)</sup>        | RE1 <sup>(1)</sup> | RE0 <sup>(1)</sup> | (4)                   |
| TRISE <sup>(1)</sup> | —  | —                     | —                                     | —      | —                  | TRISE2                    | TRISE1             | TRISE0             | (4)                   |
| LATE <sup>(1)</sup>  | —  | —                     | —                                     | —      | —                  | PORTE Data Latch Register |                    |                    | (4)                   |

**Legend:** — = unimplemented, read as '0'. Shaded cells are not used for A/D conversion.

**Note 1:** These registers and/or bits are not implemented on 28-pin devices and are read as '0'.

**2:** RA6 and its associated latch and data direction bits are enabled as I/O pins based on oscillator configuration; otherwise, they are read as '0'.

**3:** RE3 port bit is available only as an input pin when the MCLRE Configuration bit is '0'.

**4:** For these Reset values, see the "PIC18F2455/2550/4455/4550 Data Sheet".

# PIC18F2458/2553/4458/4553

## 3.0 SPECIAL FEATURES OF THE CPU

**Note:** For additional details on the Configuration bits, refer to the “PIC18F2455/2550/4455/4550 Data Sheet”, Section 25.1 “Configuration Bits”. Device ID information presented in this section is for PIC18F2458/2553/4458/4553 only.

PIC18F2458/2553/4458/4553 devices include several features intended to maximize reliability and minimize cost through elimination of external components. These include:

- Device ID Registers

## 3.1 Device ID Registers

The Device ID registers are “read-only” registers. They identify the device type and revision to device programmers, and can be read by firmware using table reads.

**TABLE 3-1: DEVICE IDs**

| File Name | Bit 7  | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default/<br>Unprogrammed<br>Value |                          |
|-----------|--------|-------|-------|-------|-------|-------|-------|-------|-----------------------------------|--------------------------|
| 3FFFFEh   | DEVID1 | DEV2  | DEV1  | DEV0  | REV4  | REV3  | REV2  | REV1  | REV0                              | xxxx xxxx <sup>(1)</sup> |
| 3FFFFFh   | DEVID2 | DEV10 | DEV9  | DEV8  | DEV7  | DEV6  | DEV5  | DEV4  | DEV3                              | xxxx xxxx <sup>(1)</sup> |

**Legend:** x = unknown, u = unchanged

**Note 1:** See Register 3-1 and Register 3-2 for DEVID values. DEVID registers are read-only and cannot be programmed by the user.

# PIC18F2458/2553/4458/4553

## REGISTER 3-1: DEVID1: DEVICE ID REGISTER 1 FOR PIC18F2458/2553/4458/4553 DEVICES

|       |      |      |      |      |      |      |       |
|-------|------|------|------|------|------|------|-------|
| R     | R    | R    | R    | R    | R    | R    | R     |
| DEV2  | DEV1 | DEV0 | REV4 | REV3 | REV2 | REV1 | REV0  |
| bit 7 |      |      |      |      |      |      | bit 0 |

### Legend:

R = Read-only bit                      P = Programmable bit                      U = Unimplemented bit, read as '0'  
 -n = Value when device is unprogrammed                      u = Unchanged from programmed state

bit 7-5                      **DEV2:DEV0:** Device ID bits  
 See Register 3-2 for a complete listing.

bit 4-0                      **REV3:REV0:** Revision ID bits  
 These bits are used to indicate the device revision.

## REGISTER 3-2: DEVID2: DEVICE ID REGISTER 2 FOR PIC18F2458/2553/4458/4553 DEVICES

|       |      |      |      |      |      |      |       |
|-------|------|------|------|------|------|------|-------|
| R     | R    | R    | R    | R    | R    | R    | R     |
| DEV10 | DEV9 | DEV8 | DEV7 | DEV6 | DEV5 | DEV4 | DEV3  |
| bit 7 |      |      |      |      |      |      | bit 0 |

### Legend:

R = Read-only bit                      P = Programmable bit                      U = Unimplemented bit, read as '0'  
 -n = Value when device is unprogrammed                      u = Unchanged from programmed state

bit 7-0                      **DEV10:DEV3:** Device ID bits

| DEV10:DEV3<br>(DEVID2<7:0>) | DEV2:DEV0<br>(DEVID1<7:5>) | Device     |
|-----------------------------|----------------------------|------------|
| 0010 1010                   | 011                        | PIC18F2458 |
| 0010 1010                   | 010                        | PIC18F2553 |
| 0010 1010                   | 001                        | PIC18F4458 |
| 0010 1010                   | 000                        | PIC18F4553 |



## 4.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings (†)

|  |                       |
|--|-----------------------|
| Ambient temperature under bias .....   | -40°C to +125°C       |
| Storage temperature .....  | -65°C to +150°C       |
| Voltage on any pin with respect to VSS (except VDD and $\overline{\text{MCLR}}$ ) .....  | -0.3V to (VDD + 0.3V) |
| Voltage on VDD with respect to VSS .....   | -0.3V to +7.5V        |
| Voltage on $\overline{\text{MCLR}}$ with respect to VSS ( <b>Note 2</b> ) .....          | 0V to +13.25V         |
| Total power dissipation ( <b>Note 1</b> ) .....  | 1.0W                  |
| Maximum current out of VSS pin .....   | 300 mA                |
| Maximum current into VDD pin .....   | 250 mA                |
| Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0 or V <sub>I</sub> > VDD).....   | ±20 mA                |
| Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0 or V <sub>O</sub> > VDD) ..... | ±20 mA                |
| Maximum output current sunk by any I/O pin.....  | 25 mA                 |
| Maximum output current sourced by any I/O pin .....                                      | 25 mA                 |
| Maximum current sunk by all ports .....  | 200 mA                |
| Maximum current sourced by all ports .....   | 200 mA                |

**Note 1:** Power dissipation is calculated as follows:

$$P_{dis} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum (V_{OL} \times I_{OL})$$

- 2:** Voltage spikes below VSS at the  $\overline{\text{MCLR}}/\text{VPP}/\text{RE3}$  pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a “low” level to the  $\overline{\text{MCLR}}/\text{VPP}/\text{RE3}$  pin, rather than pulling this pin directly to VSS.

† **NOTICE:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

# PIC18F2458/2553/4458/4553

FIGURE 4-1: PIC18F2458/2553/4458/4553 VOLTAGE-FREQUENCY GRAPH (INDUSTRIAL)

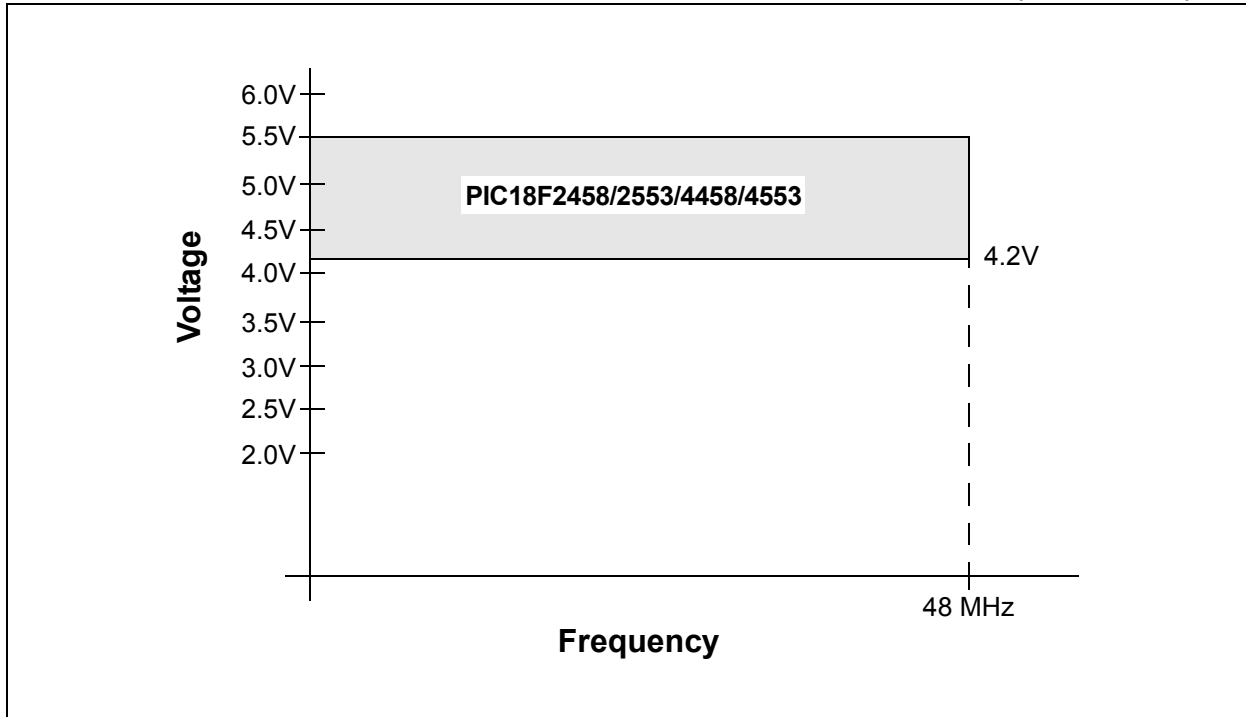
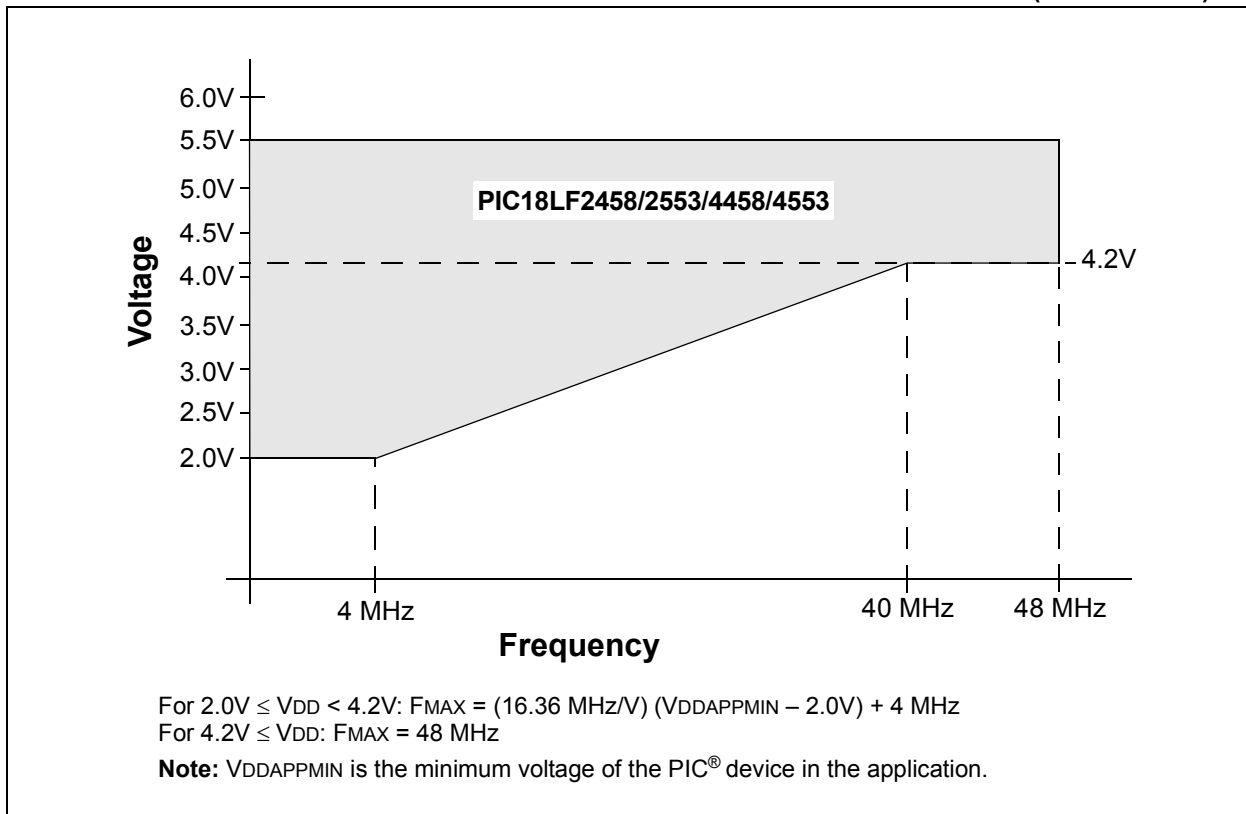


FIGURE 4-2: PIC18LF2458/2553/4458/4553 VOLTAGE-FREQUENCY GRAPH (INDUSTRIAL)



# PIC18F2458/2553/4458/4553

**TABLE 4-1: A/D CONVERTER CHARACTERISTICS: PIC18F2458/2553/4458/4553 (INDUSTRIAL)  
PIC18LF2458/2553/4458/4553 (INDUSTRIAL)**

| Param No. | Sym              | Characteristic                                       | Min                       | Typ     | Max               | Units      | Conditions  |                            |
|-----------|------------------|--|---------------------------|---------|-------------------|------------|---|----------------------------|
| A01       | NR               | Resolution   | —                         | —       | 12                | bit        |   | $\Delta V_{REF} \geq 3.0V$ |
| A03       | EIL              | Integral Linearity Error                             | —                         | $\pm 1$ | $\pm 2.0$         | LSB        | $V_{DD} = 3.0V$   | $\Delta V_{REF} \geq 3.0V$ |
|           |                  |  | —                         | —       | $\pm 2.0$         | LSB        | $V_{DD} = 5.0V$   |                            |
| A04       | EDL              | Differential Linearity Error                         | —                         | $\pm 1$ | +1.5/-1.0         | LSB        | $V_{DD} = 3.0V$   | $\Delta V_{REF} \geq 3.0V$ |
|           |                  |  | —                         | —       | +1.5/-1.0         | LSB        | $V_{DD} = 5.0V$   |                            |
| A06       | EOFF             | Offset Error   | —                         | $\pm 1$ | $\pm 5$           | LSB        | $V_{DD} = 3.0V$   | $\Delta V_{REF} \geq 3.0V$ |
|           |                  |  | —                         | —       | $\pm 3$           | LSB        | $V_{DD} = 5.0V$   |                            |
| A07       | EGN              | Gain Error   | —                         | $\pm 1$ | $\pm 1.25$        | LSB        | $V_{DD} = 3.0V$   | $\Delta V_{REF} \geq 3.0V$ |
|           |                  |  | —                         | —       | $\pm 2.00$        | LSB        | $V_{DD} = 5.0V$   |                            |
| A10       | —                | Monotonicity   | Guaranteed <sup>(1)</sup> |         |                   | —          | $V_{SS} \leq V_{AIN} \leq V_{REF}$                            |                            |
| A20       | $\Delta V_{REF}$ | Reference Voltage Range<br>( $V_{REFH} - V_{REFL}$ ) | 3                         | —       | $V_{DD} - V_{SS}$ | V          | For 12-bit resolution   |                            |
| A21       | $V_{REFH}$       | Reference Voltage High                               | $V_{SS} + 3.0V$           | —       | $V_{DD} + 0.3V$   | V          | For 12-bit resolution   |                            |
| A22       | $V_{REFL}$       | Reference Voltage Low                                | $V_{SS} - 0.3V$           | —       | $V_{DD} - 3.0V$   | V          | For 12-bit resolution   |                            |
| A25       | $V_{AIN}$        | Analog Input Voltage                                 | $V_{REFL}$                | —       | $V_{REFH}$        | V          |   |                            |
| A30       | $Z_{AIN}$        | Recommended Impedance of Analog Voltage Source       | —                         | —       | 2.5               | k $\Omega$ |   |                            |
| A50       | IREF             | $V_{REF}$ Input Current <sup>(2)</sup>               | —                         | —       | 5                 | $\mu A$    | During $V_{AIN}$ acquisition.<br>During A/D conversion cycle. |                            |
|           |                  |  | —                         | —       | 150               | $\mu A$    |   |                            |

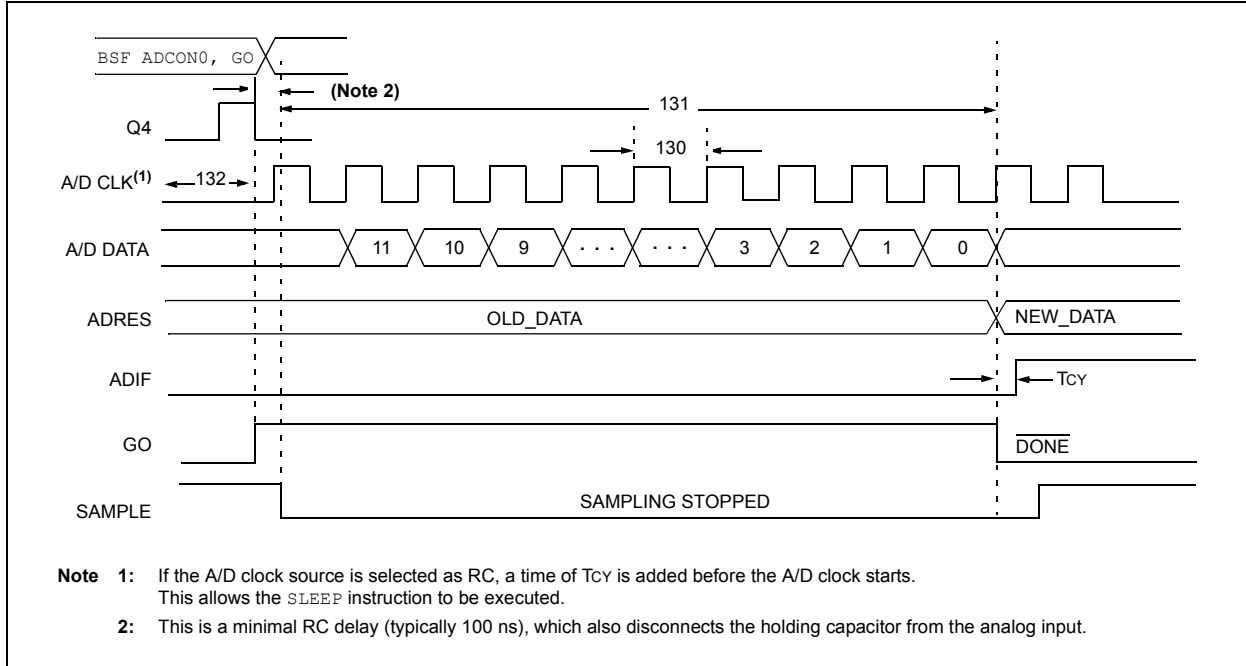
**Note 1:** The A/D conversion result never decreases with an increase in the input voltage and has no missing codes.

**Note 2:**  $V_{REFH}$  current is from the RA3/AN3/ $V_{REF+}$  pin or  $V_{DD}$ , whichever is selected as the  $V_{REFH}$  source.

$V_{REFL}$  current is from the RA2/AN2/ $V_{REF-}/CV_{REF}$  pin or  $V_{SS}$ , whichever is selected as the  $V_{REFL}$  source.

# PIC18F2458/2553/4458/4553

**FIGURE 4-3: A/D CONVERSION TIMING**



**TABLE 4-2: A/D CONVERSION REQUIREMENTS**

| Param No. | Symbol           | Characteristic  | Min         | Max      | Units               | Conditions |  |
|-----------|------------------|---|-------------|----------|---------------------|------------|--|
| 130       | TAD              | A/D Clock Period  | PIC18FXXXX  | 0.8      | 12.5 <sup>(1)</sup> | μS         | TOSC based, VREF ≥ 3.0V                    |
|           |                  |   | PIC18LFXXXX | 1.4      | 25.0 <sup>(1)</sup> | μS         | VDD = 3.0V;<br>TOSC based, VREF full range |
|           |                  |   | PIC18FXXXX  | —        | 1                   | μS         | A/D RC mode                                |
|           |                  |   | PIC18LFXXXX | —        | 3                   | μS         | VDD = 3.0V; A/D RC mode                    |
| 131       | T <sub>cnv</sub> | Conversion Time (not including acquisition time) <sup>(2)</sup> | 13          | 14       | TAD                 |            |  |
| 132       | T <sub>acq</sub> | Acquisition Time <sup>(3)</sup>                                 | 1.4         | —        | μS                  |            |  |
| 135       | T <sub>swc</sub> | Switching Time from Convert → Sample                            | —           | (Note 4) |                     |            |  |
| 137       | T <sub>dis</sub> | Discharge Time  | 0.2         | —        | μS                  |            |  |

- Note 1:** The time of the A/D clock period is dependent on the device frequency and the TAD clock divider.
- Note 2:** ADRES registers may be read on the following T<sub>cy</sub> cycle.
- Note 3:** The time for the holding capacitor to acquire the “New” input voltage when the voltage changes full scale after the conversion (VDD to VSS or VSS to VDD). The source impedance (RS) on the input channels is 50Ω.
- Note 4:** On the following cycle of the device clock.

## 5.0 PACKAGING INFORMATION

For packaging information, see the “*PIC18F2455/2550/4455/4550 Data Sheet*” (DS39632).

# PIC18F2458/2553/4458/4553

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NOTES:

# PIC18F2458/2553/4458/4553

## APPENDIX A: REVISION HISTORY

### Revision A (May 2007)

Original data sheet for the PIC18F2458/2553/4458/4553 devices.

### Revision B (June 2007)

Changes to Figure 4-2: PIC18LF2458/2553/4458/4553 Voltage-Frequency Graph (Industrial).

### Revision C (October 2009)

Removed "Preliminary" marking.

## APPENDIX B: DEVICE DIFFERENCES

The differences between the devices listed in this data sheet are shown in Table B-1.

**TABLE B-1: DEVICE DIFFERENCES**

| Features                             | PIC18F2458                  | PIC18F2553                  | PIC18F4458                               | PIC18F4553                               |
|--------------------------------------|-----------------------------|-----------------------------|--|--|
| Program Memory (Bytes)               | 24576                       | 32768                       | 24576                                    | 32768                                    |
| Program Memory (Instructions)        | 12288                       | 16384                       | 12288                                    | 16384                                    |
| Interrupt Sources                    | 19                          | 19                          | 20                                       | 20                                       |
| I/O Ports                            | Ports A, B, C, (E)          | Ports A, B, C, (E)          | Ports A, B, C, D, E                      | Ports A, B, C, D, E                      |
| Capture/Compare/PWM Modules          | 2                           | 2                           | 1  | 1  |
| Enhanced Capture/Compare/PWM Modules | 0                           | 0                           | 1  | 1  |
| Parallel Communications (SPP)        | No                          | No                          | Yes                                      | Yes                                      |
| 12-Bit Analog-to-Digital Module      | 10 Input Channels           | 10 Input Channels           | 13 Input Channels                        | 13 Input Channels                        |
| Packages                             | 28-Pin SPDIP<br>28-Pin SOIC | 28-Pin SPDIP<br>28-Pin SOIC | 40-Pin PDIP<br>44-Pin TQFP<br>44-Pin QFN | 40-Pin PDIP<br>44-Pin TQFP<br>44-Pin QFN |

# PIC18F2458/2553/4458/4553

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## **APPENDIX C: MIGRATION FROM MID-RANGE TO ENHANCED DEVICES**

A detailed discussion of the differences between the mid-range MCU devices (i.e., PIC16CXXX) and the enhanced devices (i.e., PIC18FXXX) is provided in AN716, "*Migrating Designs from PIC16C74A/74B to PIC18C442*". The changes discussed, while device specific, are generally applicable to all mid-range to enhanced device migrations.

This Application Note is available as Literature Number DS00716.

## **APPENDIX D: MIGRATION FROM HIGH-END TO ENHANCED DEVICES**

A detailed discussion of the migration pathway and differences between the high-end MCU devices (i.e., PIC17CXXX) and the enhanced devices (i.e., PIC18FXXX) is provided in AN726, "*PIC17CXXX to PIC18CXXX Migration*".

This Application Note is available as Literature Number DS00726.



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# PIC18F2458/2553/4458/4553

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

| <u>PART NO.</u>   | <u>X</u>   | <u>/XX</u> | <u>XXX</u> |
|-------------------|--|------------|------------|
| Device            | Temperature Range  | Package    | Pattern    |
| Device            | PIC18F2458/2553 <sup>(1)</sup> , PIC18F4458/4553 <sup>(1)</sup> ,<br>PIC18F2458/2553T <sup>(2)</sup> , PIC18F4458/4553T <sup>(2)</sup> ;<br>V <sub>DD</sub> range 4.2V to 5.5V<br>PIC18LF2458/2553 <sup>(1)</sup> , PIC18LF4458/4553 <sup>(1)</sup> ,<br>PIC18LF2458/2553T <sup>(2)</sup> , PIC18LF4458/4553T <sup>(2)</sup> ;<br>V <sub>DD</sub> range 2.0V to 5.5V |            |            |
| Temperature Range | I = -40°C to +85°C (Industrial)<br>E = -40°C to +125°C (Extended)  |            |            |
| Package           | PT = TQFP (Thin Quad Flatpack)<br>SO = SOIC<br>SP = Skinny PDIP<br>P = PDIP<br>ML = QFN  |            |            |
| Pattern           | QTP, SQTP, Code or Special Requirements<br>(blank otherwise)   |            |            |

**Examples:**

- a) PIC18LF4553-I/P 301 = Industrial temp., PDIP package, Extended V<sub>DD</sub> limits, QTP pattern #301.
- b) PIC18LF2458-I/SO = Industrial temp., SOIC package, Extended V<sub>DD</sub> limits.
- c) PIC18F4458-I/P = Industrial temp., PDIP package, normal V<sub>DD</sub> limits.

**Note 1:** F = Standard Voltage Range  
 LF = Wide Voltage Range  
**2:** T = In tape and reel TQFP packages only.



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**China - Shenzhen**  
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Fax: 86-755-8203-1760

**China - Wuhan**  
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Fax: 86-27-5980-5118

**China - Xiamen**  
Tel: 86-592-2388138  
Fax: 86-592-2388130

**China - Xian**  
Tel: 86-29-8833-7252  
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**China - Zhuhai**  
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### ASIA/PACIFIC

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Fax: 91-80-3090-4080

**India - New Delhi**  
Tel: 91-11-4160-8631  
Fax: 91-11-4160-8632

**India - Pune**  
Tel: 91-20-2566-1512  
Fax: 91-20-2566-1513

**Japan - Yokohama**  
Tel: 81-45-471- 6166  
Fax: 81-45-471-6122

**Korea - Daegu**  
Tel: 82-53-744-4301  
Fax: 82-53-744-4302

**Korea - Seoul**  
Tel: 82-2-554-7200  
Fax: 82-2-558-5932 or  
82-2-558-5934

**Malaysia - Kuala Lumpur**  
Tel: 60-3-6201-9857  
Fax: 60-3-6201-9859

**Malaysia - Penang**  
Tel: 60-4-227-8870  
Fax: 60-4-227-4068

**Philippines - Manila**  
Tel: 63-2-634-9065  
Fax: 63-2-634-9069

**Singapore**  
Tel: 65-6334-8870  
Fax: 65-6334-8850

**Taiwan - Hsin Chu**  
Tel: 886-3-6578-300  
Fax: 886-3-6578-370

**Taiwan - Kaohsiung**  
Tel: 886-7-536-4818  
Fax: 886-7-536-4803

**Taiwan - Taipei**  
Tel: 886-2-2500-6610  
Fax: 886-2-2508-0102

**Thailand - Bangkok**  
Tel: 66-2-694-1351  
Fax: 66-2-694-1350

### EUROPE

**Austria - Wels**  
Tel: 43-7242-2244-39  
Fax: 43-7242-2244-393

**Denmark - Copenhagen**  
Tel: 45-4450-2828  
Fax: 45-4485-2829

**France - Paris**  
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Fax: 33-1-69-30-90-79

**Germany - Munich**  
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Fax: 49-89-627-144-44

**Italy - Milan**  
Tel: 39-0331-742611  
Fax: 39-0331-466781

**Netherlands - Drunen**  
Tel: 31-416-690399  
Fax: 31-416-690340

**Spain - Madrid**  
Tel: 34-91-708-08-90  
Fax: 34-91-708-08-91

**UK - Wokingham**  
Tel: 44-118-921-5869  
Fax: 44-118-921-5820



Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



#### Как с нами связаться

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