

GC1115 Daughterboard EVM

User's Guide

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GC1115 Daughterboard Description

The GC1115 Daughterboard and GC101 EVM comprise a two-part daughterboard and motherboard used for demonstrating the GC1115 CFR. The GC1115 Daughterboard hardware is a plug-in board to the GC101 EVM.

The GC1115 is a flexible, programmable, wideband crest factor reduction (CFR) processor with a maximum composite bandwidth of 20 MHz. The GC1115 selectively reduces the peak-to-average ratio (PAR) of wideband digital signals provided in quadrature (I & Q) format, such as those used in third-generation (3G) code division multiple access (CDMA) wireless applications. Reducing the PAR of digital signals can improve the efficiency of follow-on power amplifiers (PAs), ease the D/A converter requirements and eliminate the out-of-band spectral regrowth caused by simple hard limiting.

This document will describe the hardware portion of the GC1115 and its interface to the GC101 EVM. More information about the GC101 EVM can be found in the GC101 EVM User's Guide. Figure 1-1 is a high level block diagram of the GC101 and the interface it provides to the GC1115. Figure 1-2 is a block diagram of the GC1115 Daughterboard.

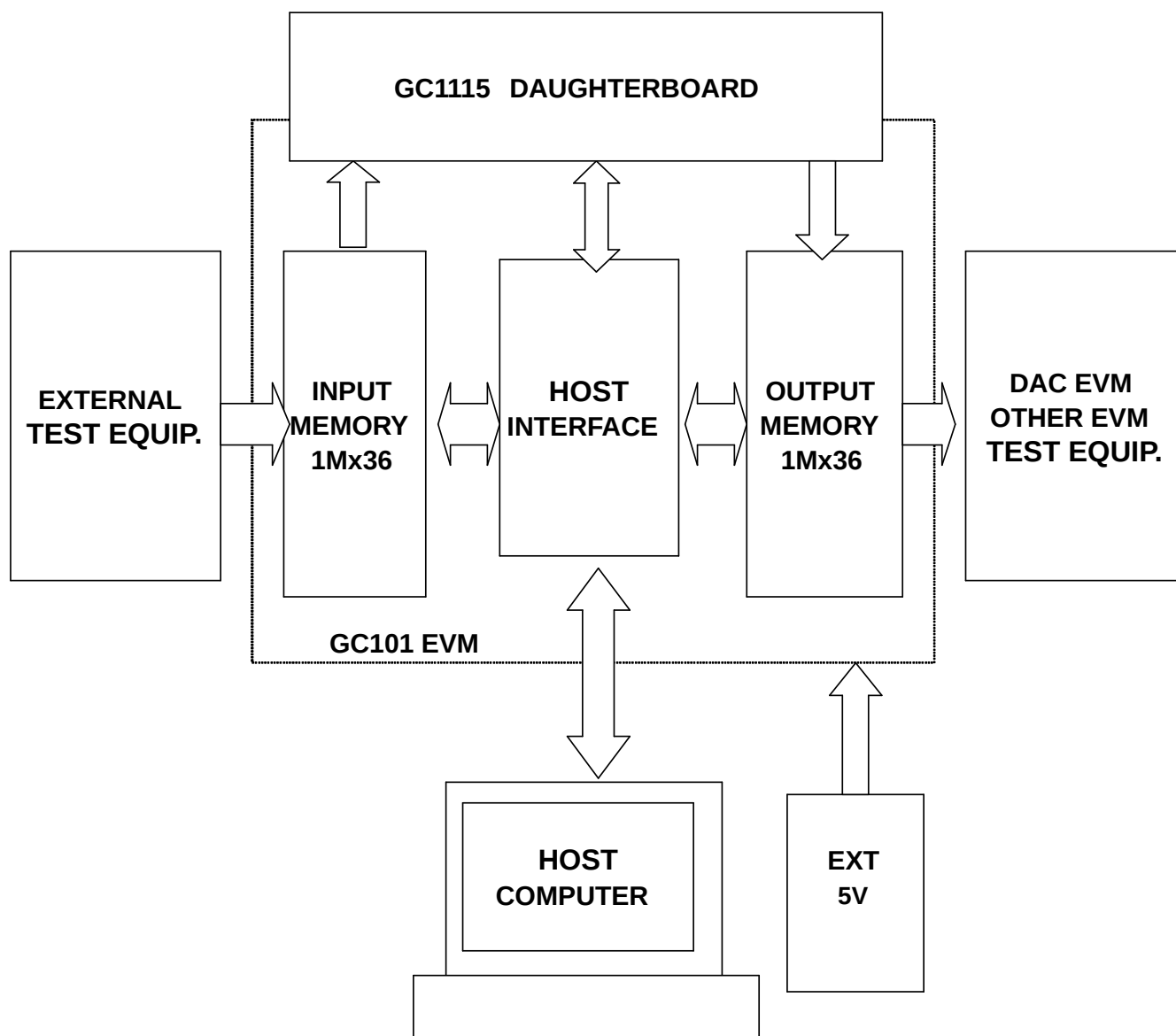


Figure 1-1. GC101 EVM and GC1115 Daughterboard

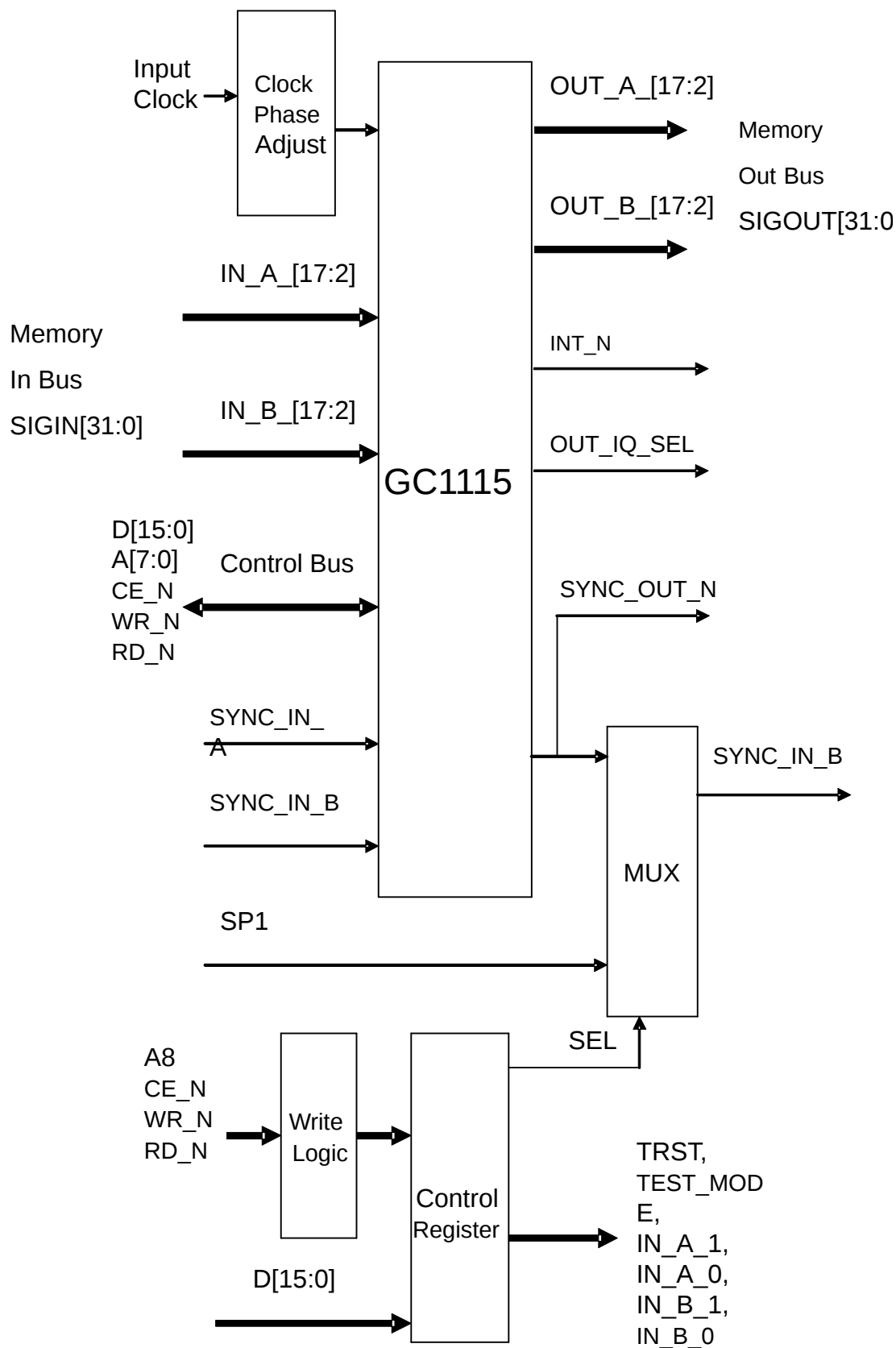


Figure 1-2. GC1115 Daughterboard Block Diagram

1.1 GC1115 Daughterboard to GC101 EVM I/O Description

The GC1115 Daughterboard has a PC-133 form-factor that utilizes the 168-pin DIMM memory connector. The 168 pin interface signals are divided into several groups:

- CLK+: Input Clock for GC1115
- Memory Input Bus: 36 inputs used to stimulate the GC1115 inputs
 - SIGIN[15..0]: Memory Input Bus A
 - SIGIN[31..16]: Memory Input Bus B
 - SYNCIN+: SYNC_A_N Input. Used to synchronize the GC1115
 - SP1: Option for providing a SYNC_B_N signal from GC101
 - SP2-SP4: Unused spare inputs
- Memory Output Bus: 36 outputs from the two GC1115 output busses, sent back to the GC101 EVM for recording and/or output
 - SIGOUT[15..0]: Memory Output Bus A
 - SIGOUT[31..16]: Memory Output Bus B
 - SYNCOUT+: Sync Output. Used to output synchronization signal from GC1115
 - SP5: OUT_IQ_SEL. Used to identify I and Q data during multiplexed I/Q output mode
 - SP6: INT_N. Active low interrupt
 - SP7, SP8: Unused spare outputs
- Control Bus: Bus to program the internal registers
 - 16 Bidirectional data lines
 - 8 Address lines for GC1115
 - 1 Address line for board control register
 - Controls $\overline{CE}$, $\overline{RD}$, $\overline{WR}$, and $\overline{RST}$
- JTAG: 5 pin JTAG Test Port for GC1115
 - $\overline{TRST}$, TCLK, TMS, TDI, TDO
- Power: Input power to Daughterboard
 - VDUT1: 3.3 VDC power from GC101 EVM
 - GND: 3.3 VDC return from GC101 EVM

See the GC101 EVM User's Guide for the 168-pin DIMM connector pin description. The pins used for the GC1115 Daughterboard are shown in the schematic at the end of this document.

1.2 GC1115 Daughterboard Memory Input and Output

The Memory Input Bus and Special Input Bus connect through the GC101 36-bit Memory Input Bus. The Memory Input Bus is mapped to the GC1115 and one bit (SP1) of the Special Input Bus is mapped to an input of a sync multiplexer. The GC101 EVM data input formats are based on input files from the PC-supplied software. The data buses between the boards map as follows:

GC101 DID[15..0] -> maps to GC1115 IN_A[17..2]. Inputs IN_A[1..0] are set by the control register.

GC101 DID[31..16] -> maps to GC1115 IN_B[17..2]. Inputs IN_B[1..0] are set by the control register.

GC101 DID[32] -> SP1.

GC101 D[33-35] -> Unused

The GC1115 data input ports can either be 2's complement or unsigned format.

The Memory Output Bus, and Special Output Bus pins are used to monitor data from the GC1115 Daughterboard.

Memory Output Bus:

GC101 DOD[15..0] -> maps to GC1115 OUT_A[17..2]. OUT_A[1..0] go to test points to allow for measuring signal timing and levels.

GC101 DOD[31..16] -> maps to GC1115 OUT_B[17..2]. OUT_B[1..0] go to test points to allow for measuring signal timing and levels.

The Special Output Bus has several additional signals:

GC1115 SP5 -> maps to GC101 DOD[32] . This is the OUT_IQ_SEL from the GC1115.

GC1115 SP6 -> maps to GC101 DOD[33]. This is the INT_N signal from the GC1115.

GC1115 SP7 and SP8 are not used

1.3 Input Clock

The GC1115 Daughterboard operates with a single-ended CMOS input clock. The clock enters the daughterboard on pin 34, and has pullup and pulldown termination resistors located near U5 (CDCVF25081). U5 is a Phase-Lock Loop Clock Driver, which provides the clock to the GC1115. With the use of delay module U10, the user can adjust the phase of the clock. The board default setup is with this part removed and an output of U5 connected to the feedback input. This provides a zero delay clock source to the GC1115 with respect to the input clock from the GC101. The input clock phase and frequency can also be changed by an adjustable clock skew buffer device on the GC101. See the GC101 EVM User's Guide for more information on this.

1.4 Input Sync

The GC1115 has two input sync pins, SYNC_A_N and SYNC_B_N. The GC1115 Daughterboard routes an input sync from pin 37 to the SYNC_A_N input of the GC1115. This signal has a test point to allow for easy monitoring. The board also contains a sync multiplexer that allows the user to send either the GC1115 output sync (SYNC_OUT_N) or SP1 from the input connector to the SYNC_B_N signal of the GC1115. The sync signals are used to provide a hardware event for the GC1115 internal sync registers. See the data sheet for more information on the operation of these sync signals.

1.5 Output Clock

The GC1115 Daughterboard provides a test point to allow monitoring of the output clock. This signal does not go to the output connector. There are several internal registers that effects the frequency and relationship of the output clock with respect to the core clock. See the data sheet for more information on this.

1.6 Output Sync

The GC1115 Daughterboard routes the output sync signal (OUT_SYNC_N) to both the output connector and a sync multiplexer. The multiplexer output is routed to the SYNC_B_N input of the GC1115. If selected by the control register, this signal can be used to synchronize the GC1115. SYNC_OUT_N trace has a test point to allow for monitoring.

1.7 Output Interrupt

The GC1115 Daughterboard routes an active low interrupt signal (INT_N) to pin 124 of the output connector. This signal is useful when interfacing a GC1115 with a DSP or microprocessor.

1.8 Output I Q Select

The GC1115 Daughterboard routes an I/Q select signal (OUT_IQ_SEL) to pin 124 of the output connector. This signal indicates whether the data present at the output is I (low) or Q (high). This signal is only active in multiplexed I/Q output modes.

1.9 Control Bus

The GC1115 has a 16-bit data Microprocessor port. The $\overline{CE}$, $\overline{RD}$, $\overline{WR}$, and $\overline{RST}$ control signals are active low and map directly from the GC101 EVM. The Address Bus A[8..0] is static when the control signals are asserted.

The Bidirectional Control Data D[15..0] provides the data path between the GC101 EVM and the GC1115 Daughterboard.

The $\overline{CE}$, $\overline{RD}$, $\overline{WR}$, and $\overline{RST}$ signals have test points for monitoring.

1.10 JTAG Bus

The GC1115 JTAG Bus is connected through the GC101 EVM connector. The serial chain resistors are on the GC101 EVM. The JTAG is not currently used.

1.11 Power Supplies

The 3.3-V input power is supplied from the GC101 EVM power supplies. The 1.2-V core and 1.2V PLL power for the GC1115 are supplied from regulators on the daughterboard. The board provides options to provide these two sources from two separate regulators, combined from one regulator, or from external sources. On-board jumpers allow the user to bypass the regulators and use an external power source, if desired. The function of the power supply jumpers are as follows:

Table 1-1. Power Supply Jumper List

JUMPER	FUNCTION	PINS 1-2	PINS 2-3	PINS 2-4	DEFAULT
W1	Selects regulator or external power for core supply	External power provided from connector J2	Power provided from regulator U8	N/A	2-3
W2	Selects regulator or external power for PLL supply	Power provided from regulator U9	External power provided from connector J3	Power provided from core supply	1-2
W3	Regulator enable	Disables both regulators	Enables both regulators	N/A	2-3

GC1115 Daughterboard Operational Procedure

This chapter describes the operation of the GC1115 Daughterboard with the GC101 EVM. The following sections are overviews of the hardware specifications for the GC101 EVM and GC1115 Daughterboard. For more information, the user is encouraged to read the GC101 User's Guide, and the GC Studio documentation, which is included with this software package.

2.1 GC101 EVM Hardware Features

The GC101 EVM provides the following features:

- A complete digital data path which allows the loading, processing, and analysis of a stream of digital data. The loading and analysis is performed through 1Meg Input and Output memory banks.
- Signal processing is performed through a 168-pin expansion slot which is designed to accommodate the GC1115 Daughterboard.
- Digitally controlled internal clocks and output clocks capable of synchronizing the daughterboard, the EVM capture memories, and external test and measurement equipment.
- The EVM communicates to input memory, output memory, and the GC1115 Daughterboard over an IEEE 1284 EPP or ECP parallel port. The GC1115 internal registers are programmed through this interface.

2.2 Hardware Requirements

Required Elements before Installation:

- GC101 EVM, external 5V power supply, high-speed parallel port cable, and GC1115 Software CDROM.
- GC1115 Daughterboard
- Computer with:
 - Administrator privileges
 - Supported OS of Win98 Rel.2, WinME, Win2000 SP1, WinXP, or WinXP Prof.
 - Parallel port operating in ECP for LPT1 (BIOS)

2.3 EVM Setup

2.3.1 Deliverables List

The following items should be delivered and comprise the GC1115SEK:

- GC101 Motherboard
- GC101 Motherboard power cable and power supply
- High performance parallel port cable
- GC1115 Daughtercard
- A current copy of the GC Studio application, including the GC1115 plug-in
- A current copy of the GC Scripser application, for advanced setup and use

2.3.2 Installation Instructions

The software should be installed before connecting the boards to the computer. GCStudio_Setup.exe should have been provided either through the web, or on a CD with this package. Double-click on the icon for the GCStudio_Setup.exe program. This will launch an installshield wizard. See the GC Studio Documentation for instructions on how to operate the GC1115 with a GC101 EVM.

Physical Description

This chapter describes the physical characteristics and PCB layout of the EVM and lists the components used on the module.

3.1 PCB Layout

The EVM is constructed on a 8-layer, 3.3-inch x 5.25-inch, 0.056-inch thick PCB using FR-4 material. [Figure 3-1](#) through [Figure 3-6](#) show the PCB layout for the EVM.

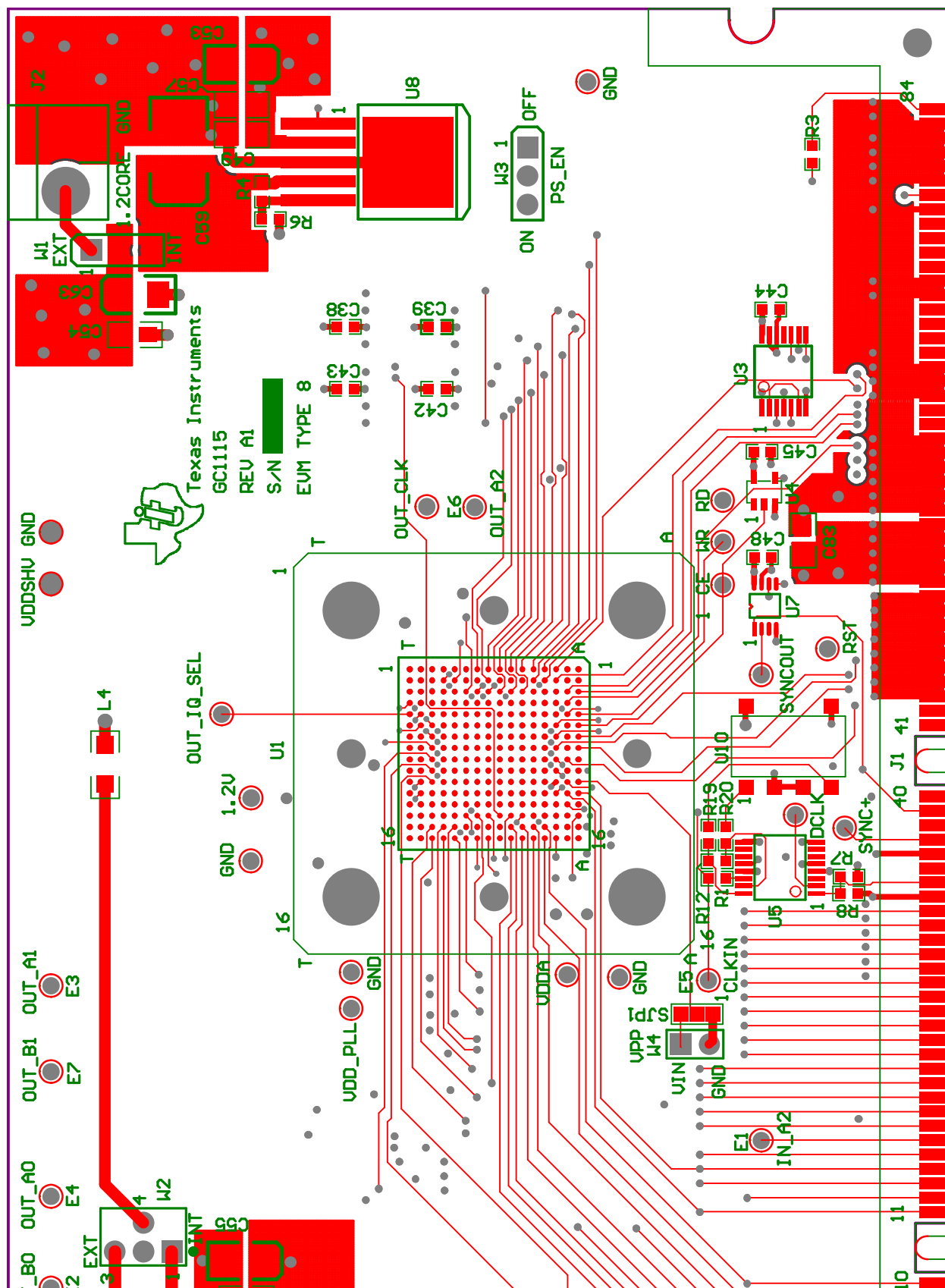


Figure 3-1. Top Layer 1

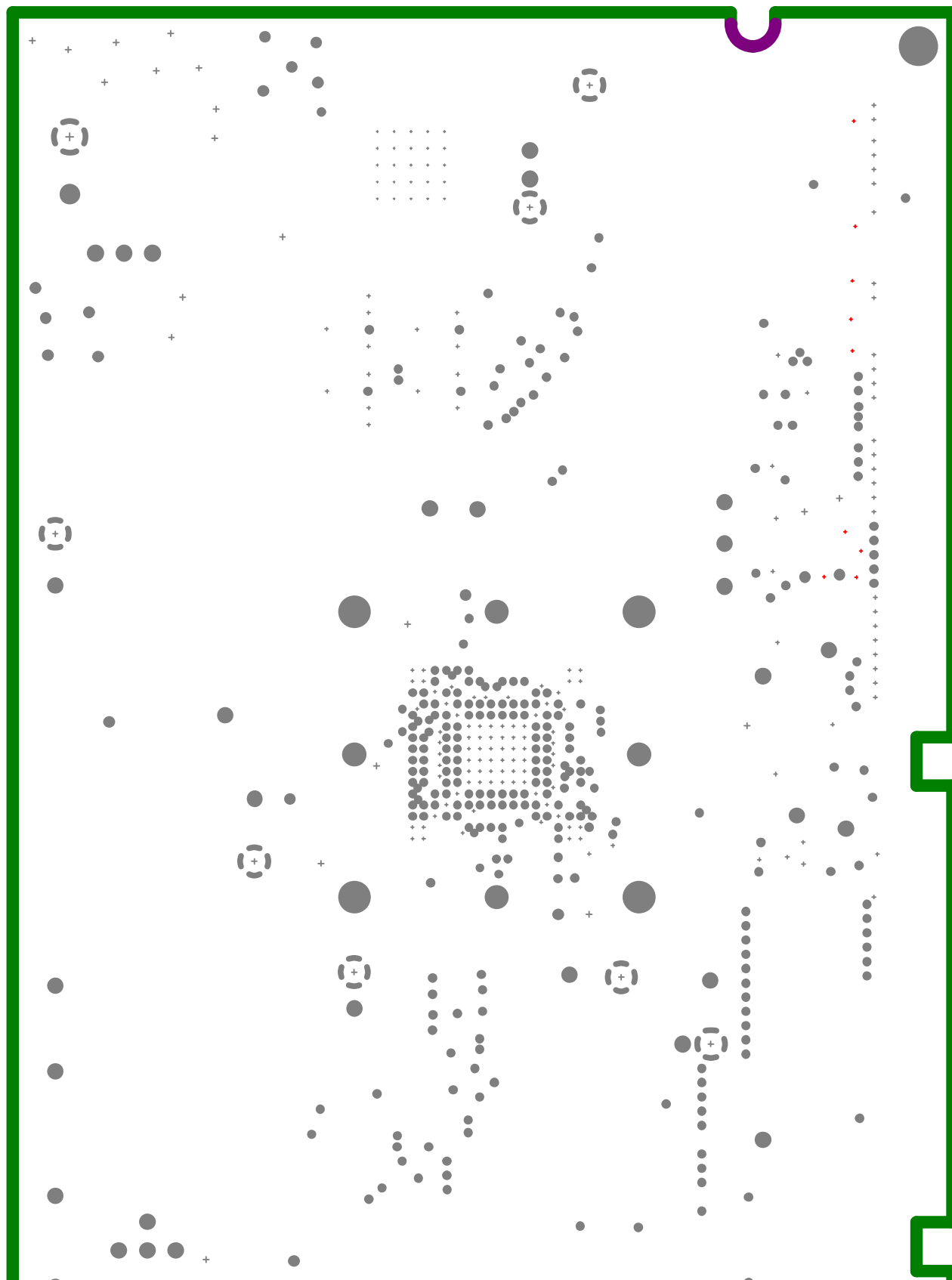


Figure 3-2. Ground Plane Layer 2

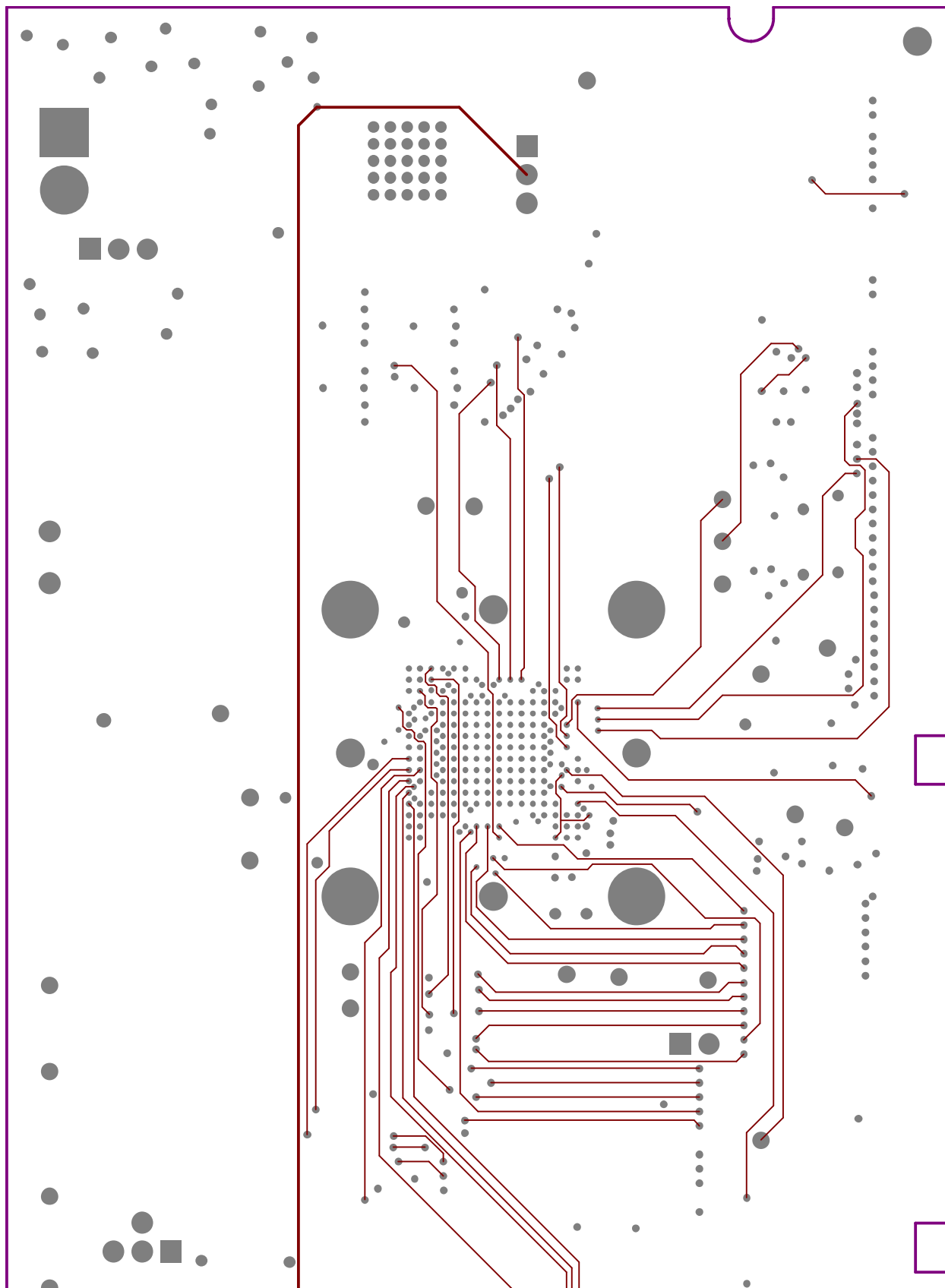


Figure 3-3. Signal Layer 3

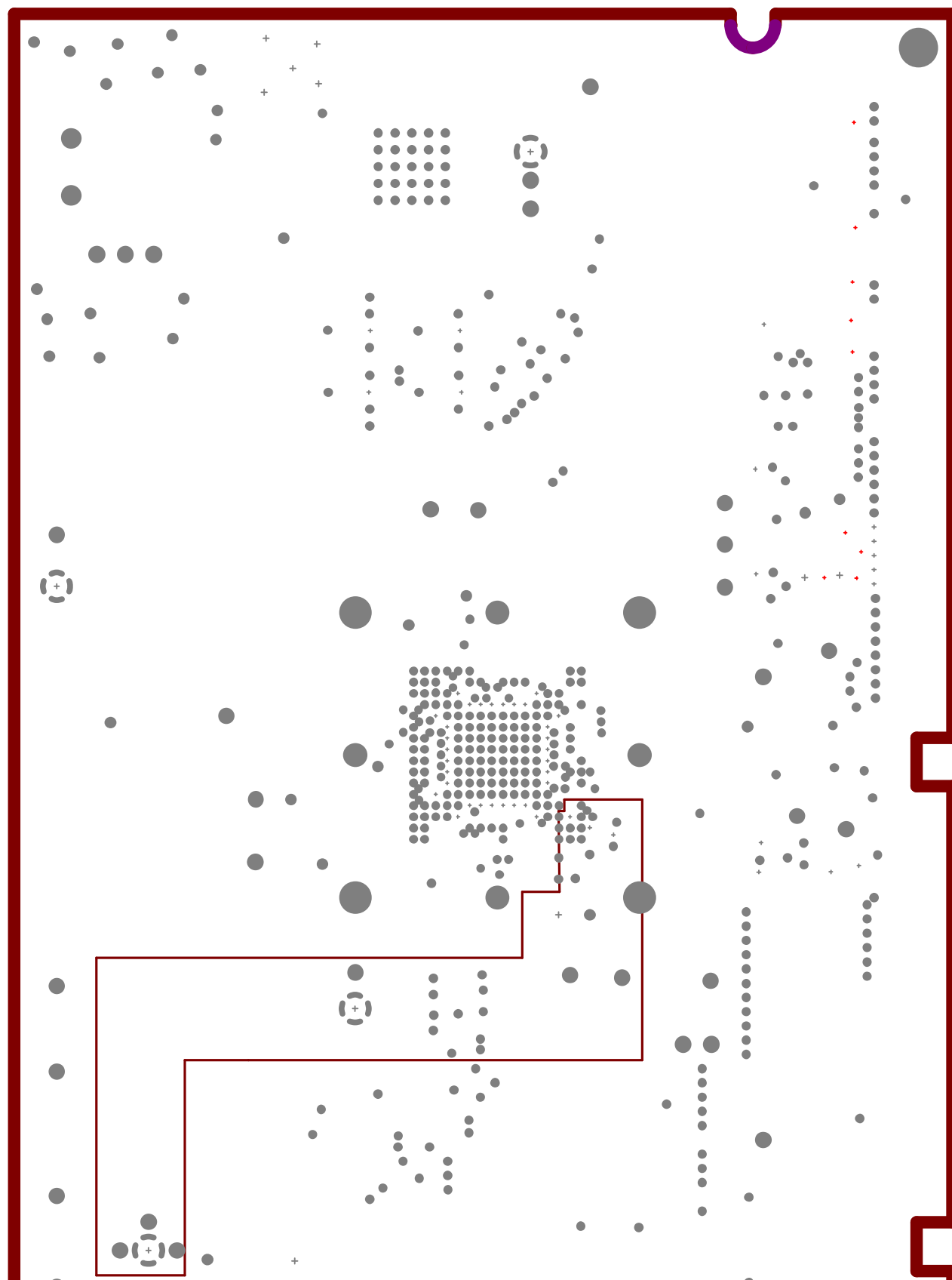


Figure 3-4. Signal Layer 4

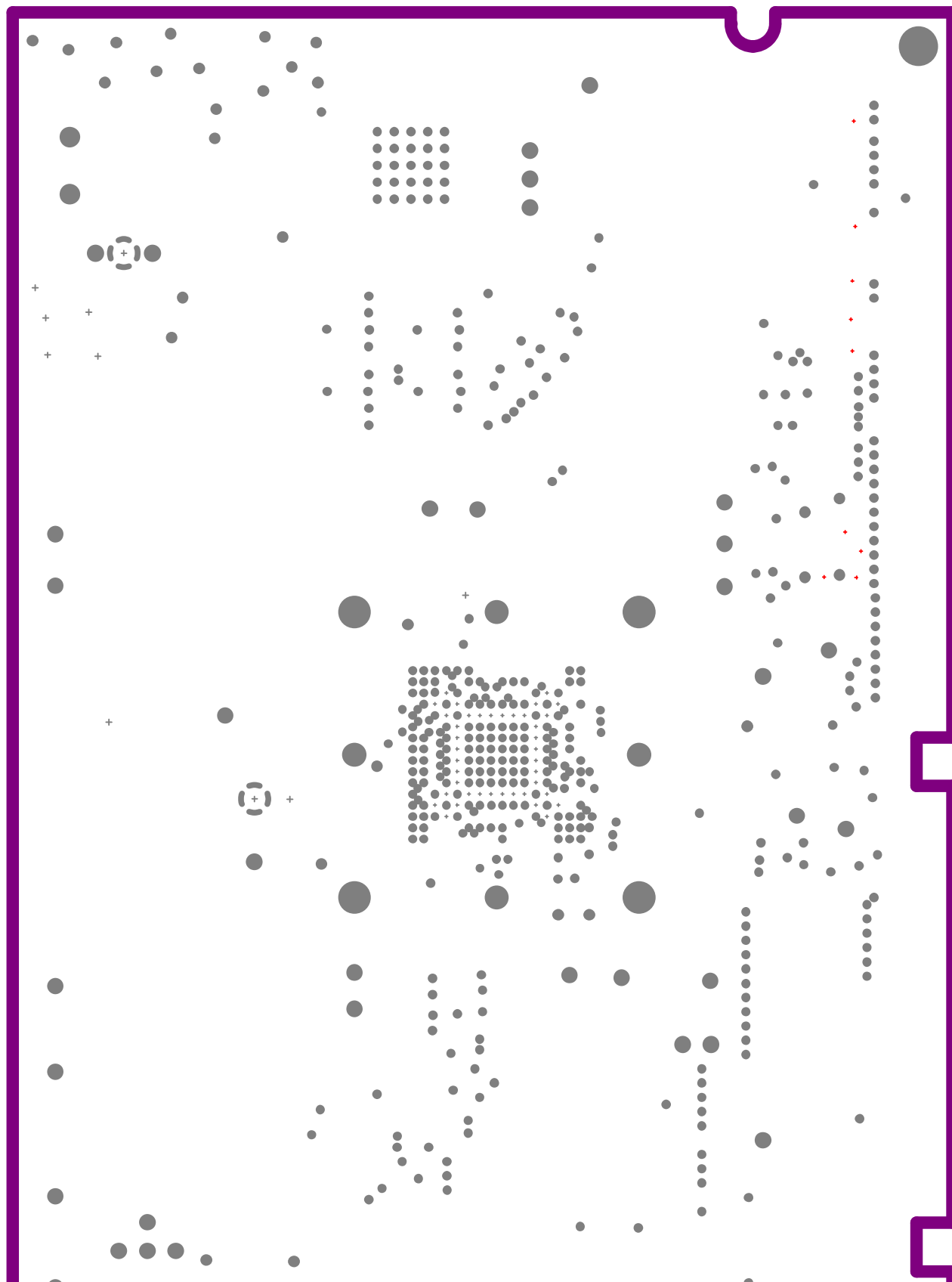


Figure 3-5. Power Plane Layer 5

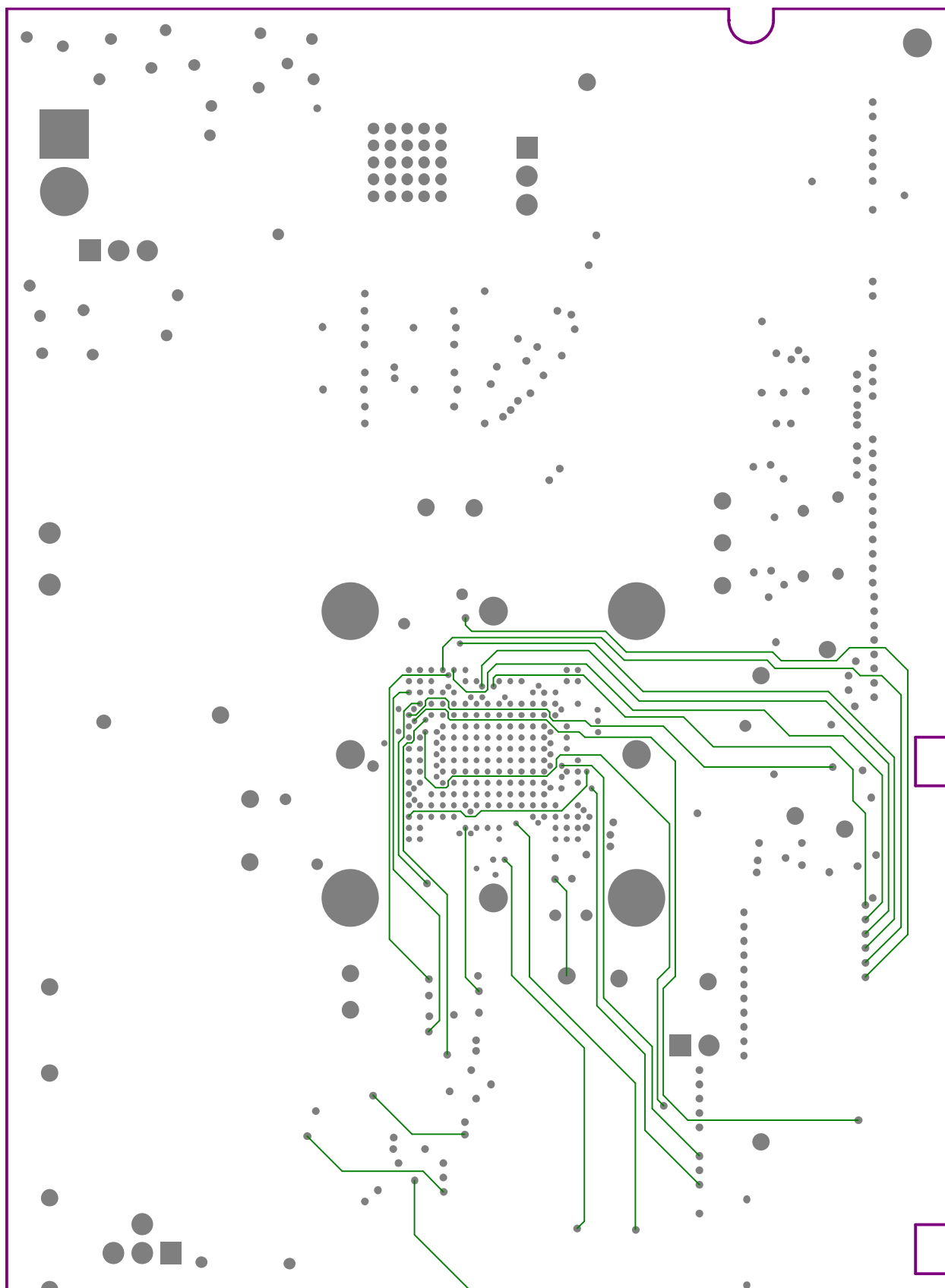


Figure 3-6. Layer 6

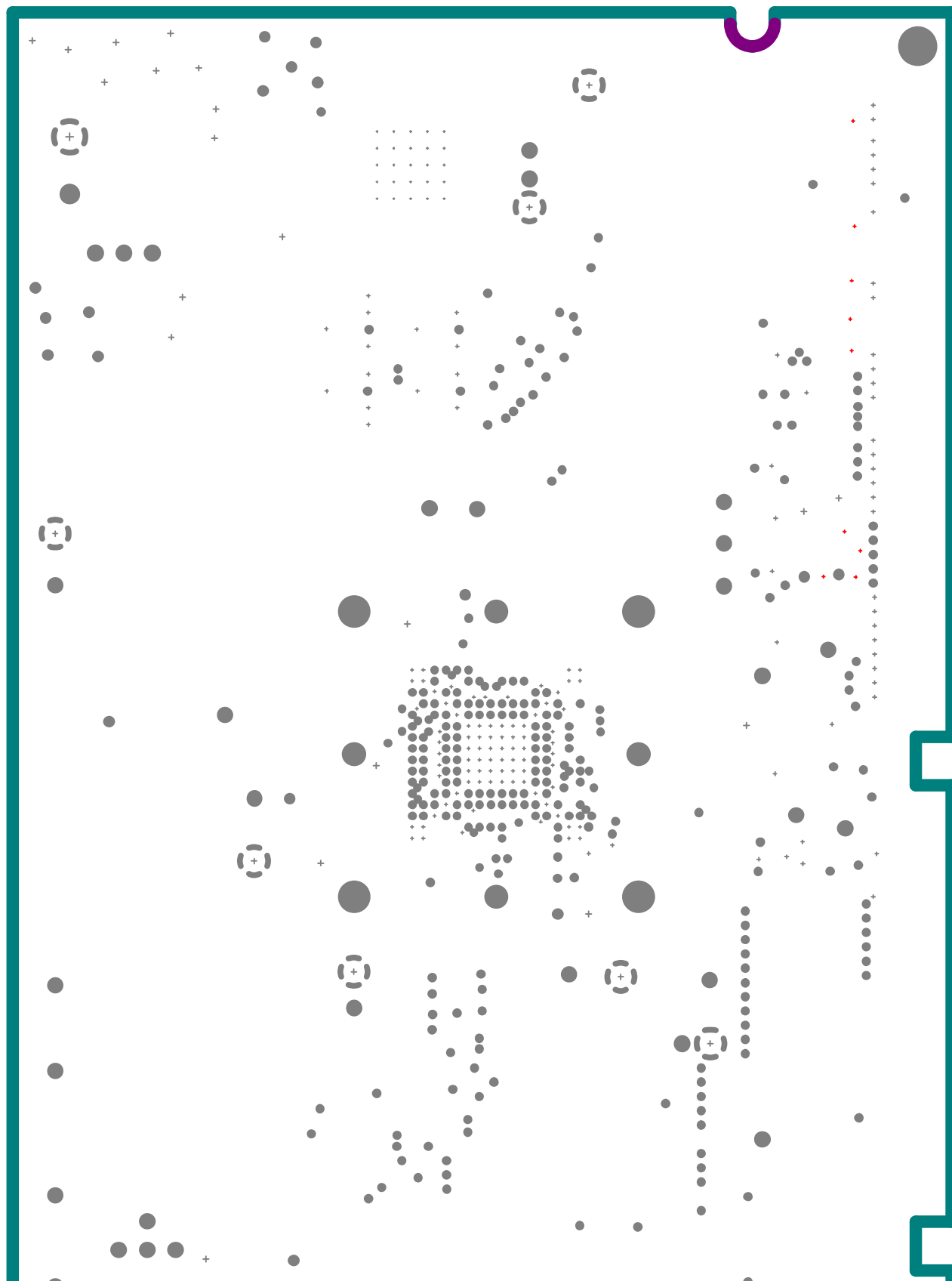


Figure 3-7. Layer 7

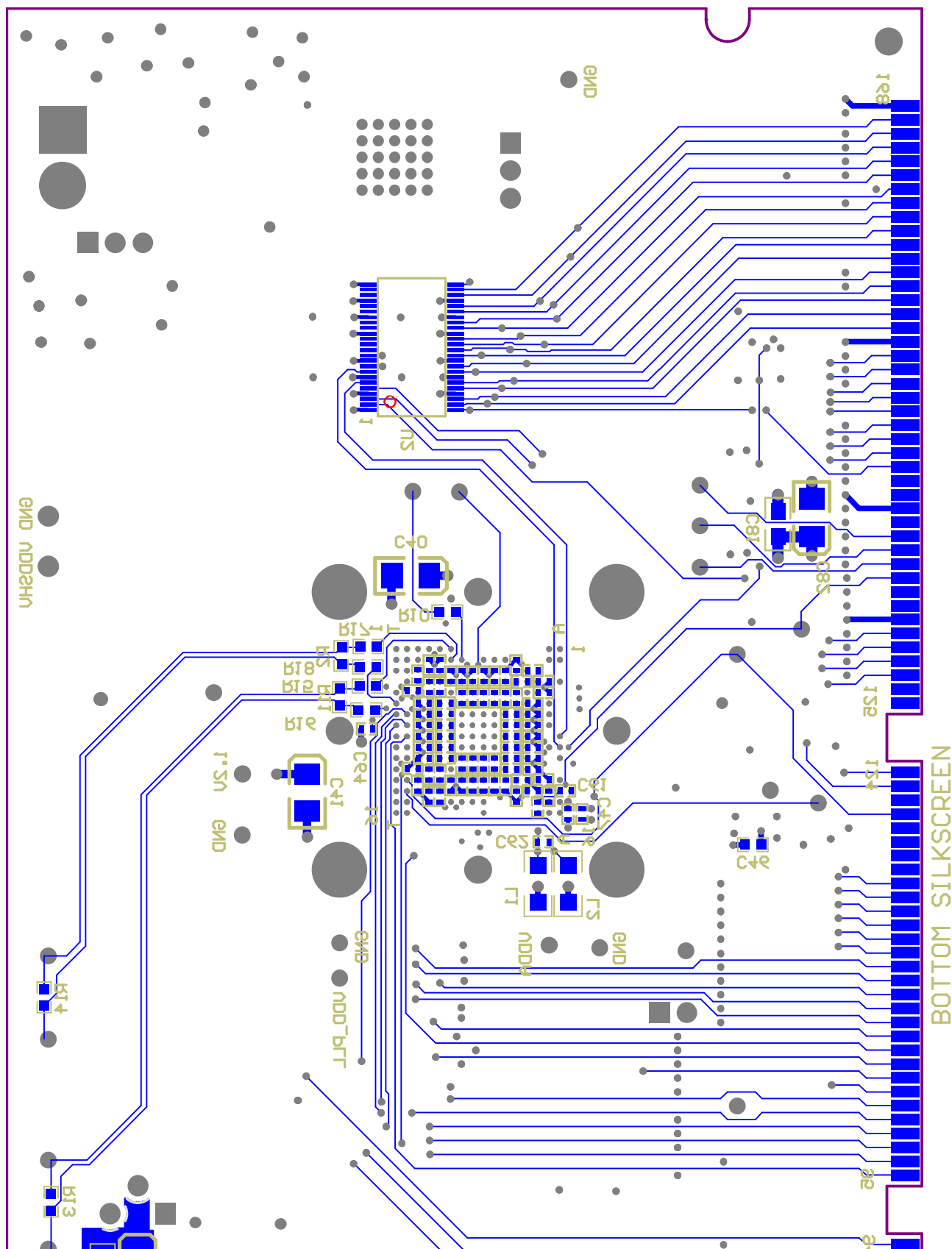


Figure 3-8. Bottom Layer 8

3.2 Parts List

Table 3-1 lists the parts used in constructing the EVM.

Table 3-1. Bill of Materials for GC1115 EVM

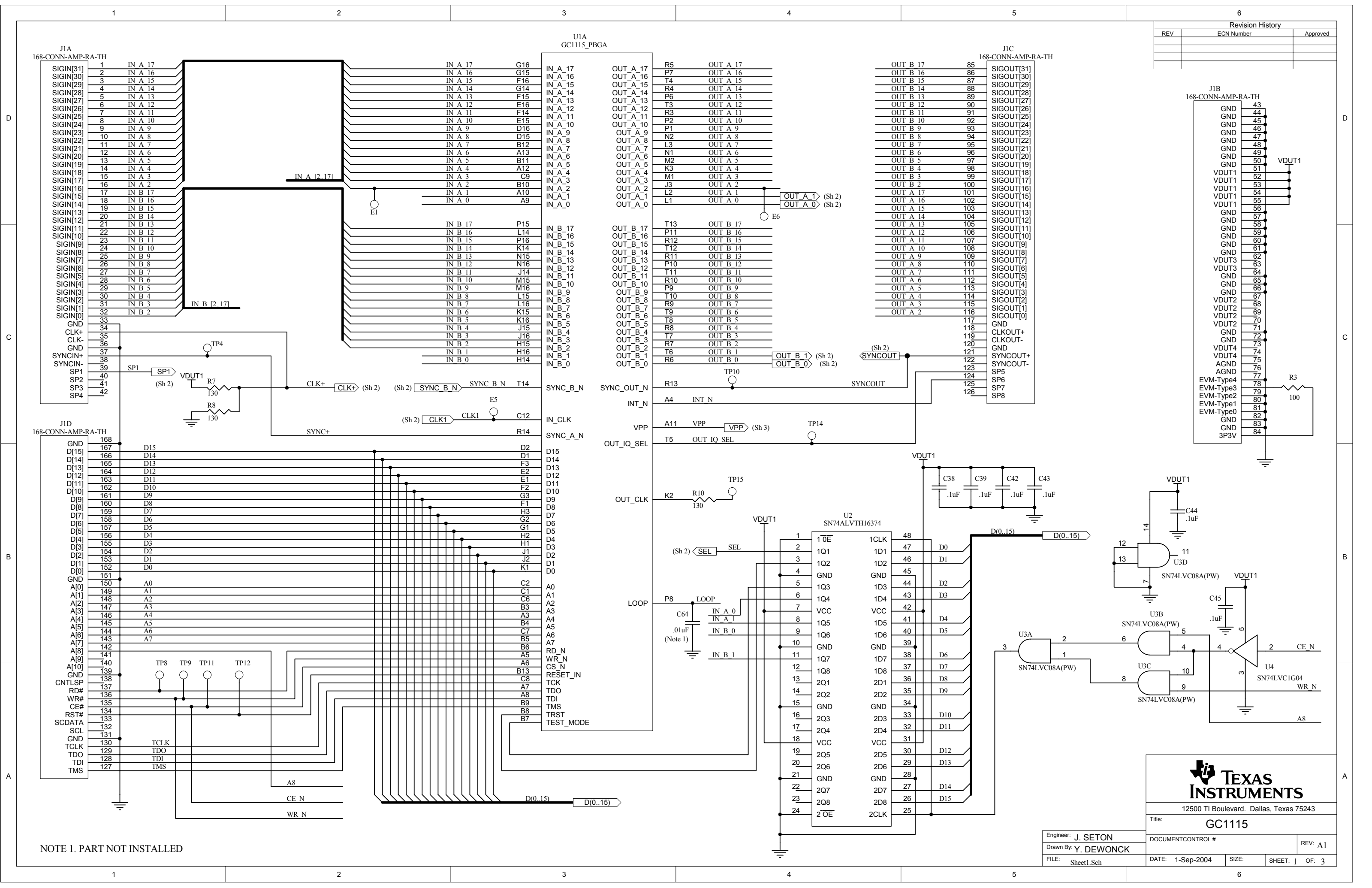
VALUE	QTY	PART NUMBER	MANUFACTURER	REF DES	NOT INSTALLED
CAPACITORS					
47uF, 20V, 10%, Capacitor	2	ECS-T1AD476R	PANASONIC	C59 C60	
2.2 uF, 20 V, 10%, Capacitor	1	ECS-T1DX225R	PANASONIC	C40	
10 uF, 20 V, 10%, Capacitor	6	ECS-T1DX106R	PANASONIC	C41 C53 C55 C56 C63 C82	
1uF, 16V, 10%, Capacitor	3		PANASONIC	C57 C58 C83	
0.1 uF, 16 V, 10%, Capacitor	5	ECJ-2VB1C104K	PANASONIC	C49 C51 C52 C54 C81	
0.1 uF, 16 V, 10%, Capacitor	8	ECJ-1VB1C104K	PANASONIC	C38 C39 C42-C46 C48	
0.01 uF, 16 V, 10%, Capacitor	2	ECJ-0EF1C103Z	PANASONIC	C61 C99	C64
0.1 uF, 16 V, 10%, Capacitor	70	ECJ-0EF1C104Z	PANASONIC	C1-C37 C47 C50 C65-C80 C84-C98	
47pF,50V,+/- 5%, Capacitor	0	ECJ-OEC1H470J	PANASONIC		C61 C100
RESISTORS					
100 Ω resistor, 1/16 W, 1%	3	ERJ-3EKF1000V	PANASONIC	R3 R13 R14	
130 Ω resistor, 1/16 W, 1%	3	ERJ-3EKF1300V	PANASONIC	R7 R8 R10	
140 Ω resistor, 1/16 W, 1%	2	ERJ-3EKF1400V	PANASONIC	R2 R11	
165 Ω resistor, 1/16 W, 1%	4	ERJ-3EKF1650V	PANASONIC	R15 R16 R17 R18	
0 Ω Resistor, 1/16 W, 1%	3	ERJ-3GEY0R00V	PANASONIC	R4 R5 R12	R19 R20
30.1 kΩ Resistor, 1/16 W, 1%	0	ERJ-3EKF3012V	PANASONIC		R6 R9
22.1 Ω resistor, 1/16 W, 1%	1	ERJ-3EKF22R1V	PANASONIC	R1	
CONNECTORS, HEADERS, FERRITE BEADS and TEST POINTS					
Red test point	13	5000k	KEYSTONE	TP4 TP5 TP7-TP16 TP18	
Black test point	6	5001k	KEYSTONE	TP1 TP2 TP3 TP6 TP17 TP19	
TESTPOINT	0				E1-E7
3POS-JUMPER SURFACE MOUNT	1			SJP1	
CON_2TERM_SCREW	2	KRMZ3	LUMBERG	J2 J3	
2POS-HEADER	1	TWS-150-07-L-S	SAMTEC	W4	
3POS-HEADER	2	TWS-150-07-L-S	SAMTEC	W1 W3	
4POS-HEADER	1		SAMTEC	W2	
FERRITE BEADS	3	EXC-ML32A680U		L1 L2 L4	
ICs					
GC1115_PBGA	1	GC1115IZDJ	Texas Instruments	U1	

Table 3-1. Bill of Materials for GC1115 EVM (continued)

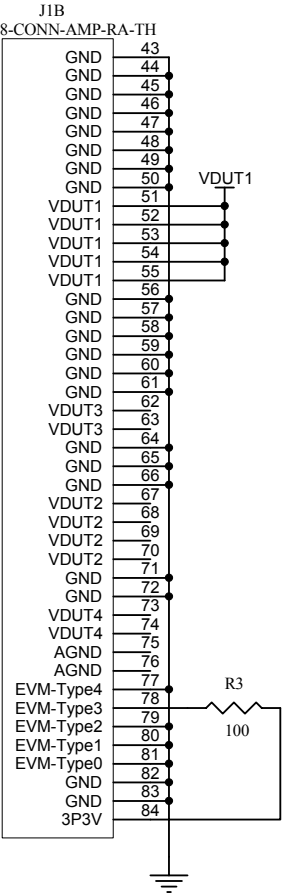
VALUE	QTY	PART NUMBER	MANUFACTURER	REF DES	NOT INSTALLED
SN74LVC08APWR	1	SN74LVC08APWR	Texas Instruments	U3	
SN74ALVTH16374	1	SN74ALVTH16374GR	Texas Instruments	U2	
SN74LVC2G157	1	SN74LVC2G157DCTR	Texas Instruments	U7	
SN74LVC1G04	1	SN74LVC1G04DBVR	Texas Instruments	U4	
TPS75701	2	TPS75701KTTT	Texas Instruments	U8 U9	
DELAY LINE	0	CDA1005	ELMEC		U10
CDCVF25081	1	CDCVF25081PW	Texas Instruments	U5	

3.3 Schematics

This chapters contains the schematics for the EVM.



Revision History		
REV	ECN Number	Approved



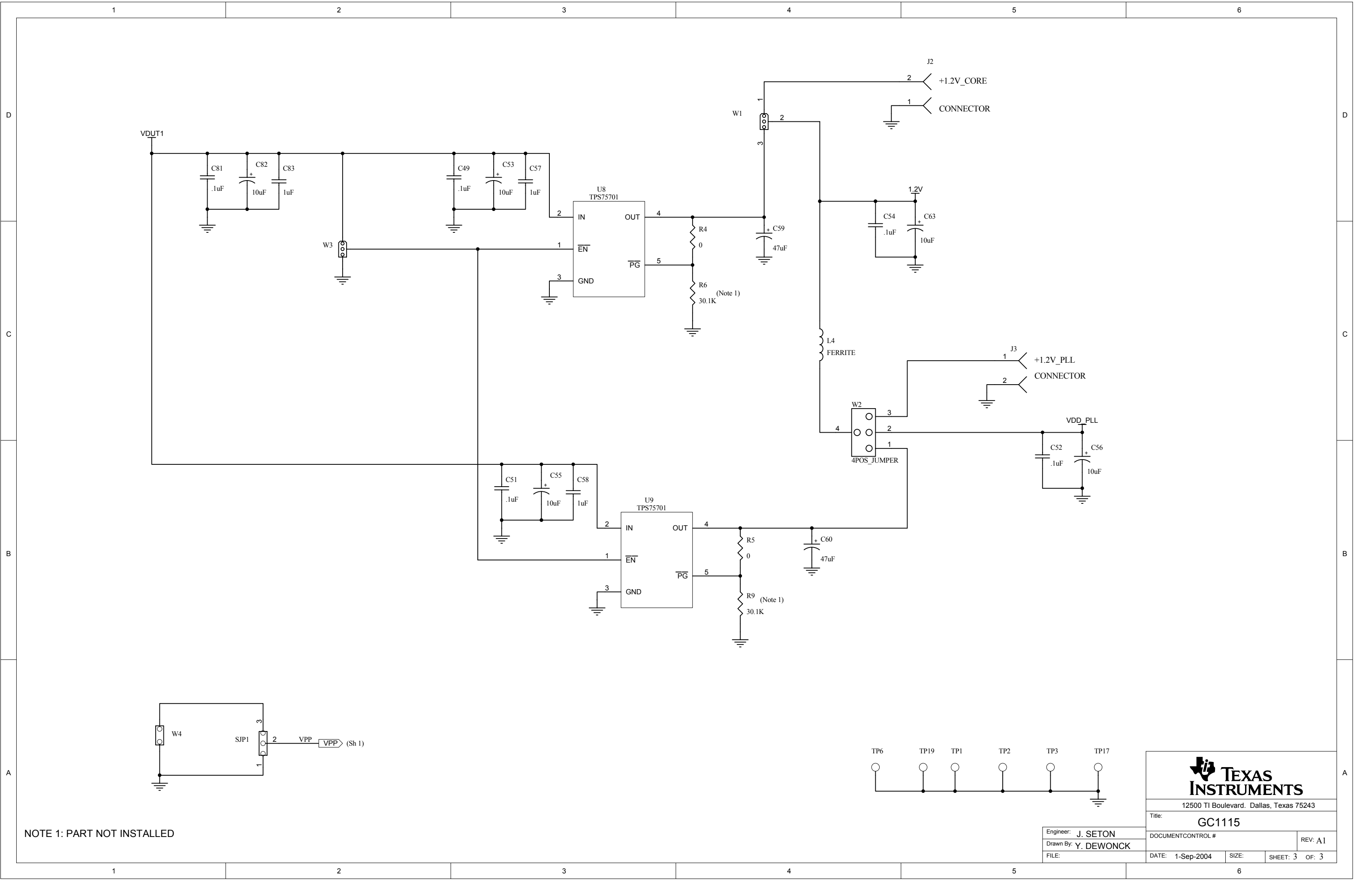
**TEXAS
INSTRUMENTS**

12500 TI Boulevard, Dallas, Texas 75243

Title: **GC1115**

Engineer: J. SETON	DOCUMENT CONTROL #	REV: A1
Drawn By: Y. DEWONCK	DATE: 1-Sep-2004	SIZE:
FILE: Sheet1.Sch	SHEET: 1	OF: 3

NOTE 1. PART NOT INSTALLED



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Title:		GC1115	
DOCUMENT CONTROL #		REV: A1	
DATE:	1-Sep-2004	SIZE:	SHEET: 3 OF: 3

Engineer:	J. SETON
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FILE:	

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