ORCA™ OR3LxxxB Series Device Datasheet

June 2010

All Devices Discontinued!

Product Change Notifications (PCNs) have been issued to discontinue all devices in this data sheet.

The original datasheet pages have not been modified and do not reflect those changes. Please refer to the table below for reference PCN and current product status.

Product Line	Ordering Part Number	Product Status	Reference PCN
OR3L165B	OR3L165B8PS208-DB	**Discontinued**	PCN#06-07
	OR3L165B7PS208-DB		
	OR3L165B7PS208I-DB		
	OR3L165B8PS240-DB		
	OR3L165B7PS240-DB		
	OR3L165B7PS240I-DB		
	OR3L165B8BA352-DB		PCN#09-10
	OR3L165B7BA352-DB		
	OR3L165B7BA352I-DB		
	OR3L165B8BC432-DB		
	OR3L165B7BC432-DB		
	OR3L165B7BC432I-DB		
	OR3L165B8BM680-DB		
	OR3L165B7BM680-DB		
	OR3L165B7BM680I-DB		
OR3L225B	OR3L225B8BC432-DB	**Discontinued**	PCN#06-07
	OR3L225B7BC432-DB		
	OR3L225B7BC432I-DB		
	OR3L225B8BM680-DB		
	OR3L225B7BM680-DB		
	OR3L225B7BM680I-DB		

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Data Addendum
March 2002

ORCA® OR3LxxxB Series Field-Programmable Gate Arrays

Introduction

This data addendum refers to the information found in the *ORCA*® *Series 3C and 3T Field-Programmable Gate Arrays* Data Sheet.

Features

- High-performance, cost-effective, 0.25 µm 5-level metal technology.
- 2.5 V internal supply voltage and 3.3 V I/O supply voltage for speed and compatibility.
- Up to 340,000 usable gates‡ in 0.25 µm.
- Up to 612 user I/Os in 0.25 µm. (OR3LxxxB I/Os are 5 V tolerant to allow interconnection to both 3.3 V and 5 V devices, selectable on a per-pin basis, when using 3.3 V I/O supply.)
- Twin-quad programmable function unit (PFU) architecture with eight 16-bit look-up tables (LUTs) per PFU, organized in two nibbles for use in nibble- or byte-wide functions. Allows for mixed arithmetic and logic functions in a single PFU.
- Nine user registers per PFU, one following each LUT, plus one extra. All have programmable clock enable and local set/reset, plus a global set/reset that can be disabled per PFU.
- Flexible input structure (FINS) of the PFUs provides a routability enhancement for LUTs with shared inputs and the logic flexibility of LUTs with independent inputs.
- Fast-carry logic and routing to adjacent PFUs for nibble-wide, byte-wide, or longer arithmetic functions, with the option to register the PFU carry-out.
- Softwired LUTs (SWL) allow fast cascading of up to three levels of LUT logic in a single PFU.
- Supplemental logic and interconnect cell (SLIC) provides 3-statable buffers, up to 10-bit decoder, and *PAL**-like AND-OR-INVERT (AOI) in each programmable logic cell (PLC).
- Abundant hierarchical routing resources based on routing two data nibbles and two control lines per set provide for faster place and route implementations and less routing delay.
- Individually programmable drive capability: 12 mA sink/6 mA source or 6 mA sink/3 mA source.
- Built-in boundary scan (*IEEE*† 1149.1 JTAG) and testability function to 3-state all I/O pins.
- Enhanced system clock routing for low-skew, high-speed clocks originating on-chip or at any I/O.
- Up to four ExpressCLK inputs allow extremely fast clocking of signals on- and off-chip plus access to internal general clock routing.
- StopCLK feature to glitchlessly stop/start the ExpressCLKs independently by user command.

* *PAL* is a trademark of Lattice Semiconductor
† *IEEE* is a registered trademark of The Institute of Electrical and Electronics Engineers, Inc.

Table 1. *ORCA* OR3LxxxB Series FPGAs

Device	System Gates‡	LUTs	Registers	Max User RAM	User I/Os	Array Size	Process Technology
OR3L165B	120K—244K	8192	10752	131K	516	32 × 32	0.25 µm/5 LM
OR3L225B	166K—340K	11552	14820	185K	612	38 × 38	0.25 µm/5 LM

‡ The usable gate counts range from a logic-only gate count to a gate count assuming 30% of the PFUs/SLICs being used as RAMs. The logic-only gate count includes each PFU/SLIC (counted as 108 gates/PFU), including 12 gates per LUT/FF pair (eight per PFU), and 12 gates per SLIC/FF pair (one per PFU). Each of the four PIOs per PIC is counted as 16 gates (three FFs, fast-capture latch, output logic, CLK, and I/O buffers). PFUs used as RAM are counted at four gates per bit, with each PFU capable of implementing a 32 × 4 RAM (or 512 gates) per PFU.

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Features (continued)

- Programmable I/O (PIO) has:
  - — Fast-capture input latch and input flip-flop (FF)/ latch for reduced input setup time and zero hold time.
  - — Capability to (de)multiplex I/O signals.
  - — Fast access to SLIC for decodes and *PAL*-like functions.
  - — Output FF and two-signal function generator to reduce CLK to output propagation delay.
  - — Fast open-drain drive capability.
- New programmable I/O 3-state FF allows 3-state buffer control signals to be set up a clock cycle early for improved clock to output delays.

System-Level Features

System-level features reduce glue logic requirements and make a system on a chip possible. These features in the *ORCA* OR3LxxxB include the following:

- Full PCI local bus compliance for all devices in 3.3 V and 5 V PCI systems. Pin-selectable I/O clamping diodes provide 3.3 V and 5 V compliance and 5 V tolerance.
- Dual-use microprocessor interface (MPI) can be used for configuration, readback, device control, and device status, as well as for a general-purpose interface to the FPGA. Glueless interface to *i960** and *PowerPC*† processors with user-configurable address space provided.
- Parallel readback of configuration data capability with the built-in microprocessor interface.
- Programmable clock manager (PCM) adjusts clock phase and duty cycle for input clock rates from 5 MHz to 120 MHz. The PCM may be combined with FPGA logic to create complex functions, such as digital phase-locked loops (DPLL), frequency counters, and frequency synthesizers. Two PCMs are provided per device.
- True internal 3-state, bidirectional buses with simple control provided by the SLIC.
- 32 × 4 RAM per PFU, configurable as single- or dual-port. Create large, fast RAM/ROM blocks (128 × 8 in only eight PFUs) using the SLIC decoders as bank drivers.
- Full UTOPIA Level III I/O compliance (6.0 ns CLK -> OUT, 2.0 ns setup with 0 ns hold).

* *i960* is a registered trademark of Intel Corporation.
† *PowerPC* is a registered trademark of International Business Machines, Inc.

Table 2. *ORCA* Series 3L System Performance

Parameter	# PFUs	-7	-8	Unit
16-bit Loadable Up/Down Counter	2	151	176	MHz
16-bit Accumulator	2	151	176	MHz
8 × 8 Parallel Multiplier:				
Multiplier Mode, Unpipelined[1]	11.5	38	46	MHz
ROM Mode, Unpipelined[2]	8	93	116	MHz
Multiplier Mode, Pipelined[3]	15	129	152	MHz
32 × 16 RAM (synchronous):				
Single-port, 3-state Bus[4]	4	173	209	MHz
Dual-port[5]	4	231	277	MHz
128 × 8 RAM (synchronous):				
Single-port, 3-state Bus[4]	8	151	181	MHz
Dual-port[5]	8	151	181	MHz
8-bit Address Decode (internal):				
Using Softwired LUTs	0.25	2.30	2.00	ns
Using SLICs[6]	0	1.29	1.12	ns
32-bit Address Decode (internal):				
Using Softwired LUTs	2	7.97	6.84	ns
Using SLICs[7]	0	3.75	3.16	ns
36-bit Parity Check (internal)	2	7.97	6.84	ns

1. Implemented using 8 × 1 multiplier mode (unpipelined), register-to-register, two 8-bit inputs, one 16-bit output.
2. Implemented using two 32 × 12 ROMs and one 12-bit adder, one 8-bit input, one fixed operand, one 16-bit output.
3. Implemented using 8 × 1 multiplier mode (fully pipelined), two 8-bit inputs, one 16-bit output (seven of 15 PFUs contain only pipelining registers).
4. Implemented using 32 × 4 RAM mode with read data on 3-state buffer to bidirectional read/write bus.
5. Implemented using 32 × 4 dual-port RAM mode.
6. Implemented in one partially occupied SLIC with decoded output set up to CE in same PLC.
7. Implemented in five partially occupied SLICs.

Support

- *ORCA* Foundry development system support.
- Supported by industry-standard CAE tools for design entry, synthesis, simulation, and timing analysis.

Description

FPGA Overview

The *ORCA* OR3LxxxB FPGAs are a new generation of SRAM-based FPGAs built on the successful Series 2 and Series 3 FPGA lines, with enhancements and innovations geared toward today's high-speed designs and tomorrow's systems on a single chip. Designed from the start to be synthesis friendly and to reduce place and route times while maintaining the complete routability of the *ORCA* Series 2 devices, the OR3LxxxB Series more than doubles the logic available in each logic block and incorporates system-level features that can further reduce logic requirements and increase system speed. *ORCA* OR3LxxxB devices contain many new patented enhancements and are offered in a variety of packages, speed grades, and temperature ranges.

The *ORCA* OR3LxxxB Series FPGAs consist of three basic elements: PLCs, programmable input/output cells (PICs), and system-level features. An array of PLCs is surrounded by PICs. Each PLC contains a PFU, a SLIC, local routing resources, and configuration RAM. Most of the FPGA logic is performed in the PFU (see Figure 1), but decoders, *PAL*-like functions, and 3-state buffering can be performed in the SLIC (see Figure 2). The PICs provide device inputs and outputs and can be used to register signals and to perform input demultiplexing, output multiplexing, and other functions on two output signals (see Figure 3). Some of the system-level functions include the MPI and the PCM.

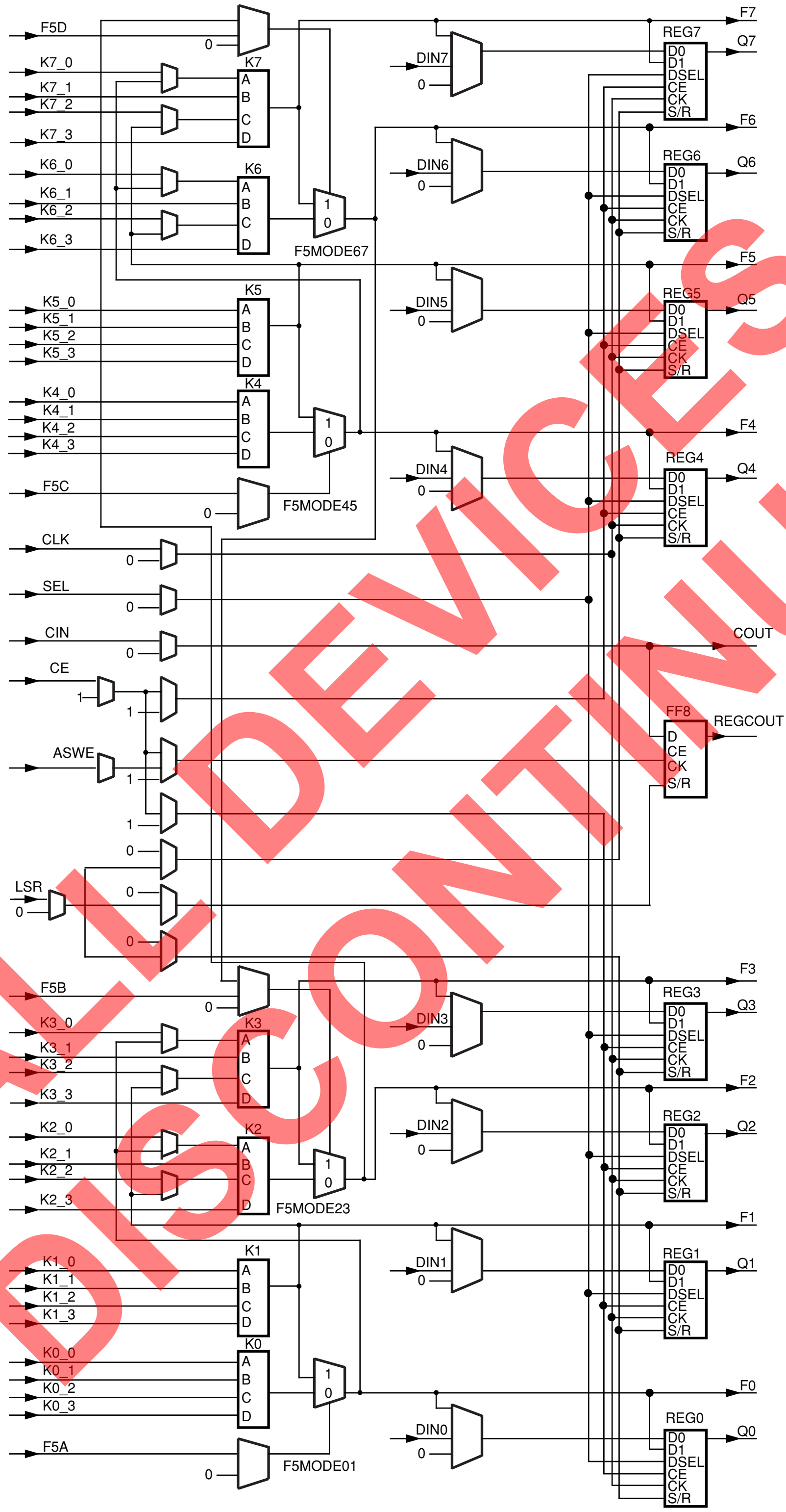
PLC Logic

Each PFU within a PLC contains eight 4-input (16-bit) LUTs, eight latches/FFs, and one additional FF that may be used independently or with arithmetic functions.

The PFU is organized in a twin-quad fashion: two sets of four LUTs and FFs that can be controlled independently. LUTs may also be combined for use in arithmetic functions using fast-carry chain logic in either 4-bit or 8-bit modes. The carry-out of either mode may be registered in the ninth FF for pipelining. Each PFU may also be configured as a synchronous 32 × 4 single- or dual-port RAM or ROM. The FFs (or latches) may obtain input from LUT outputs or directly from invertible PFU inputs, or they can be tied high or tied low. The FFs also have programmable clock polarity, clock enables, and local set/reset.

The SLIC is connected to PLC routing resources and to the outputs of the PFU. It contains 3-state, bidirectional buffers and logic to perform up to a 10-bit AND function for decoding, or an AND-OR with optional INVERT to perform *PAL*-like functions. The 3-state drivers in the SLIC and their direct connections to the PFU outputs make fast, true 3-state buses possible within the FPGA, reducing required routing and allowing for real-world system performance.

Description (continued)



5-5743

Note: All multiplexers without select inputs are configuration selector multiplexers.

Figure 1. Simplified PFU Diagram

Description (continued)

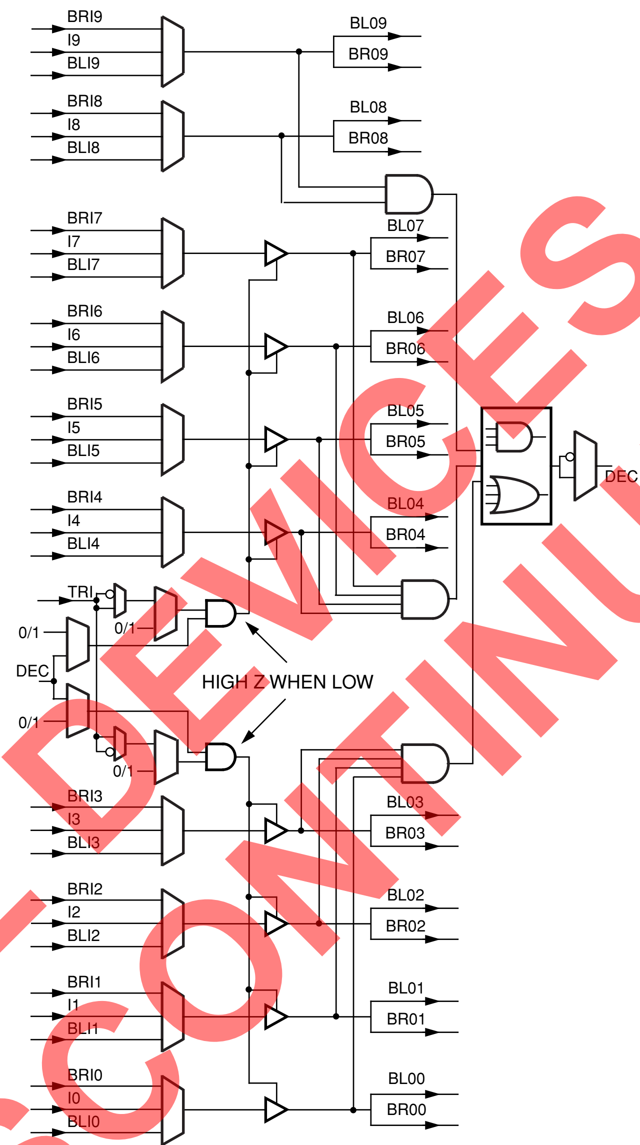


Figure 2. SLIC All Modes Diagram

Description (continued)

PIC Logic

The OR3LxxxB PIC addresses the demand for ever-increasing system clock speeds. Each PIC contains four programmable inputs/outputs (PIOs) and routing resources. On the input side, each PIO contains a fast-capture latch that is clocked by an ExpressCLK. This latch is followed by a latch/FF that is clocked by a system clock from the internal general clock routing. The combination provides for very low setup requirements and zero hold times for signals coming on-chip. It may also be used to demultiplex an input signal, such as a multiplexed address/data signal, and register the signals without explicitly building a demultiplexer. Two input signals are available to the PLC array from each PIO, and the *ORCA* Series 2 capability to use any input pin as a clock or other global input is maintained.

On the output side of each PIO, two outputs from the PLC array can be routed to each output flip-flop, and logic can be associated with each I/O pad. The output logic associated with each pad allows for multiplexing of output signals and other functions of two output signals.

The output FF, in combination with output signal multiplexing, is particularly useful for registering address signals to be multiplexed with data, allowing a full clock cycle for the data to propagate to the output. The I/O buffer associated with each pad is very similar to the Series 2 buffer with a new, fast, open-drain option for ease of use on system buses. These features may also be combined with the new 3-state FF that allows the 3-state control signal to be registered. This allows for early control setup and faster clock-to-out times.

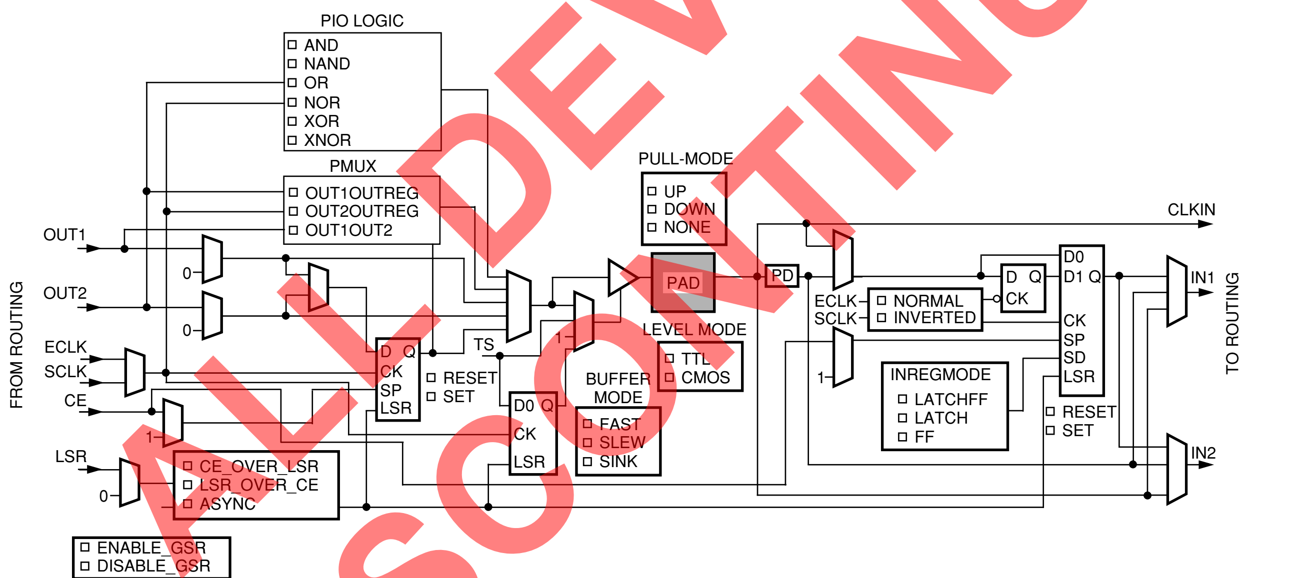


Figure 3. OR3Lxxx Programmable Input/Output Image from *ORCA* Foundry

Description (continued)

System Features

The OR3LxxxB Series also provides system-level functionality by means of its dual-use MPI and its innovative PCM. These functional blocks allow for easy glueless system interfacing and the capability to adjust to varying conditions in today's high-speed systems.

The MPI provides a glueless interface between the FPGA, *PowerPC*, and *i960* microprocessors. It can be used for configuration and readback, as well as for monitoring FPGA status. The MPI also provides a general-purpose microprocessor interface to the FPGA user-defined logic following configuration.

Two PCMs are provided on each *ORCA* 3L device. Each PCM can be used to manipulate the frequency, phase, and duty cycle of a clock signal. Clocks may be input from the dedicated corner ExpressCLK input (in the same corner as the PCM block) or from general routing. Output clocks from the PCM can be sent to the system clock spines, and/or to the ExpressCLK and fast clock spines on the edges of the device adjacent to the PCM. ExpressCLK/fast clock and system clock output frequencies can differ by up to a factor of eight to allow slow I/O clocking with fast internal processing (or vice versa). Each PCM is capable of manipulating clocks from 5 MHz to 120 MHz. Frequencies can be adjusted from 1/8× to 64× the input clock frequency, duty cycles, and phase delays can be adjusted from 3.125% to 96.875%.

Routing

The abundant routing resources of the *ORCA* 3LxxxB FPGAs are organized to route signals individually or as buses with related control signals. Clocks are routed on a low-skew, high-speed distribution network and may be sourced from PLC logic, externally from any I/O pad, or from the very fast ExpressCLK pins. ExpressCLKs may be glitchlessly and independently enabled and disabled with a programmable control signal using the new StopCLK feature. The improved PIC routing resources are now similar to the patented intra-PLC routing resources and provide great flexibility in moving signals to and from the PIOs. This flexibility translates into an improved capability to route designs at the required speeds when the I/O signals have been locked to specific pins.

Configuration

The FPGA's functionality is determined by internal configuration RAM. The FPGA's internal initialization/configuration circuitry loads the configuration data at powerup or under system control. The RAM is loaded by using one of several configuration modes. The configuration data resides externally in an EEPROM or any other storage media. Serial EEPROMs provide a simple, low pin count method for configuring FPGAs. A new, easy method for configuring the devices is through the microprocessor interface.

Configuration Data Format

The length and number of data frames and information on the PROM size for the Series OR3LxxxB FPGAs are given in Table 3.

Table 3. Configuration Frame Size

Devices	3L165B	3L225B
Number of Frames	2136	2520
Data Bits/Frame	502	592
Configuration Data (number of frames × number of data bits/frame)	1,072,272	1,552,320
Maximum Total Number Bits/Frame (align bits, 01 frame start, 8-bit checksum, eight stop bits)	520	610
Maximum Configuration Data (number bits/frame × number of frames)	1,110,720	1,537,200
Maximum PROM Size (bits) (add configuration header and postamble)	1,110,760	1,537,240

Description (continued)

Series 3L I/Os and 5 V Tolerance

Series 3L devices use the same I/O structure as *ORCA* Series 3T devices. *ORCA* Series 3L devices use a 3.3 V supply (VDD) to power the I/Os and a 2.5 V supply (VDD2) to power the internal logic. Because the I/O structure and voltage is common between 3T and 3L devices, the Series 3L devices maintain 5 V tolerance and the same I/O characteristics as Series 3T devices.

The OR3LxxxB uses a default mode that maintains a 5 V tolerant setting on all I/Os.

Designing with *ORCA* Series 3T Parts with Series 3L in Mind

Due to many package compatibilities across device sizes and families, it is possible to design using a Series 3T device today, and migrate to a Series 3L device later. The pinouts are the same on both families with the exception of additional I/O voltage pins for the Series 3L family.

To design a board that is both Series 3T compatible and Series 3L compatible, using the following procedures will allow easy and fast component swapping from Series 3T to Series 3L.

Design to the Series 3L pinouts, especially if planning to use the OR3L225B pinout. The OR3L225B has additional power pins that are not on smaller Series 3L parts. (Note that if the designer is using a Series 3L device smaller than the OR3L225B, but may eventually migrate to a OR3L225B, the OR3L225B pinout should also be used). Designing for Series 3L in this manner does sacrifice some user I/O pins available in the Series 3T (or smaller Series 3L devices if using the OR3L225B). These I/Os will have power applied to them when a Series 3T device is used on the board. However, this is acceptable and these I/Os will default to 3-state outputs which eliminates any contention risk.

Design with two power planes: one for the internal supply (2.5 V), and one for the I/O supply (3.3 V). For Series 3T operation, connect both the internal supply and I/O voltage planes to 3.3 V. For Series 3L operation, change the core plane connection from 3.3 V to 2.5 V.

Powerup Sequencing for Series 3L Devices

ORCA Series 3L devices use two power supplies: one to power the device I/Os (VDD) which is set to 3.3 V for 3.3 V operation and 5 V tolerance, and another supply for the internal logic (VDD2) which is set to 2.5 V. It is understood that many users will derive the 2.5 V core logic supply from a 3.3 V power supply, so the following recommendations are made as to the powerup sequence of the supplies and allowable delays between power supplies reaching stable voltages.

In general, both the 3.3 V and the 2.5 V supplies should ramp-up and become stable as close together in time as possible. There is no delay requirement if the VDD2 (2.5 V) supply becomes stable prior to the VDD (3.3 V) supply. There is a delay requirement imposed if the VDD supply becomes stable prior to the VDD2 supply.

The requirement is that the VDD2 (2.5 V) supply transitions from 0.8 V to 2.3 V within 15.7 ms when the VDD (3.3 V) supply is already stable at a minimum of 3.0 V. If the chosen power supplies cannot meet this delay requirement, it is always possible to delay configuration of the FPGA by asserting $\overline{\text{INIT}}$ or $\overline{\text{PRGM}}$ until the VDD2 supply has reached 2.3 V. This process eliminates any power supply sequencing issues.

Description (continued)

ORCA Foundry Development System

The *ORCA* Foundry development system is used to process a design from a netlist to a configured FPGA. This system is used to map a design onto the *ORCA* architecture and then place and route it using *ORCA* Foundry's timing-driven tools. The development system also includes interfaces to, and libraries for, other popular CAE tools for design entry, synthesis, simulation, and timing analysis.

The *ORCA* Foundry development system interfaces to front-end design entry tools and provides the tools to produce a configured FPGA. In the design flow, the user defines the functionality of the FPGA at two points in the design flow: at design entry and at the bit stream generation stage.

Following design entry, the development system's map, place, and route tools translate the netlist into a routed FPGA. A static timing analysis tool is provided to determine device speed, and a back-annotated netlist can be created to allow simulation.

Timing and simulation output files from *ORCA* Foundry are also compatible with many third-party analysis tools. Its bit stream generator is then used to generate the configuration data, which is loaded into the FPGA's internal configuration RAM.

When using the bit stream generator, the user selects options that affect the functionality of the FPGA. Combined with the front-end tools, *ORCA* Foundry produces configuration data that implements the various logic and routing options discussed in this product brief.

Additional Information

Contact your local Lattice representative for additional information regarding the *ORCA* OR3LxxxB FPGA devices, or visit our website at: **http://www.latticesemi.com**.

Timing Characteristics

Configuration Timing

Table 4. General Configuration Mode Timing Characteristics

OR3LxxB Commercial: V_{DD} = 3.0 V to 3.6 V, V_{DD2} = 2.38 V to 2.63 V, 0 °C < T_A < 70 °C; Industrial: V_{DD} = 3.0 V to 3.6 V, V_{DD2} = 2.38 V to 2.63 V, –40 °C < T_A < +85 °C.

Symbol	Parameter	Min	Max	Unit
All Configuration Modes				
T_{SMODE}	M[3:0] Setup Time to $\overline{INIT}$ High	0.00	—	ns
T_{HMODE}	M[3:0] Hold Time from $\overline{INIT}$ High	600.00	—	ns
T_{RW}	$\overline{RESET}$ Pulse Width Low to Start Reconfiguration	50.00	—	ns
T_{PGW}	$\overline{PRGM}$ Pulse Width Low to Start Reconfiguration	50.00	—	ns
Master and Asynchronous Peripheral Modes				
T_{PO}	Power-on Reset Delay	15.70	52.40	ms
T_{CCLK}	CCLK Period (M3 = 0)	60.00	200.00	ns
	(M3 = 1)	480.00	1600.00	ns
T_{CL}	Configuration Latency (autoincrement mode):			
	OR3L165B (M3 = 0)	66.65	222.15*	ms
	(M3 = 1)	533.16	1777.22*	ms
	OR3L225B (M3 = 0)	92.23	307.45*	ms
	(M3 = 1)	737.88	2459.8*	ms
Microprocessor (MPI) Mode				
T_{PO}	Power-on Reset Delay	15.70	52.40	ms
T_{CL}	Configuration Latency (autoincrement mode):			
	OR3L165B	147,405	—	write cycles
	OR3L225B	202,251	—	write cycles
T_{PR}	Partial Reconfiguration (explicit mode):			
	OR3L165B	69	—	write cycles
	OR3L225B	81	—	write cycles
Slave Serial Mode				
T_{PO}	Power-on Reset Delay	3.90	13.10	ms
T_{CCLK}	CCLK Period	15.00		ns
T_{CL}	Configuration Latency (autoincrement mode):			
	OR3L165B	16.66	—	ms
	OR3L225B	23.06	—	ms
Slave Parallel Mode				
T_{PO}	Power-on Reset Delay	3.90	13.10	ms
T_{CCLK}	CCLK Period:	15.00		ns
T_{CL}	Configuration Latency (normal mode):			
	OR3L165B	2.08	—	
	OR3L225B	2.88	—	
T_{PR}	Partial Reconfiguration (explicit mode):			
	OR3L165B	1.0	—	µs/frame
	OR3L225B	1.2	—	µs/frame

* Not applicable to asynchronous peripheral mode.

Note: T_{PO} is triggered when V_{DD} reaches between 2.7 V and 3.0 V for the OR3LxxxB.

Timing Characteristics (continued)

In addition to supply voltage, process variation, and operating temperature, circuit and process improvements of the *ORCA* Series FPGAs over time will result in significant improvement of the actual performance over those listed for a speed grade. Even though lower speed grades may still be available, the distribution of yield to timing parameters may be several speed grades higher than that designated on a product brand. Design practices need to consider best-case timing parameters (e.g., delays = 0), as well as worst-case timing.

The routing delays are a function of fan-out and the capacitance associated with the configurable interface points (CIPs) and metal interconnect in the path. The number of logic elements that can be driven (fan-out) by PFUs is unlimited, although the delay to reach a valid logic level can exceed timing requirements. It is difficult to make accurate routing delay estimates prior to design compilation based on fan-out. This is because the CAE software may delete redundant logic inserted by the designer to reduce fan-out, and/or it may also automatically reduce fan-out by net splitting.

The waveform test points are given in the Input/Output Buffer Measurement Conditions section of this data sheet. The timing parameters given in the electrical characteristics tables in this data sheet follow industry practices, and the values they reflect are described below.

Propagation Delay—The time between the specified reference points. The delays provided are the worst case of the tphh and tpll delays for noninverting functions, tplh and tphl for inverting functions, and tphz and tplz for 3-state enable.

Setup Time—The interval immediately preceding the transition of a clock or latch enable signal, during which the data must be stable to ensure it is recognized as the intended value.

Hold Time—The interval immediately following the transition of a clock or latch enable signal, during which the data must be held stable to ensure it is recognized as the intended value.

3-State Enable—The time from when a 3-state control signal becomes active and the output pad reaches the high-impedance state.

PFU Timing

Table 5. Combinatorial PFU Timing Characteristics

OR3LxxB Commercial: V_{DD} = 3.0 V to 3.6 V, V_{DD2} = 2.38 V to 2.63 V, 0 °C < T_A < 70 °C; Industrial: V_{DD} = 3.0 V to 3.6 V, V_{DD2} = 2.38 V to 2.63 V, –40 °C < T_A < +85 °C.

Symbol	Parameter	-7		-8		Unit
		Min	Max	Min	Max	
	Combinatorial Delays (T_J = +85 °C, V_{DD} = min, V_{DD2} = min):					
F4_DEL	Four-input Variables (Kz[3:0] to F[z])*	—	1.03	—	0.90	ns
F5_DEL	Five-input Variables (F5[A:D] to F[0, 2, 4, 6])	—	0.85	—	0.74	ns
SWL2_DEL	Two-level LUT Delay (Kz[3:0] to F w/feedbk)*	—	2.30	—	2.00	ns
SWL2F5_DEL	Two-level LUT Delay (F5[A:D] to F w/feedbk)	—	1.91	—	1.66	ns
SWL3_DEL	Three-level LUT Delay (Kz[3:0] to F w/feedbk)*	—	3.40	—	2.96	ns
SWL3F5_DEL	Three-level LUT Delay (F5[A:D] to F w/feedbk)	—	3.02	—	2.63	ns
CO_DEL	CIN to COUT Delay (logic mode)	—	1.66	—	1.44	ns

* Four-input variables' (KZ[3:0]) path delays are valid for LUTs in both F4 (four-input LUT) and F5 (five-input LUT) modes.

Timing Characteristics (continued)

Table 6. Sequential PFU Timing Characteristics

OR3LxxB Commercial: V_{DD} = 3.0 V to 3.6 V, V_{DD2} = 2.38 V to 2.63 V, 0 °C < T_A < 70 °C; Industrial: V_{DD} = 3.0 V to 3.6 V, V_{DD2} = 2.38 V to 2.63 V, –40 °C < T_A < +85 °C.

Symbol	Parameter	-7		-8		Unit
		Min	Max	Min	Max	
Input Requirements						
CLKL_MPW	Clock Low Time	1.00	—	0.87	—	ns
CLKH_MPW	Clock High Time	0.76	—	0.66	—	ns
GSR_MPW	Global S/R Pulse Width (GSRN)	1.00	—	0.87	—	ns
LSR_MPW	Local S/R Pulse Width	1.00	—	0.87	—	ns
	Combinatorial Setup Times (T_J = +85 °C, V_{DD} = min, V_{DD2} = min):					
F4_SET	Four-input Variables to Clock (Kz[3:0] to CLK)*	0.90	—	0.78	—	ns
F5_SET	Five-input Variables to Clock (F5[A:D] to CLK)	0.51	—	0.44	—	ns
DIN_SET	Data In to Clock (DIN[7:0] to CLK)	0.21	—	0.18	—	ns
CINDIR_SET	Carry-in to Clock, DIRECT to REGCOUT (CIN to CLK)	0.68	—	0.59	—	ns
CE1_SET	Clock Enable to Clock (CE to CLK)	1.41	—	1.23	—	ns
CE2_SET	Clock Enable to Clock (ASWE to CLK)	1.11	—	0.97	—	ns
LSR_SET	Local Set/Reset to Clock (SYNC) (LSR to CLK)	0.69	—	0.60	—	ns
SEL_SET	Data Select to Clock (SEL to CLK)	0.64	—	0.55	—	ns
SWL2_SET	Two-level LUT to Clock (Kz[3:0] to CLK w/feedbk)*	1.79	—	1.55	—	ns
SWL2F5_SET	Two-level LUT to Clock (F5[A:D] to CLK w/feedbk)	1.46	—	1.27	—	ns
SWL3_SET	Three-level LUT to Clock (Kz[3:0] to CLK w/feedbk)*	3.06	—	2.66	—	ns
SWL3F5_SET	Three-level LUT to Clock (F5[A:D] to CLK w/feedbk)	2.67	—	2.32	—	ns
	Combinatorial Hold Times (T_J = all, V_{DD} = all):					
DIN_HLD	Data In (DIN[7:0] from CLK)	0.0	—	0.0	—	ns
CINDIR_HLD	Carry-in from Clock, DIRECT to REGCOUT (CIN from CLK)	0.0	—	0.0	—	ns
CE1_HLD	Clock Enable (CE from CLK)	0.0	—	0.0	—	ns
CE2_HLD	Clock Enable from Clock (ASWE from CLK)	0.0	—	0.0	—	ns
LSR_HLD	Local Set/Reset from Clock (sync) (LSR from CLK)	0.0	—	0.0	—	ns
SEL_HLD	Data Select from Clock (SEL from CLK)	0.0	—	0.0	—	ns
—	All Others	0.0	—	0.0	—	ns
Output Characteristics						
	Sequential Delays (T_J = +85 °C, V_{DD} = min, V_{DD2} = min):					
LSR_DEL	Local S/R (async) to PFU Out (LSR to Q[7:0], REGCOUT)	—	2.82	—	2.46	ns
GSR_DEL	Global S/R to PFU Out (GSRN to Q[7:0], REGCOUT)	—	2.21	—	1.92	ns
REG_DEL	Clock to PFU Out—Register (CLK to Q[7:0], REGCOUT)	—	1.22	—	1.06	ns
LTCH_DEL	Clock to PFU Out—Latch (CLK to Q[7:0])	—	1.30	—	1.13	ns
LTCHD_DEL	Transparent Latch (DIN[7:0] to Q[7:0])	—	1.43	—	1.25	ns

* Four-input variables' (KZ[3:0]) setup times are valid for LUTs in both F4 (four-input LUT) and F5 (five-input LUT) modes.

Note: The table shows worst-case delays. *ORCA* Foundry reports the delays for individual paths within a group of paths representing the same timing parameter and may accurately report delays that are less than those listed.

Timing Characteristics (continued)

Table 7. Ripple Mode PFU Timing Characteristics

OR3LxxB Commercial: VDD = 3.0 V to 3.6 V, VDD2 = 2.38 V to 2.63 V, 0 °C < TA < 70 °C; Industrial: VDD = 3.0 V to 3.6 V, VDD2 = 2.38 V to 2.63 V, –40 °C < TA < +85 °C.

Symbol	Parameter (TJ = +85 °C, VDD = min, VDD2 = min)	-7		-8		Unit
		Min	Max	Min	Max	
	Full Ripple Setup Times (byte-wide):					
RIP_SET	Operands to Clock (Kz[1:0] to CLK)	1.58	—	1.37	—	ns
FRIP_SET	Bitwise Operands to Clock (Kz[1:0] to CLK at F[z])	0.90	—	0.78	—	ns
FCIN_SET	Fast Carry-in to Clock (FCIN to CLK)	1.21	—	1.05	—	ns
CIN_SET	Carry-in to Clock (CIN to CLK)	1.68	—	1.46	—	ns
AS_SET	Add/Subtract to Clock (ASWE to CLK)	4.70	—	4.09	—	ns
RIPRC_SET	Operands to Clock (Kz[1:0] to CLK at REGCOUT)	1.02	—	0.89	—	ns
FCINRC_SET	Fast Carry-in to Clock (FCIN to CLK at REGCOUT)	1.03	—	0.90	—	ns
CINRC_SET	Carry-in to Clock (CIN to CLK at REGCOUT)	1.48	—	1.29	—	ns
ASRC_SET	Add/Subtract to Clock (ASWE to CLK at REGCOUT)	4.51	—	3.92	—	ns
	Full Ripple Hold Times (TJ = all, VDD = all):					
FCINRC_HLD	Fast Carry-in from Clock (FCIN from CLK at REGCOUT)	0.0	—	0.0	—	ns
——	All Others	0.0	—	0.0	—	ns
	Half Ripple Setup Times (nibble wide):					
HRIP_SET	Operands to Clock (Kz[1:0] to CLK)	1.74	—	1.51	—	ns
HFRIP_SET	Bitwise Operands to Clock (Kz[1:0] to CLK at F[z])	0.90	—	0.78	—	ns
HFCIN_SET	Fast Carry-in to Clock (FCIN to CLK)	1.21	—	1.05	—	ns
HCIN_SET	Carry-in to Clock (CIN to CLK)	1.68	—	1.46	—	ns
HAS_SET	Add/Subtract to Clock (ASWE to CLK)	4.70	—	4.09	—	ns
HRIPRC_SET	Operands to Clock (Kz[1:0] to CLK at REGCOUT)	1.37	—	1.19	—	ns
HFCINRC_SET	Fast Carry-in to Clock (FCIN to CLK at REGCOUT)	1.03	—	0.90	—	ns
HCINRC_SET	Carry-in to Clock (CIN to CLK at REGCOUT)	1.48	—	1.29	—	ns
HASRC_SET	Add/Subtract to Clock (ASWE to CLK at REGCOUT)	4.51	—	3.92	—	ns
	Half Ripple Hold Times (TJ = all, VDD = all):					
HFCINRC_HLD	Fast Carry-in from Clock (HFCIN from CLK at RECOUT)	0.0	—	0.0	—	ns
——	All Others	0.0	—	0.0	—	ns

Note: The table shows worst-case delay for the ripple chain. *ORCA* Foundry reports the delay for individual paths within the ripple chain that will be less than or equal to those listed above.

Timing Characteristics (continued)

Table 7. Ripple Mode PFU Timing Characteristics (continued)

OR3LxxB Commercial: V_{DD} = 3.0 V to 3.6 V, V_{DD2} = 2.38 V to 2.63 V, 0 °C < T_A < 70 °C; Industrial: V_{DD} = 3.0 V to 3.6 V, V_{DD2} = 2.38 V to 2.63 V, –40 °C < T_A < +85 °C.

Symbol	Parameter (T_J = +85 °C, V_{DD} = min, V_{DD2} = min)	-7		-8		Unit
		Min	Max	Min	Max	
	Full Ripple Delays (byte-wide):					
RIPCO_DEL	Operands to Carry-out (Kz[1:0] to COUT)	—	2.26	—	1.97	ns
RIPFCO_DEL	Operands to Carry-out (Kz[1:0] to FCOUT)	—	2.23	—	1.94	ns
RIP_DEL	Operands to PFU Out (Kz[1:0] to F[7:0])	—	3.21	—	2.79	ns
FRIP_DEL	Bitwise Operands to PFU Out (Kz[1:0] to F[z])	—	1.03	—	0.90	ns
FCINCO_DEL	Fast Carry-in to Carry-out (FCIN to COUT)	—	1.36	—	1.18	ns
FCINFCO_DEL	Fast Carry-in to Fast Carry-out (FCIN to FCOUT)	—	1.33	—	1.15	ns
CINCO_DEL	Carry-in to Carry-out (CIN to COUT)	—	1.66	—	1.44	ns
CINFCO_DEL	Carry-in to Fast Carry-out (CIN to FCOUT)	—	1.61	—	1.40	ns
FCIN_DEL	Fast Carry-in PFU Out (FCIN to F[7:0])	—	2.03	—	1.77	ns
CIN_DEL	Carry-in PFU Out (CIN to F[7:0])	—	2.65	—	2.31	ns
ASCO_DEL	Add/Subtract to Carry-out (ASWE to COUT)	—	4.67	—	4.06	ns
ASFCO_DEL	Add/Subtract to Carry-out (ASWE to FCOUT)	—	4.58	—	3.98	ns
AS_DEL	Add/Subtract to PFU Out (ASWE to F[7:0])	—	5.61	—	4.88	ns
	Half Ripple Delays (nibble wide):					
HRIPCO_DEL	Operands to Carry-out (Kz[1:0] to COUT)	—	2.26	—	1.97	ns
HRIPFCO_DEL	Operands to Fast Carry-out (Kz[1:0] to FCOUT)	—	2.23	—	1.94	ns
HRIP_DEL	Operands to PFU Out (Kz[1:0] to F[3:0])	—	2.61	—	2.27	ns
HFRIP_DEL	Bitwise Operands to PFU Out (Kz[1:0] to F[z])	—	1.03	—	0.90	ns
HFCINCO_DEL	Fast Carry-in to Carry-out (FCIN to COUT)	—	1.36	—	1.18	ns
HFCINFCO_DEL	Fast Carry-in to Fast Carry-out (FCIN to FCOUT)	—	1.33	—	1.15	ns
HCINCO_DEL	Carry-in to Carry-out (CIN to COUT)	—	1.66	—	1.44	ns
HCINFCO_DEL	Carry-in to Carry-out (CIN to FCOUT)	—	1.61	—	1.40	ns
HFCIN_DEL	Fast Carry-in PFU Out (FCIN to F[3:0])	—	1.72	—	1.50	ns
HCIN_DEL	Carry-in PFU Out (CIN to F[3:0])	—	2.40	—	2.09	ns
HASCO_DEL	Add/Subtract to Carry-out (ASWE to COUT)	—	4.67	—	4.06	ns
HASFCO_DEL	Add/Subtract to Carry-out (ASWE to FCOUT)	—	4.58	—	3.98	ns
HAS_DEL	Add/Subtract to PFU Out (ASWE to F[3:0])	—	5.00	—	4.34	ns

Note: The table shows worst-case delay for the ripple chain. *ORCA* Foundry reports the delay for individual paths within the ripple chain that will be less than or equal to those listed above.

Timing Characteristics (continued)

Table 8. Synchronous Memory Write Characteristics

OR3LxxB Commercial: V_{DD} = 3.0 V to 3.6 V, V_{DD2} = 2.38 V to 2.63 V, 0 °C < T_A < 70 °C; Industrial: V_{DD} = 3.0 V to 3.6 V, V_{DD2} = 2.38 V to 2.63 V, –40 °C < T_A < +85 °C.

Symbol	Parameter	-7		-8		Unit
		Min	Max	Min	Max	
Write Operation for RAM Mode						
SMCLK_FRQ	Maximum Frequency	—	266.4	—	333.0	MHz
SMCLKL_MPW	Clock Low Time	1.03	—	0.90	—	ns
SMCLKH_MPW	Clock High Time	1.96	—	1.71	—	ns
MEM_DEL	Clock to Data Valid (CLK to F[6, 4, 2, 0])*	—	4.39	—	3.82	ns
Write Operation Setup Time						
WA4_SET	Address to Clock (CIN to CLK)	0.68	—	0.59	—	ns
WA_SET	Address to Clock (DIN[7, 5, 3, 1] to CLK)	0.35	—	0.30	—	ns
WD_SET	Data to Clock (DIN[6, 4, 2, 0] to CLK)	0.21	—	0.18	—	ns
WE_SET	Write Enable (WREN) to Clock (ASWE to CLK)	0.37	—	0.32	—	ns
WPE0_SET	Write-port Enable 0 (WPE0) to Clock (CE to CLK)	0.87	—	0.75	—	ns
WPE1_SET	Write-port Enable 1 (WPE1) to Clock (LSR to CLK)	1.10	—	0.95	—	ns
Write Operation Hold Time						
WA4_HLD	Address from Clock (CIN from CLK)	0.0	—	0.0	—	ns
WA_HLD	Address from Clock (DIN[7, 5, 3, 1] from CLK)	0.0	—	0.0	—	ns
WD_HLD	Data from Clock (DIN[6, 4, 2, 0] from CLK)	0.33	—	0.29	—	ns
WE_HLD	Write Enable (WREN) from Clock (ASWE from CLK)	0.0	—	0.0	—	ns
WPE0_HLD	Write-port Enable 0 (WPE0) from Clock (CE from CLK)	0.0	—	0.0	—	ns
WPE1_HLD	Write-port Enable 1 (WPE1) from Clock (LSR from CLK)	0.0	—	0.0	—	ns

* The RAM is written on the inactive clock edge following the active edge that latches the address, data, and control signals.

Note: The table shows worst-case delays. *ORCA* Foundry reports the delays for individual paths within a group of paths representing the same timing parameter and may accurately report delays that are less than those listed.

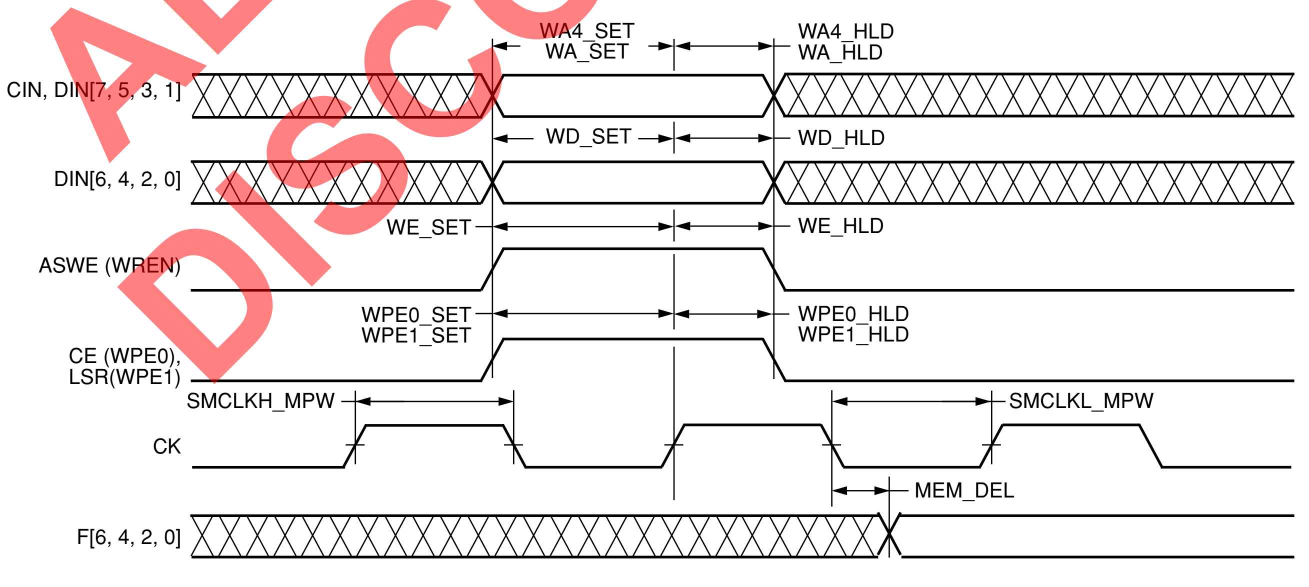


Figure 4. Synchronous Memory Write Characteristics

Timing Characteristics (continued)

Table 9. Synchronous Memory Read Characteristics

OR3LxxB Commercial: VDD = 3.0 V to 3.6 V, VDD2 = 2.38 V to 2.63 V, 0 °C < TA < 70 °C; Industrial: VDD = 3.0 V to 3.6 V, VDD2 = 2.38 V to 2.63 V, –40 °C < TA < +85 °C.

Symbol	Parameter (TJ = 85 °C, VDD = min, VDD2 = min)	-7		-8		Unit
		Min	Max	Min	Max	
Read Operation						
RA_DEL RA4_DEL	Data Valid After Address (Kz[3:0] to F[6, 4, 2, 0]) Data Valid After Address (F5[A:D] to F[6, 4, 2, 0])	— —	1.03 0.85	— —	0.90 0.74	ns ns
Read Operation, Clocking Data into Latch/FF						
RA_SET RA4_SET RA_HLD RA4_HLD REG_DEL SMRD_CYC	Address to Clock Setup Time (Kz[3:0] to CLK) Address to Clock Setup Time (F5[A:D] to CLK) Address from Clock Hold Time (Kz[3:0] from CLK) Address from Clock Hold Time (F5[A:D] from CLK) Clock to PFU Output—Register (CLK to Q[6, 4, 2, 0]) Read Cycle Delay	0.90 0.51 0.0 0.0 — —	— — — — 1.22 5.38	0.78 0.44 0.0 0.0 — —	— — — — 1.06 4.68	ns ns ns ns ns ns

Note: The table shows worst-case delays. *ORCA* Foundry reports the delays for individual paths within a group of paths representing the same timing parameter and may accurately report delays that are less than those listed.

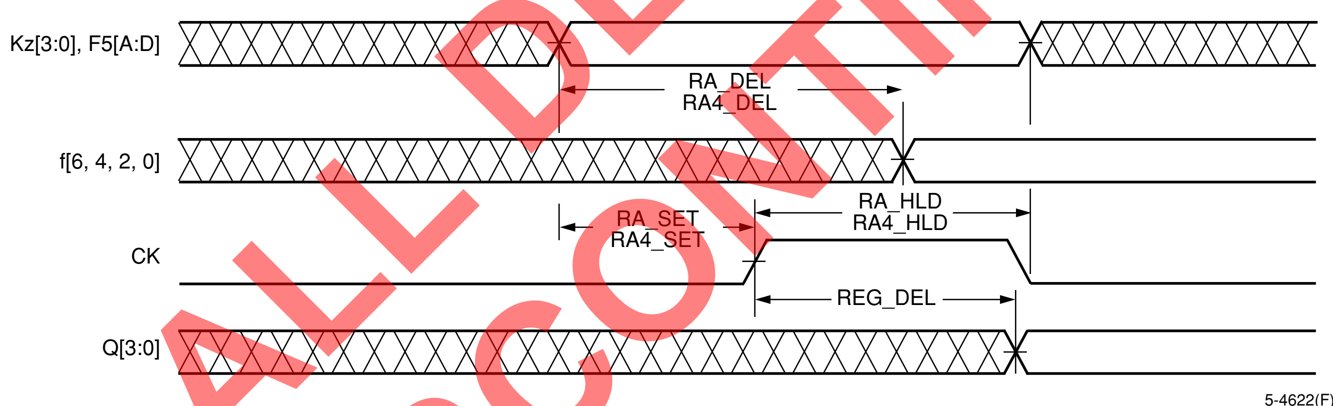


Figure 5. Synchronous Memory Read Cycle

Timing Characteristics (continued)

PLC Timing

Table 10. PFU Output MUX and Direct Routing Timing Characteristics

OR3LxxB Commercial: V_{DD} = 3.0 V to 3.6 V, V_{DD2} = 2.38 V to 2.63 V, 0 °C < T_A < 70 °C; Industrial: V_{DD} = 3.0 V to 3.6 V, V_{DD2} = 2.38 V to 2.63 V, –40 °C < T_A < +85 °C.

Symbol	Parameter (T_J = 85 °C, V_{DD} = min, V_{DD2} = min)	-7		-8		Unit
		Min	Max	Min	Max	
PFU Output MUX (Fan-out = 1)						
OMUX_DEL	Output MUX Delay (F[7:0]/Q[7:0] to O[9:0])	—	0.76	—	0.66	ns
COO9_DEL	Carry-out MUX Delay (COUT to O9)	—	0.74	—	0.64	ns
RCOO8_DEL	Registered Carry-out MUX Delay (REGCOUT to O8)	—	0.74	—	0.64	ns
Direct Routing						
FDBK_DEL	PFU Feedback (xSW)*	—	0.75	—	0.65	ns
ODIR_DEL	PFU to Orthogonal PFU Delay (xSW to xSW)	—	0.89	—	0.78	ns
DDIR_DEL	PFU to Diagonal PFU Delay (xBID to xSW)	—	1.61	—	1.40	ns

* This is general feedback using switching segments. See the combinatorial PFU timing table for softwired look-up table feedback timing.

SLIC Timing

Table 11. Supplemental Logic and Interconnect Cell Timing Characteristics

OR3LxxB Commercial: V_{DD} = 3.0 V to 3.6 V, V_{DD2} = 2.38 V to 2.63 V, 0 °C < T_A < 70 °C; Industrial: V_{DD} = 3.0 V to 3.6 V, V_{DD2} = 2.38 V to 2.63 V, –40 °C < T_A < +85 °C.

Symbol	Parameter (T_J = 85 °C, V_{DD} = min, V_{DD2} = min)	-7		-8		Unit
		Min	Max	Min	Max	
3-Statable BIDIs						
BUF_DEL	BIDI Delay (BRx to BLx, BLx to BRx)	—	0.70	—	0.61	ns
OBUF_DEL	BIDI Delay (Ox to BRx, Ox to BLx)	—	0.61	—	0.53	ns
TRI_DEL	BIDI 3-state Enable/Disable Delay (TRI to BL, BR)	—	1.18	—	1.03	ns
DECTRI_DEL	BIDI 3-state Enable/Disable Delay (BL, BR via DEC, TRI to BL, BR)	—	2.01	—	1.75	ns
Decoder						
DEC98_DEL	Decoder Delay (BR[9:8], BL[9:8] to DEC)	—	1.16	—	1.01	ns
DEC_DEL	Decoder Delay (BR[7:0], BL[7:0] to DEC)	—	1.29	—	1.12	ns

Timing Characteristics (continued)

PIO Timing.

Table 12. Programmable I/O Timing Characteristics

OR3LxxB Commercial: V_{DD} = 3.0 V to 3.6 V, V_{DD2} = 2.38 V to 2.63 V, 0 °C < T_A < 70 °C; Industrial: V_{DD} = 3.0 V to 3.6 V, V_{DD2} = 2.38 V to 2.63 V, –40 °C < T_A < +85 °C.

Symbol	Parameter	-7		-8		Unit
		Min	Max	Min	Max	
Input Delays (T_J = 85 °C, V_{DD} = min, V_{DD2} = min)						
IN_RIS	Input Rise Time	—	575	—	500	ns
IN_FAL	Input Fall Time	—	575	—	500	ns
	PIO Direct Delays:					
CKIN_DEL	Pad to In (pad to CLK IN)	—	0.77	—	0.55	ns
IN_DEL	Pad to In (pad to IN1, IN2)	—	1.35	—	1.07	ns
IND_DEL	Pad to In Delayed (pad to IN1, IN2)	—	11.55	—	9.89	ns
	PIO Transparent Latch Delays:					
LATCH_DEL	Pad to In (pad to IN1, IN2)	—	2.79	—	2.42	ns
LATCHD_DEL	Pad to In Delayed (pad to IN1, IN2)	—	12.46	—	10.87	ns
	Input Latch/FF Setup Timing:					
INREGE_SET	Pad to ExpressCLK (fast-capture latch/FF)	4.54	—	2.62	—	ns
INREGED_SET	Pad Delayed to ExpressCLK (fast-capture latch/FF)	14.53	—	11.63	—	ns
INREG_SET	Pad to Clock (input latch/FF)	0.65	—	0.46	—	ns
INREGD_SET	Pad Delayed to Clock (input latch/FF)	10.90	—	9.50	—	ns
INCE_SET	Clock Enable to Clock (CE to CLK)	0.92	—	0.82	—	ns
INLSR_SET	Local Set/Reset (sync) to Clock (LSR to CLK)	0.81	—	0.73	—	ns
	Input FF/Latch Hold Timing:					
INREGE_HLD	Pad from ExpressCLK (fast-capture latch/FF)	0.0	—	0.0	—	ns
INREGED_HLD	Pad Delayed from ExpressCLK (fast-capture latch/FF)	0.0	—	0.0	—	ns
INREG_HLD	Pad from Clock (input latch/FF)	0.0	—	0.0	—	ns
INREGD_HLD	Pad Delayed from Clock (input latch/FF)	0.0	—	0.0	—	ns
INCE_HLD	Clock Enable from Clock (CE from CLK)	0.0	—	0.0	—	ns
INLSR_HLD	Local Set/Reset (sync) from Clock (LSR from CLK)	0.0	—	0.0	—	ns
INREG_DEL	Clock-to-in Delay (FF CLK to IN1, IN2)	—	1.94	—	1.68	ns
INLTCH_DEL	Clock-to-in Delay (latch CLK to IN1, IN2)	—	1.94	—	1.68	ns
INLSR_DEL	Local S/R (async) to IN (LSR to IN1, IN2)	—	2.95	—	2.55	ns
INLSRL_DEL	Local S/R (async) to IN (LSR to IN1, IN2) Latch/FF in Latch Mode	—	2.64	—	2.30	ns
INGSR_DEL	Global S/R to In (GSRN to IN1, IN2)	—	2.69	—	2.34	ns

Note: The delays for all input buffers assume an input rise/fall time of <1 V/ns.

Timing Characteristics (continued)

Table 12. Programmable I/O Timing Characteristics (continued)

OR3LxxB Commercial: V_{DD} = 3.0 V to 3.6 V, V_{DD2} = 2.38 V to 2.63 V, 0 °C < T_A < 70 °C; Industrial: V_{DD} = 3.0 V to 3.6 V, V_{DD2} = 2.38 V to 2.63 V, –40 °C < T_A < +85 °C.

Symbol	Parameter	-7		-8		Unit
		Min	Max	Min	Max	
Output Delays (T_J = 85 °C, V_{DD} = min, C_L = 50 pF)						
	Output to Pad (OUT2, OUT1 direct to pad):					
OUTF_DEL	Fast	—	3.79	—	3.21	ns
OUTSL_DEL	Slewlim	—	4.71	—	3.91	ns
OUTSI_DEL	Sinklim	—	10.14	—	8.84	ns
	3-state Enable/Disable Delay (TS to pad):					
TSF_DEL	Fast	—	3.86	—	3.29	ns
TSSL_DEL	Slewlim	—	4.66	—	3.99	ns
TSSI_DEL	Sinklim	—	10.24	—	8.92	ns
	Local Set/Reset (async) to Pad (LSR to pad):					
OUTLSRF_DEL	Fast	—	5.70	—	4.90	ns
OUTLSRSL_DEL	Slewlim	—	6.58	—	5.60	ns
OUTLSRSI_DEL	Sinklim	—	12.09	—	10.52	ns
	Global Set/Reset to Pad (GSRN to pad):					
OUTGSRF_DEL	Fast	—	5.05	—	4.81	ns
OUTGSRSL_DEL	Slewlim	—	5.75	—	5.51	ns
OUTGSRSI_DEL	Sinklim	—	10.60	—	10.43	ns
	Output FF Setup Timing:					
OUTE_SET	Out to ExpressCLK (OUT[2:1] to ECLK)	0.0	—	0.0	—	ns
OUT_SET	Out to Clock (OUT[2:1] to CLK)	0.0	—	0.0	—	ns
OUTCE_SET	Clock Enable to Clock (CE to CLK)	0.44	—	0.39	—	ns
OUTLSR_SET	Local Set/Reset (sync) to Clock (LSR to CLK)	0.05	—	0.04	—	ns
	Output FF Hold Timing:					
OUTE_HLD	Out from ExpressCLK (OUT[2:1] from ECLK)	0.32	—	0.28	—	ns
OUT_HLD	Out from Clock (OUT[2:1] from CLK)	0.32	—	0.28	—	ns
OUTCE_HLD	Clock Enable from Clock (CE from CLK)	0.0	—	0.0	—	ns
OUTLSR_HLD	Local Set/Reset (sync) from Clock (LSR from CLK)	0.0	—	0.0	—	ns
	Clock to Pad Delay (ECLK, SCLK to pad):					
OUTREGF_DEL	Fast	—	4.67	—	4.02	ns
OUTREGSL_DEL	Slewlim	—	5.55	—	4.72	ns
OUTREGSI_DEL	Sinklim	—	11.05	—	9.64	ns
OD_DEL	Additional Delay If Using Open Drain	—	0.11	—	0.09	ns

Note: The delays for all input buffers assume an input rise/fall time of <1 V/ns

Timing Characteristics (continued)

Table 12. Programmable I/O Timing Characteristics (continued)

OR3LxxB Commercial: VDD = 3.0 V to 3.6 V, VDD2 = 2.38 V to 2.63 V, 0 °C < TA < 70 °C; Industrial: VDD = 3.0 V to 3.6 V, VDD2 = 2.38 V to 2.63 V, –40 °C < TA < +85 °C.

Symbol	Parameter	-7 Min	-7 Max	-8 Min	-8 Max	Unit
PIO Logic Block Delays						
	Out to Pad (OUT[2:1] via logic to pad):					
OUTLF_DEL	Fast	—	3.79	—	3.21	ns
OUTLSL_DEL	Slewlim	—	4.71	—	3.91	ns
OUTLSI_DEL	Sinklim	—	10.14	—	8.84	ns
	Outreg to Pad (OUTREG via logic to pad):					
OUTRF_DEL	Fast	—	4.67	—	4.02	ns
OUTRSL_DEL	Slewlim	—	5.55	—	4.72	ns
OUTRSI_DEL	Sinklim	—	11.05	—	9.64	ns
	Clock to Pad (ECLK, CLK via logic to pad):					
OUTCF_DEL	Fast	—	4.54	—	3.90	ns
OUTCSL_DEL	Slewlim	—	5.44	—	4.60	ns
OUTCSI_DEL	Sinklim	—	10.92	—	9.53	ns
3-State FF Delays						
	3-state Enable/Disable Delay (TS direct to pad):					
TSF_DEL	Fast	—	3.86	—	3.29	ns
TSSL_DEL	Slewlim	—	4.66	—	3.99	ns
TSSI_DEL	Sinklim	—	10.24	—	8.92	ns
	Local Set/Reset (async) to Pad (LSR to pad):					
TSLSRF_DEL	Fast	—	5.13	—	4.38	ns
TSLSRSL_DEL	Slewlim	—	5.93	—	5.08	ns
TSLSRSI_DEL	Sinklim	—	11.51	—	10.01	ns
	Global Set/Reset to Pad (GSRN to pad):					
TSGSRF_DEL	Fast	—	4.65	—	4.28	ns
TSGSRSL_DEL	Slewlim	—	5.35	—	4.98	ns
TSGSRSI_DEL	Sinklim	—	10.20	—	9.91	ns
	3-State FF Setup Timing:					
TSE_SET	TS to ExpressCLK (TS to ECLK)	0.0	—	0.0	—	ns
TS_SET	TS to Clock (TS to CLK)	0.0	—	0.0	—	ns
TSLSR_SET	Local Set/Reset (sync) to Clock (LSR to CLK)	0.0	—	0.0	—	ns
	3-State FF Hold Timing:					
TSE_HLD	TS from ExpressCLK (TS from ECLK)	0.34	—	0.30	—	ns
TS_HLD	TS from Clock (TS from CLK)	0.34	—	0.30	—	ns
TSLSR_HLD	Local Set/Reset (sync) from Clock (LSR from CLK)	0.0	—	0.0	—	ns
	Clock to Pad Delay (ECLK, SCLK to pad):					
TSREGF_DEL	Fast	—	4.09	—	3.49	ns
TSREGSL_DEL	Slewlim	—	4.90	—	4.19	ns
TSREGSI_DEL	Sinklim	—	10.48	—	9.12	ns

Note: The delays for all input buffers assume an input rise/fall time of <1 V/ns.

Timing Characteristics (continued)

Special Function Blocks Timing

Table 13. Microprocessor Interface (MPI) Timing Characteristics

OR3LxxB Commercial: V_{DD} = 3.0 V to 3.6 V, V_{DD2} = 2.38 V to 2.63 V, 0 °C < T_A < 70 °C; Industrial: V_{DD} = 3.0 V to 3.6 V, V_{DD2} = 2.38 V to 2.63 V, –40 °C < T_A < +85 °C.

Symbol	Parameter	–7		–8		Unit
		Min	Max	Min	Max	
***PowerPC* Interface Timing** (T_J = 85 °C, V_{DD} = min, V_{DD2} = min)						
TA_DEL	Transfer Acknowledge Delay (CLK to TA)	—	9.50	—	8.30	ns
BI_DEL	Burst Inhibit Delay (CLK to BIN)	—	9.40	—	8.20	ns
TA_DELZ	Transfer Acknowledge Delay to High Impedance[2]	—	—	—	—	ns
BI_DELZ	Burst Inhibit Delay to High Impedance[2]	—	—	—	—	ns
WD_SET	Write Data Setup Time (data to TS)	0.0	—	0.0	—	ns
WD_HLD	Write Data Hold Time (data from CLK while MPI_ACK low)	0.0	—	0.0	—	ns
A_SET	Address Setup Time (addr to TS)	0.0	—	0.0	—	ns
A_HLD	Address Hold Time (addr from CLK while MPI_ACK low)	0.0	—	0.0	—	ns
RW_SET	Read/Write Setup Time (R/W to TS)	0.0	—	0.0	—	ns
RW_HLD	Read/Write Hold Time (R/W from CLK while MPI_ACK low)	0.0	—	0.0	—	ns
CS_SET	Chip Select Setup Time (CS0, CS1 to TS)	0.46	—	0.40	—	ns
CS_HLD	Chip Select Hold Time (CS0, CS1 from CLK)	0.0	—	0.0	—	ns
UA_DEL	User Address Delay (pad to UA[3:0])	—	2.20	—	1.90	ns
URDWR_DEL	User Read/Write Delay (pad to URDWR_DEL)	—	4.60	—	4.00	ns
***i960* Interface Timing** (T_J = 85 °C, V_{DD} = min, V_{DD2} = min)						
ADSN_SET	Addr/Data Select to ALE (ADS, to ALE low)	—	—	—	—	ns
ADSN_HLD	Addr/Data Select to ALE (ADS, from ALE low)	0.0	—	0.0	—	ns
RDYRCV_DEL	Ready/Receive Delay (CLK to RDYRCV)	—	9.50	—	8.30	ns
RDYRCV_DELZ	Ready/Receive Delay to High Impedance[2]	—	—	—	—	ns
WD_SET	Write Data Setup Time[3]	—	—	—	—	ns
WD_HLD	Write Data Hold Time[4]	—	—	—	—	ns
A_SET	Address Setup Time (addr to ALE low)	—	0.12	—	0.10	ns
A_HLD	Address Hold Time (addr from ALE low)	0.80	—	0.70	—	ns
BE_SET	Byte Enable Setup Time (BE0, BE1 to ALE low)	—	0.12	—	0.10	ns
BE_HLD	Byte Enable Hold Time (BE0, BE1 from ALE low)	0.80	—	0.70	—	ns

1. For user system flexibility, CS0 and CS1 may be set up to any one of the three rising clock edges, beginning with the rising clock edge when MPI_STRB is low. If both chip selects are valid and the setup time is met, the MPI will latch the chip select state, and CS0 and CS1 may go inactive before the end of the read/write cycle.
2. 0.5 MPI_CLK.
3. Write data and W/R have to be valid starting from the clock cycle after both ADS and CS0 and CS1 are recognized.
4. Write data and W/R have to be held until the microprocessor receives a valid RDYRCV.
5. User Logic Delay has no predefined value. The user must generate a UEND signal to complete the cycle.
6. USTART_DEL is based on the falling clock edge.
7. There is no specific time associated with this delay. The user must assert UEND low to complete this cycle.
8. The user must assert interrupt request low until a service routine is executed.
9. This should be at least one MPI_CLK cycle.
10. User should set up read data so that RDS_SET and RDS_HLD can be met for the microprocessor timing.

Notes:

Read and write descriptions are referenced to the host microprocessor; e.g., a read is a read by the host (*PowerPC*, *i960*) from the FPGA.

PowerPC and *i960* timings to/from the clock are relative to the clock at the FPGA microprocessor interface clock pin (MPI_CLK).

Timing Characteristics (continued)

Table 13. Microprocessor Interface (MPI) Timing Characteristics (continued)

OR3LxxB Commercial: V_{DD} = 3.0 V to 3.6 V, V_{DD2} = 2.38 V to 2.63 V, 0 °C < T_A < 70 °C; Industrial: V_{DD} = 3.0 V to 3.6 V, V_{DD2} = 2.38 V to 2.63 V, –40 °C < T_A < +85 °C.

Symbol	Parameter	–7		–8		Unit
		Min	Max	Min	Max	
***i960* Interface Timing** (T_J = 85 °C, V_{DD} = min, V_{DD2} = min) (continued)						
RW_SET	Read/Write Setup Time[3]	—	—	—	—	ns
RW_HLD	Read/Write Hold Time[4]	—	—	—	—	ns
CS_SET	Chip Select Setup Time ($\overline{\text{CS0}}$, CS1 to CLK)[1]	0.80	—	0.70	—	ns
CS_HLD	Chip Select Hold Time ($\overline{\text{CS0}}$, CS1 from CLK)[1]	0.0	—	0.0	—	ns
UA_DEL	User Address Delay (CLK low to UA[3:0])	—	6.21	—	5.40	ns
URDWR_DEL	User Read/Write Delay (pad to URDWR_DEL)	—	4.60	—	4.00	ns
User Logic Delay[5]						
USTART_DEL	User Start Delay (MPI_CLK falling to USTART)[6]	—	3.80	—	3.30	ns
USTARTCLR_DEL	User Start Clear Delay (MPI_CLK to USTART)	—	6.90	—	6.00	ns
UEND_DEL	User End Delay (USTART low to UEND low)[7]	—	—	—	—	ns
Synchronous User Timing						
UEND_SET	User End Setup (UEND to MPI_CLK)	0.0	—	0.0	—	ns
UEND_HLD	User End Hold (UEND to MPI_CLK)	1.40	—	1.20	—	ns
RDS_SET	Data Setup for Read (D[7:0] to MPI_CLK)[9]	—	—	—	—	ns
RDS_HLD	Data Hold for Read (D[7:0] from MPI_CLK)[9]	—	—	—	—	ns
Asynchronous User Timing						
RDA_DEL	User End to Read Data Delay (UEND to D[7:0])[10]	—	—	—	—	ns
RDA_HLD	Data Hold from User Start (low)[9]	—	—	—	—	ns
TUIRQ_PW	Interrupt Request Pulse Width[8]	—	—	—	—	ns

1. For user system flexibility, $\overline{\text{CS0}}$ and CS1 may be set up to any one of the three rising clock edges, beginning with the rising clock edge when $\overline{\text{MPI\_STRB}}$ is low. If both chip selects are valid and the setup time is met, the MPI will latch the chip select state, and $\overline{\text{CS0}}$ and CS1 may go inactive before the end of the read/write cycle.
2. 0.5 MPI_CLK.
3. Write data and W/$\overline{\text{R}}$ have to be valid starting from the clock cycle after both $\overline{\text{ADS}}$ and $\overline{\text{CS0}}$ and CS1 are recognized.
4. Write data and W/$\overline{\text{R}}$ have to be held until the microprocessor receives a valid $\overline{\text{RDYRCV}}$.
5. User Logic Delay has no predefined value. The user must generate a UEND signal to complete the cycle.
6. USTART_DEL is based on the falling clock edge.
7. There is no specific time associated with this delay. The user must assert UEND low to complete this cycle.
8. The user must assert interrupt request low until a service routine is executed.
9. This should be at least one MPI_CLK cycle.
10. User should set up read data so that RDS_SET and RDS_HLD can be met for the microprocessor timing.

Notes:

Read and write descriptions are referenced to the host microprocessor; e.g., a read is a read by the host (*PowerPC*, *i960*) from the FPGA.

PowerPC and *i960* timings to/from the clock are relative to the clock at the FPGA microprocessor interface clock pin (MPI_CLK).

Timing Characteristics (continued)

Clock Timing

Table 14. ExpressCLK (ECLK) and Fast Clock (FCLK) Timing Characteristics

OR3LxxB Commercial: V_{DD} = 3.0 V to 3.6 V, V_{DD2} = 2.38 V to 2.63 V, 0 °C < T_A < 70 °C; Industrial: V_{DD} = 3.0 V to 3.6 V, V_{DD2} = 2.38 V to 2.63 V, –40 °C < T_A < +85 °C.

Symbol	Device (T_J = 85 °C, V_{DD} = min, V_{DD2} = min)	-7		-8		Unit
		Min	Max	Min	Max	
ECLKC_DEL	Clock Control Timing Delay Through CLKCNTRL (input from corner)	0.31	—	0.27	—	ns
ECLKM_DEL	Delay Through CLKCNTRL (input from internal clock controller PAD)	1.06	—	0.92	—	ns
	Clock Shutoff Timing:					
OFFM_SET	Setup from Middle ECLK (shut off to CLK)	0.41	—	0.36	—	ns
OFFM_HLD	Hold from Middle ECLK (shut off from CLK)	0.0	—	0.0	—	ns
OFFC_SET	Setup from Corner ECLK (shut off to CLK)	0.41	—	0.36	—	ns
OFFC_HLD	Hold from Corner ECLK (shut off from CLK)	0.0	—	0.0	—	ns
ECLKM_DEL	ECLK Delay (middle pad):					
	OR3L165	—	2.32	—	2.02	ns
	OR3L225	—	2.37	—	2.07	ns
ECLKC_DEL	ECLK Delay (corner pad):					
	OR3L165	—	5.02	—	4.23	ns
	OR3L225	—	5.27	—	4.45	ns
FCLKM_DEL	FCLK Delay (middle pad):					
	OR3L165	—	5.74	—	5.06	ns
	OR3L225	—	6.04	—	5.35	ns
FCLKC_DEL	FCLK Delay (corner pad):					
	OR3L165	—	8.41	—	7.24	ns
	OR3L225	—	8.89	—	7.68	ns

Notes:

The ECLK delays are to all of the PICs on one side of the device for middle pin input, or two sides of the device for corner pin input. The delay includes both the input buffer delay and the clock routing to the PIC clock input.

The FCLK delays are for a fully routed clock tree that uses the ExpressCLK input into the fast clock network. It includes both the input buffer delay and the clock routing to the PFU CLK input. The delay will be reduced if any of the clock branches are not used.

Timing Characteristics (continued)

Table 15. General-Purpose Clock Timing Characteristics (Internally Generated Clock)

OR3LxxB Commercial: V_{DD} = 3.0 V to 3.6 V, V_{DD2} = 2.38 V to 2.63 V, 0 °C < T_A < 70 °C; Industrial: V_{DD} = 3.0 V to 3.6 V, V_{DD2} = 2.38 V to 2.63 V, –40 °C < T_A < +85 °C.

Symbol	Device (T_J = 85 °C, V_{DD} = min, V_{DD2} = min)	-7		-8		Unit
		Min	Max	Min	Max	
CLK_DEL	OR3L165	—	4.56	—	3.98	ns
CLK_DEL	OR3L225	—	4.58	—	3.99	ns

Notes:

This table represents the delay for an internally generated clock from the clock tree input in one of the four middle PICs (using pSW routing) on any side of the device which is then distributed to the PFU/PIO clock inputs. If the clock tree input used is located at any other PIC, see the results reported by *ORCA* Foundry.

This clock delay is for a fully routed clock tree that uses the general clock network. The delay will be reduced if any of the clock branches are not used. See pin-to-pin timing in Table 18 for clock delays of clocks input on general I/O pins.

Timing Characteristics (continued)

Table 16. OR3Lxxx ExpressCLK to Output Delay (Pin-to-Pin)

OR3LxxB Commercial: V_{DD} = 3.0 V to 3.6 V, V_{DD2} = 2.38 V to 2.63 V, 0 °C < T_A < 70 °C; Industrial: V_{DD} = 3.0 V to 3.6 V, V_{DD2} = 2.38 V to 2.63 V, –40 °C < T_A < +85 °C.

Description (T_J = 85 °C, V_{DD} = min, V_{DD2} = min)	Device	-7		-8		Unit
		Min	Max	Min	Max	
ECLK Middle Input Pin→OUTPUT Pin (Fast)	OR3L165 OR3L225	— —	6.94 6.99	— —	5.84 5.89	ns ns
ECLK Middle Input Pin→OUTPUT Pin (Slewlim)	OR3L165 OR3L225	— —	7.79 7.84	— —	6.64 6.69	ns ns
ECLK Middle Input Pin→OUTPUT Pin (Sinklim)	OR3L165 OR3L225	— —	12.91 12.96	— —	11.08 11.13	ns ns
Additional Delay if ECLK Corner Pin Used	OR3L165 OR3L225	— —	2.70 2.90	— —	2.21 2.38	ns ns

Notes:

Timing is without the use of the PCM.

This clock delay is for a fully routed clock tree that uses the ExpressCLK network. It includes both the input buffer delay, the clock routing to the PIO CLK input, the clock→Q of the FF, and the delay through the output buffer. The given timing requires that the input clock pin be located at one of the six ExpressCLK inputs of the device, and that a PIO FF be used.

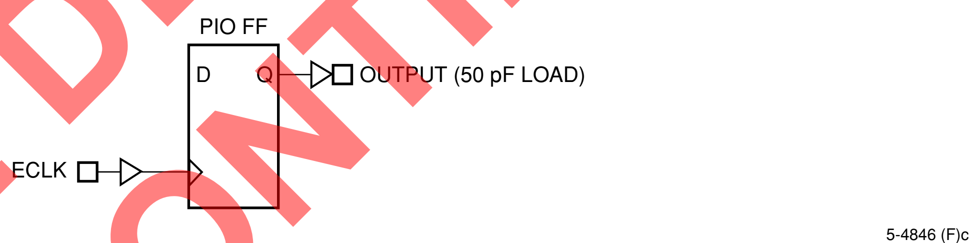


Figure 6. ExpressCLK to Output Delay

Timing Characteristics (continued)

Table 17. OR3Lxxx Fast Clock (FCLK) to Output Delay (Pin-to-Pin)

OR3LxxB Commercial: V_{DD} = 3.0 V to 3.6 V, V_{DD2} = 2.38 V to 2.63 V, 0 °C < T_A < 70 °C; Industrial: V_{DD} = 3.0 V to 3.6 V, V_{DD2} = 2.38 V to 2.63 V, –40 °C < T_A < +85 °C.

Description (T_J = 85 °C, V_{DD} = min, V_{DD2} = min)	Device	-7		-8		Unit
		Min	Max	Min	Max	
Output Not on Same Side of Device as Input Clock (Fast Clock Delays Using ExpressCLK Inputs)						
ECLK Middle Input Pin →OUTPUT Pin (Fast)	OR3L165 OR3L225	— —	10.37 10.66	— —	8.89 9.17	ns ns
ECLK Middle Input Pin →OUTPUT Pin (Slewlim)	OR3L165 OR3L225	— —	11.22 11.54	— —	9.69 9.97	ns ns
ECLK Middle Input Pin →OUTPUT Pin (Sinklim)	OR3L165 OR3L225	— —	16.33 16.63	— —	14.13 14.41	ns ns
Additional Delay if ECLK Corner Pin Used	OR3L165 OR3L225	— —	2.66 2.85	— —	2.17 2.33	ns ns

Notes:

Timing is without the use of the PCM.

This clock delay is for a fully routed clock tree that uses the primary clock network. It includes both the input buffer delay, the clock routing to the PIO CLK input, the clock→Q of the FF, and the delay through the output buffer. The delay will be reduced if any of the clock branches are not used. The given timing requires that the input clock pin be located at one of the six ExpressCLK inputs of the device and that a PIO FF be used.

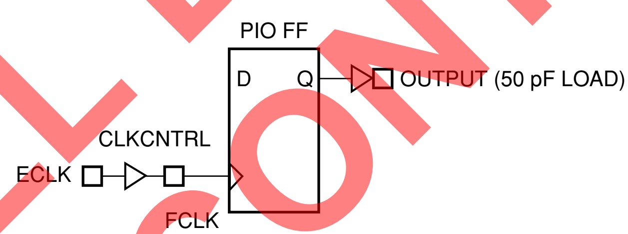


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Figure 7. Fast Clock to Output Delay

Timing Characteristics (continued)

Table 18. OR3Lxxx General System Clock (SCLK) to Output Delay (Pin-to-Pin)

OR3LxxB Commercial: V_{DD} = 3.0 V to 3.6 V, V_{DD2} = 2.38 V to 2.63 V, 0 °C < T_A < 70 °C; Industrial: V_{DD} = 3.0 V to 3.6 V, V_{DD2} = 2.38 V to 2.63 V, –40 °C < T_A < +85 °C.

Description (T_J = 85 °C, V_{DD} = min, V_{DD2} = min)	Device	-7		-8		Unit
		Min	Max	Min	Max	
Output On Same Side of Device As Input Clock (System Clock Delays Using General User I/O Inputs)						
Clock Input Pin (mid-PIC) →OUTPUT Pin (Fast)	OR3L165 OR3L225	— —	11.81 12.32	— —	10.06 10.54	ns ns
Clock Input Pin (mid-PIC) →OUTPUT Pin (Slewlim)	OR3L165 OR3L225	— —	12.66 13.16	— —	11.85 11.34	ns ns
Clock Input Pin (mid-PIC) →OUTPUT Pin (Sinklim)	OR3L165 OR3L225	— —	17.78 18.28	— —	15.29 15.78	ns ns
Additional Delay if Non-mid-PIC Used as Clock Pin	OR3L165 OR3L225	— —	1.04 1.43	— —	1.03 1.43	ns ns
Output Not on Same Side of Device As Input Clock (System Clock Delays Using General User I/O Inputs)						
Additional Delay if Output Not on Same Side as Input Clock Pin	OR3L165 OR3L225	— —	1.04 1.43	— —	1.03 1.43	ns ns

Note: This clock delay is for a fully routed clock tree that uses the primary clock network. It includes both the input buffer delay, the clock routing to the PIO CLK input, the clock→Q of the FF, and the delay through the output buffer. The delay will be reduced if any of the clock branches are not used. The given timing requires that the input clock pin be located at one of the four center PICs on any side of the device and that a PIO FF be used. For clock pins located at any other PIO, see the results reported by *ORCA* Foundry.

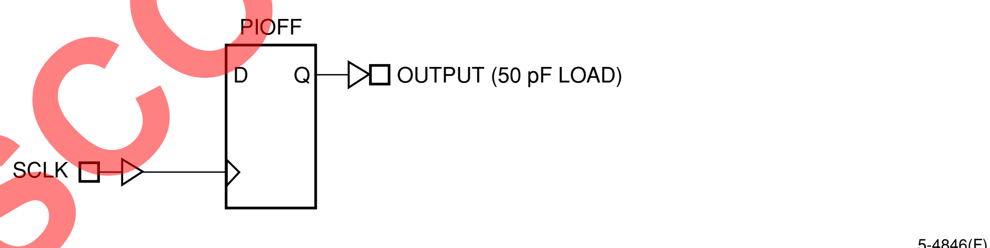

Figure 8. System Clock to Output Delay

Timing Characteristics (continued)

Table 19. OR3Lxxx Input to ExpressCLK (ECLK) Fast-Capture Setup/Hold Time (Pin-to-Pin)

OR3LxxB Commercial: V_{DD} = 3.0 V to 3.6 V, V_{DD2} = 2.38 V to 2.63 V, 0 °C < T_A < 70 °C; Industrial: V_{DD} = 3.0 V to 3.6 V, V_{DD2} = 2.38 V to 2.63 V, –40 °C < T_A < +85 °C.

Description (T_J = 85 °C, V_{DD} = min, V_{DD2} = min)	Device	-7		-8		Unit
		Min	Max	Min	Max	
Input to ECLK Setup Time (middle ECLK pin)	OR3L165 OR3L225	2.63 2.61	— —	0.96 0.95	— —	ns ns
Input to ECLK Setup Time (middle ECLK pin, delayed data input)	OR3L165 OR3L225	12.62 12.60	— —	9.97 9.96	— —	ns ns
Input to ECLK Setup Time (corner ECLK pin)	OR3L165 OR3L225	0.0 0.0	— —	0.0 0.0	— —	ns ns
Input to ECLK Setup Time (corner ECLK pin, delayed data input)	OR3L165 OR3L225	10.33 10.13	— —	8.09 7.93	— —	ns ns
Input to ECLK Hold Time (middle ECLK pin)	OR3L165 OR3L225	0.0 0.0	— —	0.0 0.0	— —	ns ns
Input to ECLK Hold Time (middle ECLK pin, delayed data input)	OR3L165 OR3L225	0.0 0.0	— —	0.0 0.0	— —	ns ns

Notes:

The pin-to-pin timing parameters in this table should be used instead of results reported by *ORCA* Foundry.

The ECLK delays are to all of the PIOs on one side of the device for middle pin input, or two sides of the device for corner pin input. The delay includes both the input buffer delay and the clock routing to the PIO clock input.

Timing Characteristics (continued)

Table 19. OR3Lxxx Input to ExpressCLK (ECLK) Fast-Capture Setup/Hold Time (Pin-to-Pin) (continued)

OR3LxxB Commercial: V_{DD} = 3.0 V to 3.6 V, V_{DD2} = 2.38 V to 2.63 V, 0 °C < T_A < 70 °C; Industrial: V_{DD} = 3.0 V to 3.6 V, V_{DD2} = 2.38 V to 2.63 V, –40 °C < T_A < +85 °C.

Description (T_J = 85 °C, V_{DD} = min, V_{DD2} = min)	Device	-7		-8		Unit
		Min	Max	Min	Max	
Input to ECLK Hold Time (corner ECLK pin)	OR3L165 OR3L225	0.0 0.0	— —	0.0 0.0	— —	ns ns
Input to ECLK Hold Time (corner ECLK pin, delayed data input)	OR3L165 OR3L225	0.0 0.0	— —	0.0 0.0	— —	ns ns

Notes:

The pin-to-pin timing parameters in this table should be used instead of results reported by *ORCA* Foundry.

The ECLK delays are to all of the PIOs on one side of the device for middle pin input, or two sides of the device for corner pin input. The delay includes both the input buffer delay and the clock routing to the PIO clock input.

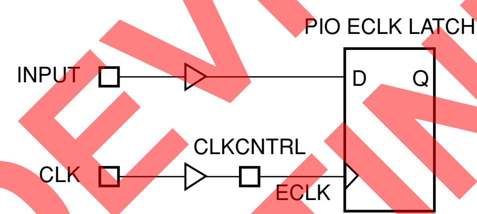

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Figure 9. Input to ExpressCLK Setup/Hold Time

Timing Characteristics (continued)

Table 20. OR3Lxxx Input to Fast Clock Setup/Hold Time (Pin-to-Pin)

OR3LxxB Commercial: V_{DD} = 3.0 V to 3.6 V, V_{DD2} = 2.38 V to 2.63 V, 0 °C < T_A < 70 °C; Industrial: V_{DD} = 3.0 V to 3.6 V, V_{DD2} = 2.38 V to 2.63 V, –40 °C < T_A < +85 °C.

Description (T_J = 85 °C, V_{DD} = min, V_{DD2} = min)	**Device**	**-7**		**-8**		**Unit**
		Min	**Max**	**Min**	**Max**	
Output Not on Same Side of Device As Input Clock (Fast Clock Delays Using ExpressCLK Inputs)						
Input to FCLK Setup Time (middle ECLK pin)	OR3L165 OR3L225	0.0 0.0	— —	0.0 0.0	— —	ns ns
Input to FCLK Setup Time (middle ECLK pin, delayed data input)	OR3L165 OR3L225	6.39 6.37	— —	5.56 5.55	— —	ns ns
Input to FCLK Setup Time (corner ECLK pin)	OR3L165 OR3L225	0.0 0.0	— —	0.0 0.0	— —	ns ns
Input to FCLK Setup Time (corner ECLK pin, delayed data input)	OR3L165 OR3L225	4.17 3.97	— —	3.76 3.58	— —	ns ns
Input to FCLK Hold Time (middle ECLK pin)	OR3L165 OR3L225	4.93 5.22	— —	4.44 4.72	— —	ns ns

Notes:

The pin-to-pin timing parameters in this table should be used instead of results reported by *ORCA* Foundry.

The FCLK delays are for a fully routed clock tree that uses the ExpressCLK input into the fast clock network. It includes both the input buffer delay and the clock routing to the PFU CLK input. The delay will be reduced if any of the clock branches are not used.

Timing Characteristics (continued)

Table 20. OR3Lxxx Input to Fast Clock Setup/Hold Time (Pin-to-Pin) (continued)

OR3LxxB Commercial: V_{DD} = 3.0 V to 3.6 V, V_{DD2} = 2.38 V to 2.63 V, 0 °C < T_A < 70 °C; Industrial: V_{DD} = 3.0 V to 3.6 V, V_{DD2} = 2.38 V to 2.63 V, –40 °C < T_A < +85 °C.

Description (T_J = 85 °C, V_{DD} = min, V_{DD2} = min)	Device	-7		-8		Unit
		Min	Max	Min	Max	
Input to FCLK Hold Time (middle ECLK pin, delayed data input)	OR3L165 OR3L225	0.0 0.0	— —	0.0 0.0	— —	ns ns
Input to FCLK Hold Time (corner ECLK pin)	OR3L165 OR3L225	7.59 8.08	— —	6.61 7.06	— —	ns ns
Input to FCLK Hold Time (corner ECLK pin, delayed data input)	OR3L165 OR3L225	0.0 0.0	— —	0.0 0.0	— —	ns ns

Notes:

The pin-to-pin timing parameters in this table should be used instead of results reported by *ORCA* Foundry.

The FCLK delays are for a fully routed clock tree that uses the ExpressCLK input into the fast clock network. It includes both the input buffer delay and the clock routing to the PFU CLK input. The delay will be reduced if any of the clock branches are not used.

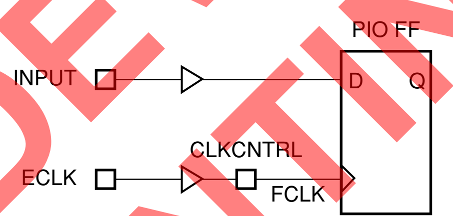

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Figure 10. Input to Fast Clock Setup/Hold Time

Timing Characteristics (continued)

Table 21. OR3Lxxx Input to General System Clock (SCLK) Setup/Hold Time (Pin-to-Pin)

OR3LxxB Commercial: V_{DD} = 3.0 V to 3.6 V, V_{DD2} = 2.38 V to 2.63 V, 0 °C < T_A < 70 °C; Industrial: V_{DD} = 3.0 V to 3.6 V, V_{DD2} = 2.38 V to 2.63 V, –40 °C < T_A < +85 °C.

Description (T_J = 85 °C, V_{DD} = min, V_{DD2} = min)	Device	-7		-8		Unit
		Min	Max	Min	Max	
Input to SCLK Setup Time	OR3L165 OR3L225	0.0 0.0	— —	0.0 0.0	— —	ns ns
Input to SCLK Setup Time (delayed data input)	OR3L165 OR3L225	5.69 5.57	— —	5.07 4.96	— —	ns ns
Input to SCLK Hold Time	OR3L165 OR3L225	6.46 6.96	— —	5.67 6.16	— —	ns ns
Input to SCLK Hold Time (delayed data input)	OR3L165 OR3L225	0.0 0.0	— —	0.0 0.0	— —	ns ns
Additional Hold Time if Non-mid-PIC Used as SCLK Pin (no delay on data input)	OR3L165 OR3L225	1.04 1.43	— —	1.03 1.43	— —	ns ns

Notes:

The pin-to-pin timing parameters in this table should be used instead of results reported by *ORCA* Foundry.

This clock delay is for a fully routed clock tree that uses the clock network. It includes both the input buffer delay and the clock routing to the PIO FF CLK input. The delay will be reduced if any of the clock branches are not used. The given setup (delayed and no delay) and hold (delayed) timing allows the input clock pin to be located in any PIO on any side of the device, but a PIO FF must be used. The hold (no delay) timing assumes the clock pin is located at one of the four middle PICs on any side of the device and that a PIO FF is used. If the clock pin is located elsewhere, then the last parameter in the table must be added to the hold (no delay) timing.

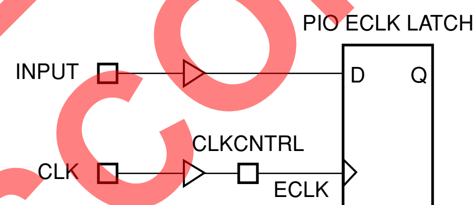

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Figure 11. Input to System Clock Setup/Hold Time

Timing Characteristics (continued)

Description

To define speed grades, the *ORCA* Series part number designation (see Ordering Information) uses a single-digit number to designate a speed grade. This number is not related to any single ac parameter. Higher numbers indicate a faster set of timing parameters. The actual speed sorting is based on testing the delay in a path consisting of an input buffer, combinatorial delay through all PLCs in a row, and an output buffer. Other tests are then done to verify other delay parameters, such as routing delays, setup times to FFs, etc.

The most accurate timing characteristics are reported by the timing analyzer in the *ORCA* Foundry Development System. A timing report provided by the development system after layout divides path delays into logic and routing delays. The timing analyzer can also provide logic delays prior to layout. While this allows routing budget estimates, there is wide variance in routing delays associated with different layouts.

The logic timing parameters noted in the Electrical Characteristics section of this data sheet are the same as those in the design tools. In the PFU timing, symbol names are generally a concatenation of the PFU operating mode and the parameter type. The setup, hold, and propagation delay parameters, defined below, are designated in the symbol name by the SET, HLD, and DEL characters, respectively.

The values given for the parameters are the same as those used during production testing and speed binning of the devices. The junction temperature and supply voltage used to characterize the devices are listed in the delay tables. Actual delays at nominal temperature and voltage for best-case processes can be much better than the values given.

It should be noted that the junction temperature used in the tables is generally 85 °C. The junction temperature for the FPGA depends on the power dissipated by the device, the package thermal characteristics (Θ_{JA}), and the ambient temperature, as calculated in the following equation and as discussed further in the Package Thermal Characteristics section:

$$T_{Jmax} = T_{Amax} + (P \cdot \Theta_{JA})\ °C$$

Note: The user must determine this junction temperature to see if the delays from *ORCA* Foundry should be derated based on the following derating tables.

Table 22 and Table 23 provide approximate power supply and junction temperature derating for OR3Lxxx commercial and industrial devices. The delay values in this data sheet and reported by *ORCA* Foundry are shown as 1.00 in the tables. The method for determining the maximum junction temperature is defined in the Package Thermal Characteristics section. Taken cumulatively, the range of parameter values for best-case vs. worst-case processing, supply voltage, and junction temperature can approach three to one.

Timing Characteristics (continued)

Table 22. Derating for Commercial/Industrial OR3Lxxx Devices (I/O Supply VDD)

T_J (°C)	Power Supply Voltage		
	3.0 V	**3.3 V**	**3.6 V**
–40	0.82	0.72	0.66
0	0.91	0.80	0.72
25	0.98	0.85	0.77
85	1.00	0.99	0.90
100	1.23	1.07	0.94
125	1.34	1.15	1.01

Table 23. Derating for Commercial/Industrial OR3Lxxx Devices (I/O Supply VDD2)

T_J (°C)	Power Supply Voltage		
	2.3 V	**2.5 V**	**2.6 V**
–40	0.86	0.71	0.67
0	0.94	0.79	0.73
25	0.99	0.84	0.77
85	1.00	0.99	0.92
100	1.23	1.05	0.96
125	1.33	1.13	1.03

Note: The derating tables shown above are for a typical critical path that contains 33% logic delay and 66% routing delay. Since the routing delay derates at a higher rate than the logic delay, paths with more than 66% routing delay will derate at a higher rate than shown in the table. The approximate derating values vs. temperature are 0.26% per °C for logic delay and 0.45% per °C for routing delay. The approximate derating values vs. voltage are 0.13% per mV for both logic and routing delays at 25 °C.

In addition to supply voltage, process variation, and operating temperature, circuit and process improvements of the *ORCA* Series FPGAs over time will result in significant improvement of the actual performance over those listed for a speed grade. Even though lower speed grades may still be available, the distribution of yield to timing parameters may be several speed grades higher than that designated on a product brand. Design practices need to consider best-case timing parameters (e.g., delays = 0), as well as worst-case timing.

The routing delays are a function of fan-out and the capacitance associated with the CIPs and metal interconnect in the path. The number of logic elements that can be driven (fan-out) by PFUs is unlimited, although the delay to reach a valid logic level can exceed timing requirements. It is difficult to make accurate routing delay estimates prior to design compilation based on fan-out. This is because the CAE software may delete redundant logic inserted by the designer to reduce fan-out, and/or it may also automatically reduce fan-out by net splitting.

Estimating Power Dissipation

OR3LxxxB

The total operating power dissipated is estimated by adding the standby (I_{DDSB}), internal, and external power dissipated. The internal and external power is the power consumed in the PLCs and PICs, respectively. In general, the standby power is small and may be neglected. The total operating power is as follows:

$$P_T = \Sigma\, P_{PLC} + \Sigma\, P_{PIC}$$

The internal operating power is made up of two parts: clock generation and PFU output power. The PFU output power can be estimated based upon the number of PFU outputs switching when driving an average fan-out of two:

$$P_{PFU} = 0.078 \text{ mW/MHz}$$

For each PFU output that switches, 0.136 mW/MHz needs to be multiplied times the frequency (in MHz) that the output switches. Generally, this can be estimated by using one-half the clock rate, multiplied by some activity factor; for example, 20%.

The power dissipated by the clock generation circuitry is based upon four parts: the fixed clock power, the power/clock branch row or column, the clock power dissipated in each PFU that uses this particular clock, and the power from the subset of those PFUs that are configured as synchronous memory. Therefore, the clock power can be calculated for the four parts using the following equations.

OR3L165B Clock Power

P = [0.039 mW/MHz
+ (0.046 mW/MHz/Branch) (# Branches)
+ (0.008 mW/MHz/PFU) (# PFUs)
+ (0.002 mW/MHz/PIO (# PIOs)]

For a quick estimate, the worst-case (typical circuit) OR3L165B clock power = 9.8 mW/MHz

OR3L225B Clock Power

P = [0.045 mW/MHz
+ (0.053 mW/MHz/Branch) (# Branches)
+ (0.008 mW/MHz/PFU) (# PFUs)
+ (0.002 mW/MHz/PIO (# PIOs)]

For a quick estimate, the worst-case (typical circuit) OR3L225B clock power = 13.5 mW/MHz

The power dissipated in a PIC is the sum of the power dissipated in the four PIOs in the PIC. This consists of power dissipated by inputs and ac power dissipated by outputs. The power dissipated in each PIO depends on whether it is configured as an input, output, or input/output. If a PIO is operating as an output, then there is a power dissipation component for P_{IN}, as well as P_{OUT}. This is because the output feeds back to the input.

The power dissipated by an input buffer is ($V_{IH} = V_{DD} - 0.3$ V or higher) estimated as:

$$P_{IN} = 0.09 \text{ mW/MHz}$$

The ac power dissipation from an output or bidirectional is estimated by the following:

$$P_{OUT} = (C_L + 8.8 \text{ pF}) \times V_{DD}^2 \times F \text{ Watts}$$

where the unit for C_L is farads, and the unit for F is Hz.

Pin Information

Table 24. 208-Pin SQFP2 Pinout

Pin	OR3L165B	Function
1	VSS	VSS
2	VSS	VSS
3	PL1D	I/O
4	PL3D	I/O-A0/MPI_BE0
5	VDD2	VDD2
6	PL6D	I/O
7	PL8D	I/O-A1/MPI_BE1
8	PL9A	I/O-A2
9	PL10D	I/O
10	PL10B	I/O
11	PL10A	I/O-A3
12	VDD	VDD
13	PL11D	I/O
14	PL11A	I/O
15	PL12D	I/O
16	PL12A	I/O-A4
17	PL13D	I/O-A5
18	PL13A	I/O
19	PL14D	I/O
20	PL14A	I/O-A6
21	VSS	VSS
22	PECKL	I/O-ECKL
23	PL15A	I/O
24	PL16C	I/O
25	PL16A	I/O-A7/MPI_CLK
26	VDD	VDD
27	PL17D	I/O
28	VDD2	VDD2
29	PL18C	I/O
30	PL18A	I/O-A8/MPI_RW
31	VSS	VSS
32	PL19D	I/O-A9/MPI_ACK
33	PL19A	I/O
34	PL20D	I/O
35	PL20A	I/O-A10/MPI_BI
36	PL21D	I/O
37	PL21A	I/O
38	PL22D	I/O
39	PL22A	I/O-A11/MPI_IRQ
40	VDD	VDD
41	PL23D	I/O-A12
42	PL23B	I/O
43	PL24D	I/O
44	PL24B	I/O-A13
45	PL25D	I/O
46	PL27A	I/O-A14
47	PL29D	I/O
48	PL30D	I/O
49	PL30A	I/O-SECKLL
50	PL32A	I/O-A15
51	VSS	VSS
52	PCCLK	CCLK
53	VSS	VSS
54	VSS	VSS
55	PB1A	I/O-A16
56	PB3A	I/O
57	VDD2	VDD2
58	PB4D	I/O
59	PB5D	I/O-A17
60	PB6D	I/O
61	PB7D	I/O
62	PB8D	I/O
63	PB9D	I/O
64	PB10D	I/O
65	VDD	VDD
66	PB11A	I/O
67	PB11D	I/O
68	PB12A	I/O
69	PB12D	I/O
70	PB13A	I/O
71	PB13D	I/O
72	PB14A	I/O
73	PB14D	I/O
74	VSS	VSS
75	PB15A	I/O
76	PB15D	I/O
77	PB16B	I/O
78	PB16D	I/O
79	VSS	VSS
80	PECKB	I/O-ECKB
81	PB17D	I/O
82	PB18B	I/O
83	PB18D	I/O
84	VSS	VSS

Pin Information (continued)

Table 24. 208-Pin SQFP2 Pinout (continued)

Pin	OR3L165B	Function	Pin	OR3L165B	Function
85	VDD2	VDD2	127	PR18D	I/O
86	PB19D	I/O	128	PR17B	I/O
87	PB20A	I/O	129	PR17D	I/O
88	PB20D	I/O	130	VDD	VDD
89	PB21A	I/O-HDC	131	PECKR	I/O-ECKR
90	PB21D	I/O	132	PR16D	I/O
91	PB22A	I/O	133	PR15B	I/O
92	PB22D	I/O	134	PR15D	I/O
93	VDD	VDD	135	VSS	VSS
94	PB23A	I/O-$\overline{\text{LDC}}$	136	VDD2	VDD2
95	PB24D	I/O	137	PR14D	I/O
96	PB25A	I/O	138	PR13A	I/O
97	PB26D	I/O	139	PR13D	I/O
98	PB27A	I/O-$\overline{\text{INIT}}$	140	PR12A	I/O-CS1
99	PB28A	I/O	141	PR12D	I/O
100	PB29A	I/O	142	PR11A	I/O
101	PB30D	I/O	143	PR11D	I/O
102	PB32D	I/O	144	VDD	VDD
103	VSS	VSS	145	PR10A	I/O-$\overline{\text{CS0}}$
104	PDONE	DONE	146	PR10B	I/O
105	VSS	VSS	147	PR9B	I/O
106	PRESETN	$\overline{\text{RESET}}$	148	PR9D	I/O
107	PPRGMN	$\overline{\text{PRGM}}$	149	PR8A	I/O-$\overline{\text{RD}}$/$\overline{\text{MPI\_STRB}}$
108	PR32A	I/O-M0	150	PR6A	I/O
109	PR30A	I/O	151	PR5A	I/O
110	PR29A	I/O	152	PR4A	I/O-$\overline{\text{WR}}$
111	PR28A	I/O	153	PR3A	I/O
112	PR25D	I/O-M1	154	PR2A	I/O
113	PR24A	I/O	155	VSS	VSS
114	VDD2	VDD2	156	PRD_CFGN	$\overline{\text{RD\_CFG}}$
115	PR23A	I/O	157	VSS	VSS
116	VDD	VDD	158	VSS	VSS
117	PR22A	I/O-M2	159	PT32D	I/O-SECKUR
118	PR22D	I/O	160	PT30A	I/O-RDY/RCLK/MPI_ALE
119	PR21A	I/O	161	PT28D	I/O
120	PR21D	I/O	162	PT28A	I/O
121	PR20A	I/O-M3	163	PT27D	I/O-D7
122	PR20D	I/O	164	VDD2	VDD2
123	PR19A	I/O	165	PT25D	I/O
124	PR19D	I/O	166	PT24D	I/O
125	VSS	VSS	167	PT23D	I/O-D6
126	PR18A	I/O	168	VDD	VDD

Pin Information (continued)

Table 24. 208-Pin SQFP2 Pinout (continued)

Pin	OR3L165B	Function	Pin	OR3L165B	Function
169	PT22D	I/O	189	PT14A	I/O
170	PT22A	I/O	190	PT13D	I/O
171	PT21D	I/O	191	PT13A	I/O-D0/DIN
172	PT21A	I/O-D5	192	PT12D	I/O
173	PT20D	I/O	193	PT12A	I/O
174	PT20A	I/O	194	PT11D	I/O
175	PT19D	I/O	195	PT11A	I/O-DOUT
176	PT19A	I/O-D4	196	VDD	VDD
177	VSS	VSS	197	PT10D	I/O
178	PECKT	I/O-ECKT	198	PT9A	I/O
179	PT18B	I/O	199	PT8A	I/O
180	PT17D	I/O	200	PT7A	I/O-TDI
181	PT17A	I/O-D3	201	PT6A	I/O
182	VSS	VSS	202	PT5A	I/O-TMS
183	PT16D	I/O	203	PT4A	I/O
184	PT16C	I/O	204	PT3A	I/O
185	VDD2	VDD2	205	PT2D	I/O
186	PT15A	I/O-D2	206	PT1A	I/O-TCK
187	VSS	VSS	207	VSS	VSS
188	PT14D	I/O-D1	208	PRD_DATA	RD_DATA/TDO

Pin Information (continued)

Table 25. 240-Pin SQFP2 Pinout

Pin	OR3L165B	Function	Pin	OR3L165B	Function
1	VSS	VSS	42	PL22D	I/O
2	VDD	VDD	43	PL22A	I/O-A11/$\overline{\text{MPI\_IRQ}}$
3	PL1D	I/O	44	VDD	VDD
4	PL1A	I/O	45	PL23D	I/O-A12
5	PL2D	I/O	46	PL23B	I/O
6	PL3D	I/O-A0/$\overline{\text{MPI\_BE0}}$	47	PL24D	I/O
7	VSS	VSS	48	PL24B	I/O-A13
8	VDD2	VDD2	49	PL24A	I/O
9	PL6D	I/O	50	PL25D	I/O
10	PL7D	I/O	51	PL26D	I/O
11	PL8D	I/O-A1/$\overline{\text{MPI\_BE1}}$	52	PL27A	I/O-A14
12	PL9A	I/O-A2	53	VSS	VSS
13	PL10D	I/O	54	PL29D	I/O
14	PL10B	I/O	55	PL30D	I/O
15	PL10A	I/O-A3	56	PL30A	I/O-SECKLL
16	VDD	VDD	57	PL32A	I/O-A15
17	PL11D	I/O	58	VSS	VSS
18	PL11A	I/O	59	PCCLK	CCLK
19	PL12D	I/O	60	VDD	VDD
20	PL12A	I/O-A4	61	VSS	VSS
21	PL13D	I/O-A5	62	VSS	VSS
22	PL13A	I/O	63	PB1A	I/O-A16
23	PL14D	I/O	64	PB3A	I/O
24	PL14A	I/O-A6	65	VDD2	VDD2
25	VSS	VSS	66	PB4D	I/O
26	PECKL	I/O-ECKL	67	VSS	VSS
27	PL15A	I/O	68	PB5D	I/O-A17
28	PL16C	I/O	69	PB6D	I/O
29	PL16A	I/O-A7/MPI_CLK	70	PB7A	I/O
30	VDD	VDD	71	PB7D	I/O
31	PL17D	I/O	72	PB8D	I/O
32	VDD2	VDD2	73	PB9A	I/O
33	PL18C	I/O	74	PB9D	I/O
34	PL18A	I/O-A8/MPI_RW	75	PB10D	I/O
35	VSS	VSS	76	VDD	VDD
36	PL19D	I/O-A9/MPI_ACK	77	PB11A	I/O
37	PL19A	I/O	78	PB11D	I/O
38	PL20D	I/O	79	PB12A	I/O
39	PL20A	I/O-A10/MPI_BI	80	PB12D	I/O
40	PL21D	I/O	81	PB13A	I/O
41	PL21A	I/O	82	PB13D	I/O

Pin Information (continued)

Table 25. 240-Pin SQFP2 Pinout (continued)

Pin	OR3L165B	Function
83	PB14A	I/O
84	PB14D	I/O
85	VSS	VSS
86	PB15A	I/O
87	PB15D	I/O
88	PB16B	I/O
89	PB16D	I/O
90	VSS	VSS
91	PECKB	I/O-ECKB
92	PB17D	I/O
93	PB18B	I/O
94	PB18D	I/O
95	VSS	VSS
96	VDD2	VDD2
97	PB19D	I/O
98	PB20A	I/O
99	PB20D	I/O
100	PB21A	I/O-HDC
101	PB21D	I/O
102	PB22A	I/O
103	PB22D	I/O
104	VDD	VDD
105	PB23A	I/O-$\overline{LDC}$
106	PB24D	I/O
107	PB25A	I/O
108	PB26D	I/O
109	PB27A	I/O-$\overline{INIT}$
110	PB27D	I/O
111	PB28A	I/O
112	PB28D	I/O
113	VSS	VSS
114	PB29A	I/O
115	PB30A	I/O
116	PB30D	I/O
117	PB32D	I/O
118	VSS	VSS
119	PDONE	DONE
120	VDD	VDD
121	VSS	VSS
122	PRESETN	$\overline{RESET}$
123	PPRGMN	$\overline{PRGM}$
124	PR32A	I/O-M0
125	PR31D	I/O
126	PR30A	I/O
127	PR29A	I/O
128	VSS	VSS
129	PR28A	I/O
130	PR27A	I/O
131	PR26A	I/O
132	PR26D	I/O
133	PR25D	I/O-M1
134	PR24A	I/O
135	VDD2	VDD2
136	PR23A	I/O
137	VDD	VDD
138	PR22A	I/O-M2
139	PR22D	I/O
140	PR21A	I/O
141	PR21D	I/O
142	PR20A	I/O-M3
143	PR20D	I/O
144	PR19A	I/O
145	PR19D	I/O
146	VSS	VSS
147	PR18A	I/O
148	PR18D	I/O
149	PR17B	I/O
150	PR17D	I/O
151	VDD	VDD
152	PECKR	I/O-ECKR
153	PR16D	I/O
154	PR15B	I/O
155	PR15D	I/O
156	VSS	VSS
157	VDD2	VDD2
158	PR14D	I/O
159	PR13A	I/O
160	PR13D	I/O
161	PR12A	I/O-CS1
162	PR12D	I/O
163	PR11A	I/O
164	PR11D	I/O
165	VDD	VDD
166	PR10A	I/O-$\overline{CS0}$

Pin Information (continued)

Table 25. 240-Pin SQFP2 Pinout (continued)

Pin	OR3L165B	Function
167	PR10B	I/O
168	PR9B	I/O
169	PR9D	I/O
170	PR8A	I/O-RD/MPI_STRB
171	PR7A	I/O
172	PR6A	I/O
173	PR5A	I/O
174	VSS	VSS
175	PR4A	I/O-WR
176	PR3A	I/O
177	PR2A	I/O
178	PR1D	I/O
179	VSS	VSS
180	PRD_CFGN	RD_CFG
181	VSS	VSS
182	VDD	VDD
183	VSS	VSS
184	PT32D	I/O-SECKUR
185	PT31A	I/O
186	PT30D	I/O
187	PT30A	I/O-RDY/RCLK/MPI_ALE
188	VSS	VSS
189	PT28D	I/O
190	PT28C	I/O
191	PT28A	I/O
192	PT27D	I/O-D7
193	VDD2	VDD2
194	PT25D	I/O
195	PT24D	I/O
196	PT23D	I/O-D6
197	VDD	VDD
198	PT22D	I/O
199	PT22A	I/O
200	PT21D	I/O
201	PT21A	I/O-D5
202	PT20D	I/O
203	PT20A	I/O
204	PT19D	I/O
205	PT19A	I/O-D4
206	VSS	VSS
207	PECKT	I/O-ECKT
208	PT18B	I/O
209	PT17D	I/O
210	PT17A	I/O-D3
211	VSS	VSS
212	PT16D	I/O
213	PT16C	I/O
214	VDD2	VDD2
215	PT15A	I/O-D2
216	VSS	VSS
217	PT14D	I/O-D1
218	PT14A	I/O
219	PT13D	I/O
220	PT13A	I/O-D0/DIN
221	PT12D	I/O
222	PT12A	I/O
223	PT11D	I/O
224	PT11A	I/O-DOUT
225	VDD	VDD
226	PT10D	I/O
227	PT9A	I/O
228	PT8A	I/O
229	PT7A	I/O-TDI
230	PT6D	I/O
231	PT6A	I/O
232	PT5D	I/O
233	PT5A	I/O-TMS
234	VSS	VSS
235	PT4A	I/O
236	PT3A	I/O
237	PT2D	I/O
238	PT1A	I/O-TCK
239	VSS	VSS
240	PRD_DATA	RD_DATA/TDO

Pin Information (continued)

Table 26. 352-Pin PBGA Pinout

Pin	OR3L165B	Function	Pin	OR3L165B	Function
B1	PL1D	I/O	P2	PL17D	I/O
C2	PL1A	I/O	P4	VDD2	VDD2
C1	PL2D	I/O	P1	PL18C	I/O
D2	PL2A	I/O	N3	PL18A	I/O-A8/MPI_RW
D3	PL3D	I/O-A0/MPI_BE0	R2	PL19D	I/O-A9/MPI_ACK
D1	PL3A	I/O	P3	PL19A	I/O
E2	PL4D	I/O	R1	PL20D	I/O
E4	PL4B	I/O	T2	PL20A	I/O-A10/MPI_BI
E3	PL4A	I/O	R3	PL21D	I/O
E1	VDD2	VDD2	T1	PL21A	I/O
F2	PL5C	I/O	R4	PL22D	I/O
G4	PL5B	I/O	U2	PL22A	I/O-A11/MPI_IRQ
F3	PL6D	I/O	T3	PL23D	I/O-A12
F1	PL7D	I/O	U1	PL23C	I/O
G2	PL7C	I/O	U4	PL23B	I/O
G1	PL7B	I/O	V2	PL23A	I/O
G3	PL8D	I/O-A1/MPI_BE1	U3	PL24D	I/O
H2	PL9D	I/O	V1	PL24C	I/O
J4	PL9C	I/O	W2	PL24B	I/O-A13
H1	PL9B	I/O	W1	PL24A	I/O
H3	PL9A	I/O-A2	V3	PL25D	I/O
J2	PL10D	I/O	Y2	PL25C	I/O
J1	PL10C	I/O	W4	PL26D	I/O
K2	PL10B	I/O	Y1	PL27D	I/O
J3	PL10A	I/O-A3	W3	PL27A	I/O-A14
K1	PL11D	I/O	AA2	PL28C	I/O
K4	PL11A	I/O	Y4	PL28B	I/O
L2	PL12D	I/O	AA1	PL28A	I/O
K3	PL12A	I/O-A4	Y3	VDD2	VDD2
L1	PL13D	I/O-A5	AB2	PL29C	I/O
M2	PL13A	I/O	AB1	PL29A	I/O
M1	PL14D	I/O	AA3	PL30D	I/O
L3	PL14A	I/O-A6	AC2	PL30C	I/O
N2	PECKL	I/O-ECKL	AB4	PL30A	I/O-SECKLL
M4	PL15A	I/O	AC1	PL31A	I/O
N1	PL16C	I/O	AB3	PL32C	I/O
M3	PL16A	I/O-A7/MPI_CLK	AD2	PL32B	I/O

Pin Information (continued)

Table 26. 352-Pin PBGA Pinout (continued)

Pin	OR3L165B	Function
AC3	PL32A	I/O-A15
AD1	PCCLK	CCLK
AF2	PB1A	I/O-A16
AE3	PB1B	I/O
AF3	PB2A	I/O
AE4	PB2D	I/O
AD4	PB3A	I/O
AF4	V_{DD2}	V_{DD2}
AE5	PB4A	I/O
AC5	PB4C	I/O
AD5	PB4D	I/O
AF5	PB5A	I/O
AE6	PB5B	I/O
AC7	PB5C	I/O
AD6	PB5D	I/O-A17
AF6	PB6A	I/O
AE7	PB6B	I/O
AF7	PB6C	I/O
AD7	PB6D	I/O
AE8	PB7A	I/O
AC9	PB7D	I/O
AF8	PB8A	I/O
AD8	PB8D	I/O
AE9	PB9A	I/O
AF9	PB9D	I/O
AE10	PB10A	I/O
AD9	PB10D	I/O
AF10	PB11A	I/O
AC10	PB11D	I/O
AE11	PB12A	I/O
AD10	PB12D	I/O
AF11	PB13A	I/O
AE12	PB13D	I/O
AF12	PB14A	I/O
AD11	PB14D	I/O
AE13	PB15A	I/O
AC12	PB15D	I/O
AF13	PB16B	I/O
AD12	PB16D	I/O

Pin	OR3L165B	Function
AE14	PECKB	I/O-ECKB
AC14	PB17D	I/O
AF14	PB18B	I/O
AD13	PB18D	I/O
AE15	V_{DD2}	V_{DD2}
AD14	PB19D	I/O
AF15	PB20A	I/O
AE16	PB20D	I/O
AD15	PB21A	I/O-HDC
AF16	PB21D	I/O
AC15	PB22A	I/O
AE17	PB22D	I/O
AD16	PB23A	I/O-$\overline{LDC}$
AF17	PB23D	I/O
AC17	PB24A	I/O
AE18	PB24D	I/O
AD17	PB25A	I/O
AF18	PB26A	I/O
AE19	PB26C	I/O
AF19	PB26D	I/O
AD18	PB27A	I/O-$\overline{INIT}$
AE20	PB27B	I/O
AC19	PB27C	I/O
AF20	PB27D	I/O
AD19	V_{DD2}	V_{DD2}
AE21	PB28B	I/O
AC20	PB28C	I/O
AF21	PB28D	I/O
AD20	PB29A	I/O
AE22	PB29B	I/O
AF22	PB29D	I/O
AD21	PB30A	I/O
AE23	PB30B	I/O
AC22	PB30D	I/O
AF23	PB31A	I/O
AD22	PB31D	I/O
AE24	PB32C	I/O
AD23	PB32D	I/O
AF24	PDONE	DONE

Pin Information (continued)

Table 26. 352-Pin PBGA Pinout (continued)

Pin	OR3L165B	Function	Pin	OR3L165B	Function
AE26	PRESETN	RESET	N26	PR16D	I/O
AD25	PPRGMN	PRGM	P24	PR15B	I/O
AD26	PR32A	I/O-M0	M25	PR15D	I/O
AC25	PR31A	I/O	N24	VDD2	VDD2
AC24	PR31D	I/O	M26	PR14D	I/O
AC26	PR30A	I/O	L25	PR13A	I/O
AB25	PR30D	I/O	M24	PR13D	I/O
AB23	PR29A	I/O	L26	PR12A	I/O-CS1
AB24	PR29B	I/O	M23	PR12D	I/O
AB26	PR29D	I/O	K25	PR11A	I/O
AA25	PR28A	I/O	L24	PR11D	I/O
Y23	PR28B	I/O	K26	PR10A	I/O-$\overline{\text{CS0}}$
AA24	PR28C	I/O	K23	PR10B	I/O
AA26	PR27A	I/O	J25	PR10C	I/O
Y25	PR26A	I/O	K24	PR10D	I/O
Y26	PR26B	I/O	J26	PR9A	I/O
Y24	PR26D	I/O	H25	PR9B	I/O
W25	PR25D	I/O-M1	H26	PR9C	I/O
V23	PR24A	I/O	J24	PR9D	I/O
W26	PR24B	I/O	G25	PR8A	I/O-$\overline{\text{RD}}$/$\overline{\text{MPI\_STRB}}$
W24	PR24C	I/O	H23	PR7A	I/O
V25	VDD2	VDD2	G26	PR7C	I/O
V26	PR23A	I/O	H24	PR6A	I/O
U25	PR23B	I/O	F25	VDD2	VDD2
V24	PR23C	I/O	G23	PR5B	I/O
U26	PR23D	I/O	F26	PR5C	I/O
U23	PR22A	I/O-M2	G24	PR5D	I/O
T25	PR22D	I/O	E25	PR4A	I/O-$\overline{\text{WR}}$
U24	PR21A	I/O	E26	PR4B	I/O
T26	PR21D	I/O	F24	PR4D	I/O
R25	PR20A	I/O-M3	D25	PR3A	I/O
R26	PR20D	I/O	E23	PR3D	I/O
T24	PR19A	I/O	D26	PR2A	I/O
P25	PR19D	I/O	E24	PR2D	I/O
R23	PR18A	I/O	C25	PR1A	I/O
P26	PR18D	I/O	D24	PR1D	I/O
R24	PR17B	I/O	C26	PRD_CFGN	RD_CFG
N25	PR17D	I/O	A25	PT32D	I/O-SECKUR
N23	PECKR	I/O-ECKR	B24	PT32A	I/O

Pin Information (continued)

Table 26. 352-Pin PBGA Pinout (continued)

Pin	OR3L165B	Function
A24	PT31B	I/O
B23	PT31A	I/O
C23	PT30D	I/O
A23	PT30A	I/O-RDY/RCLK/MPI_ALE
B22	PT29D	I/O
D22	PT29C	I/O
C22	PT29A	I/O
A22	PT28D	I/O
B21	PT28C	I/O
D20	PT28B	I/O
C21	PT28A	I/O
A21	PT27D	I/O-D7
B20	PT27C	I/O
A20	PT27B	I/O
C20	PT27A	I/O
B19	VDD2	VDD2
D18	PT26C	I/O
A19	PT26B	I/O
C19	PT25D	I/O
B18	PT24D	I/O
A18	PT24A	I/O
B17	PT23D	I/O-D6
C18	PT23A	I/O
A17	PT22D	I/O
D17	PT22A	I/O
B16	PT21D	I/O
C17	PT21A	I/O-D5
A16	PT20D	I/O
B15	PT20A	I/O
A15	PT19D	I/O
C16	PT19A	I/O-D4
B14	PECKT	I/O-ECKT
D15	PT18B	I/O
A14	PT17D	I/O
C15	PT17A	I/O-D3
B13	PT16D	I/O
D13	PT16C	I/O
A13	VDD2	VDD2
C14	PT15A	I/O-D2
B12	PT14D	I/O-D1
C13	PT14A	I/O
A12	PT13D	I/O
B11	PT13A	I/O-D0/DIN
C12	PT12D	I/O
A11	PT12A	I/O
D12	PT11D	I/O
B10	PT11A	I/O-DOUT
C11	PT10D	I/O
A10	PT10A	I/O
D10	PT9D	I/O
B9	PT9A	I/O
C10	PT8D	I/O
A9	PT8A	I/O
B8	PT7D	I/O
A8	PT7A	I/O-TDI
C9	PT6D	I/O
B7	PT6C	I/O
D8	PT6B	I/O
A7	VDD2	VDD2
C8	PT5D	I/O
B6	PT5C	I/O
D7	PT5B	I/O
A6	PT5A	I/O-TMS
C7	PT4D	I/O
B5	PT4A	I/O
A5	PT3D	I/O
C6	PT3C	I/O
B4	PT3B	I/O
D5	PT3A	I/O
A4	PT2D	I/O
C5	PT2A	I/O
B3	PT1D	I/O
C4	PT1A	I/O-TCK
A3	PRD_DATA	RD_DATA/TDO
A1	VSS	VSS
A2	VSS	VSS
A26	VSS	VSS
AC13	VSS	VSS

Pin Information (continued)

Table 26. 352-Pin PBGA Pinout (continued)

Pin	OR3L165B	Function
AC18	VSS	VSS
AC23	VSS	VSS
AC4	VSS	VSS
AC8	VSS	VSS
AD24	VSS	VSS
AD3	VSS	VSS
AE1	VSS	VSS
AE2	VSS	VSS
AE25	VSS	VSS
AF1	VSS	VSS
AF25	VSS	VSS
AF26	VSS	VSS
B2	VSS	VSS
B25	VSS	VSS
B26	VSS	VSS
C24	VSS	VSS
C3	VSS	VSS
D14	VSS	VSS
D19	VSS	VSS
D23	VSS	VSS
D4	VSS	VSS
D9	VSS	VSS
H4	VSS	VSS
J23	VSS	VSS
N4	VSS	VSS
P23	VSS	VSS
V4	VSS	VSS
W23	VSS	VSS
L11	VSS	VSS
L12	VSS	VSS
L13	VSS	VSS
L14	VSS	VSS
L15	VSS	VSS
L16	VSS	VSS
M11	VSS	VSS
M12	VSS	VSS
M13	VSS	VSS
M14	VSS	VSS
M15	VSS	VSS
M16	VSS	VSS

Pin	OR3L165B	Function
N11	VSS	VSS
N12	VSS	VSS
N13	VSS	VSS
N14	VSS	VSS
N15	VSS	VSS
N16	VSS	VSS
P11	VSS	VSS
P12	VSS	VSS
P13	VSS	VSS
P14	VSS	VSS
P15	VSS	VSS
P16	VSS	VSS
R11	VSS	VSS
R12	VSS	VSS
R13	VSS	VSS
R14	VSS	VSS
R15	VSS	VSS
R16	VSS	VSS
T11	VSS	VSS
T12	VSS	VSS
T13	VSS	VSS
T14	VSS	VSS
T15	VSS	VSS
T16	VSS	VSS
AA23	VDD	VDD
AA4	VDD	VDD
AC11	VDD	VDD
AC16	VDD	VDD
AC21	VDD	VDD
AC6	VDD	VDD
D11	VDD	VDD
D16	VDD	VDD
D21	VDD	VDD
D6	VDD	VDD
F23	VDD	VDD
F4	VDD	VDD
L23	VDD	VDD
L4	VDD	VDD
T23	VDD	VDD
T4	VDD	VDD

Pin Information (continued)

Table 27. 432-Pin EBGA Pinout

Pin	OR3L165B	OR3L225B	Function
E4	PRD_CFGN	PRD_CFGN	$\overline{\text{RD\_CFG}}$
D3	PR1D	PR1D	I/O
D2	PR1A	PR1A	I/O
D1	PR2D	PR2D	I/O
F4	PR2A	PR2A	I/O
E3	PR3D	PR3D	I/O
E2	PR3C	PR3C	I/O
E1	PR3B	PR3B	I/O
F3	PR3A	PR3A	I/O
F2	PR4D	PR4D	I/O
F1	PR4C	PR4C	I/O
H4	PR4B	PR4B	I/O
G3	PR4A	PR4A	I/O-$\overline{\text{WR}}$
G2	PR5D	PR5D	I/O
G1	PR5C	PR5C	I/O
J4	PR5B	PR5B	I/O
H3	VDD2	VDD2	VDD2
H2	PR6A	PR6A	I/O
J3	PR7C	PR7C	I/O
K4	PR7A	PR7A	I/O
J2	PR8A	PR8A	I/O-$\overline{\text{RD}}$/$\overline{\text{MPI\_STRB}}$
J1	PR9D	PR9D	I/O
K3	PR9C	PR9A	I/O
K2	PR9B	PR10D	I/O
K1	PR9A	PR10C	I/O
L3	PR10D	PR10A	I/O
M4	PR10C	PR11D	I/O
L2	PR10B	PR11C	I/O
L1	PR10A	PR11A	I/O-$\overline{\text{CS0}}$
M3	PR11D	PR12D	I/O
N4	PR11A	PR12A	I/O
M2	PR12D	PR13D	I/O
N3	PR12A	PR13A	I/O-CS1
N2	PR13D	PR14D	I/O
P4	PR13C	PR14A	I/O
N1	PR13A	PR15A	I/O
P3	PR14D	PR16D	I/O
P2	PR14C	PR16A	I/O
P1	VDD2	VDD2	VDD2
R3	PR15D	PR18D	I/O
R2	PR15B	PR18B	I/O

Pin Information (continued)

Table 27. 432-Pin EBGA Pinout (continued)

Pin	OR3L165B	OR3L225B	Function
R1	PR16D	PR19D	I/O
T2	PECKR	PECKR	I/O-ECKR
T4	PR17D	PR20D	I/O
T3	PR17B	PR20B	I/O
U1	PR18D	PR21D	I/O
U2	PR18A	PR21A	I/O
U3	PR19D	PR22D	I/O
V1	PR19B	PR23D	I/O
V2	PR19A	PR23A	I/O
V3	PR20D	PR24D	I/O
W1	PR20A	PR25A	I/O-M3
V4	PR21D	PR26D	I/O
W2	PR21B	PR26B	I/O
W3	PR21A	PR26A	I/O
Y2	PR22D	PR27D	I/O
W4	PR22A	PR27A	I/O-M2
Y3	PR23D	PR28D	I/O
AA1	PR23C	PR28C	I/O
AA2	PR23B	PR28B	I/O
Y4	PR23A	PR28A	I/O
AA3	VDD2	VDD2	VDD2
AB1	PR24C	PR29A	I/O
AB2	PR24B	PR30D	I/O
AB3	PR24A	PR30A	I/O
AC1	PR25D	PR31D	I/O-M1
AC2	PR26D	PR32D	I/O
AB4	PR26B	PR32B	I/O
AC3	PR26A	PR32A	I/O
AD2	PR27A	PR33A	I/O
AD3	PR28C	PR34C	I/O
AC4	PR28B	PR34B	I/O
AE1	PR28A	PR34A	I/O
AE2	PR29D	PR35D	I/O
AE3	PR29C	PR35C	I/O
AD4	PR29B	PR35B	I/O
AF1	PR29A	PR35A	I/O
AF2	PR30D	PR36D	I/O
AF3	PR30C	PR36C	I/O
AG1	PR30B	PR36B	I/O
AG2	VDD2	VDD2	VDD2
AG3	PR31D	PR37D	I/O

Pin Information (continued)

Table 27. 432-Pin EBGA Pinout (continued)

Pin	OR3L165B	OR3L225B	Function
AF4	PR31A	PR37A	I/O
AH1	PR32B	PR38B	I/O
AH2	PR32A	PR38A	I/O-M0
AH3	PPRGMN	PPRGMN	$\overline{\text{PRGM}}$
AG4	PRESETN	PRESETN	$\overline{\text{RESET}}$
AH5	PDONE	PDONE	DONE
AJ4	PB32D	PB38D	I/O
AK4	PB32C	PB38C	I/O
AL4	PB31D	PB37D	I/O
AH6	PB31A	PB37A	I/O
AJ5	PB30D	PB36D	I/O
AK5	PB30C	PB36C	I/O
AL5	PB30B	PB36B	I/O
AJ6	PB30A	PB36A	I/O
AK6	PB29D	PB35D	I/O
AL6	PB29C	PB35C	I/O
AH8	PB29B	PB35B	I/O
AJ7	PB29A	PB35A	I/O
AK7	PB28D	PB34D	I/O
AL7	PB28C	PB34C	I/O
AH9	PB28B	PB34B	I/O
AJ8	VDD2	VDD2	VDD2
AK8	PB27D	PB33D	I/O
AJ9	PB27C	PB33C	I/O
AH10	PB27B	PB33B	I/O
AK9	PB27A	PB33A	I/O-$\overline{\text{INIT}}$
AL9	PB26D	PB32D	I/O
AJ10	PB26C	PB32C	I/O
AK10	PB26A	PB32A	I/O
AL10	PB25A	PB31A	I/O
AJ11	PB24D	PB30D	I/O
AH12	PB24A	PB30A	I/O
AK11	PB23D	PB29D	I/O
AL11	PB23A	PB29A	I/O-$\overline{\text{LDC}}$
AJ12	PB22D	PB28D	I/O
AH13	PB22B	PB27D	I/O
AK12	PB22A	PB27A	I/O
AJ13	PB21D	PB26D	I/O
AK13	PB21B	PB25D	I/O
AH14	PB21A	PB25A	I/O-HDC
AL13	PB20D	PB24D	I/O

Pin Information (continued)

Table 27. 432-Pin EBGA Pinout (continued)

Pin	OR3L165B	OR3L225B	Function
AJ14	PB20B	PB24B	I/O
AK14	PB20A	PB24A	I/O
AL14	PB19D	PB23D	I/O
AJ15	VDD2	VDD2	VDD2
AK15	PB18D	PB22D	I/O
AL15	PB18B	PB21D	I/O
AK16	PB17D	PB20D	I/O
AH16	PECKB	PECKB	I/O-ECKB
AJ16	PB16D	PB19D	I/O
AL17	PB16B	PB18D	I/O
AK17	PB15D	PB17D	I/O
AJ17	PB15A	PB17A	I/O
AL18	PB14D	PB16D	I/O
AK18	PB14B	PB15D	I/O
AJ18	PB14A	PB15A	I/O
AL19	PB13D	PB14D	I/O
AH18	PB13A	PB13A	I/O
AK19	PB12D	PB12D	I/O
AJ19	PB12B	PB12B	I/O
AK20	PB12A	PB12A	I/O
AH19	PB11D	PB11D	I/O
AJ20	PB11B	PB11B	I/O
AL21	VDD2	VDD2	VDD2
AK21	PB10D	PB10D	I/O
AH20	PB10A	PB10A	I/O
AJ21	PB9D	PB9D	I/O
AL22	PB9A	PB9A	I/O
AK22	PB8D	PB8D	I/O
AJ22	PB8A	PB8A	I/O
AL23	PB7D	PB7D	I/O
AK23	PB7A	PB7A	I/O
AH22	PB6D	PB6D	I/O
AJ23	PB6C	PB6C	I/O
AK24	PB6B	PB6B	I/O
AJ24	PB6A	PB6A	I/O
AH23	PB5D	PB5D	I/O-A17
AL25	PB5C	PB5C	I/O
AK25	PB5B	PB5B	I/O
AJ25	PB5A	PB5A	I/O
AH24	PB4D	PB4D	I/O
AL26	PB4C	PB4C	I/O

Pin Information (continued)

Table 27. 432-Pin EBGA Pinout (continued)

Pin	OR3L165B	OR3L225B	Function
AK26	PB4B	PB4B	I/O
AJ26	PB4A	PB4A	I/O
AL27	VDD2	VDD2	VDD2
AK27	PB3C	PB3C	I/O
AJ27	PB3B	PB3B	I/O
AH26	PB3A	PB3A	I/O
AL28	PB2D	PB2D	I/O
AK28	PB2A	PB2A	I/O
AJ28	PB1B	PB1B	I/O
AH27	PB1A	PB1A	I/O-A16
AG28	PCCLK	PCCLK	CCLK
AH29	PL32A	PL38A	I/O-A15
AH30	PL32B	PL38B	I/O
AH31	PL32C	PL38C	I/O
AF28	PL31A	PL37A	I/O
AG29	PL30A	PL36A	I/O-SECKLL
AG30	PL30B	PL36B	I/O
AG31	PL30C	PL36C	I/O
AF29	PL30D	PL36D	I/O
AF30	PL29A	PL35A	I/O
AF31	PL29B	PL35B	I/O
AD28	PL29C	PL35C	I/O
AE29	VDD2	VDD2	VDD2
AE30	PL28A	PL34A	I/O
AE31	PL28B	PL34B	I/O
AC28	PL28C	PL34C	I/O
AD29	PL27A	PL33A	I/O-A14
AD30	PL27D	PL33D	I/O
AC29	PL26D	PL32D	I/O
AB28	PL25C	PL31C	I/O
AC30	PL25D	PL31D	I/O
AC31	PL24A	PL30A	I/O
AB29	PL24B	PL30B	I/O-A13
AB30	PL24C	PL30C	I/O
AB31	PL24D	PL30D	I/O
AA29	PL23A	PL29C	I/O
Y28	PL23B	PL29D	I/O
AA30	PL23C	PL28B	I/O
AA31	PL23D	PL28D	I/O-A12
Y29	PL22A	PL27A	I/O-A11/$\overline{\text{MPI\_IRQ}}$
W28	PL22D	PL27D	I/O

Pin Information (continued)

Table 27. 432-Pin EBGA Pinout (continued)

Pin	OR3L165B	OR3L225B	Function
Y30	PL21A	PL26A	I/O
W29	PL21C	PL26C	I/O
W30	PL21D	PL26D	I/O
V28	PL20A	PL25A	I/O-A10/MPI_BI
W31	PL20C	PL24A	I/O
V29	PL20D	PL24D	I/O
V30	PL19A	PL23A	I/O
V31	PL19C	PL22A	I/O
U29	PL19D	PL22D	I/O-A9/MPI_ACK
U30	PL18A	PL21A	I/O-A8/MPI_RW
U31	PL18C	PL21C	I/O
T30	VDD2	VDD2	VDD2
T28	PL17D	PL20D	I/O
T29	PL16A	PL19A	I/O-A7/MPI_CLK
R31	PL16C	PL19C	I/O
R30	PL15A	PL18A	I/O
R29	PECKL	PECKL	I/O-ECKL
P31	PL14A	PL17A	I/O-A6
P30	PL14D	PL16D	I/O
P29	PL13A	PL15A	I/O
N31	PL13C	PL14A	I/O
P28	PL13D	PL14D	I/O-A5
N30	PL12A	PL13A	I/O-A4
N29	PL12C	PL13C	I/O
M30	PL12D	PL13D	I/O
N28	PL11A	PL12A	I/O
M29	PL11C	PL12C	I/O
L31	VDD2	VDD2	VDD2
L30	PL10A	PL11A	I/O-A3
M28	PL10B	PL11D	I/O
L29	PL10C	PL10A	I/O
K31	PL10D	PL10D	I/O
K30	PL9A	PL9A	I/O-A2
K29	PL9B	PL9B	I/O
J31	PL9C	PL9C	I/O
J30	PL9D	PL9D	I/O
K28	PL8D	PL8D	I/O-A1/MPI_BE1
J29	PL7B	PL7B	I/O
H30	PL7C	PL7C	I/O
H29	PL7D	PL7D	I/O
J28	PL6D	PL6D	I/O

Pin Information (continued)

Table 27. 432-Pin EBGA Pinout (continued)

Pin	OR3L165B	OR3L225B	Function
G31	PL5B	PL5B	I/O
G30	PL5C	PL5C	I/O
G29	VDD2	VDD2	VDD2
H28	PL4A	PL4A	I/O
F31	PL4B	PL4B	I/O
F30	PL4C	PL4C	I/O
F29	PL4D	PL4D	I/O
E31	PL3A	PL3A	I/O
E30	PL3B	PL3B	I/O
E29	PL3C	PL3C	I/O
F28	PL3D	PL3D	I/O-A0/MPI_BE0
D31	PL2A	PL2A	I/O
D30	PL2D	PL2D	I/O
D29	PL1A	PL1A	I/O
E28	PL1D	PL1D	I/O
D27	PRD_DATA	PRD_DATA	RD_DATA/TDO
C28	PT1A	PT1A	I/O-TCK
B28	PT1D	PT1D	I/O
A28	PT2A	PT2A	I/O
D26	PT2D	PT2D	I/O
C27	PT3A	PT3A	I/O
B27	PT3B	PT3B	I/O
A27	PT3C	PT3C	I/O
C26	PT3D	PT3D	I/O
B26	PT4A	PT4A	I/O
A26	PT4B	PT4B	I/O
D24	PT4C	PT4C	I/O
C25	PT4D	PT4D	I/O
B25	PT5A	PT5A	I/O-TMS
A25	PT5B	PT5B	I/O
D23	PT5C	PT5C	I/O
C24	PT5D	PT5D	I/O
B24	VDD2	VDD2	VDD2
C23	PT6B	PT6B	I/O
D22	PT6C	PT6C	I/O
B23	PT6D	PT6D	I/O
A23	PT7A	PT7A	I/O-TDI
C22	PT7D	PT7D	I/O
B22	PT8A	PT8A	I/O
A22	PT8D	PT8D	I/O
C21	PT9A	PT9A	I/O

Pin Information (continued)

Table 27. 432-Pin EBGA Pinout (continued)

Pin	OR3L165B	OR3L225B	Function
D20	PT9D	PT9D	I/O
B21	PT10A	PT10A	I/O
A21	PT10D	PT10D	I/O
C20	PT11A	PT11A	I/O-DOUT
D19	PT11D	PT12D	I/O
B20	PT12A	PT13A	I/O
C19	PT12C	PT14A	I/O
B19	PT12D	PT14D	I/O
D18	PT13A	PT15A	I/O-D0/DIN
A19	PT13C	PT15C	I/O
C18	PT13D	PT15D	I/O
B18	PT14A	PT16A	I/O
A18	PT14C	PT16C	I/O
C17	PT14D	PT16D	I/O-D1
B17	PT15A	PT17A	I/O-D2
A17	VDD2	VDD2	VDD2
B16	PT16C	PT18D	I/O
D16	PT16D	PT19D	I/O
C16	PT17A	PT20A	I/O-D3
A15	PT17D	PT21A	I/O
B15	PT18B	PT22A	I/O
C15	PECKT	PECKT	I/O-ECKT
A14	PT19A	PT23A	I/O-D4
B14	PT19B	PT23D	I/O
C14	PT19D	PT24D	I/O
A13	PT20A	PT25A	I/O
D14	PT20B	PT25D	I/O
B13	PT20D	PT26D	I/O
C13	PT21A	PT27A	I/O-D5
B12	PT21B	PT27B	I/O
D13	VDD2	VDD2	VDD2
C12	PT22A	PT28A	I/O
A11	PT22D	PT28D	I/O
B11	PT23A	PT29A	I/O
D12	PT23D	PT29D	I/O-D6
C11	PT24A	PT30A	I/O
A10	PT24D	PT30D	I/O
B10	PT25D	PT31D	I/O
C10	PT26B	PT32B	I/O
A9	PT26C	PT32C	I/O
B9	VDD2	VDD2	VDD2

Pin Information (continued)

Table 27. 432-Pin EBGA Pinout (continued)

Pin	OR3L165B	OR3L225B	Function
D10	PT27A	PT33A	I/O
C9	PT27B	PT33B	I/O
B8	PT27C	PT33C	I/O
C8	PT27D	PT33D	I/O-D7
D9	PT28A	PT34A	I/O
A7	PT28B	PT34B	I/O
B7	PT28C	PT34C	I/O
C7	PT28D	PT34D	I/O
D8	PT29A	PT35A	I/O
A6	PT29B	PT35B	I/O
B6	PT29C	PT35C	I/O
C6	PT29D	PT35D	I/O
A5	PT30A	PT36A	I/O-RDY/RCLK/MPI_ALE
B5	PT30B	PT36B	I/O
C5	PT30C	PT36C	I/O
D6	PT30D	PT36D	I/O
A4	PT31A	PT37A	I/O
B4	PT31B	PT37B	I/O
C4	PT32A	PT38A	I/O
D5	PT32D	PT38D	I/O-SECKUR
A12	Vss	Vss	Vss
A16	Vss	Vss	Vss
A2	Vss	Vss	Vss
A20	Vss	Vss	Vss
A24	Vss	Vss	Vss
A29	Vss	Vss	Vss
A3	Vss	Vss	Vss
A30	Vss	Vss	Vss
A8	Vss	Vss	Vss
AD1	Vss	Vss	Vss
AD31	Vss	Vss	Vss
AJ1	Vss	Vss	Vss
AJ2	Vss	Vss	Vss
AJ30	Vss	Vss	Vss
AJ31	Vss	Vss	Vss
AK1	Vss	Vss	Vss
AK29	Vss	Vss	Vss
AK3	Vss	Vss	Vss
AK31	Vss	Vss	Vss
AL12	Vss	Vss	Vss
AL16	Vss	Vss	Vss

Pin Information (continued)

Table 27. 432-Pin EBGA Pinout (continued)

Pin	OR3L165B	OR3L225B	Function
AL2	VSS	VSS	VSS
AL20	VSS	VSS	VSS
AL24	VSS	VSS	VSS
AL29	VSS	VSS	VSS
AL3	VSS	VSS	VSS
AL30	VSS	VSS	VSS
AL8	VSS	VSS	VSS
B1	VSS	VSS	VSS
B29	VSS	VSS	VSS
B3	VSS	VSS	VSS
B31	VSS	VSS	VSS
C1	VSS	VSS	VSS
C2	VSS	VSS	VSS
C30	VSS	VSS	VSS
C31	VSS	VSS	VSS
H1	VSS	VSS	VSS
H31	VSS	VSS	VSS
M1	VSS	VSS	VSS
M31	VSS	VSS	VSS
T1	VSS	VSS	VSS
T31	VSS	VSS	VSS
Y1	VSS	VSS	VSS
Y31	VSS	VSS	VSS
A1	VDD	VDD	VDD
A31	VDD	VDD	VDD
AA28	VDD	VDD	VDD
AA4	VDD	VDD	VDD
AE28	VDD	VDD	VDD
AE4	VDD	VDD	VDD
AH11	VDD	VDD	VDD
AH15	VDD	VDD	VDD
AH17	VDD	VDD	VDD
AH21	VDD	VDD	VDD
AH25	VDD	VDD	VDD
AH28	VDD	VDD	VDD
AH4	VDD	VDD	VDD
AH7	VDD	VDD	VDD
AJ29	VDD	VDD	VDD
AJ3	VDD	VDD	VDD
AK2	VDD	VDD	VDD
AK30	VDD	VDD	VDD

Pin Information (continued)

Table 27. 432-Pin EBGA Pinout (continued)

Pin	OR3L165B	OR3L225B	Function
AL1	VDD	VDD	VDD
AL31	VDD	VDD	VDD
B2	VDD	VDD	VDD
B30	VDD	VDD	VDD
C29	VDD	VDD	VDD
C3	VDD	VDD	VDD
D11	VDD	VDD	VDD
D15	VDD	VDD	VDD
D17	VDD	VDD	VDD
D21	VDD	VDD	VDD
D25	VDD	VDD	VDD
D28	VDD	VDD	VDD
D4	VDD	VDD	VDD
D7	VDD	VDD	VDD
G28	VDD	VDD	VDD
G4	VDD	VDD	VDD
L28	VDD	VDD	VDD
L4	VDD	VDD	VDD
R28	VDD	VDD	VDD
R4	VDD	VDD	VDD
U28	VDD	VDD	VDD
U4	VDD	VDD	VDD

Pin Information (continued)

Table 28. 680-Pin PBGAM Pinout

Pin	OR3L165B	OR3L225B	Function
D1	PL1D	PL1D	I/O
E2	PL1C	PL1C	I/O
E1	PL1B	PL1B	I/O
F4	PL1A	PL1A	I/O
F3	PL2D	PL2D	I/O
F2	PL2A	PL2A	I/O
F1	PL3D	PL3D	I/O-A0/MPI_BE0
G5	PL3C	PL3C	I/O
G4	PL3B	PL3B	I/O
G2	PL3A	PL3A	I/O
G1	PL4D	PL4D	I/O
H5	PL4C	PL4C	I/O
H4	PL4B	PL4B	I/O
H2	PL4A	PL4A	I/O
H1	PL5C	PL5C	I/O
J5	PL5B	PL5B	I/O
J4	PL5A	PL5A	I/O
J3	PL6D	PL6D	I/O
J2	PL6C	PL6C	I/O
J1	PL6B	PL6B	I/O
K5	PL6A	PL6A	I/O
K4	PL7D	PL7D	I/O
K3	PL7C	PL7C	I/O
K2	PL7B	PL7B	I/O
K1	PL7A	PL7A	I/O
L5	PL8D	PL8D	I/O-A1/MPI_BE1
L4	PL8C	PL8C	I/O
L2	PL8B	PL8B	I/O
L1	PL8A	PL8A	I/O
M5	PL9D	PL9D	I/O
M4	PL9C	PL9C	I/O
M2	PL9B	PL9B	I/O
M1	PL9A	PL9A	I/O-A2
N5	PL10D	PL10D	I/O
N4	PL10C	PL10A	I/O
N3	PL10B	PL11D	I/O
N2	PL10A	PL11A	I/O-A3
N1	PL11C	PL12C	I/O
P5	PL11B	PL12B	I/O
P4	PL11A	PL12A	I/O
P3	PL12D	PL13D	I/O
P2	PL12C	PL13C	I/O
P1	PL12B	PL13B	I/O

Pin Information (continued)

Table 28. 680-Pin PBGAM Pinout (continued)

Pin	OR3L165B	OR3L225B	Function
R5	PL12A	PL13A	I/O-A4
R4	PL13D	PL14D	I/O-A5
R2	PL13C	PL14A	I/O
R1	PL13B	PL15D	I/O
T5	PL14D	PL16D	I/O
T4	PL14C	PL16A	I/O
T2	PL14B	PL17D	I/O
T1	PL14A	PL17A	I/O-A6
U5	PECKL	PECKL	I/O-ECKL
U4	PL15C	PL18C	I/O
U3	PL15A	PL18A	I/O
U2	PL16C	PL19C	I/O
U1	PL16A	PL19A	I/O-A7/MPI_CLK
V1	PL17D	PL20D	I/O
V2	PL18C	PL21C	I/O
V3	PL18A	PL21A	I/O-A8/MPI_RW
V4	PL19D	PL22D	I/O-A9/$\overline{\text{MPI\_ACK}}$
V5	PL19C	PL22A	I/O
W1	PL19B	PL23D	I/O
W2	PL19A	PL23A	I/O
W4	PL20D	PL24D	I/O
W5	PL20C	PL24A	I/O
Y1	PL20B	PL25D	I/O
Y2	PL20A	PL25A	I/O-A10/$\overline{\text{MPI\_B1}}$
Y4	PL21D	PL26D	I/O
Y5	PL21C	PL26C	I/O
AA1	PL21B	PL26B	I/O
AA2	PL21A	PL26A	I/O
AA3	PL22D	PL27D	I/O
AA4	PL22C	PL27C	I/O
AA5	PL22B	PL27B	I/O
AB1	PL22A	PL27A	I/O-A11/$\overline{\text{MPI\_IRQ}}$
AB2	PL23D	PL28D	I/O-A12
AB3	PL23C	PL28B	I/O
AB4	PL23A	PL29C	I/O
AB5	PL24D	PL30D	I/O
AC1	PL24C	PL30C	I/O
AC2	PL24B	PL30B	I/O-A13
AC4	PL24A	PL30A	I/O
AC5	PL25D	PL31D	I/O
AD1	PL25C	PL31C	I/O
AD2	PL25B	PL31B	I/O
AD4	PL25A	PL31A	I/O

Pin Information (continued)

Table 28. 680-Pin PBGAM Pinout (continued)

Pin	OR3L165B	OR3L225B	Function
AD5	PL26D	PL32D	I/O
AE1	PL26C	PL32C	I/O
AE2	PL26B	PL32B	I/O
AE3	PL26A	PL32A	I/O
AE4	PL27D	PL33D	I/O
AE5	PL27C	PL33C	I/O
AF1	PL27B	PL33B	I/O
AF2	PL27A	PL33A	I/O-A14
AF3	PL28D	PL34D	I/O
AF4	PL28C	PL34C	I/O
AF5	PL28B	PL34B	I/O
AG1	PL28A	PL34A	I/O
AG2	PL29C	PL35C	I/O
AG4	PL29B	PL35B	I/O
AG5	PL29A	PL35A	I/O
AH1	PL30D	PL36D	I/O
AH2	PL30C	PL36C	I/O
AH4	PL30B	PL36B	I/O
AH5	PL30A	PL36A	I/O-SECKLL
AJ1	PL31D	PL37D	I/O
AJ2	PL31C	PL37C	I/O
AJ3	PL31A	PL37A	I/O
AJ4	PL32C	PL38C	I/O
AK1	PL32B	PL38B	I/O
AK2	PL32A	PL38A	I/O-A15
AL1	PCCLK	PCCLK	CCLK
AP4	PB1A	PB1A	I/O-A16
AN5	PB1B	PB1B	I/O
AP5	PB1C	PB1C	I/O
AL6	PB1D	PB1D	I/O
AM6	PB2A	PB2A	I/O
AN6	PB2D	PB2D	I/O
AP6	PB3A	PB3A	I/O
AK7	PB3B	PB3B	I/O
AL7	PB3C	PB3C	I/O
AN7	PB4A	PB4A	I/O
AP7	PB4B	PB4B	I/O
AK8	PB4C	PB4C	I/O
AL8	PB4D	PB4D	I/O
AN8	PB5A	PB5A	I/O
AP8	PB5B	PB5B	I/O
AK9	PB5C	PB5C	I/O
AL9	PB5D	PB5D	I/O-A17

Pin Information (continued)

Table 28. 680-Pin PBGAM Pinout (continued)

Pin	OR3L165B	OR3L225B	Function
AM9	PB6A	PB6A	I/O
AN9	PB6B	PB6B	I/O
AP9	PB6C	PB6C	I/O
AK10	PB6D	PB6D	I/O
AL10	PB7A	PB7A	I/O
AM10	PB7B	PB7B	I/O
AN10	PB7C	PB7C	I/O
AP10	PB7D	PB7D	I/O
AK11	PB8A	PB8A	I/O
AL11	PB8B	PB8B	I/O
AN11	PB8C	PB8C	I/O
AP11	PB8D	PB8D	I/O
AK12	PB9A	PB9A	I/O
AL12	PB9B	PB9B	I/O
AN12	PB9C	PB9C	I/O
AP12	PB9D	PB9D	I/O
AK13	PB10A	PB10A	I/O
AL13	PB10B	PB10B	I/O
AM13	PB10C	PB10C	I/O
AN13	PB10D	PB10D	I/O
AP13	PB11B	PB11B	I/O
AK14	PB11C	PB11C	I/O
AL14	PB11D	PB11D	I/O
AM14	PB12A	PB12A	I/O
AN14	PB12B	PB12B	I/O
AP14	PB12C	PB12C	I/O
AK15	PB12D	PB12D	I/O
AL15	PB13A	PB13A	I/O
AN15	PB13B	PB13D	I/O
AP15	PB13C	PB14A	I/O
AK16	PB13D	PB14D	I/O
AL16	PB14A	PB15A	I/O
AN16	PB14B	PB15D	I/O
AP16	PB14C	PB16A	I/O
AK17	PB14D	PB16D	I/O
AL17	PB15B	PB17B	I/O
AM17	PB15D	PB17D	I/O
AN17	PB16A	PB18A	I/O
AP17	PB16B	PB18D	I/O
AP18	PB16D	PB19D	I/O
AN18	PECKB	PECKB	I/O-ECKB
AM18	PB17D	PB20D	I/O
AL18	PB18B	PB21D	I/O

Pin Information (continued)

Table 28. 680-Pin PBGAM Pinout (continued)

Pin	OR3L165B	OR3L225B	Function
AK18	PB18D	PB22D	I/O
AP19	PB19B	PB23B	I/O
AN19	PB19C	PB23C	I/O
AL19	PB19D	PB23D	I/O
AK19	PB20A	PB24A	I/O
AP20	PB20B	PB24B	I/O
AN20	PB20C	PB24C	I/O
AL20	PB20D	PB24D	I/O
AK20	PB21A	PB25A	I/O-HDC
AP21	PB21B	PB25D	I/O
AN21	PB21C	PB26A	I/O
AM21	PB21D	PB26D	I/O
AL21	PB22A	PB27A	I/O
AK21	PB22B	PB27D	I/O
AP22	PB22C	PB28A	I/O
AN22	PB23A	PB29A	I/O-$\overline{\text{LDC}}$
AM22	PB23B	PB29B	I/O
AL22	PB23C	PB29C	I/O
AK22	PB23D	PB29D	I/O
AP23	PB24A	PB30A	I/O
AN23	PB24B	PB30B	I/O
AL23	PB24C	PB30C	I/O
AK23	PB24D	PB30D	I/O
AP24	PB25A	PB31A	I/O
AN24	PB25B	PB31B	I/O
AL24	PB25C	PB31C	I/O
AK24	PB25D	PB31D	I/O
AP25	PB26A	PB32A	I/O
AN25	PB26B	PB32B	I/O
AM25	PB26C	PB32C	I/O
AL25	PB26D	PB32D	I/O
AK25	PB27A	PB33A	I/O-$\overline{\text{INIT}}$
AP26	PB27B	PB33B	I/O
AN26	PB27C	PB33C	I/O
AM26	PB27D	PB33D	I/O
AL26	PB28B	PB34B	I/O
AK26	PB28C	PB34C	I/O
AP27	PB28D	PB34D	I/O
AN27	PB29A	PB35A	I/O
AL27	PB29B	PB35B	I/O
AK27	PB29C	PB35C	I/O
AP28	PB29D	PB35D	I/O
AN28	PB30A	PB36A	I/O

Pin Information (continued)

Table 28. 680-Pin PBGAM Pinout (continued)

Pin	OR3L165B	OR3L225B	Function
AL28	PB30B	PB36B	I/O
AK28	PB30C	PB36C	I/O
AP29	PB30D	PB36D	I/O
AN29	PB31A	PB37A	I/O
AM29	PB31D	PB37D	I/O
AL29	PB32A	PB38A	I/O
AP30	PB32C	PB38C	I/O
AN30	PB32D	PB38D	I/O
AP31	PDONE	PDONE	DONE
AL34	PRESETN	PRESETN	$\overline{\text{RESET}}$
AK33	PPRGMN	PPRGMN	$\overline{\text{PRGM}}$
AK34	PR32A	PR38A	I/O-M0
AJ31	PR32B	PR38B	I/O
AJ32	PR31A	PR37A	I/O
AJ33	PR31D	PR37D	I/O
AJ34	PR30B	PR36B	I/O
AH30	PR30C	PR36C	I/O
AH31	PR30D	PR36D	I/O
AH33	PR29A	PR35A	I/O
AH34	PR29B	PR35B	I/O
AG30	PR29C	PR35C	I/O
AG31	PR29D	PR35D	I/O
AG33	PR28A	PR34A	I/O
AG34	PR28B	PR34B	I/O
AF30	PR28C	PR34C	I/O
AF31	PR28D	PR34D	I/O
AF32	PR27A	PR33A	I/O
AF33	PR27B	PR33B	I/O
AF34	PR27C	PR33C	I/O
AE30	PR27D	PR33D	I/O
AE31	PR26A	PR32A	I/O
AE32	PR26B	PR32B	I/O
AE33	PR26C	PR32C	I/O
AE34	PR26D	PR32D	I/O
AD30	PR25A	PR31A	I/O
AD31	PR25B	PR31B	I/O
AD33	PR25C	PR31C	I/O
AD34	PR25D	PR31D	I/O-M1
AC30	PR24A	PR30A	I/O
AC31	PR24B	PR30D	I/O
AC33	PR24C	PR29A	I/O
AC34	PR23A	PR28A	I/O
AB30	PR23B	PR28B	I/O

Pin Information (continued)

Table 28. 680-Pin PBGAM Pinout (continued)

Pin	OR3L165B	OR3L225B	Function
AB31	PR23C	PR28C	I/O
AB32	PR23D	PR28D	I/O
AB33	PR22A	PR27A	I/O-M2
AB34	PR22B	PR27B	I/O
AA30	PR22C	PR27C	I/O
AA31	PR22D	PR27D	I/O
AA32	PR21A	PR26A	I/O
AA33	PR21B	PR26B	I/O
AA34	PR21C	PR26C	I/O
Y30	PR21D	PR26D	I/O
Y31	PR20A	PR25A	I/O-M3
Y33	PR20B	PR25D	I/O
Y34	PR20C	PR24A	I/O
W30	PR20D	PR24D	I/O
W31	PR19A	PR23A	I/O
W33	PR19B	PR23D	I/O
W34	PR19C	PR22B	I/O
V30	PR18A	PR21A	I/O
V31	PR18B	PR21B	I/O
V32	PR18D	PR21D	I/O
V33	PR17B	PR20B	I/O
V34	PR17D	PR20D	I/O
U34	PECKR	PECKR	I/O-ECKR
U33	PR16D	PR19D	I/O
U32	PR15B	PR18B	I/O
U31	PR15D	PR18D	I/O
U30	PR14B	PR17D	I/O
T34	PR14C	PR16A	I/O
T33	PR14D	PR16D	I/O
T31	PR13A	PR15A	I/O
T30	PR13B	PR15D	I/O
R34	PR13C	PR14A	I/O
R33	PR13D	PR14D	I/O
R31	PR12A	PR13A	I/O-CS1
R30	PR12B	PR13B	I/O
P34	PR12C	PR13C	I/O
P33	PR12D	PR13D	I/O
P32	PR11A	PR12A	I/O
P31	PR11B	PR12B	I/O
P30	PR11C	PR12C	I/O
N34	PR10A	PR11A	I/O-$\overline{CS0}$
N33	PR10B	PR11C	I/O
N32	PR10C	PR11D	I/O

Pin Information (continued)

Table 28. 680-Pin PBGAM Pinout (continued)

Pin	OR3L165B	OR3L225B	Function
N31	PR10D	PR10A	I/O
N30	PR9A	PR10C	I/O
M34	PR9B	PR10D	I/O
M33	PR9C	PR9A	I/O
M31	PR9D	PR9D	I/O
M30	PR8A	PR8A	I/O-$\overline{RD}$/MPI_STRB
L34	PR8B	PR8B	I/O
L33	PR8C	PR8C	I/O
L31	PR8D	PR8D	I/O
L30	PR7A	PR7A	I/O
K34	PR7B	PR7B	I/O
K33	PR7C	PR7C	I/O
K32	PR7D	PR7D	I/O
K31	PR6A	PR6A	I/O
K30	PR6B	PR6B	I/O
J34	PR6C	PR6C	I/O
J33	PR6D	PR6D	I/O
J32	PR5B	PR5B	I/O
J31	PR5C	PR5C	I/O
J30	PR5D	PR5D	I/O
H34	PR4A	PR4A	I/O-$\overline{WR}$
H33	PR4B	PR4B	I/O
H31	PR4C	PR4C	I/O
H30	PR4D	PR4D	I/O
G34	PR3A	PR3A	I/O
G33	PR3B	PR3B	I/O
G31	PR3C	PR3C	I/O
G30	PR3D	PR3D	I/O
F34	PR2A	PR2A	I/O
F33	PR2B	PR2B	I/O
F32	PR2D	PR2D	I/O
F31	PR1A	PR1A	I/O
E34	PR1B	PR1B	I/O
E33	PR1D	PR1D	I/O
D34	PRD_CFGN	PRD_CFGN	$\overline{RD\_CFG}$
A31	PT32D	PT38D	I/O-SECKUR
B30	PT32C	PT38C	I/O
A30	PT32A	PT38A	I/O
D29	PT31D	PT37D	I/O
C29	PT31B	PT37B	I/O
B29	PT31A	PT37A	I/O
A29	PT30D	PT36D	I/O
E28	PT30C	PT36C	I/O

Pin Information (continued)

Table 28. 680-Pin PBGAM Pinout (continued)

Pin	OR3L165B	OR3L225B	Function
D28	PT30B	PT36B	I/O
B28	PT30A	PT36A	I/O-RDY/RCLK/MPI_ALE
A28	PT29D	PT35D	I/O
E27	PT29C	PT35C	I/O
D27	PT29B	PT35B	I/O
B27	PT29A	PT35A	I/O
A27	PT28D	PT34D	I/O
E26	PT28C	PT34C	I/O
D26	PT28B	PT34B	I/O
C26	PT28A	PT34A	I/O
B26	PT27D	PT33D	I/O-D7
A26	PT27C	PT33C	I/O
E25	PT27B	PT33B	I/O
D25	PT27A	PT33A	I/O
C25	PT26C	PT32C	I/O
B25	PT26B	PT32B	I/O
A25	PT26A	PT32A	I/O
E24	PT25D	PT31D	I/O
D24	PT25C	PT31C	I/O
B24	PT25B	PT31B	I/O
A24	PT25A	PT31A	I/O
E23	PT24D	PT30D	I/O
D23	PT24C	PT30C	I/O
B23	PT24B	PT30B	I/O
A23	PT24A	PT30A	I/O
E22	PT23D	PT29D	I/O-D6
D22	PT23C	PT29C	I/O
C22	PT23B	PT29B	I/O
B22	PT23A	PT29A	I/O
A22	PT22D	PT28D	I/O
E21	PT22C	PT28C	I/O
D21	PT22B	PT28B	I/O
C21	PT22A	PT28A	I/O
B21	PT21C	PT27C	I/O
A21	PT21B	PT27B	I/O
E20	PT21A	PT27A	I/O-D5
D20	PT20D	PT26D	I/O
B20	PT20C	PT26A	I/O
A20	PT20B	PT25D	I/O
E19	PT20A	PT25A	I/O
D19	PT19D	PT24D	I/O
B19	PT19C	PT24A	I/O
A19	PT19B	PT23D	I/O

Pin Information (continued)

Table 28. 680-Pin PBGAM Pinout (continued)

Pin	OR3L165B	OR3L225B	Function
E18	PT19A	PT23A	I/O-D4
D18	PECKT	PECKT	I/O-ECKT
C18	PT17D	PT21A	I/O
B18	PT17C	PT20D	I/O
A18	PT17A	PT20A	I/O-D3
A17	PT16D	PT19D	I/O
B17	PT16C	PT18D	I/O
C17	PT15A	PT17A	I/O-D2
D17	PT14D	PT16D	I/O-D1
E17	PT14C	PT16C	I/O
A16	PT14B	PT16B	I/O
B16	PT14A	PT16A	I/O
D16	PT13D	PT15D	I/O
E16	PT13C	PT15C	I/O
A15	PT13B	PT15B	I/O
B15	PT13A	PT15A	I/O-D0/DIN
D15	PT12D	PT14D	I/O
E15	PT12C	PT14A	I/O
A14	PT12B	PT13D	I/O
B14	PT12A	PT13A	I/O
C14	PT11D	PT12D	I/O
D14	PT11C	PT12A	I/O
E14	PT11B	PT11D	I/O
A13	PT11A	PT11A	I/O-DOUT
B13	PT10C	PT10C	I/O
C13	PT10B	PT10B	I/O
D13	PT10A	PT10A	I/O
E13	PT9D	PT9D	I/O
A12	PT9C	PT9C	I/O
B12	PT9B	PT9B	I/O
D12	PT9A	PT9A	I/O
E12	PT8D	PT8D	I/O
A11	PT8C	PT8C	I/O
B11	PT8B	PT8B	I/O
D11	PT8A	PT8A	I/O
E11	PT7D	PT7D	I/O
A10	PT7C	PT7C	I/O
B10	PT7B	PT7B	I/O
C10	PT7A	PT7A	I/O-TDI
D10	PT6D	PT6D	I/O
E10	PT6C	PT6C	I/O
A9	PT6B	PT6B	I/O
B9	PT5D	PT5D	I/O

Pin Information (continued)

Table 28. 680-Pin PBGAM Pinout (continued)

Pin	OR3L165B	OR3L225B	Function
C9	PT5C	PT5C	I/O
D9	PT5B	PT5B	I/O
E9	PT5A	PT5A	I/O-TMS
A8	PT4D	PT4D	I/O
B8	PT4C	PT4C	I/O
D8	PT4B	PT4B	I/O
E8	PT4A	PT4A	I/O
A7	PT3D	PT3D	I/O
B7	PT3C	PT3C	I/O
D7	PT3B	PT3B	I/O
E7	PT3A	PT3A	I/O
A6	PT2D	PT2D	I/O
B6	PT2C	PT2C	I/O
C6	PT2A	PT2A	I/O
D6	PT1D	PT1D	I/O
A5	PT1C	PT1C	I/O
B5	PT1A	PT1A	I/O-TCK
A4	PRD_DATA	PRD_DATA	RD_DATA/TDO
A1	Vss	Vss	Vss
A2	Vss	Vss	Vss
A33	Vss	Vss	Vss
A34	Vss	Vss	Vss
B1	Vss	Vss	Vss
B2	Vss	Vss	Vss
B33	Vss	Vss	Vss
B34	Vss	Vss	Vss
C3	Vss	Vss	Vss
C8	Vss	Vss	Vss
C12	Vss	Vss	Vss
C16	Vss	Vss	Vss
C19	Vss	Vss	Vss
C23	Vss	Vss	Vss
C27	Vss	Vss	Vss
C32	Vss	Vss	Vss
D4	Vss	Vss	Vss
D31	Vss	Vss	Vss
H3	Vss	Vss	Vss
H32	Vss	Vss	Vss
M3	Vss	Vss	Vss
M32	Vss	Vss	Vss
N13	Vss	Vss	Vss
N14	Vss	Vss	Vss
N15	Vss	Vss	Vss

Pin Information (continued)

Table 28. 680-Pin PBGAM Pinout (continued)

Pin	OR3L165B	OR3L225B	Function
N20	Vss	Vss	Vss
N21	Vss	Vss	Vss
N22	Vss	Vss	Vss
P13	Vss	Vss	Vss
P14	Vss	Vss	Vss
P15	Vss	Vss	Vss
P20	Vss	Vss	Vss
P21	Vss	Vss	Vss
P22	Vss	Vss	Vss
R13	Vss	Vss	Vss
R14	Vss	Vss	Vss
R15	Vss	Vss	Vss
R20	Vss	Vss	Vss
R21	Vss	Vss	Vss
R22	Vss	Vss	Vss
T3	Vss	Vss	Vss
T16	Vss	Vss	Vss
T17	Vss	Vss	Vss
T18	Vss	Vss	Vss
T19	Vss	Vss	Vss
T32	Vss	Vss	Vss
U16	Vss	Vss	Vss
U17	Vss	Vss	Vss
U18	Vss	Vss	Vss
U19	Vss	Vss	Vss
V16	Vss	Vss	Vss
V17	Vss	Vss	Vss
V18	Vss	Vss	Vss
V19	Vss	Vss	Vss
W3	Vss	Vss	Vss
W16	Vss	Vss	Vss
W17	Vss	Vss	Vss
W18	Vss	Vss	Vss
W19	Vss	Vss	Vss
W32	Vss	Vss	Vss
Y13	Vss	Vss	Vss
Y14	Vss	Vss	Vss
Y15	Vss	Vss	Vss
Y20	Vss	Vss	Vss
Y21	Vss	Vss	Vss
Y22	Vss	Vss	Vss
AA13	Vss	Vss	Vss
AA14	Vss	Vss	Vss

Pin Information (continued)

Table 28. 680-Pin PBGAM Pinout (continued)

Pin	OR3L165B	OR3L225B	Function
AA15	VSS	VSS	VSS
AA20	VSS	VSS	VSS
AA21	VSS	VSS	VSS
AA22	VSS	VSS	VSS
AB13	VSS	VSS	VSS
AB14	VSS	VSS	VSS
AB15	VSS	VSS	VSS
AB20	VSS	VSS	VSS
AB21	VSS	VSS	VSS
AB22	VSS	VSS	VSS
AC3	VSS	VSS	VSS
AC32	VSS	VSS	VSS
AG3	VSS	VSS	VSS
AG32	VSS	VSS	VSS
AL4	VSS	VSS	VSS
AL31	VSS	VSS	VSS
AM3	VSS	VSS	VSS
AM8	VSS	VSS	VSS
AM12	VSS	VSS	VSS
AM16	VSS	VSS	VSS
AM19	VSS	VSS	VSS
AM23	VSS	VSS	VSS
AM27	VSS	VSS	VSS
AM32	VSS	VSS	VSS
AN1	VSS	VSS	VSS
AN2	VSS	VSS	VSS
AN33	VSS	VSS	VSS
AN34	VSS	VSS	VSS
AP1	VSS	VSS	VSS
AP2	VSS	VSS	VSS
AP33	VSS	VSS	VSS
AP34	VSS	VSS	VSS
C5	VDD2	VDD2	VDD2
C30	VDD2	VDD2	VDD2
D5	VDD2	VDD2	VDD2
D30	VDD2	VDD2	VDD2
E3	VDD2	VDD2	VDD2
E4	VDD2	VDD2	VDD2
E5	VDD2	VDD2	VDD2
E6	VDD2	VDD2	VDD2
E29	VDD2	VDD2	VDD2
E30	VDD2	VDD2	VDD2
E31	VDD2	VDD2	VDD2

Pin Information (continued)

Table 28. 680-Pin PBGAM Pinout (continued)

Pin	OR3L165B	OR3L225B	Function
E32	VDD2	VDD2	VDD2
F5	VDD2	VDD2	VDD2
F30	VDD2	VDD2	VDD2
N16	VDD2	VDD2	VDD2
N17	VDD2	VDD2	VDD2
N18	VDD2	VDD2	VDD2
N19	VDD2	VDD2	VDD2
P16	VDD2	VDD2	VDD2
P17	VDD2	VDD2	VDD2
P18	VDD2	VDD2	VDD2
P19	VDD2	VDD2	VDD2
R16	VDD2	VDD2	VDD2
R17	VDD2	VDD2	VDD2
R18	VDD2	VDD2	VDD2
R19	VDD2	VDD2	VDD2
T13	VDD2	VDD2	VDD2
T14	VDD2	VDD2	VDD2
T15	VDD2	VDD2	VDD2
T20	VDD2	VDD2	VDD2
T21	VDD2	VDD2	VDD2
T22	VDD2	VDD2	VDD2
U13	VDD2	VDD2	VDD2
U14	VDD2	VDD2	VDD2
U15	VDD2	VDD2	VDD2
U20	VDD2	VDD2	VDD2
U21	VDD2	VDD2	VDD2
U22	VDD2	VDD2	VDD2
V13	VDD2	VDD2	VDD2
V14	VDD2	VDD2	VDD2
V15	VDD2	VDD2	VDD2
V20	VDD2	VDD2	VDD2
V21	VDD2	VDD2	VDD2
V22	VDD2	VDD2	VDD2
W13	VDD2	VDD2	VDD2
W14	VDD2	VDD2	VDD2
W15	VDD2	VDD2	VDD2
W20	VDD2	VDD2	VDD2
W21	VDD2	VDD2	VDD2
W22	VDD2	VDD2	VDD2
Y16	VDD2	VDD2	VDD2
Y17	VDD2	VDD2	VDD2
Y18	VDD2	VDD2	VDD2
Y19	VDD2	VDD2	VDD2

Pin Information (continued)

Table 28. 680-Pin PBGAM Pinout (continued)

Pin	OR3L165B	OR3L225B	Function
AA16	VDD2	VDD2	VDD2
AA17	VDD2	VDD2	VDD2
AA18	VDD2	VDD2	VDD2
AA19	VDD2	VDD2	VDD2
AB16	VDD2	VDD2	VDD2
AB17	VDD2	VDD2	VDD2
AB18	VDD2	VDD2	VDD2
AB19	VDD2	VDD2	VDD2
AJ5	VDD2	VDD2	VDD2
AJ30	VDD2	VDD2	VDD2
AK3	VDD2	VDD2	VDD2
AK4	VDD2	VDD2	VDD2
AK5	VDD2	VDD2	VDD2
AK6	VDD2	VDD2	VDD2
AK29	VDD2	VDD2	VDD2
AK30	VDD2	VDD2	VDD2
AK31	VDD2	VDD2	VDD2
AK32	VDD2	VDD2	VDD2
AL5	VDD2	VDD2	VDD2
AL30	VDD2	VDD2	VDD2
AM5	VDD2	VDD2	VDD2
AM30	VDD2	VDD2	VDD2
A3	VDD	VDD	VDD
A32	VDD	VDD	VDD
B3	VDD	VDD	VDD
B4	VDD	VDD	VDD
B31	VDD	VDD	VDD
B32	VDD	VDD	VDD
C1	VDD	VDD	VDD
C2	VDD	VDD	VDD
C4	VDD	VDD	VDD
C7	VDD	VDD	VDD
C11	VDD	VDD	VDD
C15	VDD	VDD	VDD
C20	VDD	VDD	VDD
C24	VDD	VDD	VDD
C28	VDD	VDD	VDD
C31	VDD	VDD	VDD
C33	VDD	VDD	VDD
C34	VDD	VDD	VDD
D2	VDD	VDD	VDD
D3	VDD	VDD	VDD
D32	VDD	VDD	VDD

Pin Information (continued)

Table 28. 680-Pin PBGAM Pinout (continued)

Pin	OR3L165B	OR3L225B	Function
D33	VDD	VDD	VDD
G3	VDD	VDD	VDD
G32	VDD	VDD	VDD
L3	VDD	VDD	VDD
L32	VDD	VDD	VDD
R3	VDD	VDD	VDD
R32	VDD	VDD	VDD
Y3	VDD	VDD	VDD
Y32	VDD	VDD	VDD
AD3	VDD	VDD	VDD
AD32	VDD	VDD	VDD
AH3	VDD	VDD	VDD
AH32	VDD	VDD	VDD
AL2	VDD	VDD	VDD
AL3	VDD	VDD	VDD
AL32	VDD	VDD	VDD
AL33	VDD	VDD	VDD
AM1	VDD	VDD	VDD
AM2	VDD	VDD	VDD
AM4	VDD	VDD	VDD
AM7	VDD	VDD	VDD
AM11	VDD	VDD	VDD
AM15	VDD	VDD	VDD
AM20	VDD	VDD	VDD
AM24	VDD	VDD	VDD
AM28	VDD	VDD	VDD
AM31	VDD	VDD	VDD
AM33	VDD	VDD	VDD
AM34	VDD	VDD	VDD
AN3	VDD	VDD	VDD
AN4	VDD	VDD	VDD
AN31	VDD	VDD	VDD
AN32	VDD	VDD	VDD
AP3	VDD	VDD	VDD
AP32	VDD	VDD	VDD

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operations sections of this data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

The *ORCA* Series FPGAs include circuitry designed to protect the chips from damaging substrate injection currents and to prevent accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use to avoid exposure to excessive electrical stress.

Table 29. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Storage Temperature	T_{stg}	–65	150	°C
I/O Supply Voltage with Respect to Ground	VDD	—	<4.2	V
Internal Supply Voltage	VDD2	—	<3.2	V
Input Signal with Respect to Ground				
CMOS I/O	—	–0.5	VDD + 0.3	V
5 V tolerant I/O	—	–0.5	5.8	V
Signal Applied to High-impedance Output	—	–0.5	VDD + 0.3	V
Maximum Package Body Temperature	—	—	220	°C
Junction Temperature	T_J	–40	125	°C

Recommended Operating Conditions

Table 30. Recommended Operating Conditions

Mode	OR3LxxxB		
	Temperature Range (Ambient)	I/O Supply Voltage (VDD)	Internal Supply Voltage (VDD2)
Commercial	0 °C to 70 °C	3.0 V to 3.6 V	2.5 V ± 5%
Industrial	–40 °C to +85 °C	3.0 V to 3.6 V	2.5 V ± 5%

Electrical Characteristics

Table 31. Electrical Characteristics

OR3LxxxB Commercial: V_{DD} = 3.0 V to 3.6 V, V_{DD2} = 2.38 V to 2.63 V, 0 °C < T_A < 70 °C; Industrial: V_{DD} = 3.0 V to 3.6 V, V_{DD2} = 2.38 V to 2.63 V, –40 °C < T_A < +85 °C.

Parameter	Symbol	Test Conditions	OR3LxxxB Min	OR3LxxxB Max	Unit
Input Voltage: High Low	 V_{IH} V_{IL}	Input configured as CMOS (clamped to V_{DD})	 50% V_{DD} GND – 0.5	 V_{DD} + 0.5 30% V_{DD}	 V V
Input Voltage: High Low	 V_{IH} V_{IL}	Input configured as TTL (5 V tolerant)	 50% V_{DD} GND – 0.5	 5.8 V 30% V_{DD}	 V V
Output Voltage: High Low	 V_{OH} V_{OL}	 V_{DD} = min, I_{OH} = 6 mA or 3 mA V_{DD} = min, I_{OL} = 12 mA or 6 mA	 2.4 —	 — 0.4	 V V
Input Leakage Current	I_L	V_{DD} = max, V_{IN} = V_{SS} or V_{DD}	–10	10	µA
Standby Current: OR3L165B OR3L225B	I_{DDSB}	(T_A = 25 °C, V_{DD} = 3.3 V, V_{DD2} = 2.5 V) internal oscillator running, no output loads, inputs V_{DD} or GND	 — —	V_{DD2} / V_{DD} 1.5 / 1.0 2.0 / 1.0	 mA mA
Standby Current: OR3L165B OR3L225B	I_{DDSB}	(T_A = 25 °C, V_{DD} = 3.3 V, V_{DD2} = 2.5 V) internal oscillator stopped, no output loads, inputs V_{DD} or GND (after configuration)	 — —	V_{DD2} / V_{DD} 1.1 / 1.0 1.5 / 1.0	 mA mA
Powerup Current: OR3L165B OR3L225B	I_{pp}	Power supply current at approximately 1 V, within a recommended power supply ramp rate of 1 ms—200 ms	 0.4 0.8	 — —	 mA mA
Input Capacitance	C_{IN}	T_A = 25 °C, V_{DD} = 3.3 V, V_{DD2} = 2.5 V Test frequency = 1 MHz	—	8	pF
Output Capacitance	C_{OUT}	T_A = 25 °C, V_{DD} = 3.3 V, V_{DD2} = 2.5 V Test frequency = 1 MHz	—	8	pF
DONE Pull-up Resistor*	R_{DONE}	—	100	—	kΩ
M[3:0] Pull-up Resistors*	R_M	—	100	—	kΩ
I/O Pad Static Pull-up Current*	I_{PU}	V_{DD} = 3.6 V, V_{IN} = V_{SS}, T_A = 0 °C	14.4	50.9	µA
I/O Pad Static Pull-down Current	I_{PD}	V_{DD} = 3.6 V, V_{IN} = V_{SS}, T_A = 0 °C	26	103	µA
I/O Pad Pull-up Resistor*	R_{PU}	V_{DD} = all, V_{IN} = V_{SS}, T_A = 0 °C	100	—	kΩ
I/O Pad Pull-down Resistor	R_{PD}	V_{DD} = all, V_{IN} = V_{SS}, T_A = 0 °C	50	—	kΩ

* On the Series 3L devices, the pull-up resistor will externally pull the pin to a level 1.0 V below V_{DD}.

Package Thermal Characteristics

There are four thermal parameters that are in common use: Θ_{JA}, ψ_{JC}, Θ_{JC}, and Θ_{JB}. It should be noted that all the parameters are affected, to varying degrees, by package design (including paddle size) and choice of materials, the amount of copper in the test board or system board, and system airflow.

Table 32 contains the currently available thermal specifications for Lattice's FPGA packages mounted on both JEDEC and non-JEDEC test boards. The thermal values for the newer package types correspond to those packages mounted on a JEDEC four-layer board. The values for the older packages, however, correspond to those packages mounted on a non-JEDEC, single-layer, sparse copper board (see Note 2). It should also be noted that the values for the older packages are considered conservative.

Θ_{JA}

This is the thermal resistance from junction to ambient (a.k.a. Θ-JA, R-Θ, etc.). It is defined by the following:

$$\Theta_{JA} = \frac{T_J - T_A}{Q}$$

where T_J is the junction temperature, T_A is the ambient air temperature, and Q is the chip power.

Experimentally, Θ_{JA} is determined when a special thermal test die is assembled into the package of interest, and the part is mounted on the thermal test board. The diodes on the test chip are separately calibrated in an oven. The package/board is placed either in a JEDEC natural convection box or in the wind tunnel, the latter for forced convection measurements. A controlled amount of power (Q) is dissipated in the test chip's heater resistor, the chip's temperature (T_J) is determined by the forward drop on the diodes, and the ambient temperature (T_A) is noted. Note that Θ_{JA} is expressed in units of °C/watt.

ψ_{JC}

This JEDEC designated parameter correlates the junction temperature to the case temperature. It is generally used to infer the junction temperature while the device is operating in the system. It is not considered a true thermal resistance, and it is defined by the following:

$$\psi_{JC} = \frac{T_J - T_C}{Q}$$

where T_C is the case temperature at top dead center, T_J is the junction temperature, and Q is the chip power. During the Θ_{JA} measurements described above, besides the other parameters measured, an additional temperature reading, T_C, is made with a thermocouple attached at top-dead-center of the case. ψ_{JC} is also expressed in units of °C/watt.

Θ_{JC}

This is the thermal resistance from junction to case. It is most often used when attaching a heat sink to the top of the package. It is defined by the following:

$$\Theta_{JC} = \frac{T_J - T_C}{Q}$$

The parameters in this equation have been defined above. However, the measurements are performed with the case of the part pressed against a water-cooled heat sink so as to draw most of the heat generated by the chip out the top of the package. It is this difference in the measurement process that differentiates Θ_{JC} from ψ_{JC}. Θ_{JC} is a true thermal resistance and is expressed in units of °C/watt.

Θ_{JB}

This is the thermal resistance from junction to board (a.k.a. Θ_{JL}). It is defined by the following:

$$\Theta_{JB} = \frac{T_J - T_B}{Q}$$

where T_B is the temperature of the board adjacent to a lead measured with a thermocouple. The other parameters on the right-hand side have been defined above. This is considered a true thermal resistance, and the measurement is made with a water-cooled heat sink pressed against the board so as to draw most of the heat out of the leads. Note that Θ_{JB} is expressed in units of °C/watt, and that this parameter and the way it is measured is still in JEDEC committee.

Package Thermal Characteristics (continued)

FPGA Maximum Junction Temperature

Once the power dissipated by the FPGA has been determined (see the Estimating Power Dissipation section), the maximum junction temperature of the FPGA can be found. This is needed to determine if speed derating of the device from the 85 °C junction temperature used in all of the delay tables is needed. Using the maximum ambient temperature, T_{Amax}, and the power dissipated by the device, Q (expressed in °C), the maximum junction temperature is approximated by the following:

$$T_{Jmax} = T_{Amax} + (Q \times \Theta_{JA})$$

Table 32 lists the plastic package thermal characteristics for the *ORCA* Series FPGAs.

Table 32. Plastic Package Thermal Characteristics for the *ORCA* Series[1]

Package	Θ_{JA} (°C/W)			T_A = 70 °C max T_J = 125 °C max at 0 fpm (W)
	0 fpm	200 fpm	500 fpm	
208-Pin SQFP2[1]	12.8	10.3	9.1	4.3
240-Pin SQFP2[1]	13.0	10.0	9.0	4.2
352-Pin PBGA[1, 2]	19.0	16.0	15.0	2.9
352-Pin PBGA[1, 3]	25.5	22.0	20.5	2.1
432-Pin EBGA[1]	11.0	8.5	7.5	5.0
680-Pin PBGAM1	14.5	TBD	TBD	3.8

1. Mounted on 4-layer JEDEC standard test board with two power/ground planes.
2. With thermal balls connected to board ground plane.
3. Without thermal balls connected to board ground plane.

Package Coplanarity

The coplanarity limits of the *ORCA* Series 3 packages are as follows.

Table 33. Package Coplanarity

Package Type	Coplanarity Limit (mils)
EBGA	8.0
PBGA	8.0
SQFP2	3.15
PBGAM1	8.0

Package Parasitics

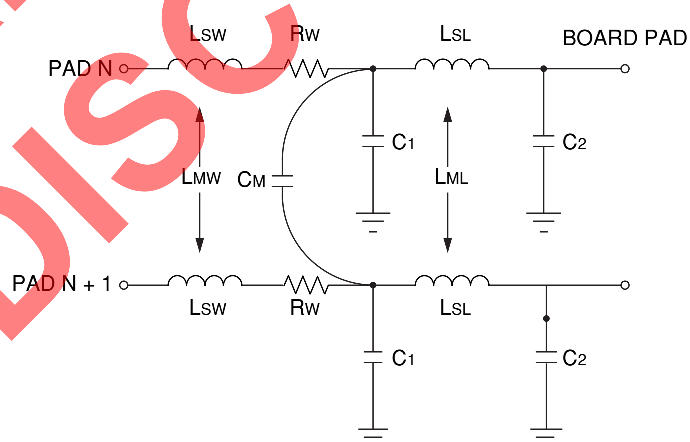
The electrical performance of an IC package, such as signal quality and noise sensitivity, is directly affected by the package parasitics. Table 34 lists eight parasitics associated with the *ORCA* packages. These parasitics represent the contributions of all components of a package, which include the bond wires, all internal package routing, and the external leads.

Four inductances in nH are listed: L_{SW} and L_{SL}, the self-inductance of the lead; and L_{MW} and L_{ML}, the mutual inductance to the nearest neighbor lead. These parameters are important in determining ground bounce noise and inductive crosstalk noise. Three capacitances in pF are listed: C_M, the mutual capacitance of the lead to the nearest neighbor lead; and C_1 and C_2, the total capacitance of the lead to all other leads (all other leads are assumed to be grounded). These parameters are important in determining capacitive crosstalk and the capacitive loading effect of the lead. The lead resistance value, R_W, is in mΩ.

The parasitic values in Table 34 are for the circuit model of bond wire and package lead parasitics. If the mutual capacitance value is not used in the designer's model, then the value listed as mutual capacitance should be added to each of the C_1 and C_2 capacitors.

Table 34. Package Parasitics

Package Type	L_{SW}	L_{MW}	R_W	C_1	C_2	C_M	L_{SL}	L_{ML}
208-Pin SQFP2	4	2	200	1	1	1	6—9	4—6
240-Pin SQFP2	4	2	200	1	1	1	7—11	4—7
352-Pin PBGA	5	2	220	1.5	1.5	1.5	7—12	3—6
432-Pin EBGA	4	1.5	500	1	1	0.3	3—5.5	0.5—1
680-Pin PBGAM1	3.8	1.3	250	1	1	0.3	2.8—5.0	0.5—1



5-3862(F).a

Figure 12. Package Parasitics

Package Outline Diagrams

Terms and Definitions

Basic Size (BSC): The basic size of a dimension is the size from which the limits for that dimension are derived by the application of the allowance and the tolerance.

Design Size: The design size of a dimension is the actual size of the design, including an allowance for fit and tolerance.

Typical (TYP): When specified after a dimension, this indicates the repeated design size if a tolerance is specified or repeated basic size if a tolerance is not specified.

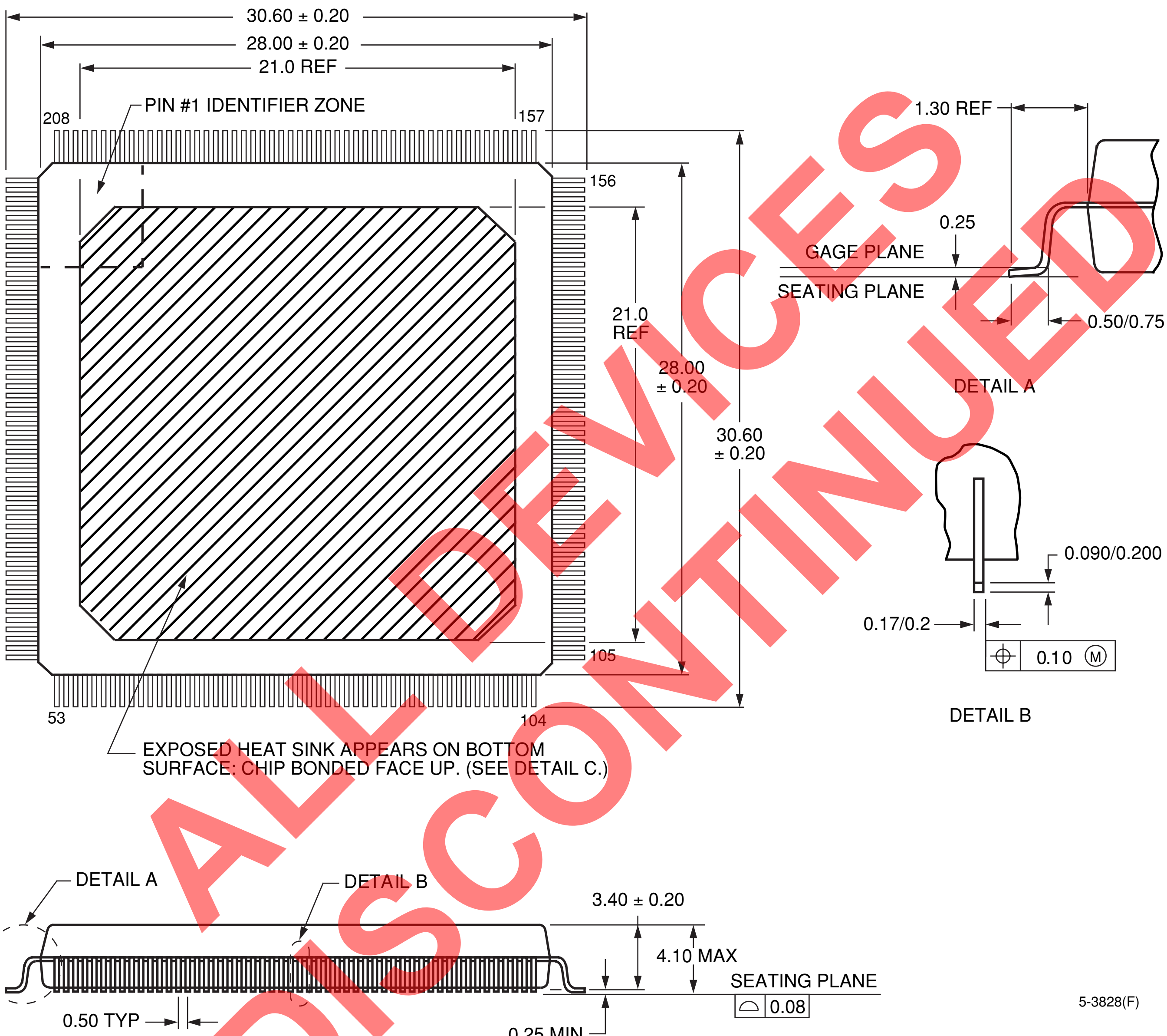
Reference (REF): The reference dimension is an untoleranced dimension used for informational purposes only. It is a repeated dimension or one that can be derived from other values in the drawing.

Minimum (MIN) or Maximum (MAX): Indicates the minimum or maximum allowable size of a dimension.

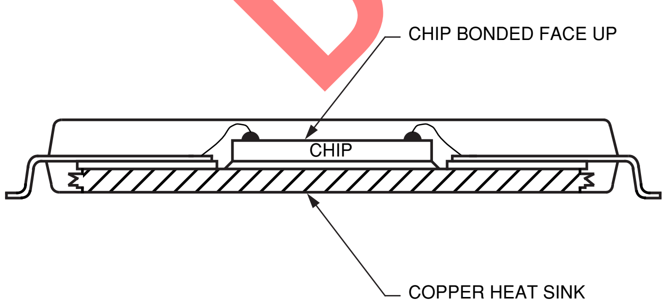
Package Outline Diagrams (continued)

208-Pin SQFP2

Dimensions are in millimeters.



5-3828(F)



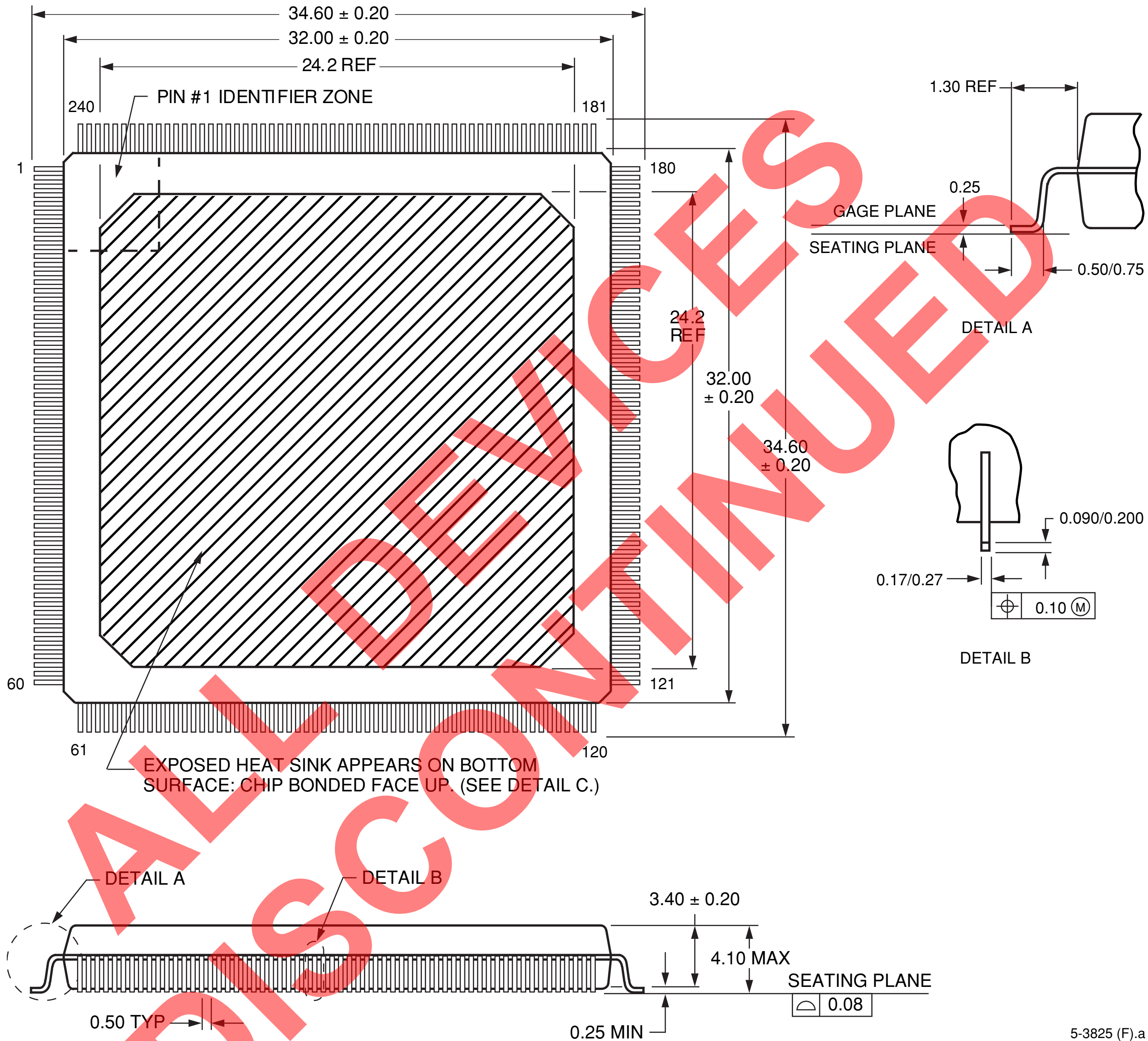
DETAIL C (SQFP2 CHIP-UP)

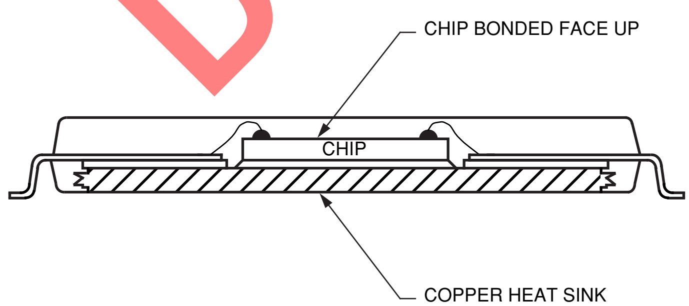
5-4946(F)

Package Outline Diagrams (continued)

240-Pin SQFP2

Dimensions are in millimeters.





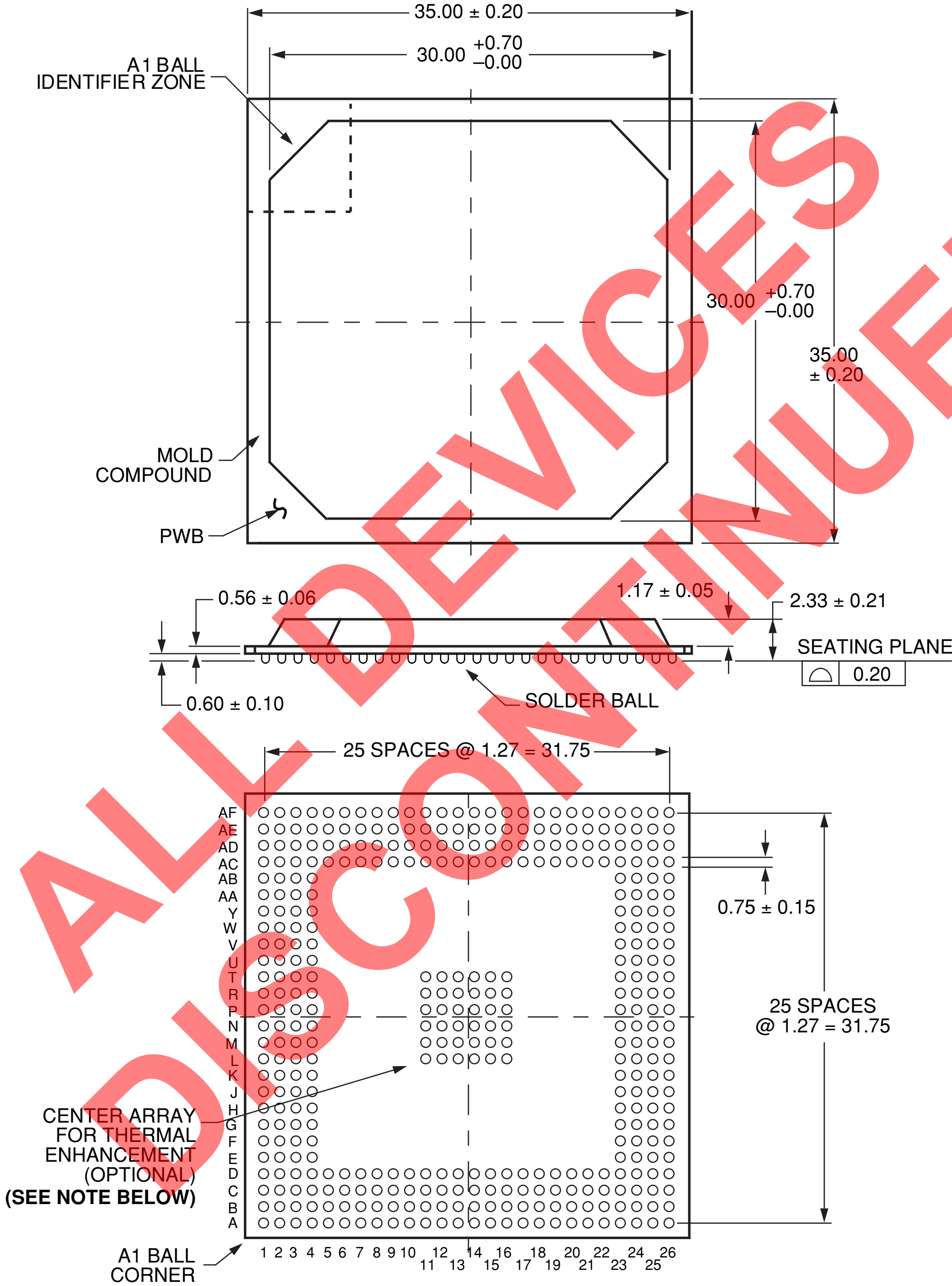
DETAIL C (SQFP2 CHIP-UP)

5-4946(F)

Package Outline Diagrams (continued)

352-Pin PBGA

Dimensions are in millimeters.



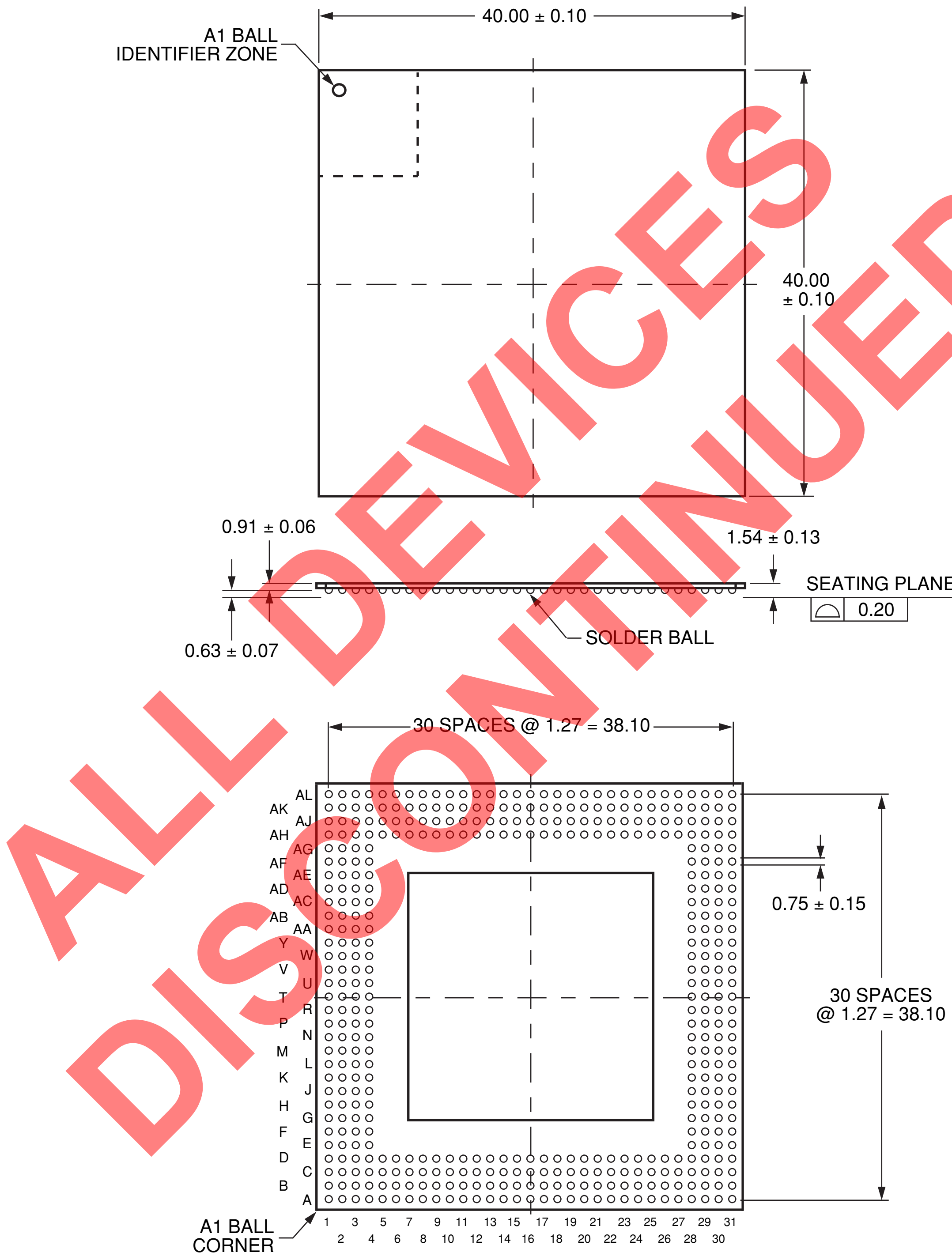
5-4407(F)

Note: Although the 36 thermal enhancement balls are stated as an option, they are standard on the 352 FPGA package.

Package Outline Diagrams (continued)

432-Pin EBGA

Dimensions are in millimeters.

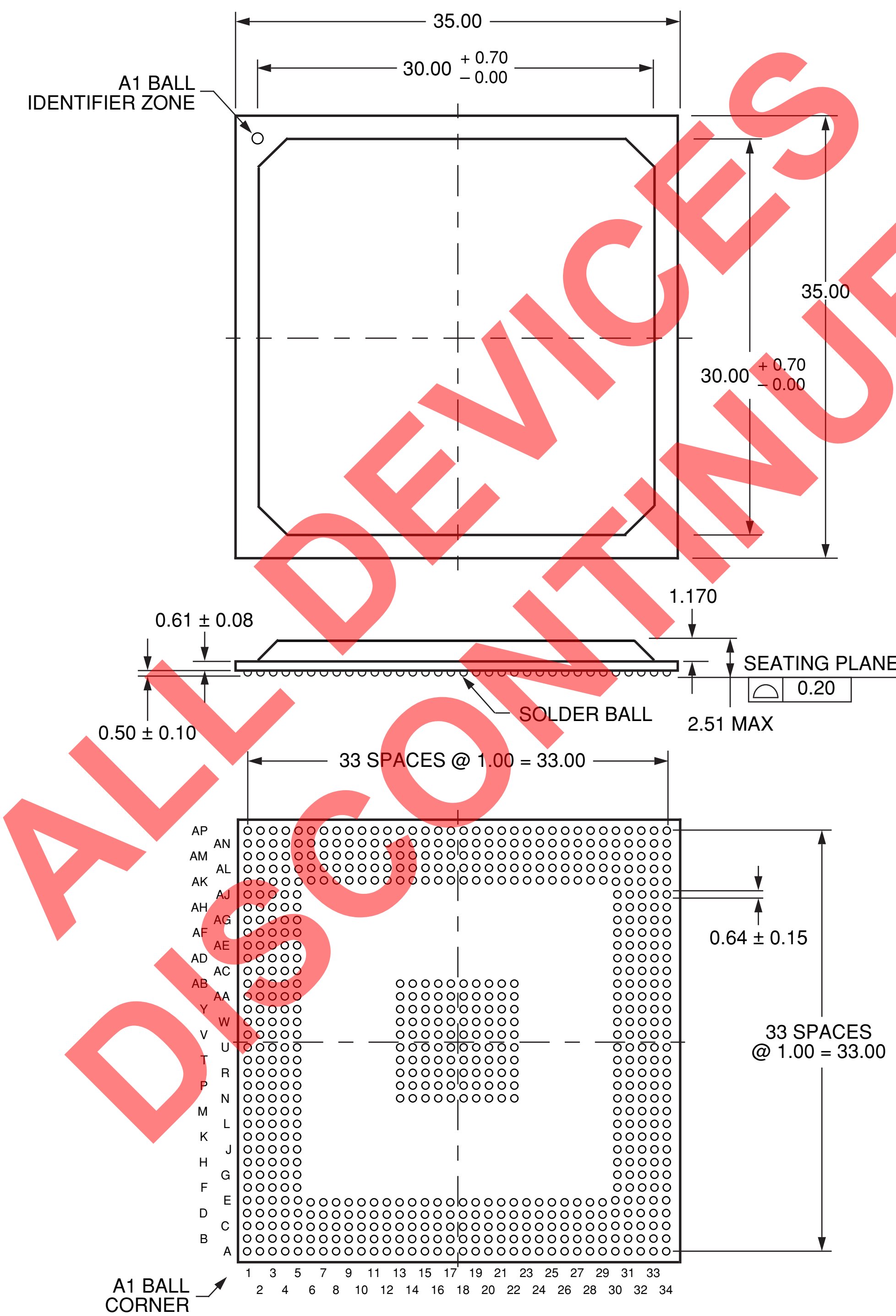


5-4409(F)

Package Outline Diagrams (continued)

680-Pin PBGAM

Dimensions are in millimeters.



5-4406(F)

Ordering Information

OR3LXXXB X XX XXX X – XX

Device Family
OR3L165B
OR3L225B

Speed Grade

Package Type
BA = Plastic Ball Grid Array (PBGA)
BC = Enhanced Ball Grid Array (EBGA)
BM = Fine-Pitch Ball Grid Array, Multilayer (PBGAM)
PS = Power Quad Shrink Flat Package (SQFP2)

Packing Designator
DB = Dry Packed Tray

Grade
Blank = Commercial
I = Industrial

Pin/Ball Count

Table 35. Voltage Options

Device	Voltage
OR3LxxxB	2.5 V internal/3.3 V I/O

Table 36. Ordering Information

Commercial

Device Family	Part Number	Speed Grade	Package Type	Pin/Ball Count	Grade	Packing Designator
OR3L165B	OR3L165B8PS208-DB[1]	8	SQFP2	208	C	DB
	OR3L165B8PS240-DB[1]	8	SQFP2	240	C	DB
	OR3L165B8BA352-DB	8	PBGA	352	C	DB
	OR3L165B8BC432-DB	8	EBGA	432	C	DB
	OR3L165B8BM680-DB	8	PBGAM	680	C	DB
	OR3L165B7PS208-DB[1]	7	SQFP2	208	C	DB
	OR3L165B7PS240-DB[1]	7	SQFP2	240	C	DB
	OR3L165B7BA352-DB	7	PBGA	352	C	DB
	OR3L165B7BC432-DB	7	EBGA	432	C	DB
	OR3L165B7BM680-DB	7	PBGAM	680	C	DB
OR3L225B	OR3L225B8BC432-DB[1]	8	EBGA	432	C	DB
	OR3L225B8BM680-DB[1]	8	PBGAM	680	C	DB
	OR3L225B7BC432-DB[1]	7	EBGA	432	C	DB
	OR3L225B7BM680-DB[1]	7	PBGAM	680	C	DB

1. Discontinued per PCN #06-07. Contact Rochester Electronics for available inventory.

Industrial

Device Family	Part Number	Speed Grade	Package Type	Pin/Ball Count	Grade	Packing Designator
OR3L165B	OR3L165B7PS208I-DB[1]	7	SQFP2	208	I	DB
	OR3L165B7PS240I-DB[1]	7	SQFP2	240	I	DB
	OR3L165B7BA352I-DB	7	PBGA	352	I	DB
	OR3L165B7BC432I-DB	7	EBGA	432	I	DB
	OR3L165B7BM680I-DB	7	PBGAM	680	I	DB
OR3L225B	OR3L225B7BC432I-DB[1]	7	EBGA	432	I	DB
	OR3L225B7BM680I-DB[1]	7	PBGAM	680	I	DB

1. Discontinued per PCN #06-07. Contact Rochester Electronics for available inventory

March 2002
DA99-011FPGA (Replaces DA99-008FPGA and must accompany DS99-087FPGA)

Lattice Semiconductor Corporation

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- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
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