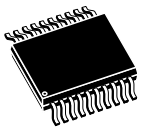
# STM8AF6213/13A STM8AF6223/23A STM8AF6226

## Automotive 8-bit MCU, with up to 8-Kbyte Flash memory, data EEPROM, 10-bit ADC, timers, LIN, SPI, I²C, 3 to 5.5 V

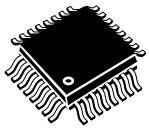
**Datasheet - production data**

## Features

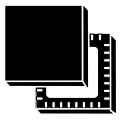
- AEC-Q100 qualified
- Core
  - Max $f_{CPU}$: 16 MHz
  - Advanced STM8A core with Harvard architecture and 3-stage pipeline
  - Extended instruction set
- Memories
  - Program memory: 4 to 8 Kbyte Flash program; data retention 20 years at 55 °C after 1 kcycle
  - Data memory: 640 byte true data EEPROM; endurance 300 kcycle
  - RAM: 1 Kbyte
- Clock management
  - Low-power crystal resonator oscillator with external clock input
  - Internal, user-trimmable 16 MHz RC and low-power 128 kHz RC oscillators
  - Clock security system with clock monitor
- Reset and supply management
  - Wait/auto-wakeup/Halt low-power modes with user definable clock gating
  - Low-consumption power-on and power-down reset
- Interrupt management
  - Nested interrupt controller with 32 interrupts
  - Up to 28 external interrupts on 7 vectors
- Timers
  - Advanced control timer: 16-bit, 4 CAPCOM channels, 3 complementary outputs, dead-time insertion and flexible synchronization
  - 16-bit general purpose timer with 3 CAPCOM channels each (IC, OC, PWM)
  - 8-bit AR basic timer with 8-bit prescaler
  - Auto-wakeup timer
  - Window and independent watchdog timers



TSSOP20 (6.4x4.4 mm)



LQFP32 7x7 mm



VFQFPN32 (5x5 mm)

- I/Os
  - Up to 28 I/Os on a 32-pin package including 21 high sink outputs
  - Highly robust I/O design, immune against current injection
- Communication interfaces
  - LINUART LIN 2.2 compliant, master/slave modes with automatic resynchronization
  - SPI interface up to 8 Mbit/s or $f_{MASTER}/2$
  - $I^2C$ interface up to 400 Kbit/s
- Analog to digital converter (ADC)
  - 10-bit, ± 1 LSB ADC with up to 7 muxed channels + 1 internal channel, scan mode and analog watchdog
  - Internal reference voltage measurement
- Operating temperature up to 150 °C



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# 1 Introduction

The datasheet contains the description of STM8AF6213, STM8AF6213A, STM8AF6223, STM8AF6223A and STM8AF6226 features, pinout, electrical characteristics, mechanical data and ordering information.

- For complete information on the STM8A microcontroller memory, registers and peripherals, please refer to STM8S series and STM8AF series 8-bit microcontrollers reference manual (RM0016).
- For information on programming, erasing and protection of the internal Flash memory please refer to the STM8 Flash programming manual (PM0051).
- For information on the debug and SWIM (single wire interface module) refer to the STM8 SWIM communication protocol and debug module user manual (UM0470).
- For information on the STM8 core, please refer to the STM8 CPU programming manual (PM0044).

# 2 Description

The STM8AF6213, STM8AF6213A, STM8AF6223, STM8AF6223A and STM8AF6226 automotive 8-bit microcontrollers offer 4 to 8 Kbytes of Flash program memory, plus integrated true data EEPROM. The STM8S series and STM8AF series 8-bit microcontrollers reference manual (RM0016) refers to devices in this family as low-density. They provide the following benefits: performance, robustness and reduced system cost.

Device performance and robustness are ensured by advanced core and peripherals made in a state-of-the-art technology, a 16 MHz clock frequency, robust I/Os, independent watchdogs with separate clock source, and a clock security system.

The system cost is reduced thanks to an integrated true data EEPROM for up to 300 k write/erase cycles and a high system integration level with internal clock oscillators, watchdog, and brown-out reset.

Full documentation is offered as well as a wide choice of development tools.

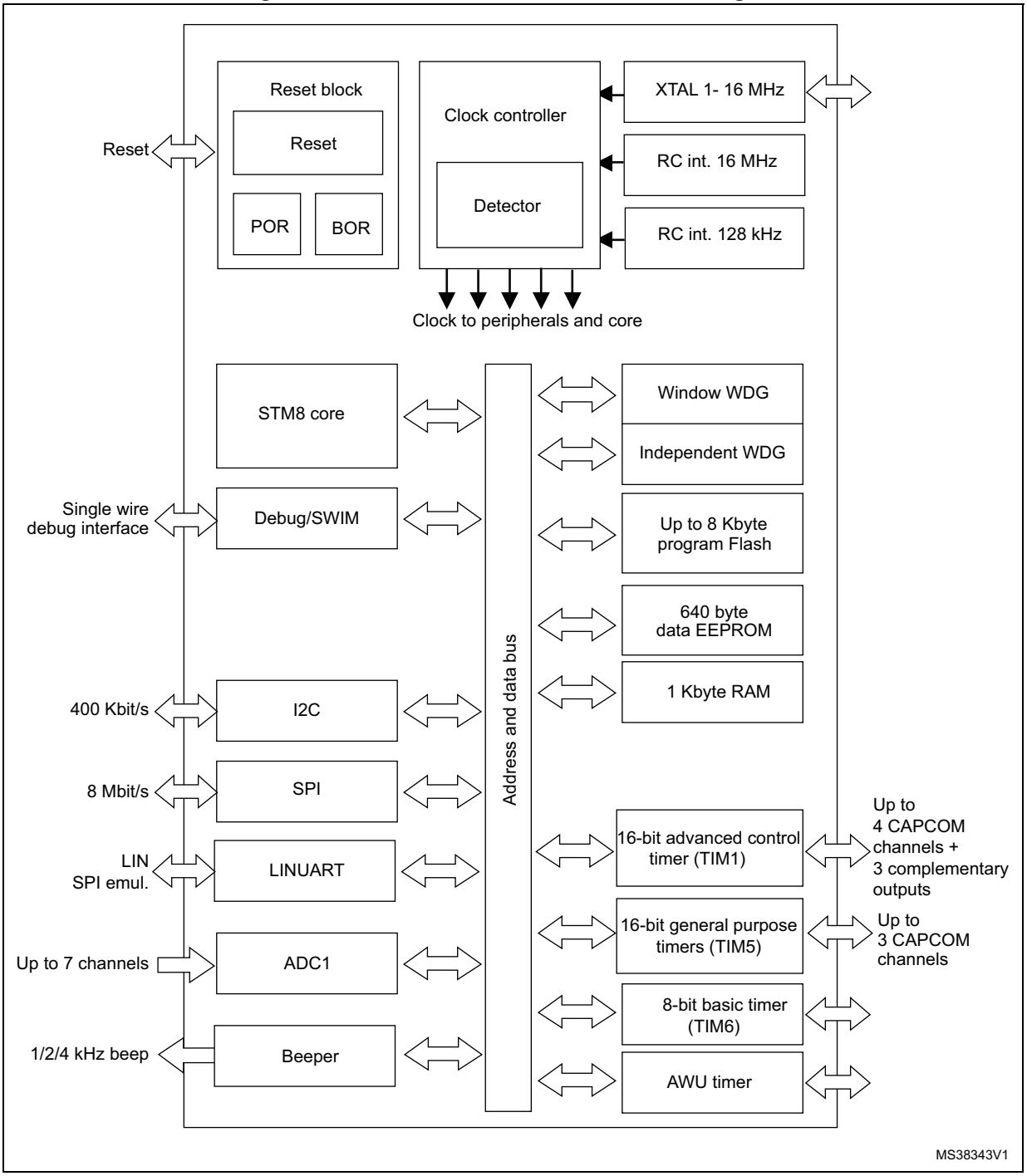
**Table 1. STM8AF6213/13A/23/23A/26 features**

| Device | STM8AF6226 | STM8AF6223 | STM8AF6223A | STM8AF6213 | STM8AF6213A |
|---|---|---|---|---|---|
| Pin count | 32 | 20 | | | |
| Max. number of GPIOs | 28 including 21 high-sink I/Os | 16 including 12 high-sink I/Os | | | |
| Ext. interrupt pins | 28 | 16 | | | |
| Timer CAPCOM channels | 6 | 7 | 6 | 7 | 6 |
| Timer complementary outputs | 3 | 1 | 2 | 1 | 2 |
| A/D converter channels | 7 | 5 | 7 | 5 | 7 |
| Low-density Flash program memory (byte) | 8 K | | | 4 K | |
| Data EEPROM (byte) | 640(1) | | | | |
| RAM (byte) | 1 K | | | | |
| Peripheral set | Multipurpose timer (TIM1), SPI, I2C, LINUART, window WDG, independent WDG, ADC, PWM timer (TIM5), 8-bit timer (TIM6) | | | | |

1. No read-while-write (RWW) capability.

# 3 Block diagram

**Figure 1. STM8AF6213/13A/23/23A/26 block diagram**




1. **Legend:** ADC (Analog-to-digital converter), beCAN (Controller area network), BOR (Brownout reset), I²C (Inter-integrated circuit multimaster interface),IWDG (Independent window watchdog), LINUART (Local interconnect network universal asynchronous receiver transmitter), POR (Power on reset), SPI (Serial peripheral interface), SWIM (Single wire interface module), USART (Universal synchronous asynchronous receiver transmitter), Window WDG (Window watchdog).

# 4 Product overview

The following section intends to give an overview of the basic features of the products covered by this datasheet.

For more detailed information on each feature please refer to STM8S series and STM8AF series 8-bit microcontrollers reference manual (RM0016).

## 4.1 Central processing unit (CPU)

The 8-bit STM8 core is designed for code efficiency and performance.

It contains 6 internal registers which are directly addressable in each execution context, 20 addressing modes including indexed indirect and relative addressing and 80 instructions.

### 4.1.1 Architecture and registers

- Harvard architecture
- 3-stage pipeline
- 32-bit wide program memory bus - single cycle fetching for most instructions
- X and Y 16-bit index registers, enabling indexed addressing modes with or without offset and read-modify-write type data manipulations
- 8-bit accumulator
- 24-bit program counter - 16-Mbyte linear memory space
- 16-bit stack pointer - access to a 64 Kbyte level stack
- 8-bit condition code register - 7 condition flags for the result of the last instruction.

### 4.1.2 Addressing

- 20 addressing modes
- Indexed indirect addressing mode for look-up tables located anywhere in the address space
- Stack pointer relative addressing mode for local variables and parameter passing

### 4.1.3 Instruction set

- 80 instructions with 2-byte average instruction size
- Standard data movement and logic/arithmetic functions
- 8-bit by 8-bit multiplication
- 16-bit by 8-bit and 16-bit by 16-bit division
- Bit manipulation
- Data transfer between stack and accumulator (push/pop) with direct stack access
- Data transfer using the X and Y registers or direct memory-to-memory transfers

## 4.2 Single wire interface module (SWIM) and debug module (DM)

The single wire interface module together with an integrated debug module permit non-intrusive, real-time in-circuit debugging and fast memory programming.

### 4.2.1 SWIM

Single wire interface module for direct access to the debug mode and memory programming. The interface can be activated in all device operation modes.The maximum data transmission speed is 145 byte/ms.

### 4.2.2 Debug module

The non-intrusive debugging module features a performance close to a full-featured emulator. Besides memory and peripheral operation, CPU operation can also be monitored in real-time by means of shadow registers.

- R/W to RAM and peripheral registers in real-time
- R/W access to all resources by stalling the CPU
- Breakpoints on all program-memory instructions (software breakpoints)
- Two advanced breakpoints, 23 predefined breakpoint configurations

## 4.3 Interrupt controller

- Nested interrupts with three software priority levels
- 32 interrupt vectors with hardware priority
- Up to 28 external interrupts on 7 vectors including TLI
- Trap and reset interrupts

## 4.4 Flash program and data EEPROM memory

- Up to 8 Kbytes of Flash program single voltage Flash memory
- 640 byte true data EEPROM
- User option byte area

### 4.4.1 Write protection (WP)

Write protection of Flash program memory and data EEPROM is provided to avoid unintentional overwriting of memory that could result from a user software malfunction.

There are two levels of write protection. The first level is known as MASS (memory access security system). MASS is always enabled and protects the main Flash program memory, data EEPROM and option byte.

To perform in-application programming (IAP), this write protection can be removed by writing a MASS key sequence in a control register. This allows the application to write to data EEPROM, modify the contents of main program memory or the device option byte.

A second level of write protection, can be enabled to further protect a specific area of memory known as UBC (user boot code). Refer to the figure below.

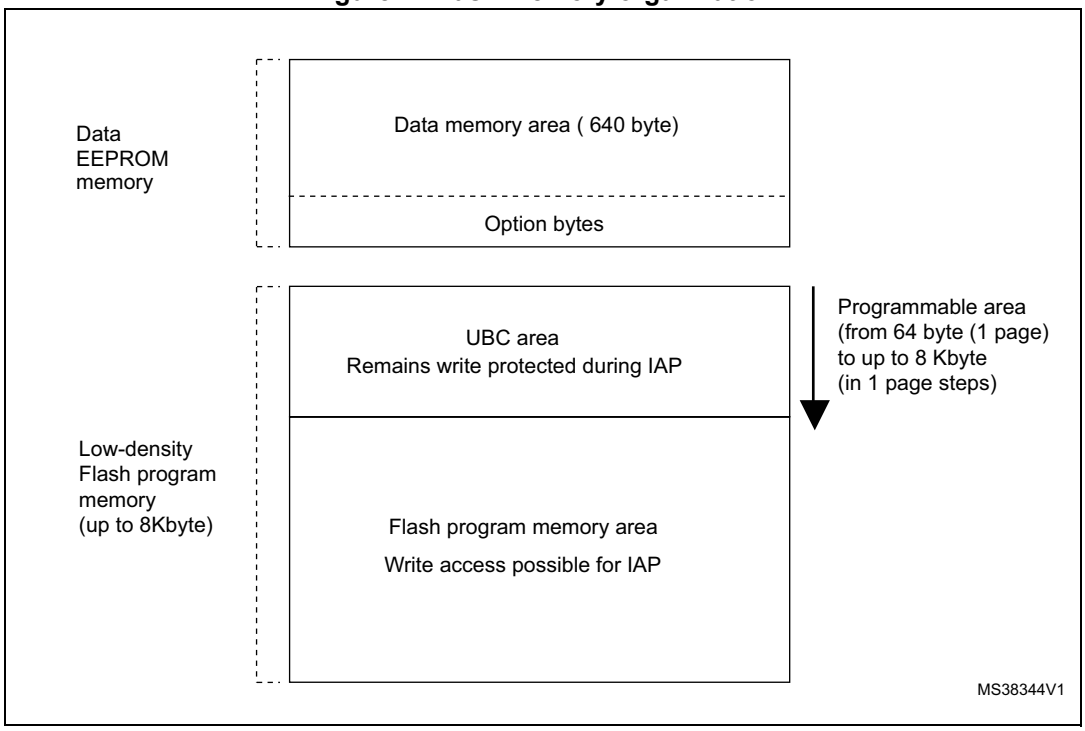
The size of the UBC is programmable through the UBC option byte, in increments of 1 page (64-byte block) by programming the UBC option byte in ICP mode.

This divides the program memory into two areas:

- Main program memory: up to 8 Kbyte minus UBC
- User-specific boot code (UBC): configurable up to 8 Kbyte

The UBC area remains write-protected during in-application programming. This means that the MASS keys do not unlock the UBC area. It protects the memory used to store the boot program, specific code libraries, reset and interrupt vectors, the reset routine and usually the IAP and communication routines.

**Figure 2. Flash memory organization**




### 4.4.2 Read-out protection (ROP)

The read-out protection blocks reading and writing the Flash program memory and data EEPROM memory in ICP mode (and debug mode). Once the read-out protection is activated, any attempt to toggle its status triggers a global erase of the program and data memory. Even if no protection can be considered as totally unbreakable, the feature provides a very high level of protection for a general purpose microcontroller.

## 4.5 Clock controller

The clock controller distributes the system clock ($f_{MASTER}$) coming from different oscillators to the core and the peripherals. It also manages clock gating for low-power modes and ensures clock robustness.

### 4.5.1 Features

- **Clock prescaler**: to get the best compromise between speed and current consumption the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler.
- **Safe clock switching**: Clock sources can be changed safely on the fly in Run mode through a configuration register. The clock signal is not switched until the new clock source is ready. The design guarantees glitch-free switching.
- **Clock management**: To reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- **Master clock sources:** four different clock sources can be used to drive the master clock:
  - 1-16 MHz high-speed external crystal (HSE)
  - Up to 16 MHz high-speed user-external clock (HSE user-ext)
  - 16 MHz high-speed internal RC oscillator (HSI)
  - 128 kHz low-speed internal RC (LSI)
- **Startup clock**: after reset, the microcontroller restarts by default with an internal 2 MHz clock (HSI/8). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.
- **Clock security system (CSS)**: this feature can be enabled by software. If an HSE clock failure occurs, the internal RC (16 MHz/8) is automatically selected by the CSS and an interrupt can optionally be generated.
- **Configurable main clock output (CCO)**: This outputs an external clock for use by the application.

**Table 2. Peripheral clock gating bit assignments in CLK_PCKENR1/2 registers**

| Bit | Peripheral clock | Bit | Peripheral clock | Bit | Peripheral clock | Bit | Peripheral clock |
|---|---|---|---|---|---|---|---|
| PCKEN17 | TIM1 | PCKEN13 | LINUART | PCKEN27 | Reserved | PCKEN23 | ADC |
| PCKEN16 | TIM5 | PCKEN12 | Reserved | PCKEN26 | Reserved | PCKEN22 | AWU |
| PCKEN15 | Reserved | PCKEN11 | SPI | PCKEN25 | Reserved | PCKEN21 | Reserved |
| PCKEN14 | TIM6 | PCKEN10 | $I^2C$ | PCKEN24 | Reserved | PCKEN20 | Reserved |

## 4.6 Power management

For efficient power management, the application can be put in one of four different low-power modes. Users can configure each mode to obtain the best compromise between lowest power consumption, fastest start-up time and available wakeup sources.

- **Wait mode**: in this mode, the CPU is stopped but peripherals are kept running. The wakeup is performed by an internal or external interrupt or reset.
- **Active-halt mode with regulator on**: in this mode, the CPU and peripheral clocks are stopped. An internal wakeup is generated at programmable intervals by the auto wake up unit (AWU). The main voltage regulator is kept powered on, so current consumption is higher than in Active-halt mode with regulator off, but the wakeup time is faster. Wakeup is triggered by the internal AWU interrupt, external interrupt or reset.
- **Active-halt mode with regulator off**: this mode is the same as Active-halt with regulator on, except that the main voltage regulator is powered off, so the wake up time is slower.
- **Halt mode**: in this mode the microcontroller uses the least power. The CPU and peripheral clocks are stopped, the main voltage regulator is powered off. Wakeup is triggered by external event or reset.

## 4.7 Watchdog timers

The watchdog system is based on two independent timers providing maximum security to the applications.

Activation of the watchdog timers is controlled by option bytes or by software. Once activated, the watchdogs cannot be disabled by the user program without performing a reset.

### Window watchdog timer

The window watchdog is used to detect the occurrence of a software fault, usually generated by external interferences or by unexpected logical conditions, which cause the application program to abandon its normal sequence.

The window function can be used to trim the watchdog behavior to match the application timing perfectly. The application software must refresh the counter before time-out and during a limited time window.

A reset is generated in two situations:

1. Timeout: at 16 MHz CPU clock the time-out period can be adjusted between 75 µs up to 64 ms.
2. Refresh out of window: the downcounter is refreshed before its value is lower than the one stored in the window register.

### Independent watchdog timer

The independent watchdog peripheral can be used to resolve processor malfunctions due to hardware or software failures.

It is clocked by the 128 kHz LSI internal RC clock source, and thus stays active even in case of a CPU clock failure.

The IWDG time base spans from 60 µs to 1 s

## 4.8 Auto wakeup counter

- Used for auto wakeup from active halt mode
- Clock source: Internal 128 kHz internal low frequency RC oscillator or external clock
- LSI clock can be internally connected to TIM1 input capture channel 1 for calibration

## 4.9 Beeper

The beeper function outputs a signal on the BEEP pin for sound generation. The signal is in the range of 1, 2 or 4 kHz.

The beeper output port is only available through the alternate function remap option bit AFR7.

## 4.10 TIM1 - 16-bit advanced control timer

This is a high-end timer designed for a wide range of control applications. With its complementary outputs, dead-time control and center-aligned PWM capability, the field of applications is extended to motor control, lighting and half-bridge driver.

- 16-bit up, down and up/down auto-reload counter with 16-bit fractional prescaler.
- Four independent capture/compare channels (CAPCOM) configurable as input capture, output compare, PWM generation (edge and center aligned mode) and single pulse mode output.
- Synchronization module to control the timer with external signals or to synchronise with TIM5 or TIM6
- Break input to force the timer outputs into a defined state
- Three complementary outputs with adjustable dead time
- Encoder mode
- Interrupt sources: 3 x input capture/output compare, 1 x overflow/update, 1 x break

## 4.11 TIM5 - 16-bit general purpose timer

- 16-bit autoreload (AR) up-counter
- 15-bit prescaler adjustable to fixed power of 2 ratios 1…32768
- 3 individually configurable capture/compare channels
- PWM mode
- Interrupt sources: 3 x input capture/output compare, 1 x overflow/update
- Synchronization module to control the timer with external signals or to synchronize with TIM1 or TIM6

## 4.12 TIM6 - 8-bit basic timer

- 8-bit autoreload, adjustable prescaler ratio to any power of 2 from 1 to 128
- Clock source: CPU clock
- Interrupt source: 1 x overflow/update
- Synchronization module to control the timer with external signals or to synchronize with TIM1 or TIM5.

**Table 3. TIM timer features**

| Timer | Counter size (bits) | Prescaler | Counting mode | CAPCOM channels | Complementary outputs | Ext. trigger | Timer synchronization/ chaining |
|---|---|---|---|---|---|---|---|
| TIM1 | 16 | Any integer from 1 to 65536 | Up/down | 4 | 3 | Yes | Yes |
| TIM5 | 16 | Any power of 2 from 1 to 32768 | Up | 3 | 0 | No | |
| TIM6 | 8 | Any power of 2 from 1 to 128 | Up | 0 | 0 | No | |

## 4.13 Analog-to-digital converter (ADC1)

The STM8AF6213, STM8AF6213A, STM8AF6223, STM8AF6223A and STM8AF6226 products contain a 10-bit successive approximation A/D converter (ADC1) with up to 7 external and 1 internal multiplexed input channels and the following main features:

- Input voltage range: 0 to $V_{DD}$
- Input voltage range: 0 to $V_{DDA}$
- Conversion time: 14 clock cycles
- Single and continuous and buffered continuous conversion modes
- Buffer size (n x 10 bits) where n = number of input channels
- Scan mode for single and continuous conversion of a sequence of channels
- Analog watchdog capability with programmable upper and lower thresholds
- Internal reference voltage on channel AIN7
- Analog watchdog interrupt
- External trigger input
- Trigger from TIM1 TRGO
- End of conversion (EOC) interrupt

*Note: Additional AIN12 analog input is not selectable in ADC scan mode or with analog watchdog. Values converted from AIN12 are stored only into the ADC_DRH/ADC_DRL registers.*

### Internal bandgap reference voltage

Channel AIN7 is internally connected to the internal bandgap reference voltage. The internal bandgap reference is constant and can be used, for example, to monitor $V_{DD}$. It is independent of variations in $V_{DD}$ and ambient temperature $T_A$.

## 4.14 Communication interfaces

The following communication interfaces are implemented:

- LINUART: Full feature UART, synchronous mode, SPI master mode, Smartcard mode, IrDA mode, single wire mode, LIN2.2 capability
- SPI: full and half-duplex, 8 Mbit/s
- I²C: up to 400 Kbit/s

Some peripheral names differ between the datasheet and STM8S series and STM8AF series 8-bit microcontrollers reference manual, RM0016 (see *Table 4*).

**Table 4. Communication peripheral naming correspondence**

| Peripheral name in datasheet | Peripheral name in reference manual (RM0016) |
|---|---|
| LINUART | UART4 |

### 4.14.1 LINUART

#### Main features

- 1 Mbit/s full duplex SCI
- SPI emulation
- High precision baud rate generator
- Smartcard emulation
- IrDA SIR encoder decoder
- LIN mode
- Single wire half duplex mode

#### LIN mode

**Master mode:**

- LIN break and delimiter generation
- LIN break and delimiter detection with separate flag and interrupt source for read back checking.

**Slave mode:**

- Autonomous header handling – one single interrupt per valid header
- Mute mode to filter responses
- Identifier parity error checking
- LIN automatic resynchronization, allowing operation with internal RC oscillator (HSI) clock source
- Break detection at any time, even during a byte reception
- Header errors detection:
  - Delimiter too short
  - Synch field error
  - Deviation error (if automatic resynchronization is enabled)
  - Framing error in synch field or identifier field
  - Header time-out

### Asynchronous communication (UART mode)

- Full duplex communication - NRZ standard format (mark/space)
- Programmable transmit and receive baud rates up to 1 Mbit/s ($f_{CPU}$/16) and capable of following any standard baud rate regardless of the input frequency
- Separate enable bits for transmitter and receiver
- Two receiver wakeup modes:
  - Address bit (MSB)
  - Idle line (interrupt)
- Transmission error detection with interrupt generation
- Parity control

### Synchronous communication

- Full duplex synchronous transfers
- SPI master operation
- 8-bit data communication
- Maximum speed: 1 Mbit/s at 16 MHz ($f_{CPU}$/16)

## 4.14.2 Serial peripheral interface (SPI)

- Maximum speed: 8 Mbit/s ($f_{MASTER}$/2) both for master and slave
- Full duplex synchronous transfers
- Simplex synchronous transfers on two lines with a possible bidirectional data line
- Master or slave operation - selectable by hardware or software
- CRC calculation
- 1 byte Tx and Rx buffer
- Slave /master selection input pin

## 4.14.3 Inter integrated circuit ($I^2C$) interface

- $I^2C$ master features:
  - Clock generation
  - Start and stop generation
- $I^2C$ slave features:
  - Programmable $I^2C$ address detection
  - Stop bit detection
- Generation and detection of 7-bit/10-bit addressing and general call
- Supports different communication speeds:
  - Standard speed (up to 100 kHz),
  - Fast speed (up to 400 kHz)

# 5 Pinout and pin description

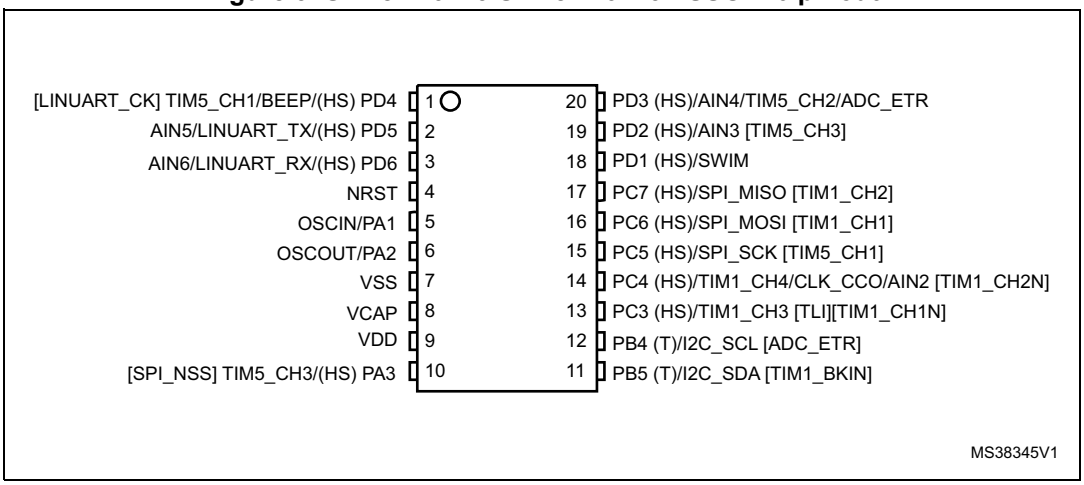
The following table presents the meaning of the abbreviations in use in the pin description tables in this section.

**Table 5. Legend/abbreviations for pinout tables**

| | | |
|---|---|---|
| Type | I= input, O = output, S = power supply | |
| Level | Input | CM = CMOS (standard for all I/Os) |
| | Output | HS = High sink |
| Output speed | O1 = Slow (up to 2 MHz)<br>O2 = Fast (up to 10 MHz)<br>O3 = Fast/slow programmability with slow as default state after reset<br>O4 = Fast/slow programmability with fast as default state after reset | |
| Port and control configuration | Input | float = floating, wpu = weak pull-up |
| | Output | T = true open drain, OD = open drain, PP = push pull |
| Reset state | Bold X (pin state after internal reset release).<br>Unless otherwise specified, the pin state is the same during the reset phase and after the internal reset release. | |

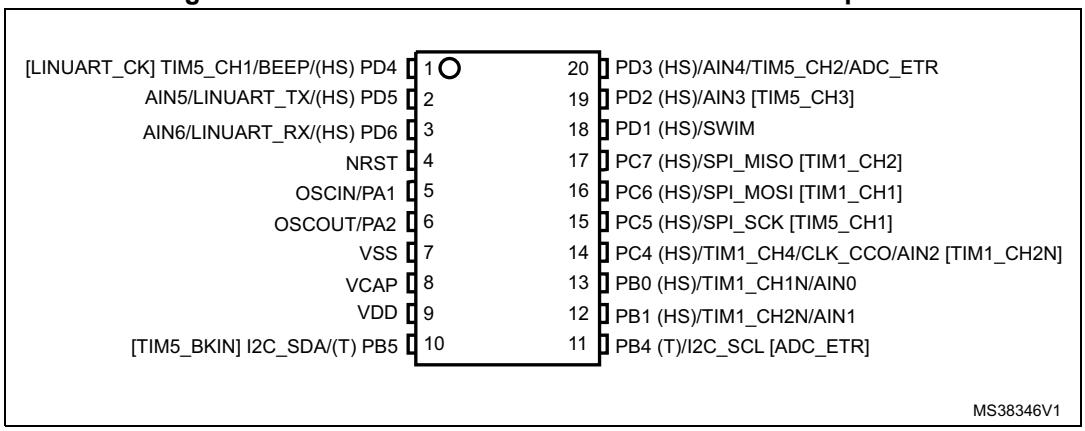
## 5.1 TSSOP20 pinouts and pin descriptions

**Figure 3. STM8AF6213/STM8AF6223 TSSOP20 pinout**




1. (HS) high sink capability.
2. (T) true open drain (P-buffer and protection diode to $V_{DD}$ not implemented).
3. [ ] alternate function remapping option (if the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).

**Figure 4. STM8AF6213A and STM8AF6223A TSSOP20 pinout**




1. (HS) high sink capability.
2. (T) true open drain (P-buffer and protection diode to $V_{DD}$ not implemented).
3. [ ] alternate function remapping option (if the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).

**Table 6. STM8AF6213/STM8AF6223 TSSOP20 pin description**

| TSSOP | Pin name | Type | Input | | | Output | | | | Main function (after reset) | Default alternate function | Alternate function after remap [option bit] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | floating | wpu | Ext. interrupt | High sink(1) | Speed | OD | PP | | | |
| 1 | PD4/ TIM5_CH1/ BEEP [LINUART_CK] | I/O | **X** | X | X | HS | O3 | X | X | Port D4 | Timer 5 - channel 1/BEEP output | LINUART clock [AFR2] |
| 2 | PD5/ AIN5/ LINUART_TX | I/O | **X** | X | X | HS | O3 | X | X | Port D5 | Analog input 5/ LINUART data transmit | - |
| 3 | PD6/ AIN6/ LINUART_RX | I/O | **X** | X | X | HS | O3 | X | X | Port D6 | Analog input 6/ LINUART data receive | - |
| 4 | NRST | I/O | - | **X** | - | - | - | - | - | Reset | | |
| 5 | PA1/ OSCIN(2) | I/O | **X** | X | X | - | O1 | X | X | Port A1 | Resonator/ crystal in | - |
| 6 | PA2/ OSCOUT | I/O | **X** | X | X | O1 | X | X | | Port A2 | Resonator/ crystal out | - |
| 7 | VSS | S | - | - | - | - | - | - | - | Digital ground | | |
| 8 | VCAP | S | - | - | - | - | - | - | - | 1.8 V regulator capacitor | | |
| 9 | VDD | S | - | - | - | - | - | - | - | Digital power supply | | |

**Table 6. STM8AF6213/STM8AF6223 TSSOP20 pin description (continued)**

| TSSOP | Pin name | Type | Input | | | Output | | | | Main function (after reset) | Default alternate function | Alternate function after remap [option bit] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | floating | wpu | Ext. interrupt | High sink(1) | Speed | OD | PP | | | |
| 10 | PA3/ TIM5_CH3 [SPI_NSS] | I/O | **X** | X | X | HS | O3 | X | X | Port A3 | Timer 5 channel 3 | SPI master/ slave select [AFR1] |
| 11 | PB5/ I2C_SDA [TIM1_BKIN] | I/O | **X** | - | X | - | O1 | T(3) | - | Port B5 | I2C data | Timer 1 - break input [AFR4] |
| 12 | PB4/ I2C_SCL [ADC_ETR] | I/O | **X** | - | X | - | O1 | T(3) | - | Port B4 | I2C clock | ADC external trigger [AFR4] |
| 13 | PC3/ TIM1_CH3/[TLI]/[ TIM1_CH1N] | I/O | **X** | X | X | HS | O3 | X | X | Port C3 | Timer 1 - channel 3 | Top level interrupt [AFR3] Timer 1 inverted channel 1 [AFR7] |
| 14 | PC4/ TIM1_CH4/ CLK_CCO/AIN2/[ TIM1_CH2N] | I/O | **X** | X | X | HS | O3 | X | X | Port C4 | Timer 1 - channel 4 /configurabl e clock output | Analog input 2 [AFR2]Time r 1 inverted channel 2 [AFR7] |
| 15 | PC5/SPI_SCK [TIM5_CH1] | I/O | **X** | X | X | HS | O3 | X | X | Port C5 | SPI clock | Timer 5 channel 1 [AFR0] |
| 16 | PC6/ SPI_MOSI [TIM1_CH1] | I/O | **X** | X | X | HS | O3 | X | X | Port C6 | PI master out/slave in | Timer 1 channel 1 [AFR0] |
| 17 | PC7/ SPI_MISO [TIM1_CH2] | I/O | **X** | X | X | HS | O3 | X | X | Port C7 | SPI master in/ slave out | Timer 1 channel 2[AFR0] |
| 18 | PD1/ SWIM(4) | I/O | **X** | X | X | HS | O4 | X | X | Port D1 | SWIM data interface | - |

**Table 6. STM8AF6213/STM8AF6223 TSSOP20 pin description (continued)**

| TSSOP | Pin name | Type | Input | | | Output | | | | Main function (after reset) | Default alternate function | Alternate function after remap [option bit] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | floating | wpu | Ext. interrupt | High sink(1) | Speed | OD | PP | | | |
| 19 | PD2/AIN3 [TIM5_CH3] | I/O | **X** | X | X | HS | O3 | X | X | Port D2 | - | Analog input 3 [AFR2] Timer 52 - channel 3 [AFR1] |
| 20 | PD3/ AIN4/ TIM5_CH2/ ADC_ETR | I/O | **X** | X | X | HS | O3 | X | X | Port D3 | Analog input 4 Timer 52 - channel 2/ADC external trigger | - |

1. I/O pins used simultaneously for high current source/sink must be uniformly spaced around the package. In addition, the total driven current must respect the absolute maximum ratings (see *Section 10.2: Absolute maximum ratings*).
2. When the MCU is in Halt/Active-halt mode, PA1 is automatically configured in input weak pull-up and cannot be used for waking up the device. In this mode, the output state of PA1 is not driven. It is recommended to use PA1 only in input mode if Halt/Active-halt is used in the application.
3. In the open-drain output column, 'T' defines a true open-drain I/O (P-buffer, weak pull-up, and protection diode to VDD are not implemented)
4. The PD1 pin is in input pull-up during the reset phase and after internal reset release.

**Table 7. STM8AF6213A and STM8AF6223A TSSOP20 pin description**

| TSSOP | Pin name | Type | Input | | | Output | | | | Main function (after reset) | Default alternate function | Alternate function after remap [option bit] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | floating | wpu | Ext. interrupt | High sink(1) | Speed | OD | PP | | | |
| 1 | PD4/ TIM5_CH1/ BEEP/SPI_NSS [LINUART_CK] | I/O | **X** | X | X | HS | O3 | X | X | Port D4 | Timer 5 - channel 1/BEEP output | LINUART clock [AFR2] |
| 2 | PD5/ AIN5/ LINUART_TX | I/O | **X** | X | X | HS | O3 | X | X | Port D5 | Analog input 5/ LINUART data transmit | - |

**Table 7. STM8AF6213A and STM8AF6223A TSSOP20 pin description (continued)**

| TSSOP | Pin name | Type | Input | | | Output | | | | Main function (after reset) | Default alternate function | Alternate function after remap [option bit] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | floating | wpu | Ext. interrupt | High sink(1) | Speed | OD | PP | | | |
| 3 | PD6/ AIN6/ LINUART_RX | I/O | **X** | X | X | HS | O3 | X | X | Port D6 | Analog input 6/ LINUART data receive | - |
| 4 | NRST | I/O | - | **X** | - | - | - | - | - | Reset | | - |
| 5 | PA1/ OSCIN(2) | I/O | **X** | X | X | - | O1 | X | X | Port A1 | Resonator/ crystal in | - |
| 6 | PA2/ OSCOUT | I/O | **X** | X | X | - | O1 | X | X | Port A2 | Resonator/ crystal out | - |
| 7 | VSS | S | - | - | - | - | - | - | - | Digital ground | | - |
| 8 | VCAP | S | - | - | - | - | - | - | - | 1.8 V regulator capacitor | | - |
| 9 | VDD | S | - | - | - | - | - | - | - | Digital power supply | | - |
| 10 | PB5/ I2C_SDA [TIM1_BKIN] | I/O | **X** | - | X | - | O1 | T(3) | - | Port B5 | I2C data | Timer 1 - break input [AFR4] |
| 11 | PB4/ I2C_SCL [ADC_ETR] | I/O | **X** | - | X | - | O1 | T(3) | - | Port B4 | I2C clock | ADC external trigger [AFR4] |
| 12 | PB1/ TIM1_CH2N/ AIN1 | I/O | **X** | X | X | HS | O3 | X | X | Port B1 | Timer 1 - inverted channel 2/Analog input 1 | - |
| 13 | PB0/ TIM1_CH1N/AIN0 | I/O | **X** | X | X | HS | O3 | X | X | Port B0 | Timer 1 - inverted channel 1/Analog input 0 | - |
| 14 | PC4/ TIM1_CH4/ CLK_CCO/AIN2/[ TIM1_CH2] | I/O | **X** | X | X | HS | O3 | X | X | Port C4 | Timer 1 - channel 4 /configurable clock output | Analog input 2 [AFR2]Timer 1 channel 2 [AFR7] |
| 15 | PC5/SPI_SCK [TIM5_CH1] | I/O | **X** | X | X | HS | O3 | X | X | Port C5 | SPI clock | Timer 5 channel 1 [AFR0] |

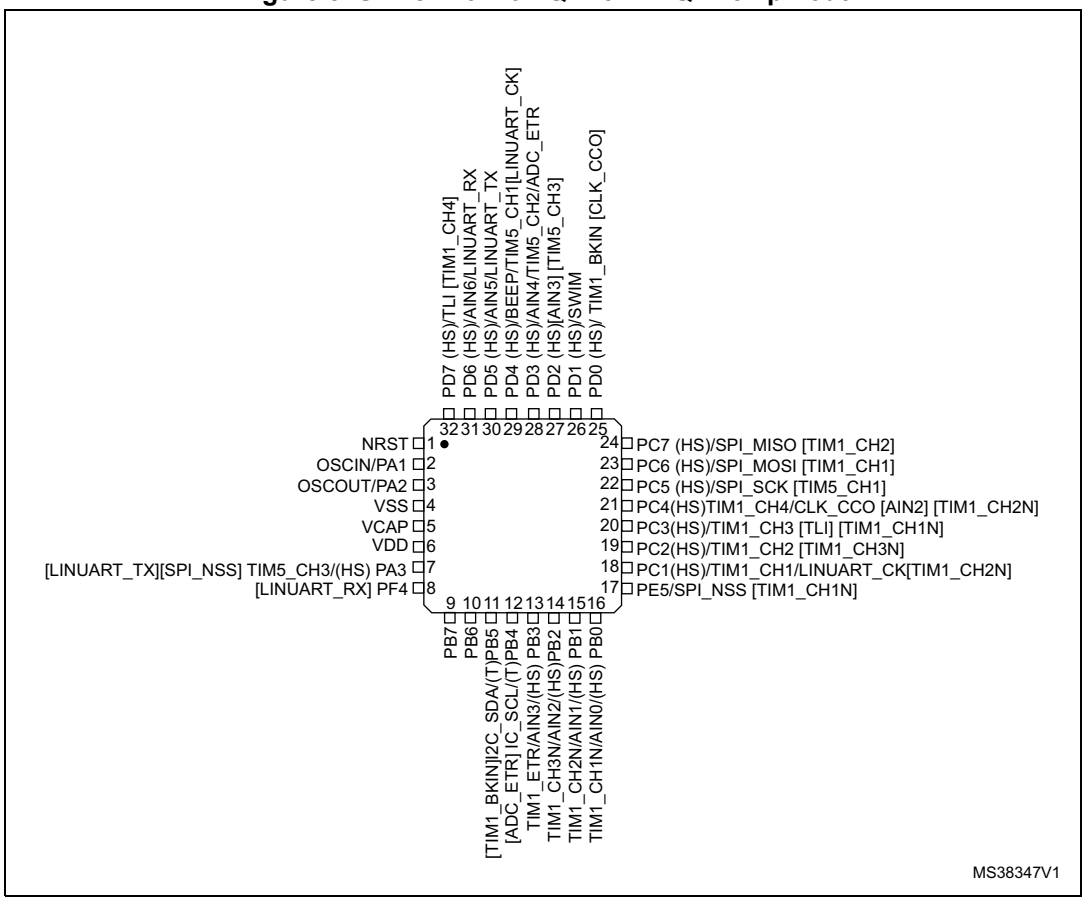
**Table 7. STM8AF6213A and STM8AF6223A TSSOP20 pin description (continued)**

| TSSOP | Pin name | Type | Input | | | Output | | | | Main function (after reset) | Default alternate function | Alternate function after remap [option bit] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | floating | wpu | Ext. interrupt | High sink(1) | Speed | OD | PP | | | |
| 16 | PC6/ SPI_MOSI [TIM1_CH1] | I/O | X | X | X | HS | O3 | X | X | Port C6 | PI master out/slave in | Timer 1 channel 1 [AFR0] |
| 17 | PC7/ SPI_MISO [TIM1_CH2] | I/O | X | X | X | HS | O3 | X | X | Port C7 | SPI master in/ slave out | Timer 1 channel 2[AFR0] |
| 18 | PD1/ SWIM(4) | I/O | X | X | X | HS | O4 | X | X | Port D1 | SWIM data interface | - |
| 19 | PD2/AIN3/ TLI[TIM5_CH3] | I/O | X | X | X | HS | O3 | X | X | Port D2 | - | Analog input 3 [AFR2] Timer 5 - channel 3 [AFR1] |
| 20 | PD3/ AIN4/ TIM5_CH2/ ADC_ETR | I/O | X | X | X | HS | O3 | X | X | Port D3 | Analog input 4 Timer 52 - channel 2/ADC external trigger | - |

1. I/O pins used simultaneously for high current source/sink must be uniformly spaced around the package. In addition, the total driven current must respect the absolute maximum ratings (see *Section 10.2: Absolute maximum ratings*).
2. When the MCU is in Halt/Active-halt mode, PA1 is automatically configured in input weak pull-up and cannot be used for waking up the device. In this mode, the output state of PA1 is not driven. It is recommended to use PA1 only in input mode if Halt/Active-halt is used in the application.
3. In the open-drain output column, 'T' defines a true open-drain I/O (P-buffer, weak pull-up, and protection diode to VDD are not implemented).
4. The PD1 pin is in input pull-up during the reset phase and after internal reset release.

## 5.2 LQFP32/VFQPN32 pinout and pin description

**Figure 5. STM8AF6226 LQFP32/VFQPN32 pinout**




1. (HS) high sink capability.
2. (T) true open drain (P-buffer and protection diode to $V_{DD}$ not implemented).
3. [ ] alternate function remapping option (if the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).

**Table 8. STM8AF6226 LQFP32/VFQPN32 pin description**

| LQFP32 VFQPN32 | Pin name | Type | Input | | | Output | | | | Main function (after reset) | Default alternate function | Alternate function after remap [option bit] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | floating | wpu | Ext. interrupt | High sink(1) | Speed | OD | PP | | | |
| 1 | NRST | I/O | - | **X** | - | - | - | - | - | Reset | | - |
| 2 | PA1/ OSCIN(2) | I/O | **X** | X | X | - | O1 | X | X | Port A1 | Resonator/ crystal in | - |
| 3 | PA2/ OSCOUT | I/O | **X** | X | X | - | O1 | X | X | Port A2 | Resonator/ crystal out | - |

**Table 8. STM8AF6226 LQFP32/VFQPN32 pin description (continued)**

| LQFP32 VFQPN32 | Pin name | Type | Input | | | Output | | | | Main function (after reset) | Default alternate function | Alternate function after remap [option bit] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | floating | wpu | Ext. interrupt | High sink(1) | Speed | OD | PP | | | |
| 4 | VSS | S | - | - | - | - | - | - | - | Digital ground | | - |
| 5 | VCAP | S | - | - | - | - | - | - | - | 1.8 V regulator capacitor | | - |
| 6 | VDD | S | - | - | - | - | - | - | - | Digital power supply | | - |
| 7 | PA3/ TIM5_CH3 [SPI_NSS] [LINUART_TX] | I/O | **X** | X | X | HS | O3 | X | X | Port A3 | Timer 52 channel 3 | SPI master/ slave select [AFR1]/ LINUART data transmit [AFR1:0] |
| 8 | PF4 [LINUART_RX] | I/O | **X** | X | - | - | O1 | X | X | Port F4 | LINUART data receive [AFR1:0] | - |
| 9 | PB7 | I/O | **X** | X | X | - | O1 | X | X | Port B7 | - | - |
| 10 | PB6 | I/O | **X** | X | X | - | O1 | X | X | Port B6 | - | - |
| 11 | PB5/ I2C_SDA [TIM1_BKIN] | I/O | **X** | - | X | - | O1 | T(3) | - | Port B5 | I2C data | Timer 1 - break input [AFR4] |
| 12 | PB4/ I2C_SCL [ADC_ETR] | I/O | **X** | - | X | - | O1 | T(3) | - | Port B4 | I2C clock | ADC external trigger [AFR4] |
| 13 | PB3/ AIN3/TIM1_ETR | I/O | **X** | X | X | HS | O3 | X | X | Port B3 | Analog input 3/ Timer 1 external trigger | - |
| 14 | PB2/ AIN2/ TIM1_CH3N | I/O | **X** | X | X | HS | O3 | X | X | Port B2 | Analog input 2/ Timer 1 - inverted channel 3 | - |
| 15 | PB1/ AIN1/ TIM1_CH2N | I/O | **X** | X | X | HS | O3 | X | X | Port B1 | Analog input 1/ Timer 1 - inverted channel 2 | - |
| 16 | PB0/ AIN0/ TIM1_CH1N | I/O | **X** | X | X | HS | O3 | X | X | Port B0 | Analog input 0/ Timer 1 - inverted channel 1 | - |

**Table 8. STM8AF6226 LQFP32/VFQPN32 pin description (continued)**

| LQFP32 VFQPN32 | Pin name | Type | Input | | | Output | | | | Main function (after reset) | Default alternate function | Alternate function after remap [option bit] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | floating | wpu | Ext. interrupt | High sink(1) | Speed | OD | PP | | | |
| 17 | PE5/ SPI_NSS [TIM1_CH1N] | I/O | **X** | X | X | HS | O3 | X | X | Port E5 | SPI master/ slave select | Timer 1 - inverted channel 1 [AFR1:0] |
| 18 | PC1/ TIM1_CH1/ LINUART_CK [TIM1_CH2N] | I/O | **X** | X | X | HS | O3 | X | X | Port C1 | Timer 1 - channel 1 LINUART clock | Timer 1 - inverted channel 2 [AFR1:0] |
| 19 | PC2/ TIM1_CH2 [TIM1_CH3N] | I/O | **X** | X | X | HS | O3 | X | X | Port C2 | Timer 1 - channel 2 | Timer 1 - inverted channel 3 [AFR1:0] |
| 20 | PC3/ TIM1_CH3/[TLI] [TIM1_CH1N] | I/O | **X** | X | X | HS | O3 | X | X | Port C3 | Timer 1 - channel 3 | Top level interrupt [AFR3] Timer 1 inverted channel 1 [AFR7] |
| 21 | PC4/ TIM1_CH4/ CLK_CCO/[AIN 2][TIM1_CH2N] | I/O | **X** | X | X | HS | O3 | X | X | Port C4 | Timer 1 - channel 4 /configurable clock output | Analog input 2 [AFR2]Timer 1 inverted channel 2 [AFR7] |
| 22 | PC5/SPI_SCK [TIM5_CH1] | I/O | **X** | X | X | HS | O3 | X | X | Port C5 | SPI clock | Timer 5 channel 1 [AFR0] |
| 23 | PC6/ SPI_MOSI [TIM1_CH1] | I/O | **X** | X | X | HS | O3 | X | X | Port C6 | PI master out/slave in | Timer 1 channel 1 [AFR0] |
| 24 | PC7/ SPI_MISO [TIM1_CH2] | I/O | **X** | X | X | HS | O3 | X | X | Port C7 | SPI master in/ slave out | Timer 1 channel 2[AFR0] |
| 25 | PD0/ TIM1_BKIN [CLK_CCO] | I/O | **X** | X | X | HS | O3 | X | X | Port D0 | Timer 1 - break input | Configurable clock output [AFR5] |
| 26 | PD1/ SWIM(4) | I/O | X | **X** | X | HS | O4 | X | X | Port D1 | SWIM data interface | - |

**Table 8. STM8AF6226 LQFP32/VFQPN32 pin description (continued)**

| LQFP32 VFQPN32 | Pin name | Type | Input | | | Output | | | | Main function (after reset) | Default alternate function | Alternate function after remap [option bit] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | floating | wpu | Ext. interrupt | High sink(1) | Speed | OD | PP | | | |
| 27 | PD2/[AIN3] [TIM5_CH3] | I/O | **X** | X | X | HS | O3 | X | X | Port D2 | - | Analog input 3 [AFR2] Timer 52 - channel 3 [AFR1] |
| 28 | PD3/ AIN4/ TIM5_CH2/ ADC_ETR | I/O | **X** | X | X | HS | O3 | X | X | Port D3 | Analog input 4 Timer 52 - channel 2/ADC external trigger | - |
| 29 | PD4/ TIM5_CH1/ BEEP [LINUART_CK] | I/O | **X** | X | X | HS | O3 | X | X | Port D4 | Timer 5 - channel 1/BEEP output | LINUART clock [AFR2] |
| 30 | PD5/ AIN5/ LINUART_TX | I/O | **X** | X | X | HS | O3 | X | X | Port D5 | Analog input 5/ LINUART data transmit | - |
| 31 | PD6/ AIN6/ LINUART_RX | I/O | **X** | X | X | HS | O3 | X | X | Port D6 | Analog input 6/ LINUART data receive | - |
| 32 | PD7/ TLI [TIM1_CH4] | I/O | **X** | X | X | HS | O3 | X | X | Port D7 | Top level interrupt | Timer 1 - channel 4 [AFR6] |

1. I/O pins used simultaneously for high current source/sink must be uniformly spaced around the package. In addition, the total driven current must respect the absolute maximum ratings (see *Section 10.2: Absolute maximum ratings*).
2. When the MCU is in Halt/Active-halt mode, PA1 is automatically configured in input weak pull-up and cannot be used for waking up the device. In this mode, the output state of PA1 is not driven. It is recommended to use PA1 only in input mode if Halt/Active-halt is used in the application.
3. In the open-drain output column, 'T' defines a true open-drain I/O (P-buffer, weak pull-up, and protection diode to VDD are not implemented).
4. The PD1 pin is in input pull-up during the reset phase and after internal reset release.

## 5.3 Alternate function remapping

As shown in the rightmost column of *Table 6*, *Table 7* and *Table 8* some alternate functions can be remapped at different I/O ports by programming one of eight AFR (alternate function remap) option bits. Refer to *Section 8: Option bytes on page 46*. When the remapping option is active, the default alternate function is no longer available.

To use an alternate function, the corresponding peripheral must be enabled in the peripheral registers.

Alternate function remapping does not effect GPIO capabilities of the I/O ports (see the GPIO section of STM8S series and STM8AF series 8-bit microcontrollers reference manual, RM0016).

# 6 Memory and register map

## 6.1 Memory map

**Figure 6. Memory map**

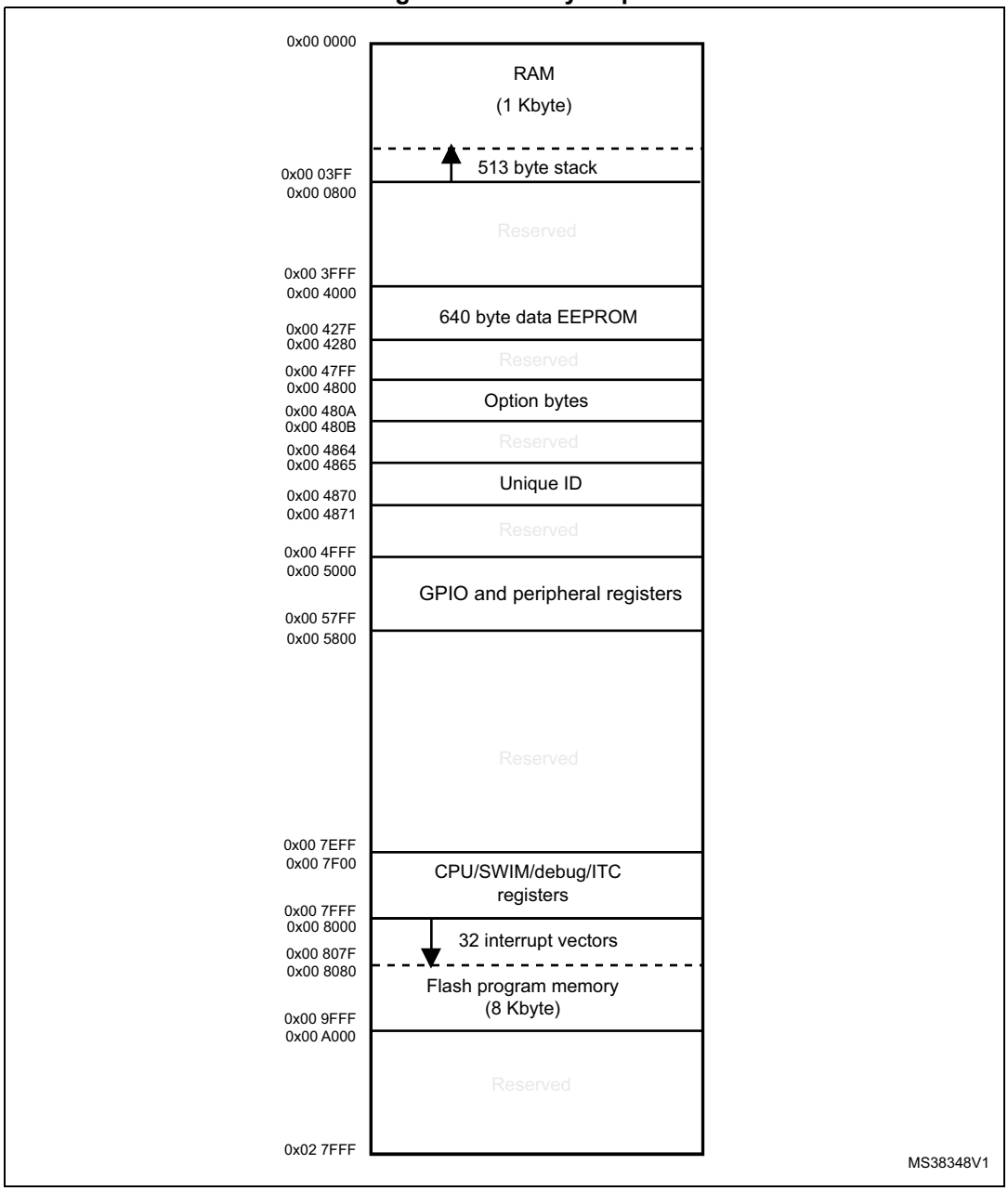


Table 9. Memory model for the devices covered in this datasheet

| Flash program memory size | Flash program memory end address | RAM size | RAM end address | Stack roll-over address |
|---|---|---|---|---|
| 8 K | 0x00 9FFF | 1 K | 0x00 03FF | 0x00 0200 |
| 4 K | 0x00 8FFF | | | |

## 6.2 Register map

### 6.2.1 I/O port hardware register map

Table 10. I/O port hardware register map

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 5000 | Port A | PA_ODR | Port A data output latch register | 0x00 |
| 0x00 5001 | | PA_IDR | Port A input pin value register | 0xXX(1) |
| 0x00 5002 | | PA_DDR | Port A data direction register | 0x00 |
| 0x00 5003 | | PA_CR1 | Port A control register 1 | 0x00 |
| 0x00 5004 | | PA_CR2 | Port A control register 2 | 0x00 |
| 0x00 5005 | Port B | PB_ODR | Port B data output latch register | 0x00 |
| 0x00 5006 | | PB_IDR | Port B input pin value register | 0xXX(1) |
| 0x00 5007 | | PB_DDR | Port B data direction register | 0x00 |
| 0x00 5008 | | PB_CR1 | Port B control register 1 | 0x00 |
| 0x00 5009 | | PB_CR2 | Port B control register 2 | 0x00 |
| 0x00 500A | Port C | PC_ODR | Port C data output latch register | 0x00 |
| 0x00 500B | | PB_IDR | Port C input pin value register | 0xXX(1) |
| 0x00 500C | | PC_DDR | Port C data direction register | 0x00 |
| 0x00 500D | | PC_CR1 | Port C control register 1 | 0x00 |
| 0x00 500E | | PC_CR2 | Port C control register 2 | 0x00 |
| 0x00 500F | Port D | PD_ODR | Port D data output latch register | 0x00 |
| 0x00 5010 | | PD_IDR | Port D input pin value register | 0xXX(1) |
| 0x00 5011 | | PD_DDR | Port D data direction register | 0x00 |
| 0x00 5012 | | PD_CR1 | Port D control register 1 | 0x02 |
| 0x00 5013 | | PD_CR2 | Port D control register 2 | 0x00 |

**Table 10. I/O port hardware register map (continued)**

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 5014 | Port E | PE_ODR | Port E data output latch register | 0x00 |
| 0x00 5015 | | PE_IDR | Port E input pin value register | 0xXX(1) |
| 0x00 5016 | | PE_DDR | Port E data direction register | 0x00 |
| 0x00 5017 | | PE_CR1 | Port E control register 1 | 0x00 |
| 0x00 5018 | | PE_CR2 | Port E control register 2 | 0x00 |
| 0x00 5019 | Port F | PF_ODR | Port F data output latch register | 0x00 |
| 0x00 501A | | PF_IDR | Port F input pin value register | 0xXX(1) |
| 0x00 501B | | PF_DDR | Port F data direction register | 0x00 |
| 0x00 501C | | PF_CR1 | Port F control register 1 | 0x00 |
| 0x00 501D | | PF_CR2 | Port F control register 2 | 0x00 |

1. Depends on the external circuitry.

**Table 11. General hardware register map**

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 501E to 0x00 5069 | Reserved area (60 byte) | | | |
| 0x00 505A | Flash | FLASH_CR1 | Flash control register 1 | 0x00 |
| 0x00 505B | | FLASH_CR2 | Flash control register 2 | 0x00 |
| 0x00 505C | | FLASH_NCR2 | Flash complementary control register 2 | 0xFF |
| 0x00 505D | | FLASH_FPR | Flash protection register | 0x00 |
| 0x00 505E | | FLASH_NFPR | Flash complementary protection register | 0xFF |
| 0x00 505F | | FLASH_IAPSR | Flash in-application programming status register | 0x40 |
| 0x00 5060 to 0x00 5061 | Reserved area (2 byte) | | | |
| 0x00 5062 | Flash | FLASH_PUKR | Flash Program memory unprotection register | 0x00 |
| 0x00 5063 | Reserved area (1 byte) | | | |
| 0x00 5064 | Flash | FLASH_DUKR | Data EEPROM unprotection register | 0x00 |
| 0x00 5065 to 0x00 509F | Reserved area (59 byte) | | | |
| 0x00 50A0 | ITC | EXTI_CR1 | External interrupt control register 1 | 0x00 |
| 0x00 50A1 | | EXTI_CR2 | External interrupt control register 2 | 0x00 |
| 0x00 50A2 to 0x00 50B2 | Reserved area (17 byte) | | | |

**Table 11. General hardware register map (continued)**

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 50B3 | RST | RST_SR | Reset status register | 0xXX(1) |
| 0x00 50B4 to 0x00 50BF | Reserved area (12 byte) | | | |
| 0x00 50C0 | CLK | CLK_ICKR | Internal clock control register | 0x01 |
| 0x00 50C1 | | CLK_ECKR | External clock control register | 0x00 |
| 0x00 50C2 | Reserved area (1 byte) | | | |
| 0x00 50C3 | CLK | CLK_CMSR | Clock master status register | 0xE1 |
| 0x00 50C4 | | CLK_SWR | Clock master switch register | 0xE1 |
| 0x00 50C5 | | CLK_SWCR | Clock switch control register | 0xXX |
| 0x00 50C6 | | CLK_CKDIVR | Clock divider register | 0x18 |
| 0x00 50C7 | | CLK_PCKENR1 | Peripheral clock gating register 1 | 0xFF |
| 0x00 50C8 | | CLK_CSSR | Clock security system register | 0x00 |
| 0x00 50C9 | | CLK_CCOR | Configurable clock control register | 0x00 |
| 0x00 50CA | | CLK_PCKENR2 | Peripheral clock gating register 2 | 0xFF |
| 0x00 50CB | Reserved area (1 byte) | | | |
| 0x00 50CC | CLK | CLK_HSITRIMR | HSI clock calibration trimming register | 0x00 |
| 0x00 50CD | | CLK_SWIMCCR | SWIM clock control register | 0bXXXX XXX0 |
| 0x00 50CE to 0x00 50D0 | Reserved area (3 byte) | | | |
| 0x00 50D1 | WWDG | WWDG_CR | WWDG control register | 0x7F |
| 0x00 50D2 | | WWDG_WR | WWDR window register | 0x7F |
| 0x00 50D3 to 0x00 50DF | Reserved area (13 byte) | | | |
| 0x00 50E0 | IWDG | IWDG_KR | IWDG key register | 0xXX(2) |
| 0x00 50E1 | | IWDG_PR | IWDG prescaler register | 0x00 |
| 0x00 50E2 | | IWDG_RLR | IWDG reload register | 0xFF |
| 0x00 50E3 to 0x00 50EF | Reserved area (13 byte) | | | |
| 0x00 50F0 | AWU | AWU_CSR1 | AWU control/status register 1 | 0x00 |
| 0x00 50F1 | | AWU_APR | AWU asynchronous prescaler buffer register | 0x3F |
| 0x00 50F2 | | AWU_TBR | AWU timebase selection register | 0x00 |
| 0x00 50F3 | BEEP | BEEP_CSR | BEEP control/status register | 0x1F |
| 0x00 50F4 to 0x00 50FF | Reserved area (12 byte) | | | |

**Table 11. General hardware register map (continued)**

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 5200 | SPI | SPI_CR1 | SPI control register 1 | 0x00 |
| 0x00 5201 | | SPI_CR2 | SPI control register 2 | 0x00 |
| 0x00 5202 | | SPI_ICR | SPI interrupt control register | 0x00 |
| 0x00 5203 | | SPI_SR | SPI status register | 0x02 |
| 0x00 5204 | | SPI_DR | SPI data register | 0x00 |
| 0x00 5205 | | SPI_CRCPR | SPI CRC polynomial register | 0x07 |
| 0x00 5206 | | SPI_RXCRCR | SPI Rx CRC register | 0xFF |
| 0x00 5207 | | SPI_TXCRCR | SPI Tx CRC register | 0xFF |
| 0x00 5208 to 0x00 520F | Reserved area (8 byte) | | | |
| 0x00 5210 | I2C | I2C_CR1 | I2C control register 1 | 0x00 |
| 0x00 5211 | | I2C_CR2 | I2C control register 2 | 0x00 |
| 0x00 5212 | | I2C_FREQR | I2C frequency register | 0x00 |
| 0x00 5213 | | I2C_OARL | I2C own address register low | 0x00 |
| 0x00 5214 | | I2C_OARH | I2C own address register high | 0x00 |
| 0x00 5215 | | Reserved area (1 byte) | | |
| 0x00 5216 | | I2C_DR | I2C data register | 0x00 |
| 0x00 5217 | | I2C_SR1 | I2C status register 1 | 0x00 |
| 0x00 5218 | | I2C_SR2 | I2C status register 2 | 0x00 |
| 0x00 5219 | | I2C_SR3 | I2C status register 3 | 0x00 |
| 0x00 521A | | I2C_ITR | I2C interrupt control register | 0x00 |
| 0x00 521B | | I2C_CCRL | I2C clock control register low | 0x00 |
| 0x00 521C | | I2C_CCRH | I2C clock control register high | 0x00 |
| 0x00 521D | | I2C_TRISER | I2C TRISE register | 0x02 |
| 0x00 521E | | I2C_PECR | I2C packet error checking register | 0x00 |
| 0x00 521F to 0x00 522F | Reserved area (17 byte) | | | |

Table 11. General hardware register map (continued)

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 5230 | LINUART | UART4_SR | LINUART status register | 0xC0 |
| 0x00 5231 | | UART4_DR | LINUART data register | 0xXX |
| 0x00 5232 | | UART4_BRR1 | LINUART baud rate register 1 | 0x00 |
| 0x00 5233 | | UART4_BRR2 | LINUART baud rate register 2 | 0x00 |
| 0x00 5234 | | UART4_CR1 | LINUART control register 1 | 0x00 |
| 0x00 5235 | | UART4_CR2 | LINUART control register 2 | 0x00 |
| 0x00 5236 | | UART4_CR3 | LINUART control register 3 | 0x00 |
| 0x00 5237 | | UART4_CR4 | LINUART control register 4 | 0x00 |
| 0x00 5238 | | Reserved | | |
| 0x00 5239 | | UART4_CR6 | LINUART control register 6 | 0x00 |
| 0x00 523A | | UART4_GTR | LINUART guard time register | 0x00 |
| 0x00 523B | | UART4_PSCR | LINUART prescaler | 0x00 |
| 0x00 523C to 0x00 523F | Reserved area (20 byte) | | | |

Table 11. General hardware register map (continued)

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 5250 | TIM1 | TIM1_CR1 | TIM1 control register 1 | 0x00 |
| 0x00 5251 | | TIM1_CR2 | TIM1 control register 2 | 0x00 |
| 0x00 5252 | | TIM1_SMCR | TIM1 slave mode control register | 0x00 |
| 0x00 5253 | | TIM1_ETR | TIM1 external trigger register | 0x00 |
| 0x00 5254 | | TIM1_IER | TIM1 Interrupt enable register | 0x00 |
| 0x00 5255 | | TIM1_SR1 | TIM1 status register 1 | 0x00 |
| 0x00 5256 | | TIM1_SR2 | TIM1 status register 2 | 0x00 |
| 0x00 5257 | | TIM1_EGR | TIM1 event generation register | 0x00 |
| 0x00 5258 | | TIM1_CCMR1 | TIM1 capture/compare mode register 1 | 0x00 |
| 0x00 5259 | | TIM1_CCMR2 | TIM1 capture/compare mode register 2 | 0x00 |
| 0x00 525A | | TIM1_CCMR3 | TIM1 capture/compare mode register 3 | 0x00 |
| 0x00 525B | | TIM1_CCMR4 | TIM1 capture/compare mode register 4 | 0x00 |
| 0x00 525C | | TIM1_CCER1 | TIM1 capture/compare enable register 1 | 0x00 |
| 0x00 525D | | TIM1_CCER2 | TIM1 capture/compare enable register 2 | 0x00 |
| 0x00 525E | | TIM1_CNTRH | TIM1 counter high | 0x00 |
| 0x00 525F | | TIM1_CNTRL | TIM1 counter low | 0x00 |
| 0x00 5260 | | TIM1_PSCRH | TIM1 prescaler register high | 0x00 |
| 0x00 5261 | | TIM1_PSCRL | TIM1 prescaler register low | 0x00 |
| 0x00 5262 | | TIM1_ARRH | TIM1 auto-reload register high | 0xFF |
| 0x00 5263 | | TIM1_ARRL | TIM1 auto-reload register low | 0xFF |
| 0x00 5264 | | TIM1_RCR | TIM1 repetition counter register | 0x00 |
| 0x00 5265 | | TIM1_CCR1H | TIM1 capture/compare register 1 high | 0x00 |
| 0x00 5266 | | TIM1_CCR1L | TIM1 capture/compare register 1 low | 0x00 |
| 0x00 5267 | | TIM1_CCR2H | TIM1 capture/compare register 2 high | 0x00 |
| 0x00 5268 | | TIM1_CCR2L | TIM1 capture/compare register 2 low | 0x00 |
| 0x00 5269 | | TIM1_CCR3H | TIM1 capture/compare register 3 high | 0x00 |
| 0x00 526A | | TIM1_CCR3L | TIM1 capture/compare register 3 low | 0x00 |
| 0x00 526B | | TIM1_CCR4H | TIM1 capture/compare register 4 high | 0x00 |
| 0x00 526C | | TIM1_CCR4L | TIM1 capture/compare register 4 low | 0x00 |
| 0x00 526D | | TIM1_BKR | TIM1 break register | 0x00 |
| 0x00 526E | | TIM1_DTR | TIM1 dead-time register | 0x00 |
| 0x00 526F | | TIM1_OISR | TIM1 output idle state register | 0x00 |
| 0x00 5270 to 0x00 52FF | Reserved area (147 byte) | | | |

**Table 11. General hardware register map (continued)**

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 5300 | TIM5 | TIM5_CR1 | TIM5 control register 1 | 0x00 |
| 0x00 5301 | | TIM5_CR2 | TIM5 control register 2 | 0x00 |
| 0x00 5302 | | TIM5_SMCR | TIM5 slave mode control register | 0x00 |
| 0x00 5303 | | TIM5_IER | TIM5 interrupt enable register | 0x00 |
| 0x00 5304 | | TIM5_SR1 | TIM5 status register 1 | 0x00 |
| 0x00 5305 | | TIM5_SR2 | TIM5 status register 2 | 0x00 |
| 0x00 5306 | | TIM5_EGR | TIM5 event generation register | 0x00 |
| 0x00 5307 | | TIM5_CCMR1 | TIM5 capture/compare mode register 1 | 0x00 |
| 0x00 5308 | | TIM5_CCMR2 | TIM5 capture/compare mode register 2 | 0x00 |
| 0x00 5309 | | TIM5_CCMR3 | TIM5 capture/compare mode register 3 | 0x00 |
| 0x00 530A | | TIM5_CCER1 | TIM5 capture/compare enable register 1 | 0x00 |
| 0x00 530B | | TIM5_CCER2 | TIM5 capture/compare enable register 2 | 0x00 |
| 00 530C0x | | TIM5_CNTRH | TIM5 counter high | 0x00 |
| 0x00 530D | | TIM5_CNTRL | TIM5 counter low | 0x00 |
| 0x00 530E | | TIM5_PSCR | TIM5 prescaler register | 0x00 |
| 0x00 530F | | TIM5_ARRH | TIM5 auto-reload register high | 0xFF |
| 0x00 5310 | | TIM5_ARRL | TIM5 auto-reload register low | 0xFF |
| 0x00 5311 | | TIM5_CCR1H | TIM5 capture/compare register 1 high | 0x00 |
| 0x00 5312 | | TIM5_CCR1L | TIM5 capture/compare register 1 low | 0x00 |
| 0x00 5313 | | TIM5_CCR2H | TIM5 capture/compare reg. 2 high | 0x00 |
| 0x00 5314 | | TIM5_CCR2L | TIM5 capture/compare register 2 low | 0x00 |
| 0x00 5315 | | TIM5_CCR3H | TIM5 capture/compare register 3 high | 0x00 |
| 0x00 5316 | | TIM5_CCR3L | TIM5 capture/compare register 3 low | 0x00 |
| 0x00 5317 to 0x00 533F | Reserved area (43 byte) | | | |
| 0x00 5340 | TIM6 | TIM6_CR1 | TIM6 control register 1 | 0x00 |
| 0x00 5341 | | TIM6_CR2 | TIM6 control register 2 | 0x00 |
| 0x00 5342 | | TIM6_SMCR | TIM6 slave mode control register | 0x00 |
| 0x00 5343 | | TIM6_IER | TIM6 interrupt enable register | 0x00 |
| 0x00 5344 | | TIM6_SR | TIM6 status register | 0x00 |
| 0x00 5345 | | TIM6_EGR | TIM6 event generation register | 0x00 |
| 0x00 5346 | | TIM6_CNTR | TIM6 counter | 0x00 |
| 0x00 5347 | | TIM6_PSCR | TIM6 prescaler register | 0x00 |
| 0x00 5348 | | TIM6_ARR | TIM6 auto-reload register | 0xFF |

**Table 11. General hardware register map (continued)**

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 5349 to 0x00 53DF | Reserved area (153 byte) | | | |
| 0x00 53E0 to 0x00 53F3 | ADC1 | ADC _DBxR | ADC data buffer registers | 0x00 |
| 0x00 53F4 to 0x00 53FF | Reserved area (12 byte) | | | |
| 0x00 5400 | ADC1 | ADC _CSR | ADC control/status register | 0x00 |
| 0x00 5401 | | ADC_CR1 | ADC configuration register 1 | 0x00 |
| 0x00 5402 | | ADC_CR2 | ADC configuration register 2 | 0x00 |
| 0x00 5403 | | ADC_CR3 | ADC configuration register 3 | 0x00 |
| 0x00 5404 | | ADC_DRH | ADC data register high | 0xXX |
| 0x00 5405 | | ADC_DRL | ADC data register low | 0xXX |
| 0x00 5406 | | ADC_TDRH | ADC Schmitt trigger disable register high | 0x00 |
| 0x00 5407 | | ADC_TDRL | ADC Schmitt trigger disable register low | 0x00 |
| 0x00 5408 | | ADC _HTRH | ADC high threshold register high | 0xFF |
| 0x00 5409 | | ADC_HTRL | ADC high threshold register low | 0x03 |
| 0x00 540A | | ADC _LTRH | ADC low threshold register high | 0x00 |
| 0x00 540B | | ADC_LTRL | ADC low threshold register low | 0x00 |
| 0x00 540C | | ADC _AWSRH | ADC watchdog status register high | 0x00 |
| 0x00 540D | | ADC_AWSRL | ADC watchdog status register low | 0x00 |
| 0x00 540E | | ADC _AWCRH | ADC watchdog control register high | 0x00 |
| 0x00 540F | | ADC _AWCRL | ADC watchdog control register low | 0x00 |
| 0x00 5410 to 0x00 57FF | Reserved area (1008 byte) | | | |

1. Depends on the previous reset source.
2. Write only register.

### 6.2.2 CPU/SWIM/debug module/interrupt controller registers

**Table 12. CPU/SWIM/debug module/interrupt controller registers**

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 7F00 | CPU(1) | A | Accumulator | 0x00 |
| 0x00 7F01 | | PCE | Program counter extended | 0x00 |
| 0x00 7F02 | | PCH | Program counter high | 0x00 |
| 0x00 7F03 | | PCL | Program counter low | 0x00 |
| 0x00 7F04 | | XH | X index register high | 0x00 |
| 0x00 7F05 | | XL | X index register low | 0x00 |
| 0x00 7F06 | | YH | Y index register high | 0x00 |
| 0x00 7F07 | | YL | Y index register low | 0x00 |
| 0x00 7F08 | | SPH | Stack pointer high | 0x03 |
| 0x00 7F09 | | SPL | Stack pointer low | 0xFF |
| 0x00 7F0A | | CCR | Condition code register | 0x28 |
| 0x00 7F0B to 0x00 7F5F | Reserved area (85 byte) | | | |
| 0x00 7F60 | CPU | CFG_GCR | Global configuration register | 0x00 |
| 0x00 7F70 | ITC | ITC_SPR1 | Interrupt software priority register 1 | 0xFF |
| 0x00 7F71 | | ITC_SPR2 | Interrupt software priority register 2 | 0xFF |
| 0x00 7F72 | | ITC_SPR3 | Interrupt software priority register 3 | 0xFF |
| 0x00 7F73 | | ITC_SPR4 | Interrupt software priority register 4 | 0xFF |
| 0x00 7F74 | | ITC_SPR5 | Interrupt software priority register 5 | 0xFF |
| 0x00 7F75 | | ITC_SPR6 | Interrupt software priority register 6 | 0xFF |
| 0x00 7F76 | | ITC_SPR7 | Interrupt software priority register 7 | 0xFF |
| 0x00 7F77 | | ITC_SPR8 | Interrupt software priority register 8 | 0xFF |
| 0x00 7F78 to 0x00 7F79 | Reserved area (2 byte) | | | |
| 0x00 7F80 | SWIM | SWIM_CSR | SWIM control status register | 0x00 |
| 0x00 7F81 to 0x00 7F8F | Reserved area (15 byte) | | | |

**Table 12. CPU/SWIM/debug module/interrupt controller registers (continued)**

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 7F90 | DM | DM_BK1RE | DM breakpoint 1 register extended byte | 0xFF |
| 0x00 7F91 | | DM_BK1RH | DM breakpoint 1 register high byte | 0xFF |
| 0x00 7F92 | | DM_BK1RL | DM breakpoint 1 register low byte | 0xFF |
| 0x00 7F93 | | DM_BK2RE | DM breakpoint 2 register extended byte | 0xFF |
| 0x00 7F94 | | DM_BK2RH | DM breakpoint 2 register high byte | 0xFF |
| 0x00 7F95 | | DM_BK2RL | DM breakpoint 2 register low byte | 0xFF |
| 0x00 7F96 | | DM_CR1 | DM debug module control register 1 | 0x00 |
| 0x00 7F97 | | DM_CR2 | DM debug module control register 2 | 0x00 |
| 0x00 7F98 | | DM_CSR1 | DM debug module control/status register 1 | 0x10 |
| 0x00 7F99 | | DM_CSR2 | DM debug module control/status register 2 | 0x00 |
| 0x00 7F9A | | DM_ENFCTR | DM enable function register | 0xFF |
| 0x00 7F9B to 0x00 7F9F | Reserved area (5 byte) | | | |

1. Accessible by debug module only

# 7 Interrupt vector mapping

**Table 13. Interrupt mapping**

| Priority | Source block | Description | Wakeup from halt mode | Wakeup from active-halt mode | Interrupt vector address |
|---|---|---|---|---|---|
| — | Reset | Reset | Yes | Yes | 0x00 8000 |
| — | TRAP | Software interrupt | - | - | 0x00 8004 |
| 0 | TLI | External top level interrupt | - | - | 0x00 8008 |
| 1 | AWU | Auto-wakeup from Halt | - | Yes | 0x00 800C |
| 2 | Clock controller | Clock controller | - | - | 0x00 8010 |
| 3 | EXTI0 | Port A external interrupts | Yes(1) | Yes(1) | 0x00 8014 |
| 4 | EXTI1 | Port B external interrupts | Yes | Yes | 0x00 8018 |
| 5 | EXTI2 | Port C external interrupts | Yes | Yes | 0x00 801C |
| 6 | EXTI3 | Port D external interrupts | Yes | Yes | 0x00 8020 |
| 7 | EXTI4 | Port E external interrupts | Yes | Yes | 0x00 8024 |
| 8 | EXTI5 | Port F | - | - | 0x00 8028 |
| 9 | Reserved | - | - | - | 0x00 802C |
| 10 | SPI | End of transfer | Yes | Yes | 0x00 8030 |
| 11 | TIM1 | TIM1 update/overflow/ underflow/trigger/break | - | - | 0x00 8034 |
| 12 | TIM1 | TIM1 capture/compare | - | - | 0x00 8038 |
| 13 | TIM5 | TIM5 update/overflow/trigger | - | - | 0x00 803C |
| 14 | TIM5 | TIM5 capture/compare | - | - | 0x00 8040 |
| 15 | Reserved | - | - | - | 0x00 8044 |
| 16 | Reserved | - | - | - | 0x00 8048 |
| 17 | LINUART | Tx complete | - | - | 0x00 804C |
| 18 | LINUART | Receive register DATA FULL | - | - | 0x00 8050 |
| 19 | $I^2C$ | $I^2C$ interrupts | Yes | Yes | 0x00 8054 |
| 20 | Reserved | - | - | - | 0x00 8058 |
| 21 | Reserved | - | - | - | 0x00 805C |
| 22 | ADC1 | ADC1 end of conversion/analog watchdog interrupt | - | - | 0x00 8060 |

**Table 13. Interrupt mapping (continued)**

| Priority | Source block | Description | Wakeup from halt mode | Wakeup from active-halt mode | Interrupt vector address |
|---|---|---|---|---|---|
| 23 | TIM6 | TIM6 update/overflow/trigger | - | - | 0x00 8064 |
| 24 | Flash | EOP/WR_PG_DIS | - | - | 0x00 8068 |

1. Except PA1.

# 8 Option bytes

Option bytes contain configurations for device hardware features as well as the memory protection of the device. Except for the ROP (read-out protection) byte, each option byte has to be stored twice, in a regular form (OPTx) and a complemented one (NOPTx) for redundancy.

Option bytes can be modified in ICP mode (via SWIM) by accessing the EEPROM address shown in *Table 14: Option bytes* below.

Option bytes can also be modified 'on the fly' by the application in IAP mode, except the ROP and UBC options that can only be modified in ICP mode (via SWIM).

Refer to the STM8 Flash programming manual (PM0051) and STM8 SWIM communication protocol and debug module user manual (UM0470) for information on SWIM programming procedures.

**Table 14. Option bytes**

| Addr. | Option name | Option byte no. | Option bits | | | | | | | | Factory default setting |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| 0x00 4800 | Read-out protection (ROP) | OPT0 | ROP[7:0] | | | | | | | | 0x00 |
| 0x00 4801 | User boot code (UBC) | OPT1 | UBC[7:0] | | | | | | | | 0x00 |
| 0x00 4802 | | NOPT1 | NUBC[7:0] | | | | | | | | 0xFF |
| 0x00 4803 | Alternate function remapping (AFR) | OPT2 | AFR7 | AFR6 | AFR5 | AFR4 | AFR3 | AFR2 | AFR1 | AFR0 | 0x00 |
| 0x00 4804 | | NOPT2 | NAFR7 | NAFR6 | NAFR 5 | NAFR 4 | NAFR 3 | NAFR 2 | NAFR 1 | NAFR 0 | 0xFF |
| 0x00 4805 | Miscell. option | OPT3 | Reserved | | | HSI TRIM | LSI _EN | IWDG _HW | WWDG _HW | WWDG _HALT | 0x00 |
| 0x00 4806 | | NOPT3 | Reserved | | | NHSI TRIM | NLSI _EN | NIWDG _HW | NWWDG _HW | NWWG _HALT | 0xFF |
| 0x00 4807 | Clock option | OPT4 | Reserved | | | | EXT CLK | CKAWU SEL | PRS C1 | PRS C0 | 0x00 |
| 0x00 4808 | | NOPT4 | Reserved | | | | NEXT CLK | NCKAWU SEL | NPRS C1 | NPRS C0 | 0xFF |
| 0x00 4809 | HSE clock startup | OPT5 | HSECNT[7:0] | | | | | | | | 0x00 |
| 0x00 480A | | NOPT5 | NHSECNT[7:0] | | | | | | | | 0xFF |

## 8.1 Option byte description

**Table 15. Option byte description**

| Option byte no. | Description |
|---|---|
| OPT0 | **ROP[7:0]: Memory readout protection (ROP)**<br>0xAA: Enable readout protection (write access via SWIM protocol)<br>*Note: Refer to STM8S series and STM8AF series 8-bit microcontrollers reference manual (RM0016) section on Flash/EEPROM memory readout protection for details.* |
| OPT1 | **UBC[7:0]: User boot code area**<br>0x00: No UBC, no write-protection<br>0x01: Page 0 defined as UBC, memory write-protected<br>0x02: Page 0 to 1 defined as UBC, memory write-protected<br>Pages 0 and 1 contain the interrupt vectors.<br>...<br>0x7F: Pages 0 to 126 defined as UBC, memory write-protected<br>Other values: Page 0 to 127 defined as UBC, memory write-protected.<br><br>*Note: Refer to STM8S series and STM8AF series 8-bit microcontrollers reference manual (RM0016) section on Flash/EEPROM write protection for more details.* |
| OPT2 | **AFR[7:0]**<br>Refer to the following sections for the alternate function remapping descriptions of bits [7:2] and [1:0] respectively. |
| OPT3 | **HSITRIM: high-speed internal clock trimming register size**<br>0: 3-bit trimming supported in CLK_HSITRIMR register<br>1: 4-bit trimming supported in CLK_HSITRIMR register |
| | **LSI_EN: low-speed internal clock enable**<br>0: LSI clock is not available as CPU clock source<br>1: LSI clock is available as CPU clock source |
| | **IWDG_HW: Independent watchdog**<br>0: IWDG independent watchdog activated by software<br>1: IWDG independent watchdog activated by hardware |
| | **WWDG_HW: Window watchdog activation**<br>0: WWDG window watchdog activated by software<br>1: WWDG window watchdog activated by hardware |
| | **WWDG_HALT: Window watchdog reset on Halt**<br>0: No reset generated on Halt if WWDG active<br>1: Reset generated on Halt if WWDG active |

**Table 15. Option byte description (continued)**

| Option byte no. | Description |
|---|---|
| OPT4 | **EXTCLK: External clock selection**<br>0: External crystal connected to OSCIN/OSCOUT<br>1: External clock signal on OSCIN |
| | **CKAWUSEL: Auto-wakeup unit/clock**<br>0: LSI clock source selected for AWU<br>1: HSE clock with prescaler selected as clock source for AWU |
| | **PRSC[1:0]: AWU clock prescaler**<br>0x: 16 MHz to 128 kHz prescaler<br>10: 8 MHz to 128 kHz prescaler<br>11: 4 MHz to 128 kHz prescaler |
| OPT5 | **HSECNT[7:0]: HSE crystal oscillator stabilization time**<br>0x00: 2048 HSE cycles<br>0xB4: 128 HSE cycles<br>0xD2: 8 HSE cycles<br>0xE1: 0.5 HSE cycles |

## 8.2 STM8AF6213/13A/23/23A/26 alternate function remapping bits

**Table 16. STM8AF6226 alternate function remapping bits [7:2] for 32-pin packages**

| Option byte number | Description(1) |
|---|---|
| OPT2 | **AFR7: Alternate function remapping option 7**<br>0: AFR7 remapping option inactive: default alternate function (2)<br>1: Port C3 alternate function = = TIM1_CH1N;<br>port C4 alternate function = TIM1_CH2N<br>**AFR6: Alternate function remapping option 6**<br>0: AFR6 remapping option inactive: default alternate function (2)<br>1: Port D7 alternate function = TIM1_CH4.<br>**AFR5: Alternate function remapping option 5**<br>0: AFR5 remapping option inactive: default alternate function (2).<br>1: Port D0 alternate function = CLK_CCO.<br>**AFR4: Alternate function remapping option 4**<br>0: AFR4 remapping option inactive: default alternate function (2).<br>1: Port B4 alternate function = ADC_ETR; port B5 alternate function = TIM1_BKIN.<br>**AFR3: Alternate function remapping option 3**<br>0: AFR3 remapping option inactive: default alternate function (2)<br>1: Port C3 alternate function = TLI<br>**AFR2: Alternate function remapping option 2**<br>0: AFR2 remapping option inactive: default alternate function (2)<br>1: Port C4 alternate function = AIN2; port D2 alternate function = AIN3;<br>port D4 alternate function = LINUART_CK |

1. Do not use more than one remapping option in the same port.
2. Refer to the pin description.

**Table 17. STM8AF6213 and STM8AF6223 alternate function remapping bits [7:2] for 20-pin packages**

| Option byte number | Description(1) |
|---|---|
| OPT2 | **AFR7: Alternate function remapping option 7**<br>0: AFR7 remapping option inactive: default alternate function (2)<br>1: Port C3 alternate function = = TIM1_CH1N;<br>port C4 alternate function = TIM1_CH2N<br>**AFR6: Alternate function remapping option 6**<br>Reserved<br>**AFR5: Alternate function remapping option 5**<br>Reserved<br>**AFR4: Alternate function remapping option 4**<br>0: AFR4 remapping option inactive: default alternate function (2).<br>1: Port B4 alternate function = ADC_ETR; port B5 alternate function = TIM1_BKIN.<br>**AFR3: Alternate function remapping option 3**<br>0: AFR3 remapping option inactive: default alternate function (2)<br>1: Port C3 alternate function = TLI<br>**AFR2: Alternate function remapping option 2**<br>0: AFR2 remapping option inactive: default alternate function (2)<br>1: Port D4 alternate function = LINUART_CK |

1. Do not use more than one remapping option in the same port.
2. Refer to the pin description.

**Table 18. STM8AF6213A and STM8AF6223A alternate function remapping bits [7:2] for 20-pin packages**

| Option byte number | Description(1) |
|---|---|
| OPT2 | **AFR7: Alternate function remapping option 7**<br>0: AFR7 remapping option inactive: default alternate function (2)<br>1: Port C4 alternate function = TIM1_CH2N<br>**AFR6: Alternate function remapping option 6**<br>Reserved<br>**AFR5: Alternate function remapping option 5**<br>Reserved<br>**AFR4: Alternate function remapping option 4**<br>0: AFR4 remapping option inactive: default alternate function (2).<br>1: Port B4 alternate function = ADC_ETR; port B5 alternate function = TIM1_BKIN.<br>**AFR3: Alternate function remapping option 3**<br>Reserved.<br>**AFR2: Alternate function remapping option 2**<br>0: AFR2 remapping option inactive: default alternate function (2)<br>1: Port D4 alternate function = LINUART_CK |

1. Do not use more than one remapping option in the same port.
2. Refer to the pin description.

**Table 19. STM8AF6226 alternate function remapping bits [1:0] for 32-pin packages**

| AFR1 option bit value | AFR0 option bit value | I/O port | Alternate function mapping |
|---|---|---|---|
| 0 | 0 | AFR1 and AFR0 remapping options inactive: Default alternate functions(1) | |
| 0 | 1 | PC5 | TIM5_CH1 |
| | | PC6 | TIM1_CH1 |
| | | PC7 | TIM1_CH2 |
| 1 | 0 | PA3 | SPI_NSS |
| | | PD2 | TIM5_CH3 |
| 1(2) | 1(2) | PD2 | TIM5_CH3 |
| | | PC5 | TIM5_CH1 |
| | | PC6 | TIM1_CH1 |
| | | PC7 | TIM1_CH2 |
| | | PC2 | TIM1_CH3N |
| | | PC1 | TIM1_CH2N |
| | | PE5 | TIM1_CH1N |
| | | PA3 | LINUART_TX |
| | | PF4 | LINUART_RX |

1. Refer to the pin descriptions.
2. If both AFR1 and AFR0 option bits are set, the SPI hardware NSS management feature is no more available. If this remapping option is selected and the SPI is enabled, the SSM bit must be configured in the SPI_CR2 register to select software NSS management.

**Table 20. STM8AF6213/STM8AF6223 alternate function remapping bits [1:0] for 20-pin packages**

| AFR1 option bit value | AFR0 option bit value | I/O port | Alternate function mapping |
|---|---|---|---|
| 0 | 0 | AFR1 and AFR0 remapping options inactive: Default alternate functions(1) | |
| 0 | 1 | PC5 | TIM5_CH1 |
| | | PC6 | TIM1_CH1 |
| | | PC7 | TIM1_CH2 |
| 1 | 0 | PA3 | SPI_NSS |
| | | PD2 | TIM5_CH3 |

**Table 20. STM8AF6213/STM8AF6223 alternate function remapping bits [1:0] for 20-pin packages (continued)**

| AFR1 option bit value | AFR0 option bit value | I/O port | Alternate function mapping |
|---|---|---|---|
| 1 | 1 | PD2 | TIM5_CH3 |
| | | PC5 | TIM5_CH1 |
| | | PC6 | TIM1_CH1 |
| | | PC7 | TIM1_CH2 |
| | | PC2 | Not available |
| | | PC1 | Not available |
| | | PE5 | Not available |
| | | PA3 | SPI_NSS |
| | | PF4 | Not available |

1. Refer to the pin descriptions.

**Table 21. STM8AF6223A alternate function remapping bits [1:0] for 20-pin packages**

| AFR1 option bit value | AFR0 option bit value | I/O port | Alternate function mapping |
|---|---|---|---|
| 0 | 0 | AFR1 and AFR0 remapping options inactive: Default alternate functions(1) | |
| 0 | 1 | PC5 | TIM5_CH1 |
| | | PC6 | TIM1_CH1 |
| | | PC7 | TIM1_CH2 |
| 1 | 0 | PA3 | Not available |
| | | PD2 | TIM5_CH3 |
| 1(2) | 1(2) | PD2 | TIM5_CH3 |
| | | PC5 | TIM5_CH1 |
| | | PC6 | TIM1_CH1 |
| | | PC7 | TIM1_CH2 |
| | | PC2 | Not available |
| | | PC1 | Not available |
| | | PE5 | Not available |
| | | PA3 | Not available |
| | | PF4 | Not available |

1. Refer to the pin descriptions.
2. If both AFR1 and AFR0 option bits are set, the SPI hardware NSS management feature is no more available. If this remapping option is selected and the SPI is enabled, the SSM bit must be configured in the SPI_CR2 register to select software NSS management.

# 9 Unique ID

The devices feature a 96-bit unique device identifier which provides a reference number that is unique for any device and in any context. The 96 bits of the identifier can never be altered by the user.

The unique device identifier can be read in single byte and may then be concatenated using a custom algorithm.

The unique device identifier is ideally suited:

- For use as serial numbers
- For use as security keys to increase the code security in the program memory while using and combining this unique ID with software cryptographic primitives and protocols before programming the internal memory.
- To activate secure boot processes.

**Table 22. Unique ID bit description**

| Address | Content description | Unique ID bits | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0x4865 | X coordinate on the wafer | U_ID[7:0] | | | | | | | |
| 0x4866 | | U_ID[15:8] | | | | | | | |
| 0x4867 | Y coordinate on the wafer | U_ID[23:16] | | | | | | | |
| 0x4868 | | U_ID[31:24] | | | | | | | |
| 0x4869 | Wafer number | U_ID[39:32] | | | | | | | |
| 0x486A | Lot number | U_ID[47:40] | | | | | | | |
| 0x486B | | U_ID[55:48] | | | | | | | |
| 0x486C | | U_ID[63:56] | | | | | | | |
| 0x486D | | U_ID[71:64] | | | | | | | |
| 0x486E | | U_ID[79:72] | | | | | | | |
| 0x486F | | U_ID[87:80] | | | | | | | |
| 0x4870 | | U_ID[95:88] | | | | | | | |

# 10 Electrical characteristics

## 10.1 Parameter conditions

Unless otherwise specified, all voltages are referred to $V_{SS}$.

### 10.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at $T_A$ = -40 °C, $T_A$ = 25 °C, and $T_A = T_{Amax}$ (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production.

### 10.1.2 Typical values

Unless otherwise specified, typical data are based on $T_A$ = 25 °C, $V_{DD}$ = 5.0 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range.

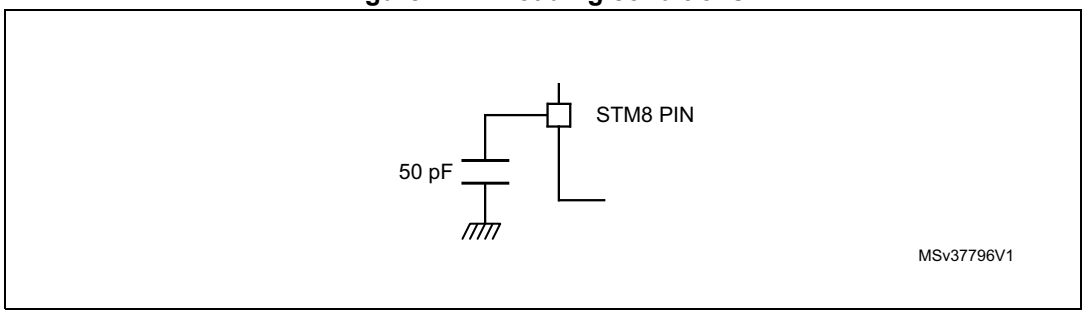
### 10.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

### 10.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 7*.

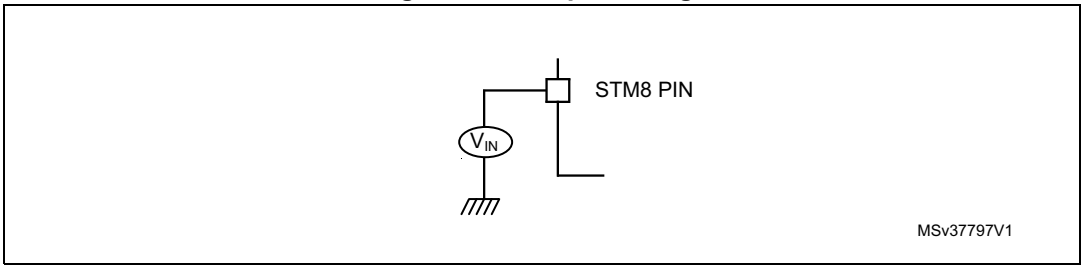
**Figure 7. Pin loading conditions**



### 10.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 8*.

**Figure 8. Pin input voltage**




## 10.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 23: Voltage characteristics*, *Table 24: Current characteristics* and *Table 25: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect the device's reliability.

Device mission profile (application conditions) is compliant with JEDEC JESD47 Qualification Standard, extended mission profiles are available on demand.

**Table 23. Voltage characteristics**

| Symbol | Ratings | Min | Max | Unit |
|---|---|---|---|---|
| $V_{DDx}$ - $V_{SS}$ | Supply voltage (including $V_{DDA}$ and $V_{DDIO}$)(1) | -0.3 | 6.5 | V |
| $V_{IN}$ | Input voltage on true open drain pins (2) | $V_{SS}$ - 0.3 | 6.5 | V |
| | Input voltage on any other pin(2) | $V_{SS}$ - 0.3 | $V_{DD}$ + 0.3 | |
| $\lvert V_{DDx} - V_{DD} \rvert$ | Variations between different power pins | - | 50 | mV |
| $\lvert V_{SSx} - V_{SS} \rvert$ | Variations between all the different ground pins | - | 50 | |
| $V_{ESD}$ | Electrostatic discharge voltage | see *Absolute maximum ratings (electrical sensitivity) on page 90* | | |

1. All power ($V_{DD}$) and ground ($V_{SS}$) pins must always be connected to the external power supply
2. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if $V_{IN}$ maximum is respected. If $V_{IN}$ maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. For true open-drain pads, there is no positive injection current, and the corresponding $V_{IN}$ maximum must always be respected

**Table 24. Current characteristics**

| Symbol | Ratings | Max.(1) | Unit |
|---|---|---|---|
| $I_{VDD}$ | Total current into $V_{DD}$ power lines (source)(2) | 100 | mA |
| $I_{VSS}$ | Total current out of $V_{SS}$ ground lines (sink)(2) | 80 | |
| $I_{IO}$ | Output current sunk by any I/O and control pin | 20 | |
| | Output current source by any I/Os and control pin | -20 | |
| $I_{INJ(PIN)}$(3) (4) | Injected current on RST pin | ±4 | |
| | Injected current on OSCIN pin | ±4 | |
| | Injected current on any other pin(5) | ±4 | |
| $\sum I_{INJ(TOT)}$(3) | Total injected current (sum of all I/O and control pins)(5) | ±20 | |

1. Guaranteed by characterization results.
2. All power ($V_{DD}$, $V_{DDIO}$, $V_{DDA}$) and ground ($V_{SS}$, $V_{SSIO}$, $V_{SSA}$) pins must always be connected to the external supply.
3. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if $V_{IN}$ maximum is respected. If $V_{IN}$ maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. For true open-drain pads, there is no positive injection current, and the corresponding VIN maximum must always be respected.
4. ADC accuracy vs. negative injection current: Injecting negative current on any of the analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current. Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and ∑IINJ(PIN) in the I/O port pin characteristics section does not affect the ADC accuracy
5. When several inputs are submitted to a current injection, the maximum ∑IINJ(PIN) is the absolute sum of the positive and negative injected currents (instantaneous values). These results are based on characterization with ∑IINJ(PIN) maximum current injection on four I/O port pins of the device.

**Table 25. Thermal characteristics**

| Symbol | Ratings | Value | Unit |
|---|---|---|---|
| $T_{STG}$ | Storage temperature range | -65 to 150 | °C |
| $T_J$ | Maximum junction temperature | 150 | |

**Table 26. Operating lifetime (OLF)**

| Symbol | Ratings | Value | Unit |
|---|---|---|---|
| OLF | Conforming to AEC-Q100 | -40 to 150 | °C |

## 10.3 Operating conditions

**Table 27. General operating conditions**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $f_{CPU}$ | Internal CPU clock frequency | - | 0 | 16 | MHz |
| $V_{DD}$ | Standard operating voltage | - | 3.0 | 5.5 | V |
| $V_{CAP}$(1) | $C_{EXT}$: capacitance of external capacitor | - | 470 | 3300 | nF |
| | ESR of external capacitor | at 1 MHz(2) | - | 0.3 | Ω |
| | ESL of external capacitor | | - | 15 | nH |
| $P_D$ (3) | Power dissipation at $T_A$ = 85 °C for suffix A version, $T_A$ = 125 °C for suffix C version, $T_A$ = 150 °C for suffix D version | TSSOP20 | - | 45 | mW |
| | | LQFP32 | - | 83 | |
| | | VQFPN32 | - | TBD | - |
| $T_A$ | Ambient temperature for suffix A version | Maximum power dissipation | -40 | 85 | °C |
| | Ambient temperature for suffix C version | | -40 | 125 | |
| | Ambient temperature for suffix D version | | -40 | 150 | |
| $T_J$ | Junction temperature range | Suffix A | -40 | 90 | |
| | | Suffix C | -40 | 130 | |
| | | Suffix D | -40 | 155 | |

1. Care should be taken when selecting the capacitor, due to its tolerance, as well as the parameter dependency on temperature, DC bias and frequency in addition to other factors. The parameter maximum value must be respected for the full application range.
2. This frequency of 1 MHz as a condition for $V_{CAP}$ parameters is given by design of internal regulator.
3. See *Section 11.4: Thermal characteristics*.

**Figure 9. $f_{CPUmax}$ versus $V_{DD}$**

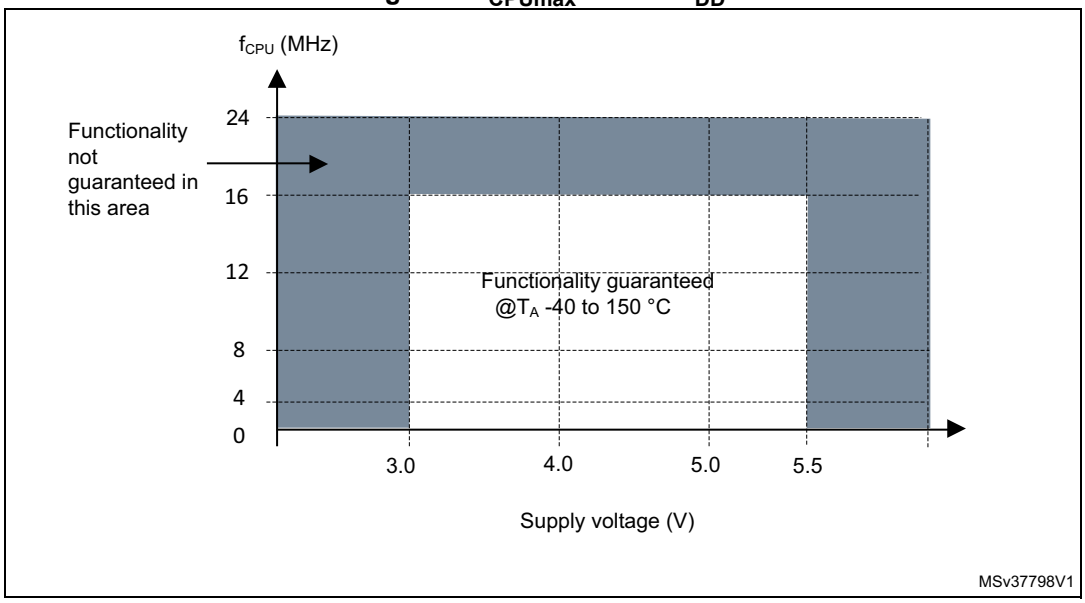



**Table 28. Operating conditions at power-up/power-down**

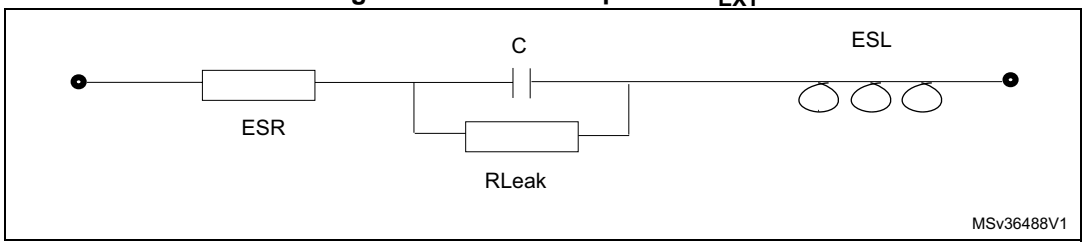
| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{VDD}$ | $V_{DD}$ rise time rate | - | 2(1) | - | ∞ | µs/V |
| | $V_{DD}$ fall time rate(2) | - | 2(1) | - | ∞ | |
| $t_{TEMP}$ | Reset release delay | $V_{DD}$ rising | - | - | 1.7 | ms |
| $V_{IT+}$ | Power-on reset threshold(3) | - | 2.6(1) | 2.7 | 2.85 | V |
| $V_{IT-}$ | Brown-out reset threshold | - | 2.5 | 2.65 | 2.8(1) | |
| $V_{HYS(BOR)}$ | Brown-out reset hysteresis | - | - | 70(1) | - | mV |

1. Guaranteed by design.
2. Reset is always generated after a $t_{TEMP}$ delay. The application must ensure that $V_{DD}$ is still above the minimum operating voltage ($V_{DD}$ min) when the $t_{TEMP}$ delay has elapsed.
3. There is inrush current into $V_{DD}$ present after device power on to charge $C_{EXT}$ capacitor. This inrush energy depends from $C_{EXT}$ capacitor value. For example, a $C_{EXT}$ of 1µF requires Q=1 µF x 1.8V = 1.8 µC.

### 10.3.1 VCAP external capacitor

Stabilization for the main regulator is achieved connecting an external capacitor $C_{EXT}$ to the $V_{CAP}$ pin. $C_{EXT}$ is specified in *Table 27*. Care should be taken to limit the series inductance to less than 15 nH.

**Figure 10. External capacitor $C_{EXT}$**




1. Legend: ESR is the equivalent series resistance and ESL is the equivalent inductance.

### 10.3.2 Supply current characteristics

The current consumption is measured as described in *Section 4.3: Interrupt controller*.

#### Total current consumption in run mode

The MCU is placed under the following conditions:

- All I/O pins in input mode with a static value at $V_{DD}$ or $V_{SS}$ (no load)
- All peripherals are disabled (clock stopped by peripheral clock gating registers) except if explicitly mentioned.

Subject to general operating conditions for $V_{DD}$ and $T_A$.

Unless otherwise specified, data are based on characterization results, and not tested in production.

**Table 29. Total current consumption with code execution in run mode at $V_{DD}$ = 5 V**

| Symbol | Parameter | Conditions | | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{DD(RUN)}$ | Supply current in run mode, code executed from RAM | $f_{CPU} = f_{MASTER}$ = 16 MHz | HSE crystal osc. (16 MHz) | 2.3 | - | mA |
| | | | HSE user ext. clock (16 MHz) | 2 | 2.35 | |
| | | | HSI RC osc. (16 MHz) | 1.7 | 2(1) | |
| | | $f_{CPU} = f_{MASTER}/128$= 125 kHz | HSE user ext. clock (16 MHz) | 0.86 | - | |
| | | | HSI RC osc. (16 MHz) | 0.7 | 0.87 | |
| | | $f_{CPU} = f_{MASTER}/128$= 15.625 kHz | HSI RC osc. (16 MHz/8) | 0.46 | 0.58 | |
| | | $f_{CPU} = f_{MASTER}$ = 28 kHz | LSI RC osc. (128 kHz) | 0.41 | 0.55 | |

**Table 29. Total current consumption with code execution in run mode at $V_{DD}$ = 5 V (continued)**

| Symbol | Parameter | Conditions | | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{DD(RUN)}$ | Supply current in run mode, code executed from Flash | $f_{CPU} = f_{MASTER}$ = 16 MHz | HSE crystal osc. (16 MHz) | 4.5 | - | mA |
| | | | HSE user ext. clock (16 MHz) | 4.3 | 4.75 | |
| | | | HSI RC osc. (16 MHz) | 3.7 | 4.5(1) | |
| | Supply current in run mode, code executed from Flash | $f_{CPU} = f_{MASTER}$ = 2 MHz | HSI RC osc. (16 MHz/8)(2) | 0.84 | 2(1) | |
| | | $f_{CPU} = f_{MASTER}$/128 = 125 kHz | HSI RC osc. (16 MHz) | 0.72 | 0.9 | |
| | | $f_{CPU} = f_{MASTER}$/128 = 15.625 kHz | HSI RC osc. (16 MHz/8) | 0.46 | 0.58 | |
| | | $f_{CPU} = f_{MASTER}$ = 128 kHz | LSI RC osc. (128 kHz) | 0.42 | 0.57 | |

1. Tested in production.
2. Default clock configuration measured with all peripherals off.

**Table 30. Total current consumption with code execution in run mode at $V_{DD}$ = 3.3 V**

| Symbol | Parameter | Conditions | | Typ | Max(1) | Unit |
|---|---|---|---|---|---|---|
| $I_{DD(RUN)}$ | Supply current in run mode, code executed from RAM | $f_{CPU} = f_{MASTER}$ =16 MHz | HSE crystal osc. (16 MHz) | 1.8 | - | mA |
| | | | HSE user ext. clock (16 MHz) | 2 | 2.3 | |
| | | | HSI RC osc. (16 MHz) | 1.5 | 2 | |
| | | $f_{CPU} = f_{MASTER}$/128 = 125 kHz | HSE user ext. clock (16 MHz) | 0.81 | - | |
| | | | HSI RC osc. (16 MHz) | 0.7 | 0.87 | |
| | | $f_{CPU} = f_{MASTER}$/ 128 = 15.625 kHz | HSI RC osc. (16 MHz/8) | 0.46 | 0.58 | |
| | | $f_{CPU} = f_{MASTER}$ =128 kHz | LSI RC osc. (128 kHz) | 0.41 | 0.55 | |
| | Supply current in run mode, code executed from Flash | $f_{CPU} = f_{MASTER}$ = 16 MHz | HSE crystal osc. (16 MHz) | 4 | - | |
| | | | HSE user ext. clock (16 MHz) | 3.9 | 4.7 | |
| | | | HSI RC osc. (16 MHz) | 3.7 | 4.5 | |
| | | $f_{CPU} = f_{MASTER}$ =2 MHz | HSI RC osc. (16 MHz/8)(2) | 0.84 | 1.05 | |
| | | $f_{CPU} = f_{MASTER}$/ 128 = 125 kHz | HSI RC osc. (16 MHz) | 0.72 | 0.9 | |
| | | $f_{CPU} = f_{MASTER}$/128 = 15.625 kHz | HSI RC osc. (16 MHz/8) | 0.46 | 0.58 | |
| | | $f_{CPU} = f_{MASTER}$ =128 kHz | LSI RC osc. (128 kHz) | 0.42 | 0.57 | |

1. Guaranteed by characterization results.
2. Default clock configuration measured with all peripherals off.

### Total current consumption in wait mode

Unless otherwise specified, data based are on characterization results, and not tested in production.

**Table 31. Total current consumption in wait mode at $V_{DD}$ = 5 V**

| Symbol | Parameter | Conditions | | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{DD(WFI)}$ | Supply current in wait mode | $f_{CPU} = f_{MASTER}$ = 16 MHz | HSE crystal osc. (16 MHz) | 1.6 | - | mA |
| | | | HSE user ext. clock (16 MHz) | 1.1 | 1.3 | |
| | | | HSI RC osc. (16 MHz) | 0.89 | 1.5(1) | |
| | | $f_{CPU} = f_{MASTER}/128$ = 125 kHz | HSI RC osc. (16 MHz) | 0.7 | 0.88 | |
| | | $f_{CPU} = f_{MASTER}/128$ = 15.625 kHz | HSI RC osc. (16 MHz/8)(2) | 0.45 | 0.57 | |
| | | $f_{CPU} = f_{MASTER}$ = 128 kHz | LSI RC osc. (128 kHz) | 0.4 | 0.54 | |

1. Tested in production.
2. Default clock configuration measured with all peripherals off.

**Table 32. Total current consumption in wait mode at $V_{DD}$ = 3.3 V**

| Symbol | Parameter | Conditions | | Typ | Max(1) | Unit |
|---|---|---|---|---|---|---|
| $I_{DD(WFI)}$ | Supply current in wait mode | $f_{CPU} = f_{MASTER}$ = 16 MHz | HSE crystal osc. (16 MHz) | 1.1 | - | mA |
| | | | HSE user ext. clock (16 MHz) | 1.1 | 1.3 | |
| | | | HSI RC osc. (16 MHz) | 0.89 | 1.1 | |
| | | $f_{CPU} = f_{MASTER}/128$ = 125 kHz | HSI RC osc. (16 MHz) | 0.7 | 0.88 | |
| | | $f_{CPU} = f_{MASTER}/128$ = 15.625 kHz | HSI RC osc. (16 MHz/8)(2) | 0.45 | 0.57 | |
| | | $f_{CPU} = f_{MASTER}$ = 128 kHz | LSI RC osc. (128 kHz) | 0.4 | 0.54 | |

1. Guaranteed by characterization results.
2. Default clock configuration measured with all peripherals off.

### Total current consumption in active halt mode

**Table 33. Total current consumption in active halt mode at $V_{DD}$ = 5 V**

| Symbol | Parameter | Conditions | | | Typ | Max at 85°C | Max at 125°C | Max at 150°C | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | Main voltage regulator (MVR)(1) | Flash mode(2) | Clock source | | | | | |
| $I_{DD(AH)}$ | Supply current in active halt mode | On | Operating mode | HSE crystal osc. (16 MHz) | 1030 | - | - | - | µA |
| | | | | LSI RC osc. (128 kHz) | 200 | 260 | 300 | - | |
| | | | Power-down mode | HSE crystal osc. (16 MHz) | 970 | - | - | - | |
| | | | | LSI RC osc. (128 kHz) | 150 | 200 | 230 | - | |
| | | Off | Operating mode | LSI RC osc. (128 kHz) | 66 | 85 | 140 | 200 | |
| | | | Power-down mode | LSI RC osc. (128 kHz) | 10 | 20 | 40 | - | |

1. Configured by the REGAH bit in the CLK_ICKR register.
2. Configured by the AHALT bit in the FLASH_CR1 register.

**Table 34. Total current consumption in active halt mode at $V_{DD}$ = 3.3 V**

| Symbol | Parameter | Conditions | | | Typ | Max at 85°C(1) | Max at 125°C | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Main voltage regulator (MVR)(2) | Flash mode(3) | Clock source | | | | |
| $I_{DD(AH)}$ | Supply current in active halt mode | On | Operating mode | HSE crystal osc. (16 MHz) | 550 | - | - | µA |
| | | | | LSI RC osc. (128 kHz) | 200 | 260 | 290 | |
| | | | Power-down mode | HSE crystal osc. (16 MHz) | 970 | - | - | |
| | | | | LSI RC osc. (128 kHz) | 150 | 200 | 230 | |
| | | Off | Operating mode | LSI RC osc. (128 kHz) | 66 | 80 | 105 | |
| | | | Power-down mode | LSI RC osc. (128 kHz) | 10 | 18 | 35 | |

1. Guaranteed by characterization results.
2. Configured by the REGAH bit in the CLK_ICKR register.
3. Configured by the AHALT bit in the FLASH_CR1 register.

### Total current consumption in halt mode

**Table 35. Total current consumption in halt mode at $V_{DD}$ = 5 V**

| Symbol | Parameter | Conditions | Typ | Max at 85°C | Max at 125°C | Max at 150°C | Unit |
|---|---|---|---|---|---|---|---|
| $I_{DD(H)}$ | Supply current in halt mode | Flash in operating mode, HSI clock after wakeup | 63 | 75 | 105 | - | µA |
| | | Flash in power-down mode, HSI clock after wakeup | 6.0 | 20(1) | 55(1) | 80(1) | |

1. Tested in production.

**Table 36. Total current consumption in halt mode at $V_{DD}$ = 3.3 V**

| Symbol | Parameter | Conditions | Typ | Max at 85°C(1) | Max at 125°C(1) | Unit |
|---|---|---|---|---|---|---|
| $I_{DD(H)}$ | Supply current in halt mode | Flash in operating mode, HSI clock after wakeup | 60 | 75 | 100 | µA |
| | | Flash in power-down mode, HSI clock after wakeup | 4.5 | 17 | 30 | |

1. Guaranteed by characterization results.

### Low-power mode wakeup times

**Table 37. Wakeup times**

| Symbol | Parameter | Conditions | | | Typ | Max(1) | Unit |
|---|---|---|---|---|---|---|---|
| $t_{WU(WFI)}$ | Wakeup time from wait mode to run mode(2) | 0 to 16 MHz | | | - | See (3) | µs |
| | | $f_{CPU}$= $f_{MASTER}$= 16 MHz | | | 0.56 | - | |
| $t_{WU(AH)}$ | Wakeup time active halt mode to run mode(2) | MVR voltage regulator on(4) | Flash in operating mode(5) | HSI (after wakeup) | 1(6) | 2(6) | |
| | | | | | 3(6) | - | |
| | | MVR voltage regulator off | | | 48(6) | - | |
| | | | | | 50(6) | - | |
| $t_{WU(H)}$ | Wakeup time from halt mode to run mode(2) | Flash in operating mode(5) | | | 52 | - | |
| | | Flash in power-down mode(5) | | | 54 | - | |

1. Guaranteed by design.
2. Measured from interrupt event to interrupt vector fetch.
3. $t_{WU(WFI)}$ = 2 x 1/$f_{MASTER}$+ 67 x 1/$f_{CPU}$.
4. Configured by the REGAH bit in the CLK_ICKR register.
5. Configured by the AHALT bit in the FLASH_CR1 register.
6. Plus 1 LSI clock depending on synchronization.

### Total current consumption and timing in forced reset state

**Table 38. Total current consumption and timing in forced reset state**

| Symbol | Parameter | Conditions | Typ | Max(1) | Unit |
|---|---|---|---|---|---|
| $I_{DD(R)}$ | Supply current in reset state(2) | $V_{DD}$= 5 V | 400 | - | µA |
| | | $V_{DD}$= 3.3 V | 300 | - | |
| $t_{RESETBL}$ | Reset pin release to vector fetch | - | - | 150 | µs |

1. Guaranteed by design.
2. Characterized with all I/Os tied to $V_{SS}$.

### Current consumption for on-chip peripherals

Subject to general operating conditions for $V_{DD}$ and $T_A$.

HSI internal RC/$f_{CPU}$ = $f_{MASTER}$ = 16 MHz, $V_{DD}$ = 5 V

**Table 39. Peripheral current consumption**

| Symbol | Parameter | Typ | Unit |
|---|---|---|---|
| $I_{DD(TIM1)}$ | TIM1 supply current(1) | 210 | µA |
| $I_{DD(TIM5)}$ | TIM5 supply current(1) | 130 | |
| $I_{DD(TIM6)}$ | TIM6 supply current(1) | 50 | |
| $I_{DD(UART1)}$ | LINUART supply current(2) | 120 | |
| $I_{DD(SPI)}$ | SPI supply current(2) | 45 | |
| $I_{DD(I2C)}$ | I2C supply current(2) | 65 | |
| $I_{DD(ADC1)}$ | ADC1 supply current(3) | 1000 | |

1. Data based on a differential $I_{DD}$ measurement between reset configuration and timer counter running at 16 MHz. No IC/OC programmed (no I/O pads toggling). Not tested in production.
2. Data based on a differential $I_{DD}$ measurement between the on-chip peripheral when kept under reset and not clocked and the on-chip peripheral when clocked and not kept under reset. No I/O pads toggling. Not tested in production.
3. Data based on a differential $I_{DD}$ measurement between reset configuration and continuous A/D conversions. Not tested in production.

### Current consumption curves

The following figures show typical current consumption measured with code executing in RAM.

**Figure 11. Typ $I_{DD(RUN)}$ vs. $V_{DD}$ HSE user external clock, $f_{CPU}$ = 16 MHz**

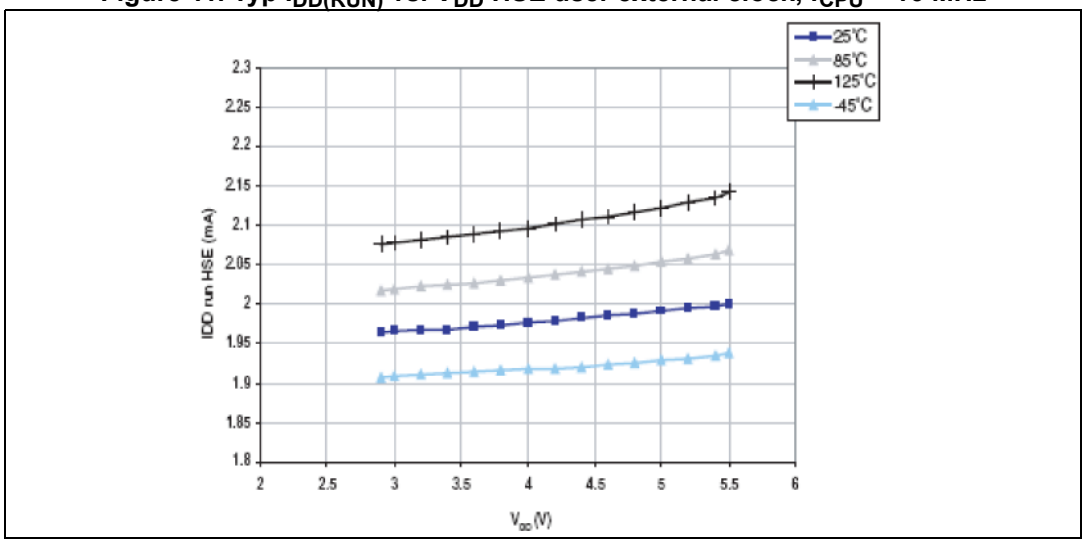



**Figure 12. Typ $I_{DD(RUN)}$ vs. $f_{CPU}$ HSE user external clock, $V_{DD}$ = 5 V**

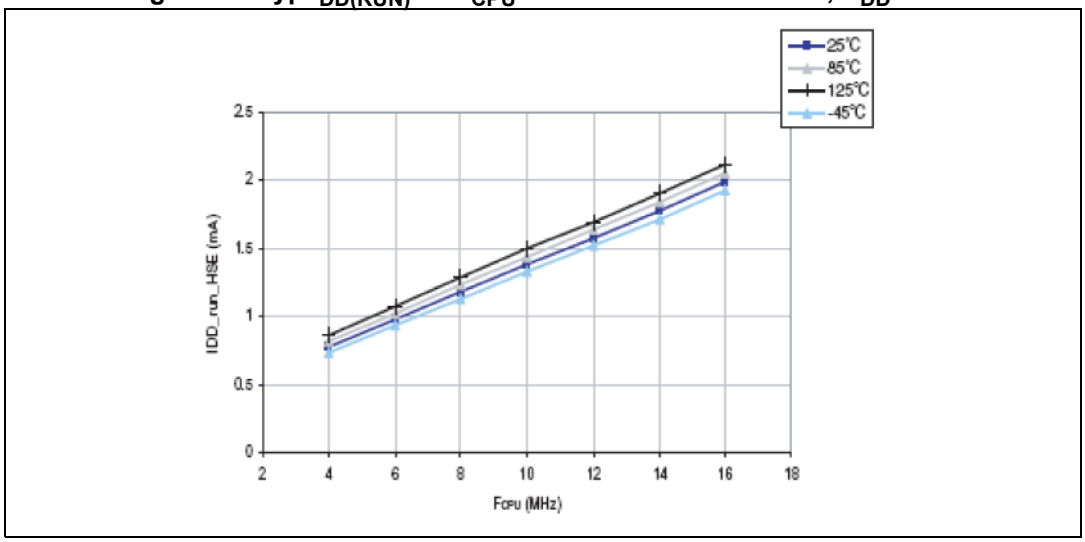


Figure 13. Typ $I_{DD(RUN)}$ vs. $V_{DD}$ HSEI RC osc., $f_{CPU}$ = 16 MHz

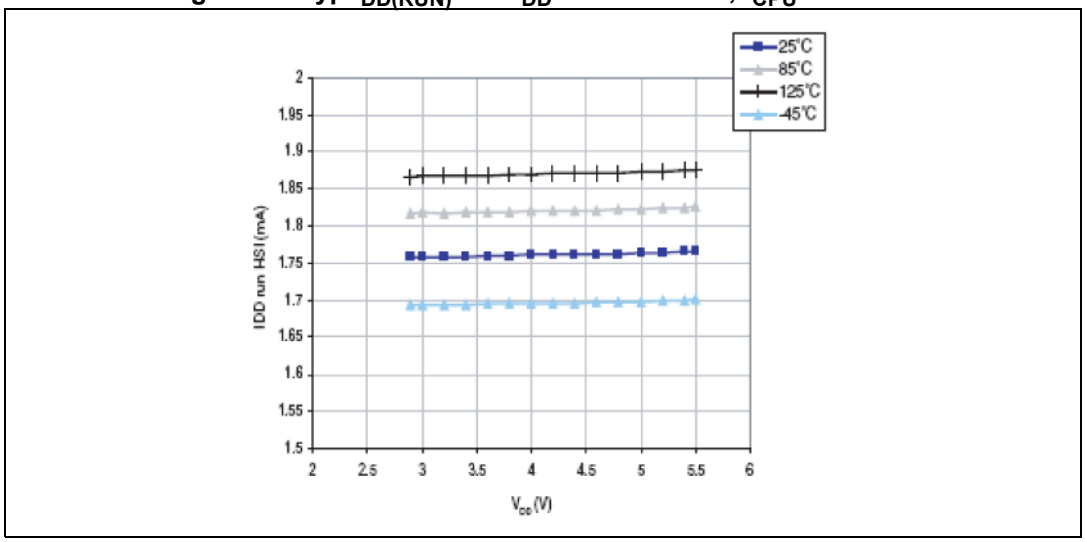



Figure 14. Typ $I_{DD(WFI)}$ vs. $V_{DD}$ HSE user external clock, $f_{CPU}$ = 16 MHz

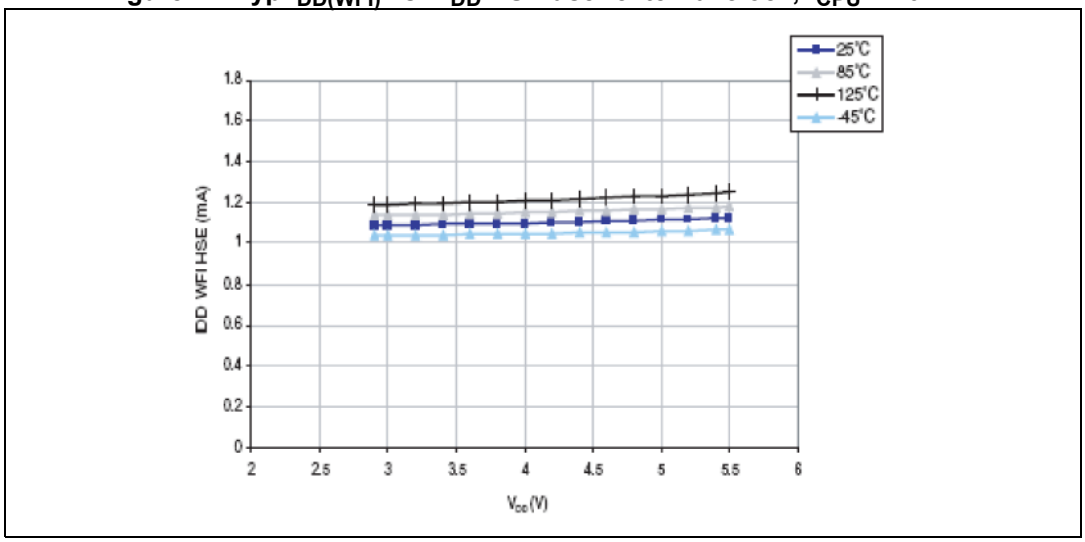


Figure 15. Typ $I_{DD(WFI)}$ vs. $f_{CPU}$ HSE user external clock, $V_{DD}$ = 5 V

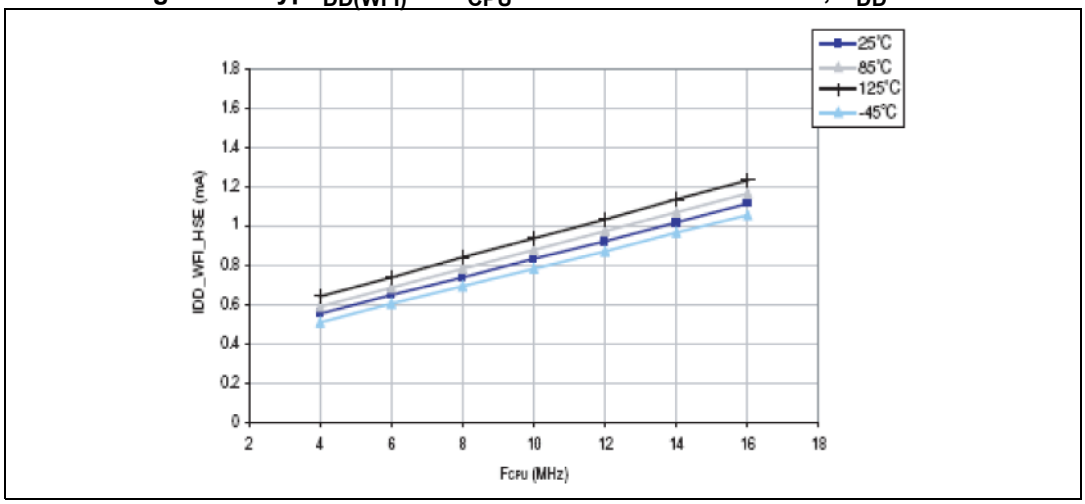
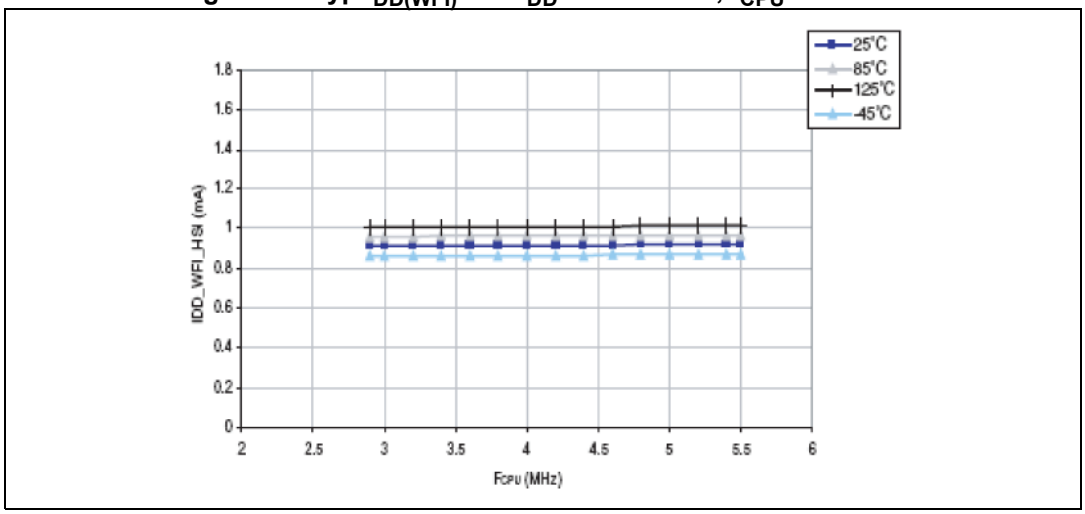



Figure 16. Typ $I_{DD(WFI)}$ vs. $V_{DD}$ HSI RC osc., $f_{CPU}$ = 16 MHz



### 10.3.3 External clock sources and timing characteristics

#### HSE user external clock

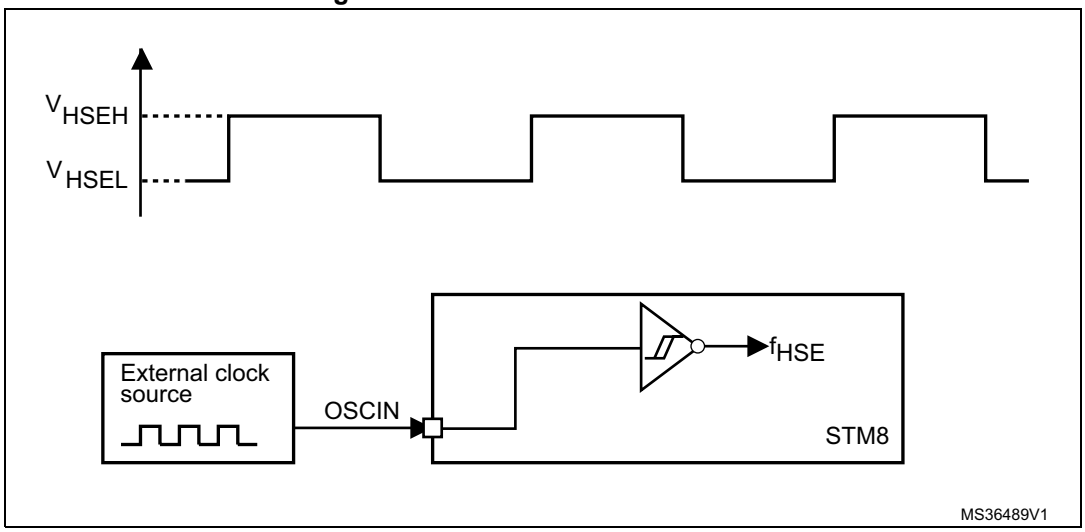
Subject to general operating conditions for $V_{DD}$ and $T_A$.

**Table 40. HSE user external clock characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{HSE_ext}$ | User external clock source frequency | - | 0 | - | 16 | MHz |
| $V_{HSEH}$(1) | OSCIN input pin high level voltage | - | 0.7 x $V_{DD}$ | - | $V_{DD}$ + 0.3 V | V |
| $V_{HSEL}$(1) | OSCIN input pin low level voltage | - | $V_{SS}$ | - | 0.3 x $V_{DD}$ | |
| $I_{LEAK_HSE}$ | OSCIN input leakage current | $V_{SS} < V_{IN} < V_{DD}$ | -1 | - | +1 | µA |

1. Guaranteed by characterization results.

**Figure 17. HSE external clock source**



### HSE crystal/ceramic resonator oscillator

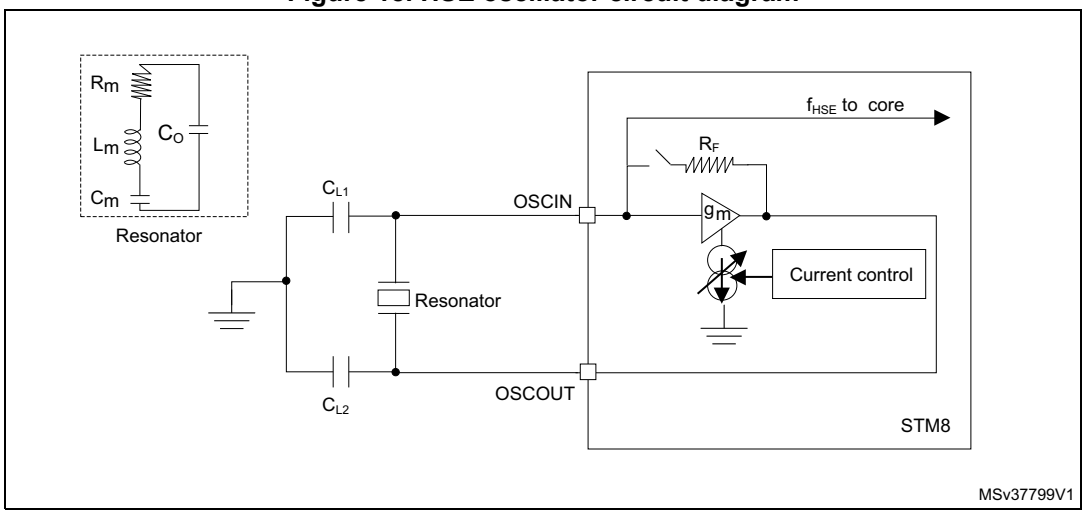
The HSE clock can be supplied with a 1 to 16 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph is based on characterization results with specified typical external components. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details (frequency, package, accuracy...).

**Table 41. HSE oscillator characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{HSE}$ | External high-speed oscillator frequency | - | 1 | - | 16 | MHz |
| $R_F$ | Feedback resistor | - | - | 220 | - | kΩ |
| $C^{(1)}$ | Recommended load capacitance(2) | - | - | - | 20 | pF |
| $I_{DD(HSE)}$ | HSE oscillator power consumption | C = 20 pF, $f_{OSC}$ = 16 MHz | - | - | 6 (startup) 1.6 (stabilized)(3) | mA |
| | | C = 10 pF, $f_{OSC}$ = 16 MHz | - | - | 6 (startup) 1.2 (stabilized)(3) | |
| $g_m$ | Oscillator transconductance | - | 5 | - | - | mA/V |
| $t_{SU(HSE)}^{(4)}$ | Startup time | $V_{DD}$ is stabilized | - | 1 | - | ms |

1. C is approximately equivalent to 2 x crystal $C_{LOAD}$.
2. The oscillator selection can be optimized in terms of supply current using a high quality resonator with small Rm value. Refer to the crystal manufacturer for more details.
3. Guaranteed by characterization results.
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) until a stabilized 16 MHz oscillation is reached. The value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

**Figure 18. HSE oscillator circuit diagram**



### HSE oscillator critical $g_m$ formula

The crystal characteristics have to be checked with the following formula:

$$g_m \gg g_{mcrit}$$

where $g_{mcrit}$ can be calculated with the crystal parameters as follows:

$$g_{mcrit} = (2 \times \Pi \times {}^{f}HSE)^2 \times R_m(2Co + C)^2$$

$R_m$: Notional resistance (see crystal specification)
$L_m$: Notional inductance (see crystal specification)
$C_m$: Notional capacitance (see crystal specification)
Co: Shunt capacitance (see crystal specification)
$C_{L1} = C_{L2} = C$: Grounded external capacitance

## 10.3.4 Internal clock sources and timing characteristics

Subject to general operating conditions for $V_{DD}$ and $T_A$.

### High speed internal RC oscillator (HSI)

**Table 42. HSI oscillator characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $f_{HSI}$ | Frequency | - | | - | 16 | - | MHz |
| $ACC_{HS}$ | HSI oscillator user trimming accuracy | Trimmed by the application for any $V_{DD}$ and $T_A$ conditions | 3-bit calibration | -1(1) | - | 1(1) | % |
| | | | 4-bit calibration | -0.5(1) | - | 0.5(1) | |
| | HSI oscillator accuracy (factory calibrated) | 3.0 V ≤ $V_{DD}$ ≤ 5.5 V, -40 °C ≤ $T_A$ ≤ 150 °C | | -5 | - | 5 | |
| | | 3.0 V ≤ $V_{DD}$ ≤ 5.5 V, -40 °C ≤ $T_A$ ≤ 125 °C | | -3(2) | - | 3(2) | |
| $t_{su(HSI)}$ | HSI oscillator wakeup time | - | | - | - | 2(3) | µs |
| $I_{DD(HSI)}$ | HSI oscillator power consumption | - | | - | 170 | 250(3) | µA |

1. Selection between legacy 3-bit calibration and 4-bit extended calibration is done using the HSITRIM bit in OPT3 and NOPT3.To achieve a higher accuracy, 4-bit calibration must be enabled.
2. These values are guaranteed for STM8AF62xxIxx order codes only.
3. Guaranteed by characterization results.

### Low speed internal RC oscillator (LSI)

Subject to general operating conditions for $V_{DD}$ and $T_A$.

**Table 43. LSI oscillator characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{LSI}$ | Frequency | - | 110(1) | 128 | 150(1) | kHz |
| $t_{su(LSI)}$ | LSI oscillator wakeup time | - | - | - | 7 | µs |
| $I_{DD(LSI)}$ | LSI oscillator power consumption | - | - | 5 | - | µA |

1. Tested in production.

## 10.3.5 Memory characteristics

### RAM and hardware registers

**Table 44. RAM and hardware registers**

| Symbol | Parameter | Conditions | Min | Unit |
|---|---|---|---|---|
| $V_{RM}$ | Data retention mode(1) | Halt mode (or reset) | $V_{IT-max}$(2) | V |

1. Minimum supply voltage without losing the data stored in RAM (in halt mode or under reset) or in hardware registers (only in halt mode). Guaranteed by design.
2. Refer to the operating conditions for the value of $V_{IT-max}$

### Flash program memory/data EEPROM memory

General conditions: $T_A$ = -40 to 150 °C.

**Table 45. Flash program memory/data EEPROM memory**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Operating voltage (all modes, execution/write/erase) | $f_{CPU}$ is 0 to 16 MHz with 0 ws | 3.0 | - | 5.5 | V |
| | Operating voltage (code execution) | | 2.6 | - | 5.5 | |
| $t_{prog}$ | Standard programming time (including erase) for byte/word/block (1 byte/4 byte/64 byte) | - | - | 6.0 | 6.6 | ms |
| | Fast programming time for 1 block (64 byte) | - | - | 3.0 | 3.3 | |
| $t_{ERASE}$ | Erase time for 1 block (64 byte) | - | - | 3.0 | 3.3 | |

**Table 46. Flash program memory**

| Symbol | Parameter | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| $T_{WE}$ | Temperature for writing and erasing | - | -40 | 150 | °C |
| $N_{WE}$ | Flash program memory endurance (erase/write cycles)(1) | $T_A$ = 25 °C | 1000 | - | cycles |
| $t_{RET}$ | Data retention time | $T_A$ = 25 °C | 40 | - | years |
| | | $T_A$ = 55 °C | 20 | - | |

1. The physical granularity of the memory is 4 byte, so cycling is performed on 4 byte even when a write/erase operation addresses a single byte.

**Table 47. Data memory**

| Symbol | Parameter | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| $T_{WE}$ | Temperature for writing and erasing | - | -40 | 150 | °C |
| $N_{WE}$ | Data memory endurance(1) (erase/write cycles) | $T_A$ = 25 °C | 300 k | - | cycles |
| | | $T_A$ = -40°C to 125 °C | 100 k(2) | - | |
| $t_{RET}$ | Data retention time | $T_A$ = 25 °C | 40(3) | - | years |
| | | $T_A$ = 55 °C | 20(2)(3) | - | |

1. The physical granularity of the memory is 4 byte, so cycling is performed on 4 byte even when a write/erase operation addresses a single byte.
2. More information on the relationship between data retention time and number of write/erase cycles is available in a separate technical document.
3. Retention time for 256B of data memory after up to 1000 cycles at 125 °C.

## 10.3.6 I/O port pin characteristics

### General characteristics

Subject to general operating conditions for $V_{DD}$ and $T_A$ unless otherwise specified. All unused pins must be kept at a fixed voltage, using the output mode of the I/O for example or an external pull-up or pull-down resistor.

**Table 48. I/O static characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Input low level voltage | - | -0.3 V | - | 0.3 x $V_{DD}$ | V |
| $V_{IH}$ | Input high level voltage | | 0.7 x $V_{DD}$ | - | $V_{DD}$ + 0.3 V | |
| $V_{hys}$ | Hysteresis(1) | | - | 700 | - | mV |
| $R_{pu}$ | Pull-up resistor | $V_{DD}$ = 5 V, $V_{IN}$ = $V_{SS}$ | 35 | 55 | 80 | kΩ |
| $t_R$, $t_F$ | Rise and fall time (10% - 90%) | Fast I/Os Load = 50 pF | - | - | 35(2) | ns |
| | | Standard and high sink I/Os Load = 50 pF | - | - | 125(2) | |
| | | Fast I/Os Load = 20 pF | | | 20(2) | |
| | | Standard and high sink I/Os Load = 20 pF | | | 50(2) | |
| $I_{lkg}$ | Digital input pad leakage current | $V_{SS} \le V_{IN} \le V_{DD}$ | - | - | ±1(3) | µA |
| $I_{lkg\ ana}$ | Analog input pad leakage current | $V_{SS} \le V_{IN} \le V_{DD}$ -40 °C < $T_A$ < 125 °C | - | - | ±250(3) | nA |
| | | $V_{SS} \le V_{IN} \le V_{DD}$ -40 °C < $T_A$ < 150 °C | - | - | ±500(3) | |
| $I_{lkg(inj)}$ | Leakage current in adjacent I/O(2) | Injection current ±4 mA | - | - | ±1(3) | µA |

1. Hysteresis voltage between Schmitt trigger switching levels. Guaranteed by characterization results.
2. Guaranteed by characterization results.
3. Guaranteed by design.

Figure 19. Typical $V_{IL}$ and $V_{IH}$ vs $V_{DD}$ @ 4 temperatures

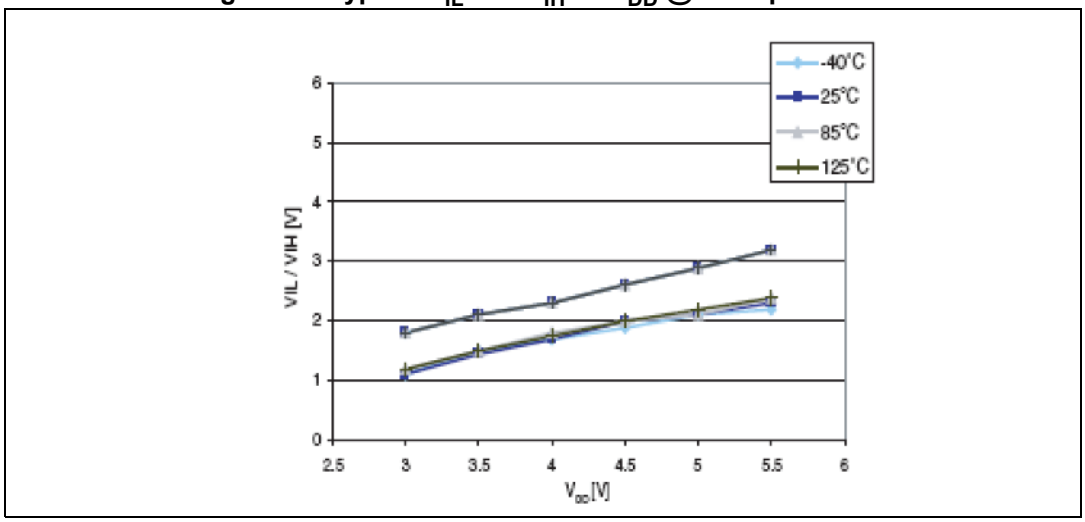



Figure 20. Typical pull-up resistance $R_{PU}$ vs $V_{DD}$ @ 4 temperatures

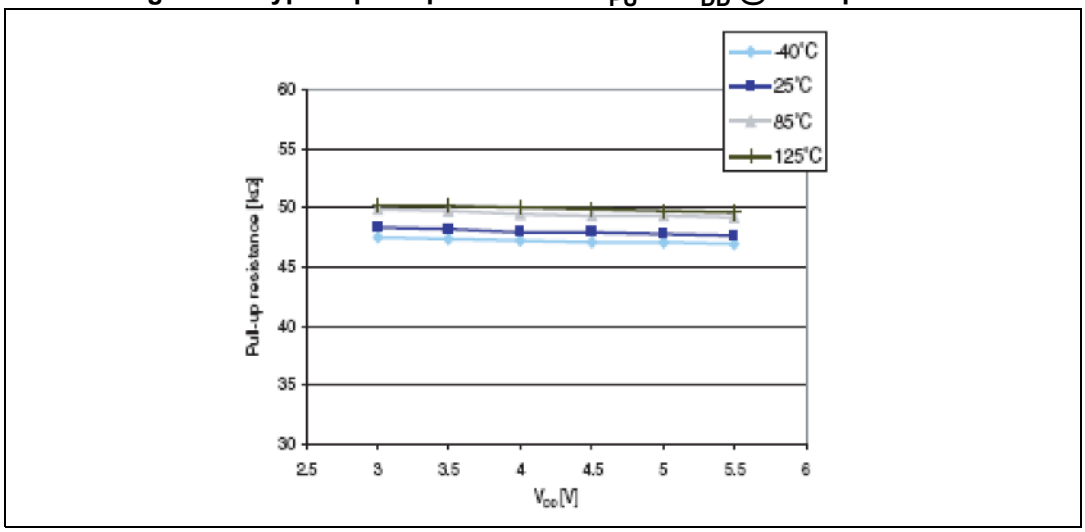


**Figure 21. Typical pull-up current $I_{pu}$ vs $V_{DD}$ @ 4 temperatures**

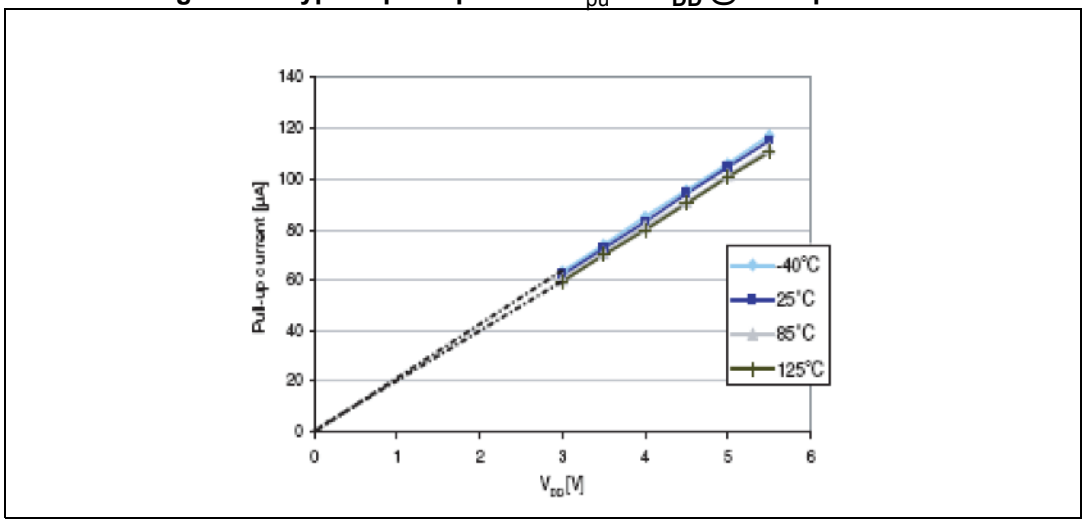



**Table 49. Output driving current (standard ports)**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{OL}$ | Output low level with 8 pins sunk | $I_{IO}$= 10 mA, $V_{DD}$ = 5 V | - | 2.0 | V |
| | Output low level with 4 pins sunk | $I_{IO}$ = 4 mA, $V_{DD}$ = 3.3 V | - | 1.0(1) | |
| $V_{OH}$ | Output high level with 8 pins sourced | $I_{IO}$ = 10 mA, $V_{DD}$ = 5 V | 2.8 | - | |
| | Output high level with 4 pins sourced | $I_{IO}$ = 4 mA, $V_{DD}$ = 3.3 V | 2.1(1) | - | |

1. Guaranteed by characterization results.

**Table 50. Output driving current (true open drain ports)**

| Symbol | Parameter | Conditions | Max | Unit |
|---|---|---|---|---|
| $V_{OL}$ | Output low level with 2 pins sunk | $I_{IO}$= 10 mA, $V_{DD}$ = 5 V | 1.0 | V |
| | | $I_{IO}$ = 10 mA, $V_{DD}$ = 3.3 V | 1.5(1) | |
| | | $I_{IO}$ = 20 mA, $V_{DD}$ = 5 V | 2.0(1) | |

1. Guaranteed by characterization results.

**Table 51. Output driving current (high sink ports)**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{OL}$ | Output low level with 8 pins sunk | $I_{IO}$= 10 mA, $V_{DD}$ = 5 V | - | 0.8 | V |
| | Output low level with 4 pins sunk | $I_{IO}$ = 10 mA, $V_{DD}$ = 3.3 V | - | 1.0(1) | |
| | | $I_{IO}$ = 20 mA, $V_{DD}$ = 5 V | | 1.5(1) | |
| $V_{OH}$ | Output high level with 8 pins sourced | $I_{IO}$ = 10 mA, $V_{DD}$ = 5 V | 4.0 | - | |
| | Output high level with 4 pins sourced | $I_{IO}$ = 10 mA, $V_{DD}$ = 3.3 V | 2.1(1) | - | |
| | | $I_{IO}$ = 20 mA, $V_{DD}$ = 5 V | 3.3(1) | - | |

1. Guaranteed by characterization results.

**Figure 22. Typ. $V_{OL}$ @ $V_{DD}$ = 5 V (standard ports)**

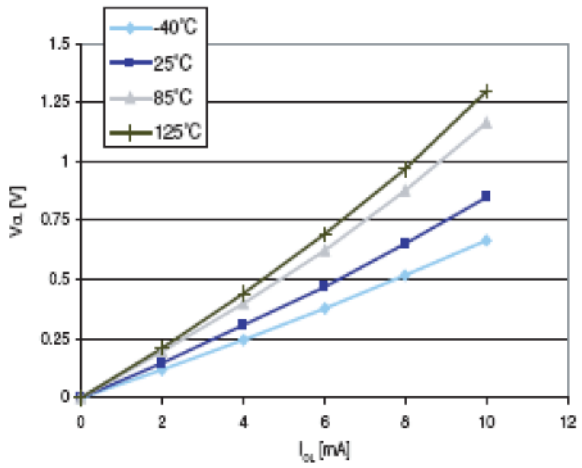



**Figure 23. Typ. $V_{OL}$ @ $V_{DD}$ = 3.3 V (standard ports)**

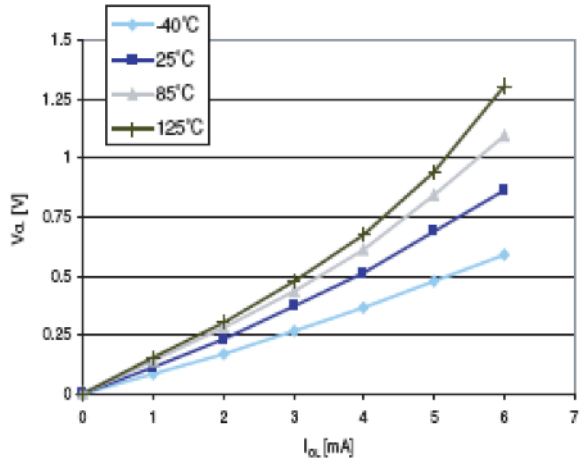


Figure 24. Typ. $V_{OL}$ @ $V_{DD}$ = 5 V (true open drain ports)

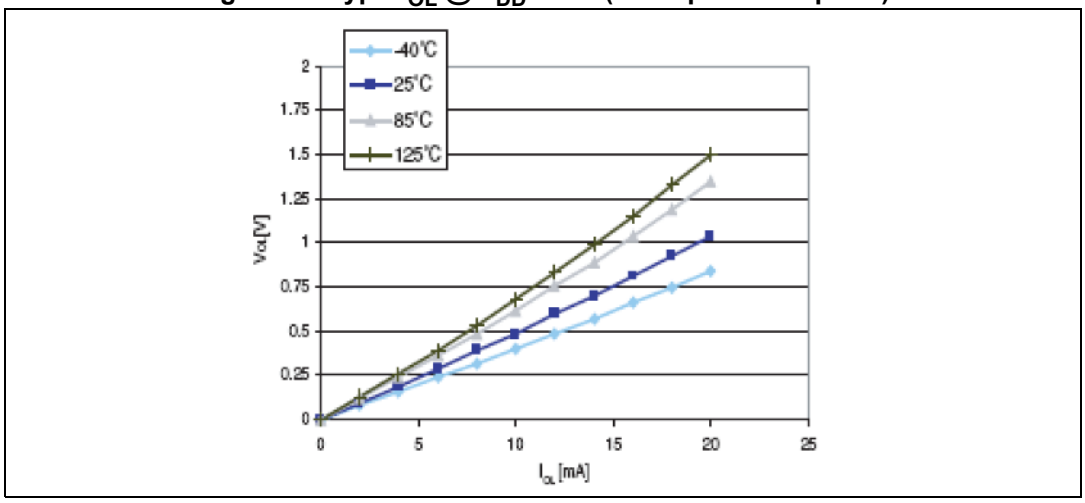



Figure 25. Typ. $V_{OL}$ @ $V_{DD}$ = 3.3 V (true open drain ports)

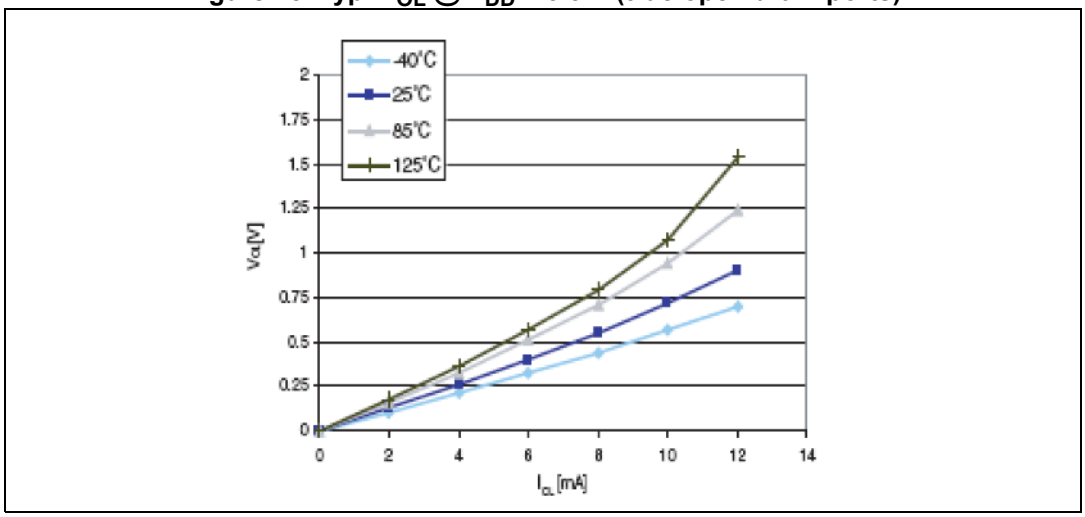



Figure 26. Typ. $V_{OL}$ @ $V_{DD}$ = 5 V (high sink ports)

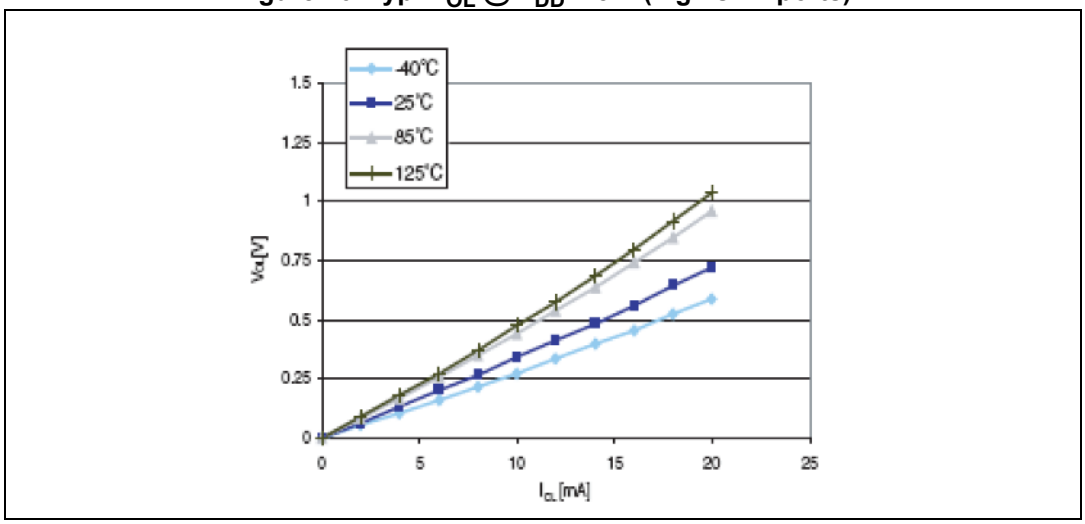


Figure 27. Typ. $V_{OL}$ @ $V_{DD}$ = 3.3 V (high sink ports)

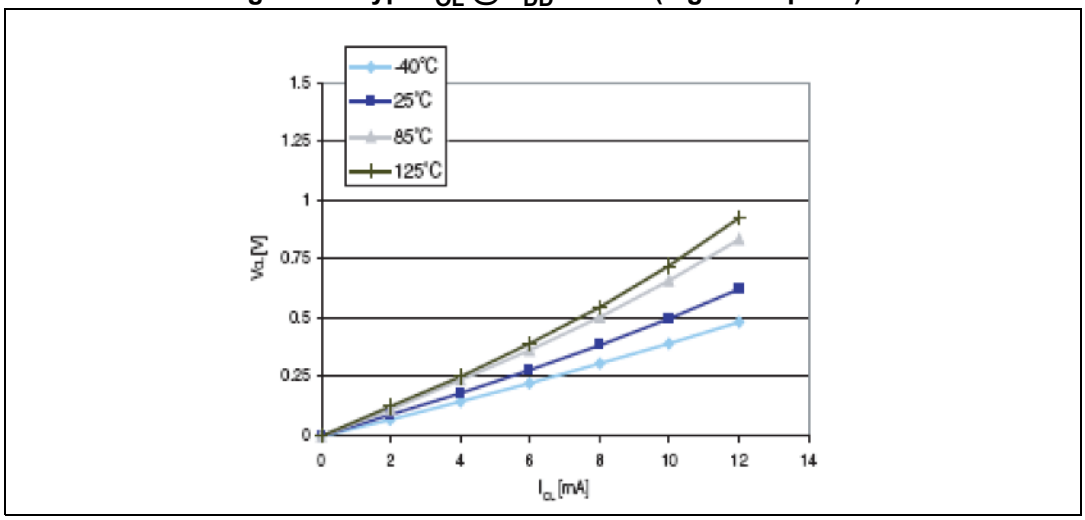



Figure 28. Typ. $V_{DD}$- $V_{OH}$ @ $V_{DD}$ = 5 V (standard ports)

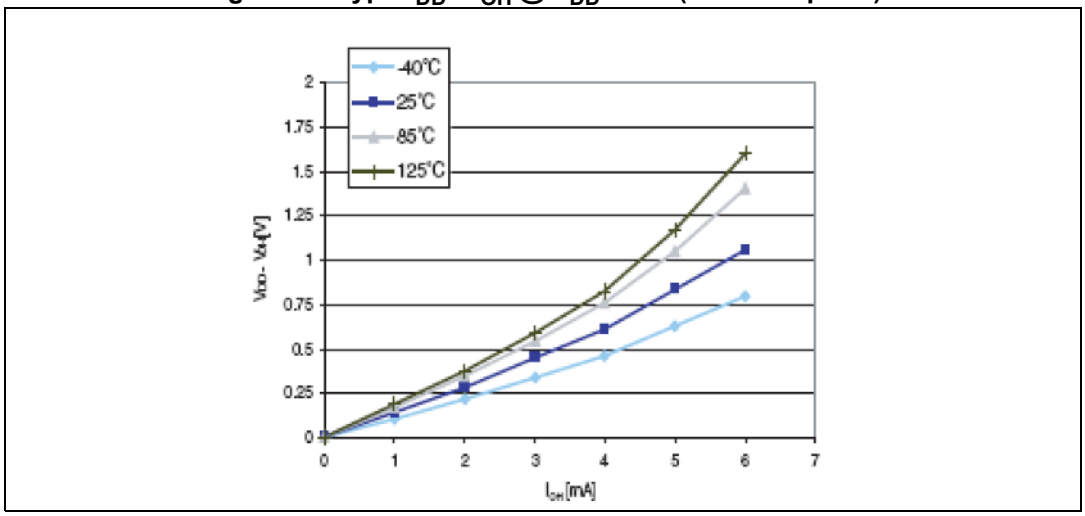



Figure 29. Typ. $V_{DD}$- $V_{OH}$ @ $V_{DD}$ = 3.3 V (standard ports)

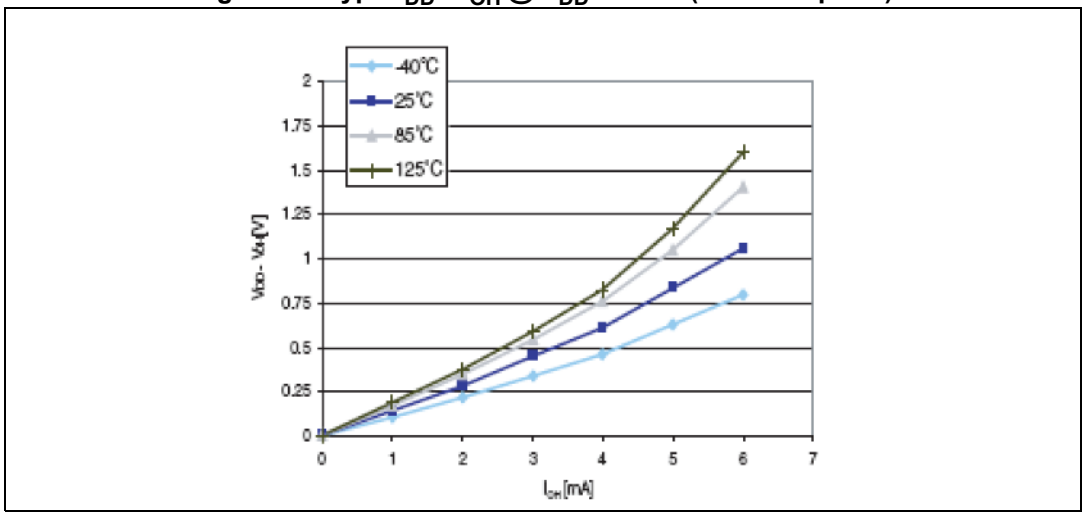


Figure 30. Typ. $V_{DD}$- $V_{OH}$ @ $V_{DD}$ = 5 V (high sink ports)

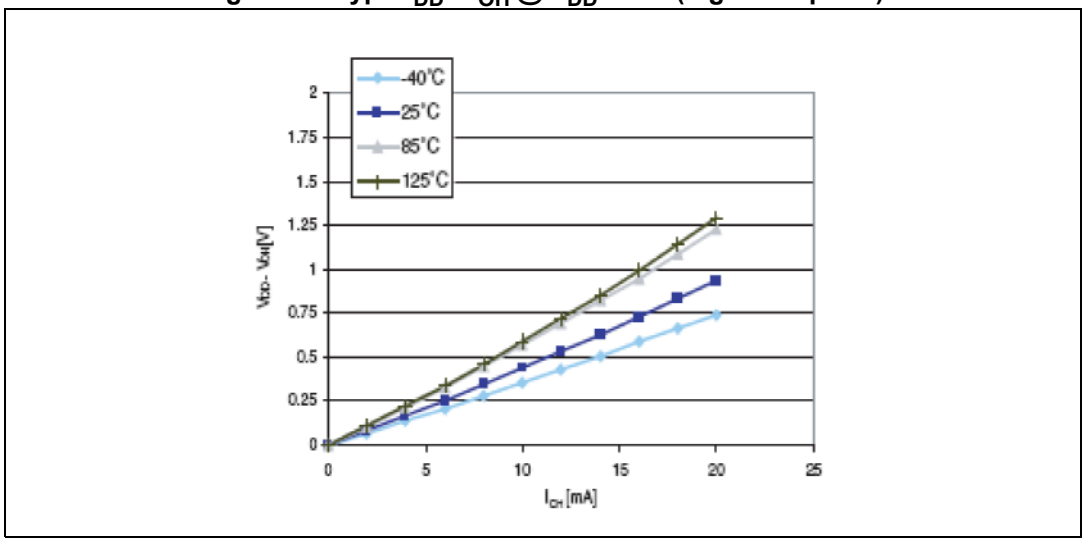
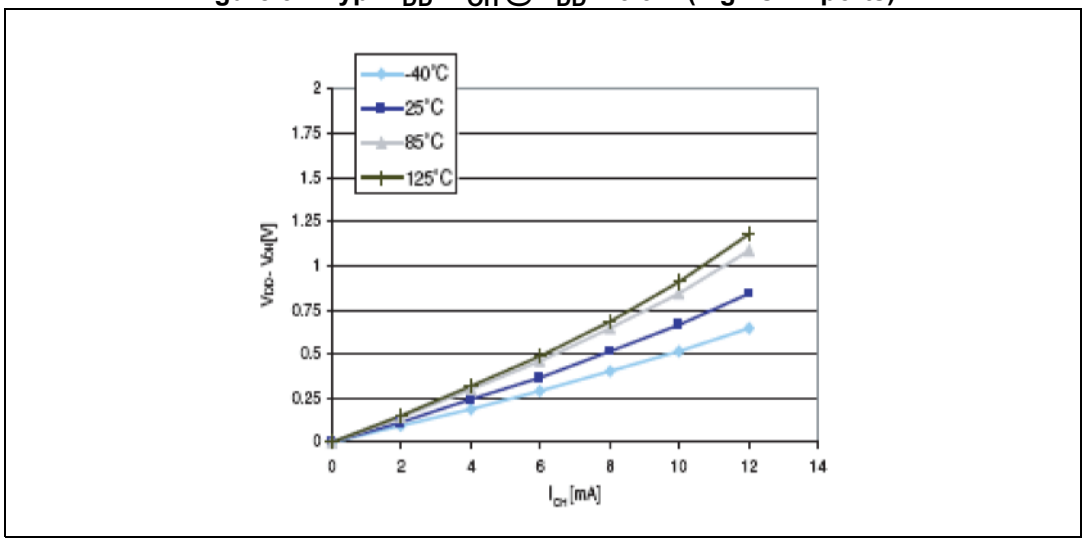



Figure 31. Typ. $V_{DD}$- $V_{OH}$ @ $V_{DD}$ = 3.3 V (high sink ports)



### 10.3.7 Reset pin characteristics

Subject to general operating conditions for $V_{DD}$ and $T_A$ unless otherwise specified.

**Table 52. NRST pin characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IL(NRST)}$ | NRST input low level voltage(1) | - | -0.3 | - | 0.3 x $V_{DD}$ | V |
| $V_{IH(NRST)}$ | NRST input high level voltage(1) | $I_{OL}$= 2 mA | 0.7 x $V_{DD}$ | - | $V_{DD}$ + 0.3 | |
| $V_{OL(NRST)}$ | NRST output low level voltage(1) | - | - | - | 0.5 | |
| $R_{PU(NRST)}$ | NRST pull-up resistor(2) | - | 30 | 55 | 80 | kΩ |
| $t_{IFP(NRST)}$ | NRST input filtered pulse(3) | - | - | - | 75 | ns |
| $t_{INFP(NRST)}$ | NRST Input not filtered pulse duration(3) | - | 500 | - | - | |
| $t_{OP(NRST)}$ | NRST output pulse(3) | - | 20 | - | - | µs |

1. Guaranteed by characterization results.
2. The $R_{PU}$ pull-up equivalent resistor is based on a resistive transistor.
3. Guaranteed by design.

**Figure 32. Typical NRST $V_{IL}$ and $V_{IH}$ vs $V_{DD}$ @ 4 temperatures**

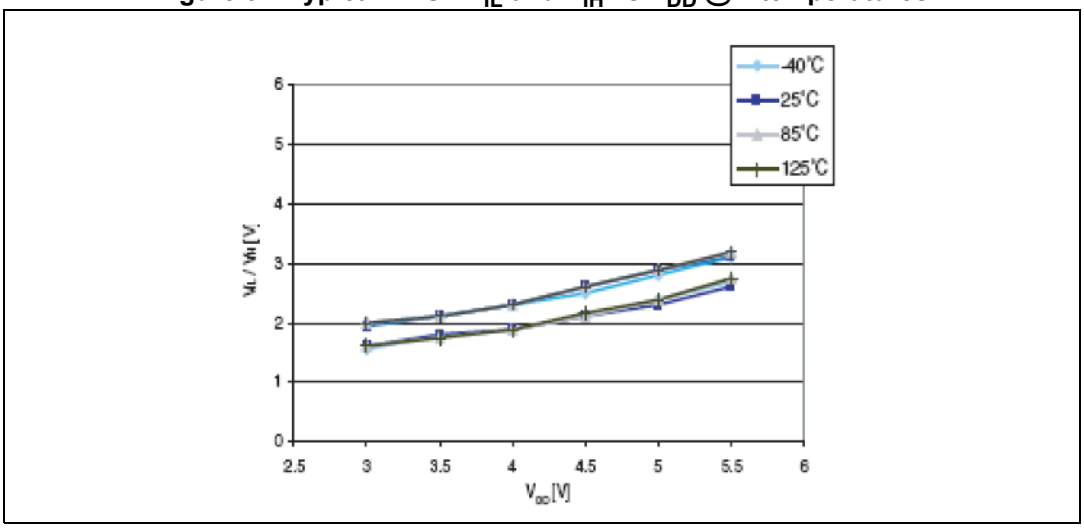


**Figure 33. Typical NRST pull-up resistance vs $V_{DD}$ @ 4 temperatures**

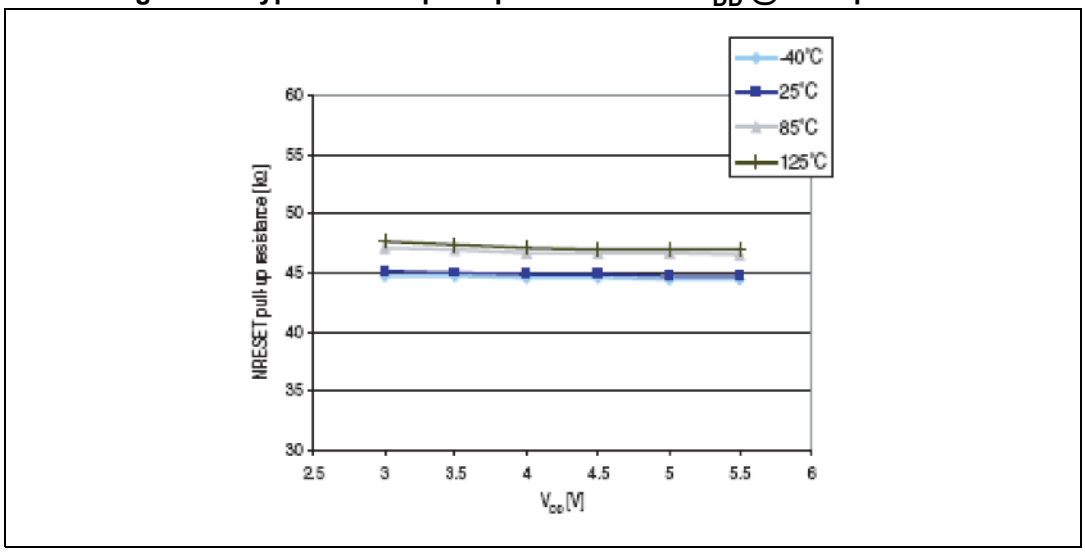
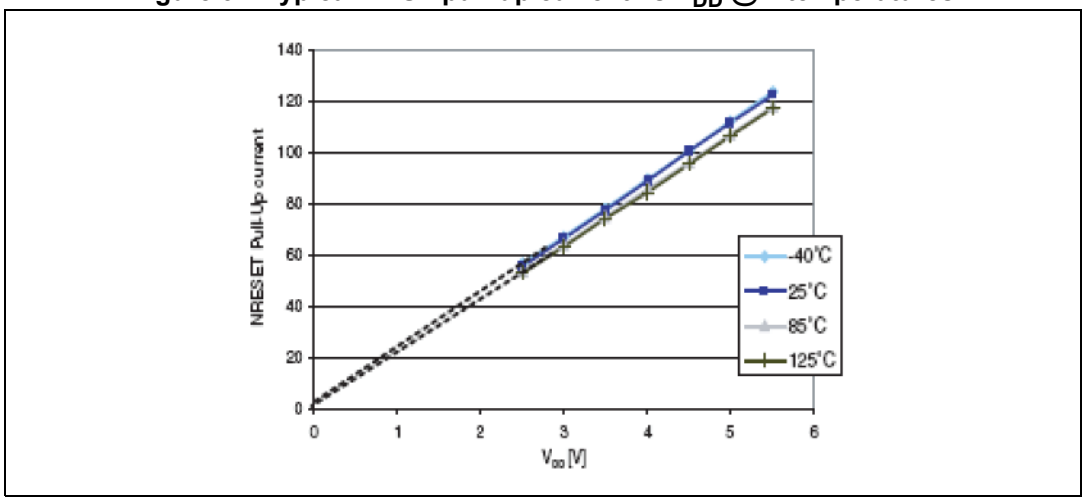


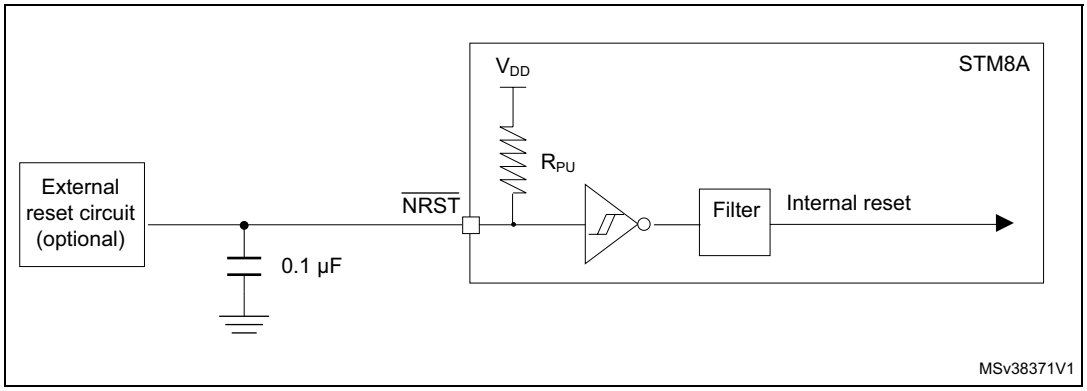

**Figure 34. Typical NRST pull-up current vs $V_{DD}$ @ 4 temperatures**




The reset network shown in *Figure 35* protects the device against parasitic resets. The user must ensure that the level on the NRST pin can go below $V_{IL(NRST)}$ max (see *Table 52: NRST pin characteristics*), otherwise the reset is not taken into account internally.

For power consumption sensitive applications, the external reset capacitor value can be reduced to limit the charge/discharge current. If NRST signal is used to reset external circuitry, attention must be taken to the charge/discharge time of the external capacitor to fulfill the external devices reset timing conditions. Minimum recommended capacity is 100 nF.

**Figure 35. Recommended reset pin protection**




## 10.3.8 SPI serial peripheral interface

Unless otherwise specified, the parameters given in *Table 53* are derived from tests performed under ambient temperature, $f_{MASTER}$ frequency and $V_{DD}$ supply voltage conditions. $t_{MASTER} = 1/f_{MASTER}$.

Refer to I/O port characteristics for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

**Table 53. SPI characteristics**

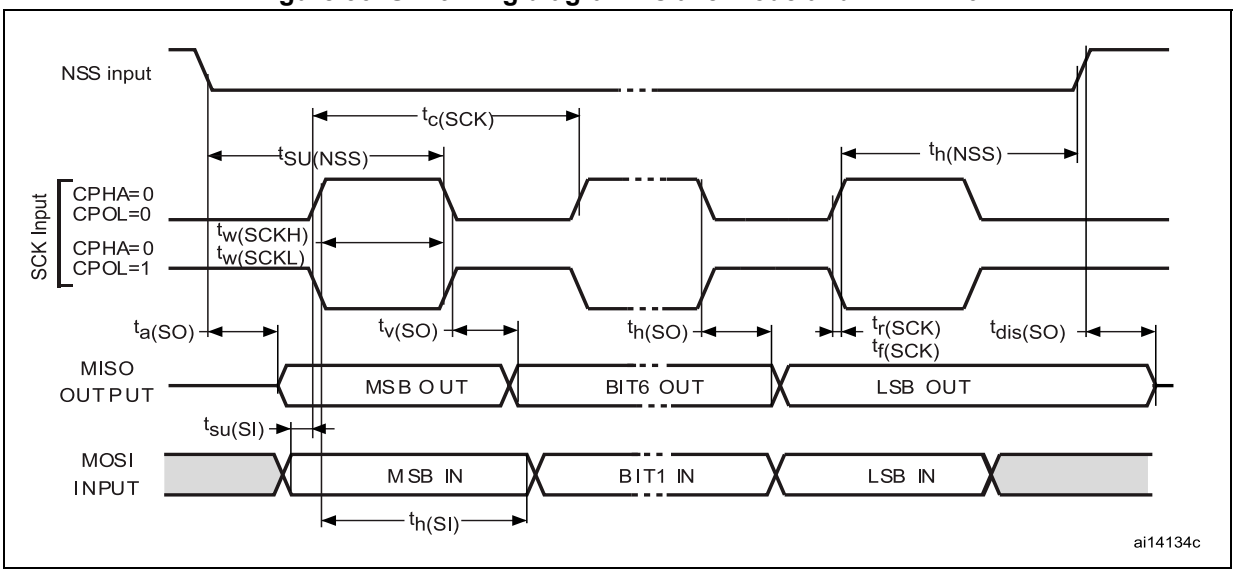
| Symbol | Parameter | Conditions(1) | Min | Max | Unit |
|---|---|---|---|---|---|
| $f_{SCK}$<br>$1/t_{c(SCK)}$ | SPI clock frequency | Master mode | 0 | 8 | MHz |
| | | Slave mode | 0 | 6 | |
| $t_{r(SCK)}$<br>$t_{f(SCK)}$ | SPI clock rise and fall time | Capacitive load:<br>C = 30 pF | - | 25 | ns |
| $t_{su(NSS)}$(2) | NSS setup time | Slave mode | 4 * $t_{MASTER}$ | - | |
| $t_{h(NSS)}$(2) | NSS hold time | Slave mode | 70 | - | |
| $t_{w(SCKH)}$(2)<br>$t_{w(SCKL)}$(2) | SCK high and low time | Master mode | $t_{SCK}/2$ - 15 | $t_{SCK}/2$ + 15 | |
| $t_{su(MI)}$(2)<br>$t_{su(SI)}$(2) | Data input setup time | Master mode | 5 | - | |
| | | Slave mode | 5 | - | |
| $t_{h(MI)}$(2)<br>$t_{h(SI)}$(2) | Data input hold time | Master mode | 7 | - | |
| | | Slave mode | 10 | - | |
| $t_{a(SO)}$(2)(3) | Data output access time | Slave mode | - | 3* $t_{MASTER}$ | |
| $t_{dis(SO)}$(2)(4) | Data output disable time | Slave mode | 25 | - | |
| $t_{v(SO)}$(2) | Data output valid time | Slave mode<br>(after enable edge) | - | 65 | |
| $t_{v(MO)}$(2) | Data output valid time | Master mode<br>(after enable edge) | - | 36 | |

**Table 53. SPI characteristics (continued)**

| Symbol | Parameter | Conditions[1] | Min | Max | Unit |
|---|---|---|---|---|---|
| $t_{h(SO)}$[2] | Data output hold time | Slave mode (after enable edge) | 27 | - | ns |
| $t_{h(MO)}$[2] | | Master mode (after enable edge) | 11 | - | |

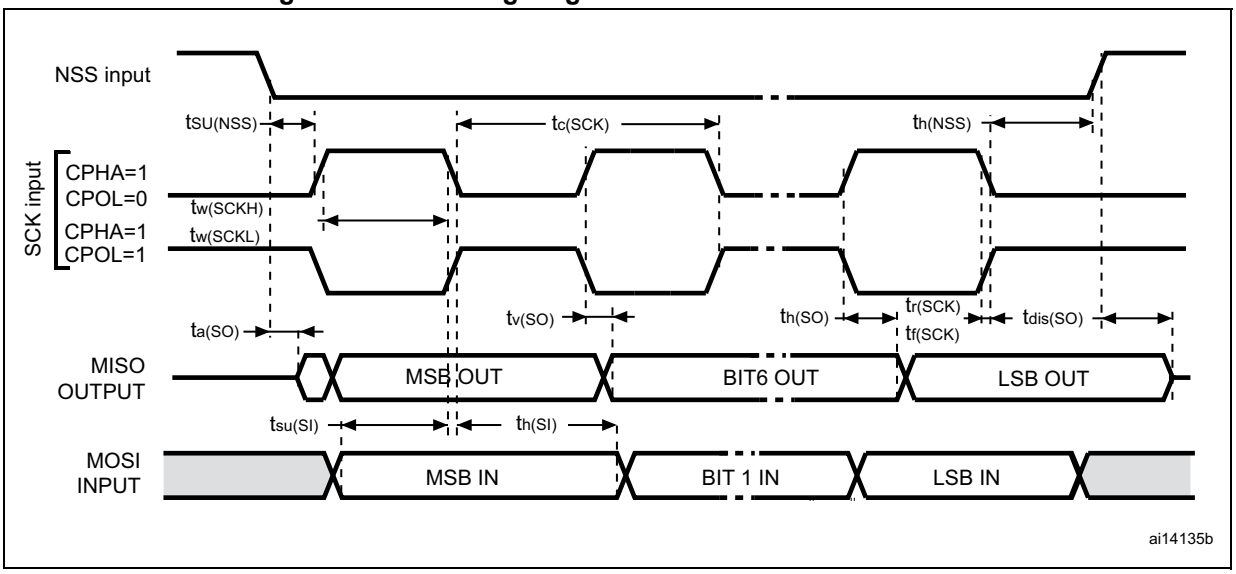
1. Parameters are given by selecting 10 MHz I/O output frequency.
2. Values based on design simulation and/or characterization results, and not tested in production.
3. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
4. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z.

**Figure 36. SPI timing diagram - slave mode and CPHA = 0**



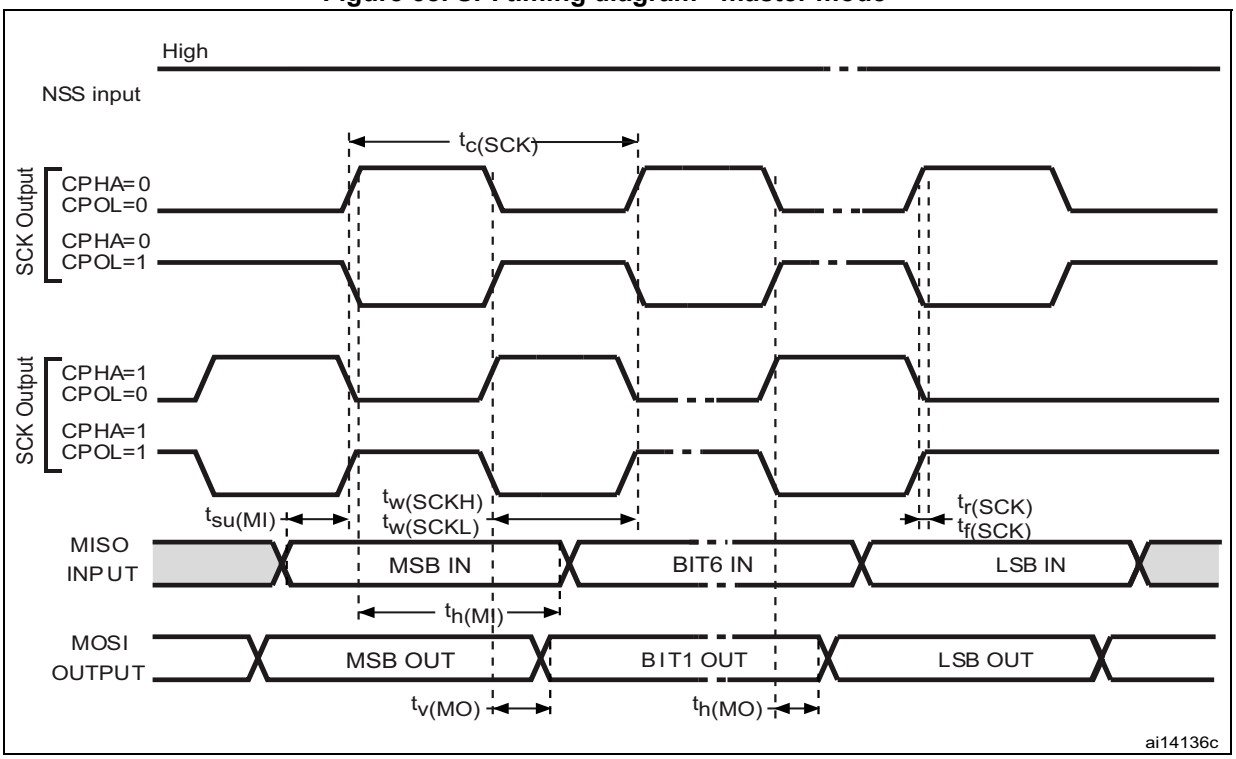

1. Measurement points are made at CMOS levels: 0.3 $V_{DD}$ and 0.7 $V_{DD}$.

**Figure 37. SPI timing diagram - slave mode and CPHA = 1**




1. Measurement points are at CMOS levels: 0.3 $V_{DD}$ and 0.7 $V_{DD}$.

**Figure 38. SPI timing diagram - master mode(1)**




1. Measurement points are at CMOS levels: 0.3 $V_{DD}$ and 0.7 $V_{DD}$.

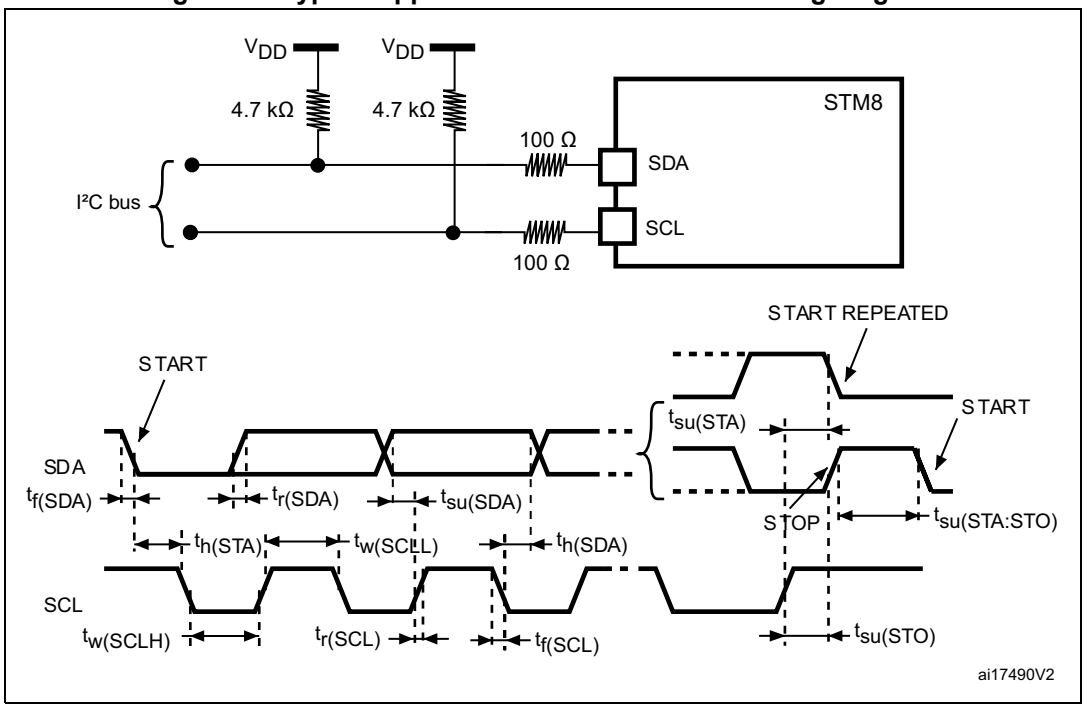
### 10.3.9 I²C interface characteristics

**Table 54. I²C characteristics**

| Symbol | Parameter | Standard mode I²C | | Fast mode I²C(1) | | Unit |
|---|---|---|---|---|---|---|
| | | Min(2) | Max(2) | Min(2) | Max(2) | |
| $t_{w(SCLL)}$ | SCL clock low time | 4.7 | - | 1.3 | - | µs |
| $t_{w(SCLH)}$ | SCL clock high time | 4.0 | - | 0.6 | - | |
| $t_{su(SDA)}$ | SDA setup time | 250 | - | 100 | - | ns |
| $t_{h(SDA)}$ | SDA data hold time | 0(3) | 3450 | 0(4) | 900(3) | |
| $t_{r(SDA)}$ $t_{r(SCL)}$ | SDA and SCL rise time | - | 1000 | - | 300 | |
| $t_{f(SDA)}$ $t_{f(SCL)}$ | SDA and SCL fall time | - | 300 | - | 300 | |
| $t_{h(STA)}$ | START condition hold time | 4.0 | - | 0.6 | - | µs |
| $t_{su(STA)}$ | Repeated START condition setup time | 4.7 | - | 0.6 | - | |
| $t_{su(STO)}$ | STOP condition setup time | 4.0 | - | 0.6 | - | |
| $t_{w(STO:STA)}$ | STOP to START condition time (bus free) | 4.7 | - | 1.3 | - | |
| $t_{SP}$ | Pulse width of spikes suppressed by the input filter | 0 | 50(5) | 0 | 50 | ns |
| $C_b$ | Capacitive load for each bus line | - | 400 | - | 400 | pF |

1. $f_{MASTER}$, must be at least 8 MHz to achieve max fast I²C speed (400 kHz)
2. Data based on standard I²C protocol requirement, not tested in production
3. The maximum hold time of the start condition has only to be met if the interface does not stretch the low time
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL
5. The minimum width of the spikes filtered by the analog filter is above $t_{SP(max)}$

**Figure 39. Typical application with I2C bus and timing diagram**




1. Measurement points are made at CMOS levels: 0.3 x $V_{DD}$ and 0.7 x $V_{DD}$.

### 10.3.10 10-bit ADC characteristics

Subject to general operating conditions for $V_{DD}$, $f_{MASTER}$, and $T_A$ unless otherwise specified.

**Table 55. ADC characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{ADC}$ | ADC clock frequency | $V_{DD}$ = 3 to 5.5 V | 1 | - | 4 | MHz |
| | | $V_{DD}$ = 4.5 to 5.5 V | 1 | - | 6 | |
| $V_{AIN}$ | Conversion voltage range(1) | - | $V_{SS}$ | - | $V_{DD}$ | V |
| $V_{BGREF}$ | Internal bandgap reference voltage | $V_{DD}$ = 3 to 5.5 V | 1.19(2) | 1.22 | 1.25(2) | V |
| $C_{ADC}$ | Internal sample and hold capacitor | - | - | 3 | - | pF |
| $t_S$(1) | Minimum sampling time | $f_{ADC}$ = 4MHz | - | 0.75 | - | µs |
| | | $f_{ADC}$ = 6 MHz | - | 0.5 | - | |
| $t_{STAB}$ | Wakeup time from standby | - | - | 7 | - | |
| $t_{CONV}$ | Minimum total conversion time including sampling time, 10-bit resolution | $f_{ADC}$ = 4 Hz | 3.5 | | | µs |
| | | $f_{ADC}$ = 6 MHz | 2.33 | | | |
| | | - | 14 | | | $1/f_{ADC}$ |

1. During the sample time the input capacitance $C_{AIN}$ (3 pF max) can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within $t_S$. After the end of the sample time $t_S$, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock $t_S$ depend on programming.
2. Tested in production.

**Table 56. ADC accuracy with RAIN < 10 kΩ, $V_{DD}$ = 5 V**

| Symbol | Parameter | Conditions | Typ | Max(1) | Unit |
|---|---|---|---|---|---|
| $\|E_T\|$ | Total unadjusted error(2) | $f_{ADC}$ = 2 MHz | 1.6 | 3.5 | LSB |
| | | $f_{ADC}$ = 4 MHz | 2.2 | 4 | |
| | | $f_{ADC}$ = 6 MHz | 2.4 | 4.5 | |
| $\|E_O\|$ | Offset error(2) | $f_{ADC}$ = 2 MHz | 1.1 | 2.5 | |
| | | $f_{ADC}$ = 4 MHz | 1.5 | 3 | |
| | | $f_{ADC}$ = 6 MHz | 1.8 | 3 | |
| $\|E_G\|$ | Gain error(2) | $f_{ADC}$ = 2 MHz | 1.5 | 3 | |
| | | $f_{ADC}$ = 4 MHz | 2.1 | 3 | |
| | | $f_{ADC}$ = 6 MHz | 2.2 | 4 | |
| $\|E_D\|$ | Differential linearity error(2) | $f_{ADC}$ = 2 MHz | 0.7 | 1.5 | |
| | | $f_{ADC}$ = 4 MHz | 0.7 | 1.5 | |
| | | $f_{ADC}$ = 6 MHz | 0.7 | 1.5 | |
| $\|E_L\|$ | Integral linearity error(2) | $f_{ADC}$ = 2 MHz | 0.6 | 1.5 | |
| | | $f_{ADC}$ = 4 MHz | 0.8 | 2 | |
| | | $f_{ADC}$ = 6 MHz | 0.8 | 2 | |

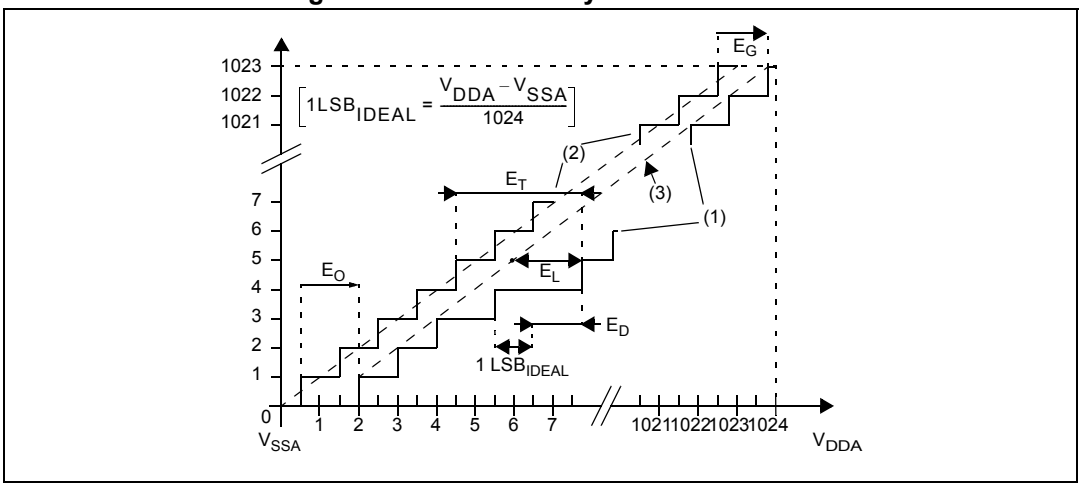
1. Max value is guaranteed by characterization results.
2. ADC accuracy vs. negative injection current: Injecting negative current on any of the analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current. Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in the I/O port pin characteristics section does not affect the ADC accuracy.

**Table 57. ADC accuracy with RAIN < 10 kΩ, $V_{DD}$ = 3.3 V**

| Symbol | Parameter | Conditions | Typ | Max(1) | Unit |
|---|---|---|---|---|---|
| $\|E_T\|$ | Total unadjusted error | $f_{ADC}$ = 2 MHz | 1.6 | 3.5 | LSB |
| | | $f_{ADC}$ = 4 MHz | 1.9 | 4 | |
| $\|E_O\|$ | Offset error | $f_{ADC}$ = 2 MHz | 1 | 2.5 | |
| | | $f_{ADC}$ = 4 MHz | 1.5 | 2.5 | |
| $\|E_G\|$ | Gain error | $f_{ADC}$ = 2 MHz | 1.3 | 3 | |
| | | $f_{ADC}$ = 4 MHz | 2 | 3 | |
| $\|E_D\|$ | Differential linearity error | $f_{ADC}$ = 2 MHz | 0.7 | 1 | |
| | | $f_{ADC}$ = 4 MHz | 0.7 | 1.5 | |
| $\|E_L\|$ | Integral linearity error | $f_{ADC}$ = 2 MHz | 0.6 | 1.5 | |
| | | $f_{ADC}$ = 4 MHz | 0.8 | 2 | |

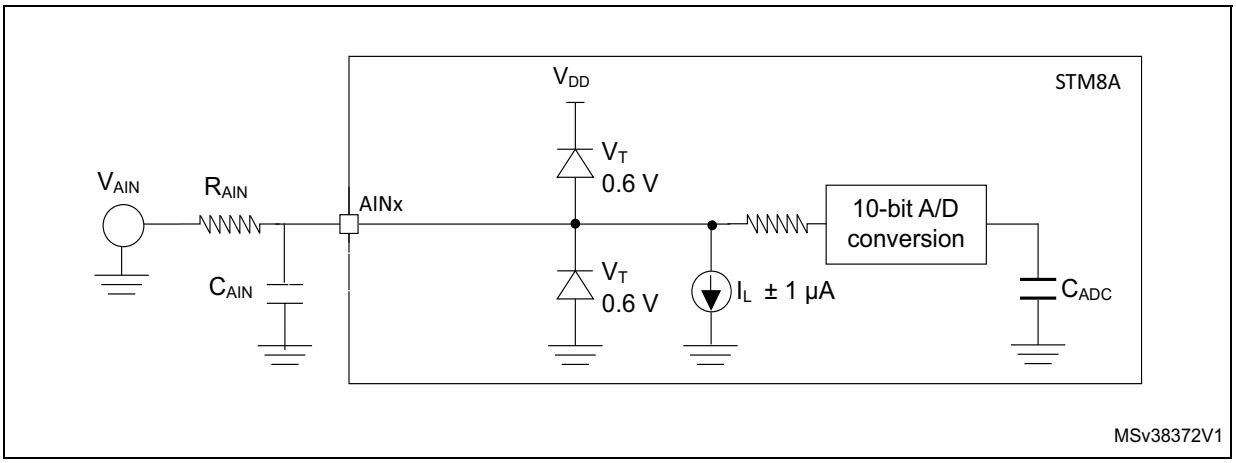
1. Max value is guaranteed by characterization results.

**Figure 40. ADC accuracy characteristics**




1. Example of an actual transfer curve
2. The ideal transfer curve
3. End point correlation line
   **$E_T$** = Total unadjusted error: Maximum deviation between the actual and the ideal transfer curves.
   **$E_O$** = Offset error: Deviation between the first actual transition and the first ideal one.
   **$E_G$** = Gain error: Deviation between the last ideal transition and the last actual one.
   **$E_D$** = Differential linearity error: Maximum deviation between actual steps and the ideal one.
   **$E_L$** = Integral linearity error: Maximum deviation between any actual transition and the end point correlation line.

**Figure 41. Typical application with ADC**




1. Legend: $R_{AIN}$ = external resistance, $C_{AIN}$ = capacitors, $C_{samp}$ = internal sample and hold capacitor.

## 10.3.11 EMC characteristics

Susceptibility tests are performed on a sample basis during product characterization.

### Functional EMS (electromagnetic susceptibility)

While executing a simple application (toggling 2 LEDs through I/O ports), the product is stressed by two electromagnetic events until a failure occurs (indicated by the LEDs).

- **FESD**: Functional electrostatic discharge (positive and negative) is applied on all pins of the device until a functional disturbance occurs. This test conforms with the IEC 61000-4-2 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to $V_{DD}$ and $V_{SS}$ through a 100 pF capacitor, until a functional disturbance occurs. This test conforms with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed. The test results are given in the table below based on the EMS levels and classes defined in application note AN1709.

### Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

***Prequalification trials***

Most of the common failures (unexpected reset and program counter corruption) can be recovered by applying a low state on the NRST pin or the oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see the application note reference AN1015).

**Table 58. EMS data**

| Symbol | Parameter | Conditions | Level/class |
|---|---|---|---|
| $V_{FESD}$ | Voltage limits to be applied on any I/O pin to induce a functional disturbance | $V_{DD}$ = 3.3 V, $T_A$= 25 °C, $f_{MASTER}$ = 16 MHz (HSI clock), Conforms to IEC 61000-4-2 | 2/B(1) |
| $V_{EFTB}$ | Fast transient voltage burst limits to be applied through 100 pF on $V_{DD}$ and $V_{SS}$ pins to induce a functional disturbance | $V_{DD}$= 3.3 V, $T_A$= 25 °C, $f_{MASTER}$ = 16 MHz (HSI clock), Conforms to IEC 61000-4-4 | 4/A |

1. Data obtained with HSI clock configuration, after applying hardware recommendations described in AN2860 (EMC guidelines for STM8S microcontrollers).

### Electromagnetic interference (EMI)

Based on a simple application running on the product (toggling 2 LEDs through the I/O ports), the product is monitored in terms of emission. This emission test is in line with the norm IEC 61967-2 which specifies the board and the loading of each pin.

**Table 59. EMI data**

| Symbol | Parameter | Conditions | | | | Unit |
|---|---|---|---|---|---|---|
| | | General conditions | Monitored frequency band | Max $f_{HSE}/f_{CPU}$(1) | | |
| | | | | 16 MHz/ 8 MHz | 16 MHz/ 16 MHz | |
| $S_{EMI}$ | Peak level | $V_{DD}$ = 5 V, $T_A$ = 25 °C, LQFP32 package conforming to IEC 61967-2 | 0.1 MHz to 30 MHz | 5 | 5 | dBµV |
| | | | 30 MHz to 130 MHz | 4 | 5 | |
| | | | 130 MHz to 1 GHz | 5 | 5 | |
| | EMI level | | — | 2.5 | 2.5 | level |

1. Guaranteed by characterization results.

### Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, DLU and LU) using specific measurement methods, the product is stressed to determine its performance in terms of electrical sensitivity. For more details, refer to the application note AN1181.

### Electrostatic discharge (ESD)

Electrostatic discharges (one positive then one negative pulses separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts*(n+1) supply pin). One model can be simulated: Human body model. This test conforms to the JESD22-A114A/A115A standard. For more details, refer to the application note AN1181.

**Table 60. ESD absolute maximum ratings**

| Symbol | Ratings | Conditions | Class | Maximum value(1) | Unit |
|---|---|---|---|---|---|
| $V_{ESD(HBM)}$ | Electrostatic discharge voltage (Human body model) | $T_A$ = 25°C, conforming to JESD22-A114 | 3A | 4000 | V |
| $V_{ESD(CDM)}$ | Electrostatic discharge voltage (Charge device model) | $T_A$= 25°C, conforming to JESD22-C101 | 3 | 500 | |
| $V_{ESD(MM)}$ | Electrostatic discharge voltage (Machine model) | $T_A$= 25°C, conforming to JESD22-A115 | B | 200 | |

1. Guaranteed by characterization results.

### Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage (applied to each power supply pin),
- A current injection (applied to each input, output and configurable I/O pin) are performed on each sample.

This test conforms to the EIA/JESD 78 IC latch-up standard. For more details, refer to the application note AN1181.

**Table 61. Electrical sensitivities**

| Symbol | Parameter | Conditions | Class(1) |
|---|---|---|---|
| LU | Static latch-up class | $T_A = 25$ °C | A |
| | | $T_A = 85$ °C | |
| | | $T_A = 125$ °C | |
| | | $T_A = 150$ °C | |

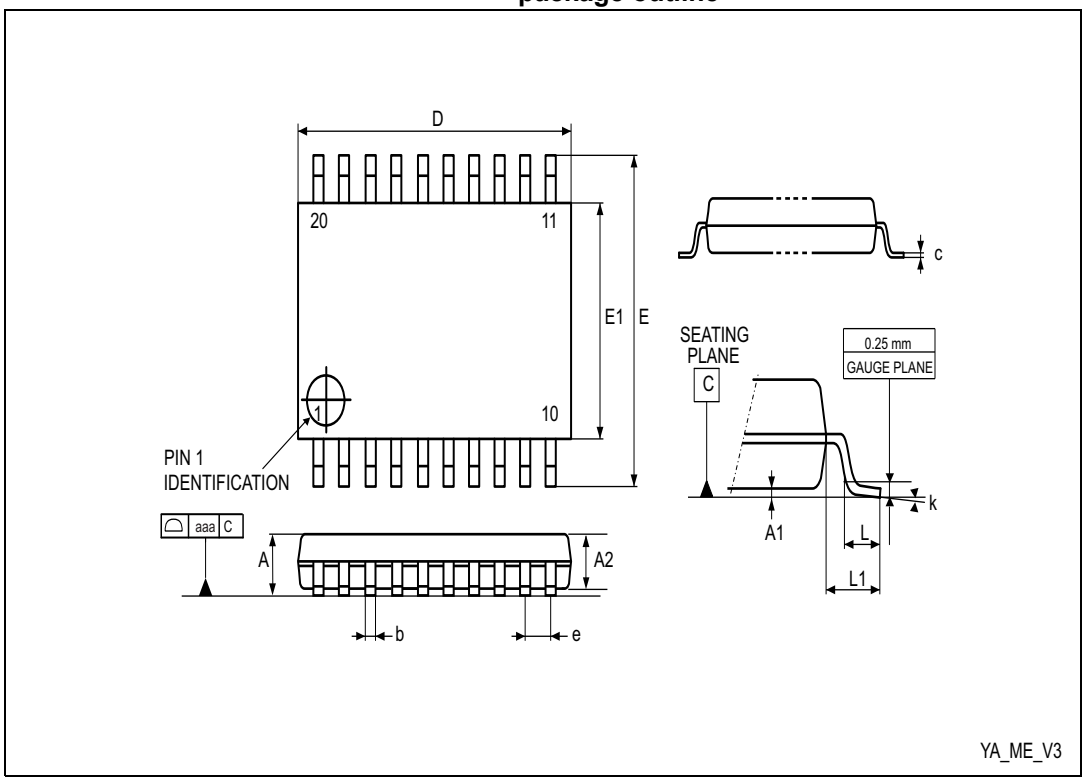
1. Class description: A Class is an STMicroelectronics internal specification. All its limits are higher than the JEDEC specifications, that means when a device belongs to class A it exceeds the JEDEC standard. B class strictly covers all the JEDEC criteria (international standard).

# 11 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

## 11.1 TSSOP20 package information

**Figure 42. TSSOP20 – 20-lead thin shrink small outline, 6.5 x 4.4 mm, 0.65 mm pitch, package outline**



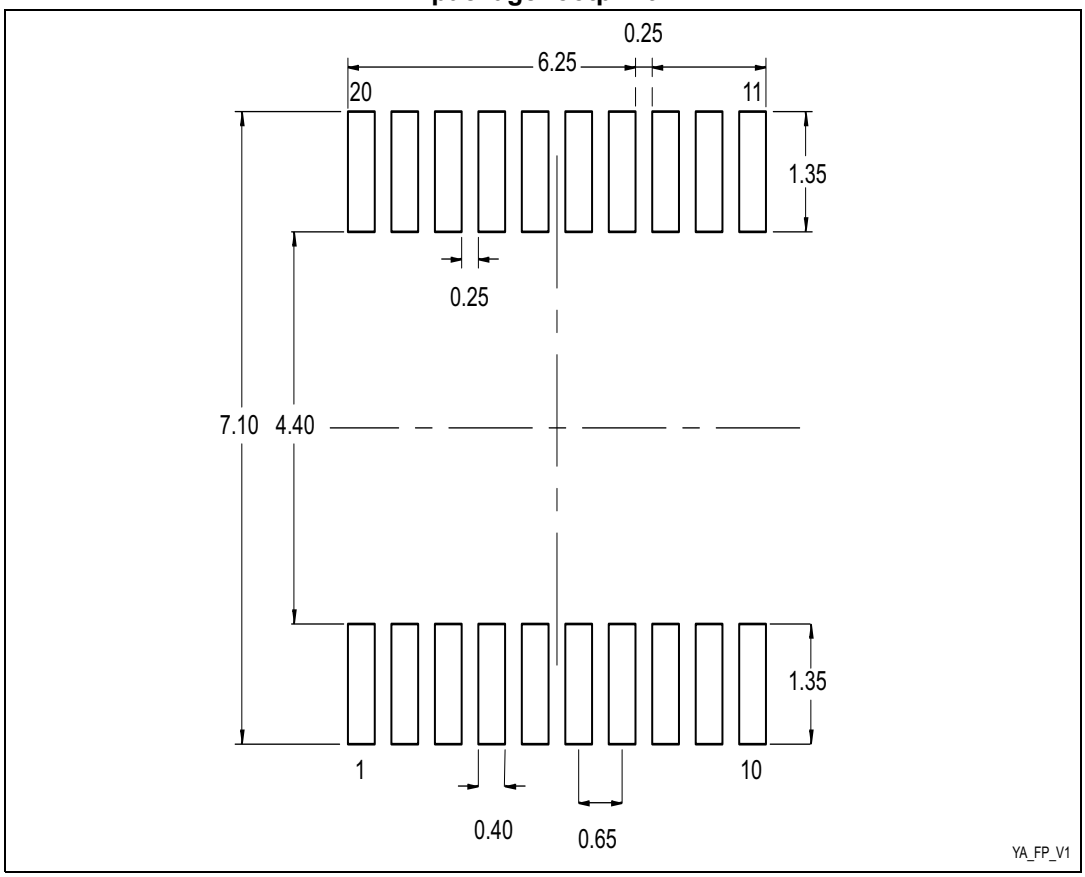

1. Drawing is not to scale.

**Table 62. TSSOP20 – 20-lead thin shrink small outline, 6.5 x 4.4 mm, 0.65 mm pitch, package mechanical data**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | - | - | 1.200 | - | - | 0.0472 |
| A1 | 0.050 | - | 0.150 | 0.0020 | - | 0.0059 |
| A2 | 0.800 | 1.000 | 1.050 | 0.0315 | 0.0394 | 0.0413 |
| b | 0.190 | - | 0.300 | 0.0075 | - | 0.0118 |
| c | 0.090 | - | 0.200 | 0.0035 | - | 0.0079 |
| D[2] | 6.400 | 6.500 | 6.600 | 0.2520 | 0.2559 | 0.2598 |
| E | 6.200 | 6.400 | 6.600 | 0.2441 | 0.2520 | 0.2598 |
| E1[3] | 4.300 | 4.400 | 4.500 | 0.1693 | 0.1732 | 0.1772 |
| e | - | 0.650 | - | - | 0.0256 | - |
| L | 0.450 | 0.600 | 0.750 | 0.0177 | 0.0236 | 0.0295 |
| L1 | - | 1.000 | - | - | 0.0394 | - |
| k | 0° | - | 8° | 0° | - | 8° |
| aaa | - | - | 0.100 | - | - | 0.0039 |

1. Values in inches are converted from mm and rounded to four decimal digits.
2. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.
3. Dimension “E1” does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25mm per side.

**Figure 43. TSSOP20 – 20-lead thin shrink small outline, 6.5 x 4.4 mm, 0.65 mm pitch, package footprint**



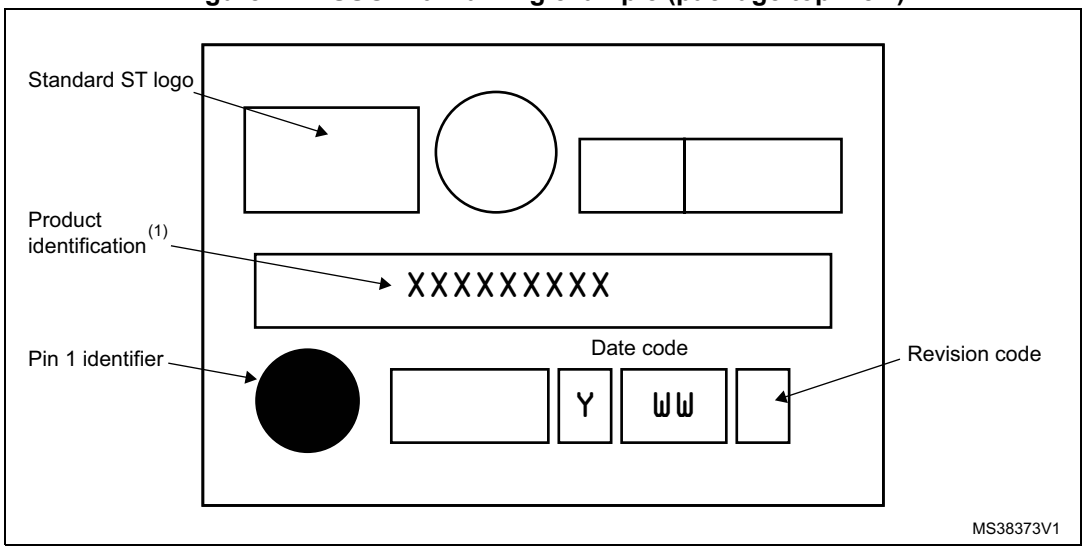

1. Dimensions are expressed in millimeters.

### Device marking for TSSOP20

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

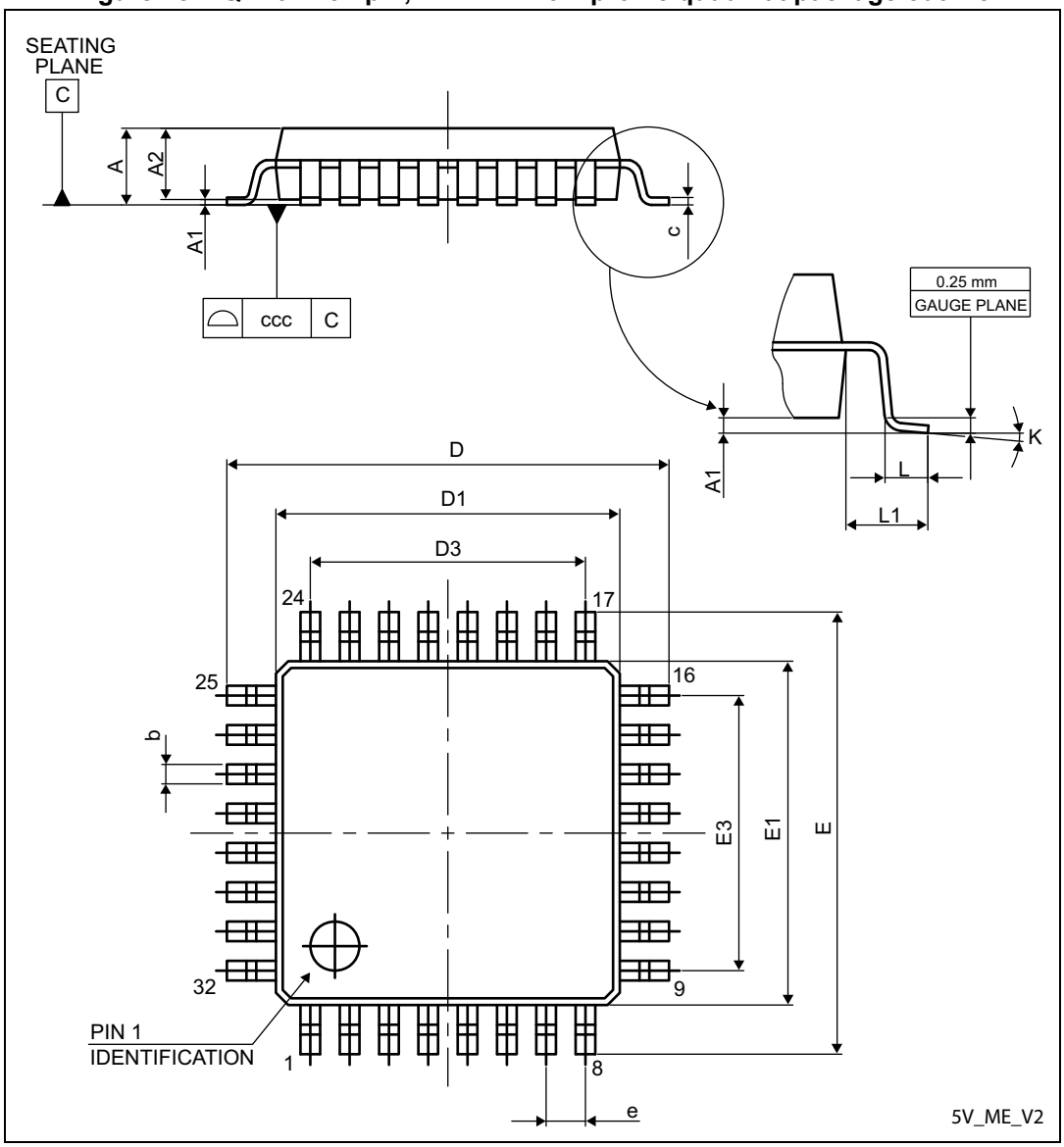
**Figure 44. TSSOP20 marking example (package top view)**




1. Parts marked as “ES” or “E” are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

## 11.2 LQFP32 package information

**Figure 45. LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package outline**



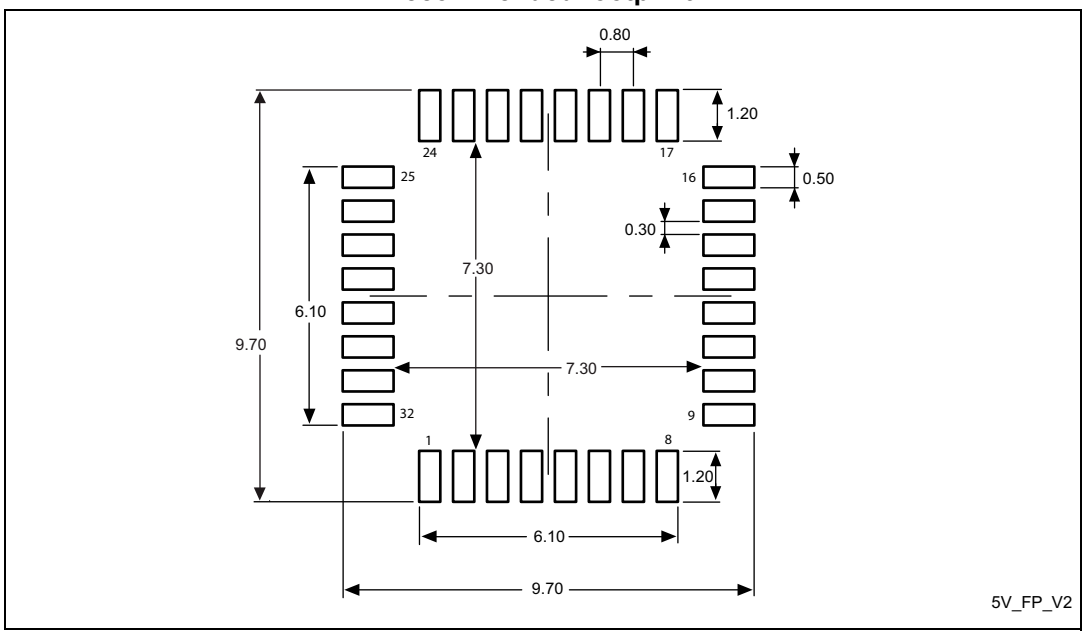

1. Drawing is not to scale.

**Table 63. LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package mechanical data**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | - | - | 1.600 | - | - | 0.0630 |
| A1 | 0.050 | - | 0.150 | 0.0020 | - | 0.0059 |
| A2 | 1.350 | 1.400 | 1.450 | 0.0531 | 0.0551 | 0.0571 |
| b | 0.300 | 0.370 | 0.450 | 0.0118 | 0.0146 | 0.0177 |
| c | 0.090 | - | 0.200 | 0.0035 | - | 0.0079 |
| D | 8.800 | 9.000 | 9.200 | 0.3465 | 0.3543 | 0.3622 |
| D1 | 6.800 | 7.000 | 7.200 | 0.2677 | 0.2756 | 0.2835 |
| D3 | - | 5.600 | - | - | 0.2205 | - |
| E | 8.800 | 9.000 | 9.200 | 0.3465 | 0.3543 | 0.3622 |
| E1 | 6.800 | 7.000 | 7.200 | 0.2677 | 0.2756 | 0.2835 |
| E3 | - | 5.600 | - | - | 0.2205 | - |
| e | - | 0.800 | - | - | 0.0315 | - |
| L | 0.450 | 0.600 | 0.750 | 0.0177 | 0.0236 | 0.0295 |
| L1 | - | 1.000 | - | - | 0.0394 | - |
| k | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| ccc | - | - | 0.100 | - | - | 0.0039 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 46. LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package recommended footprint**

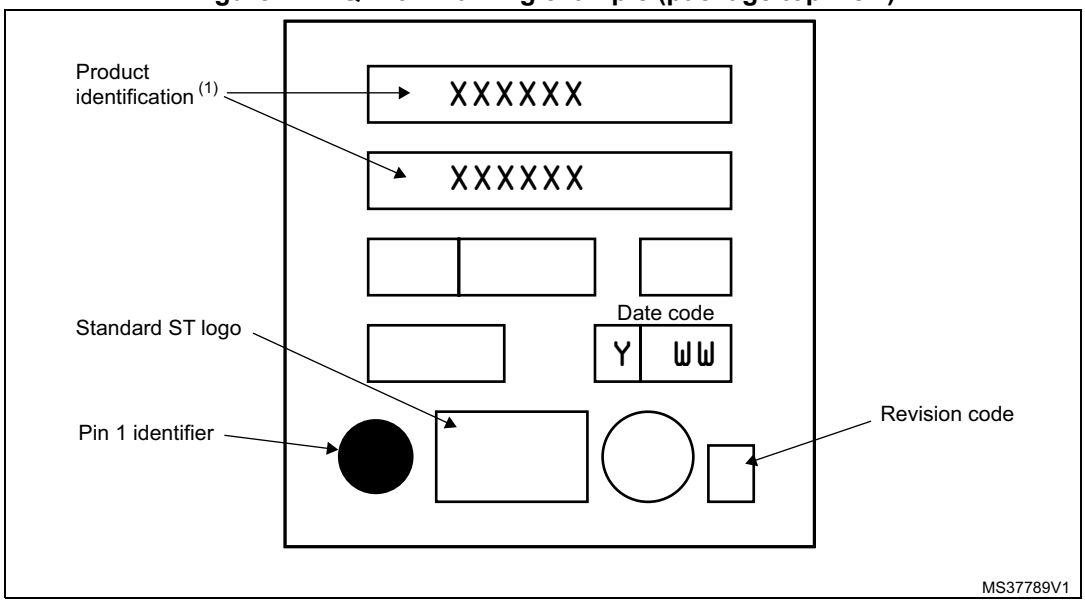



1. Dimensions are expressed in millimeters.

## Device marking for LQFP32

The following figure gives an example of topside marking orientation versus pin 1 identifier location. Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

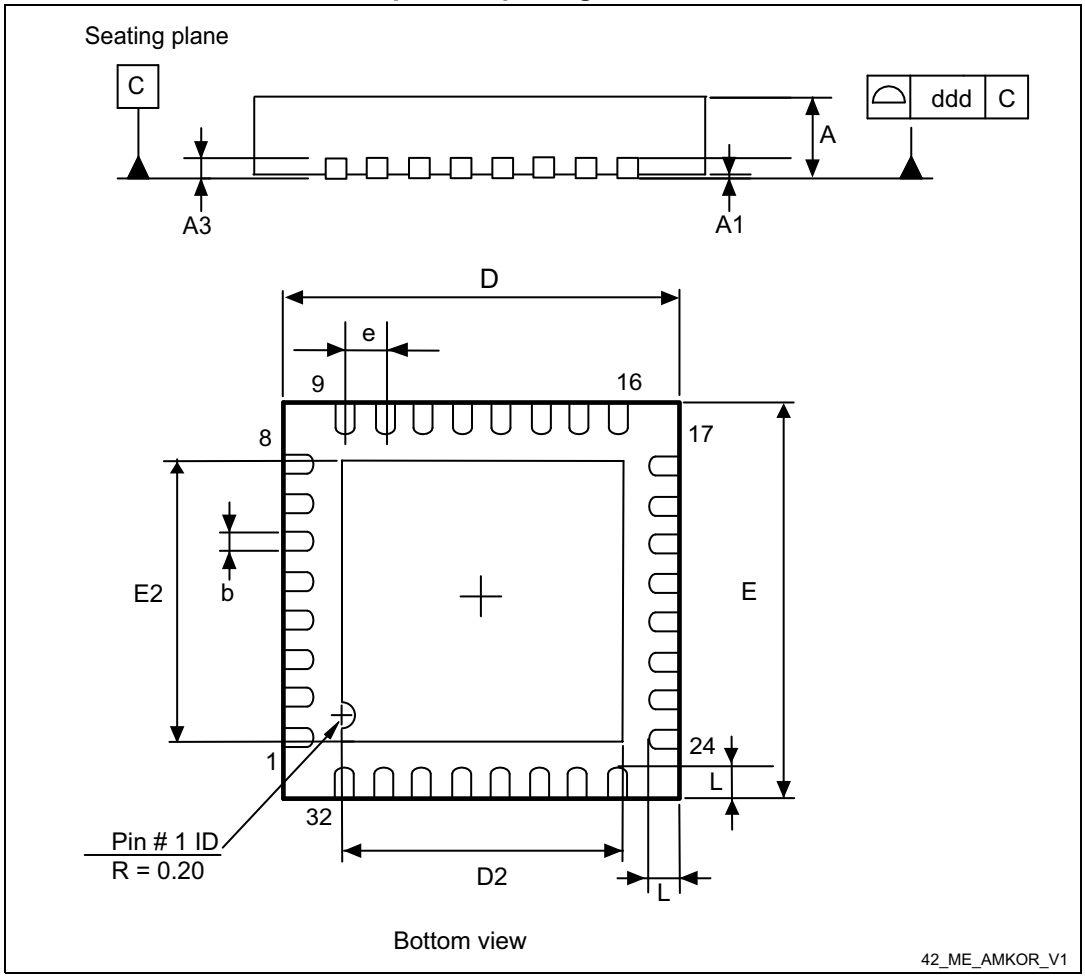
**Figure 47. LQFP32 marking example (package top view)**




1. Parts marked as “ES” or “E” are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

## 11.3 VFQFPN32 package information

**Figure 48. VFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch very thin profile fine pitch quad flat package outline**



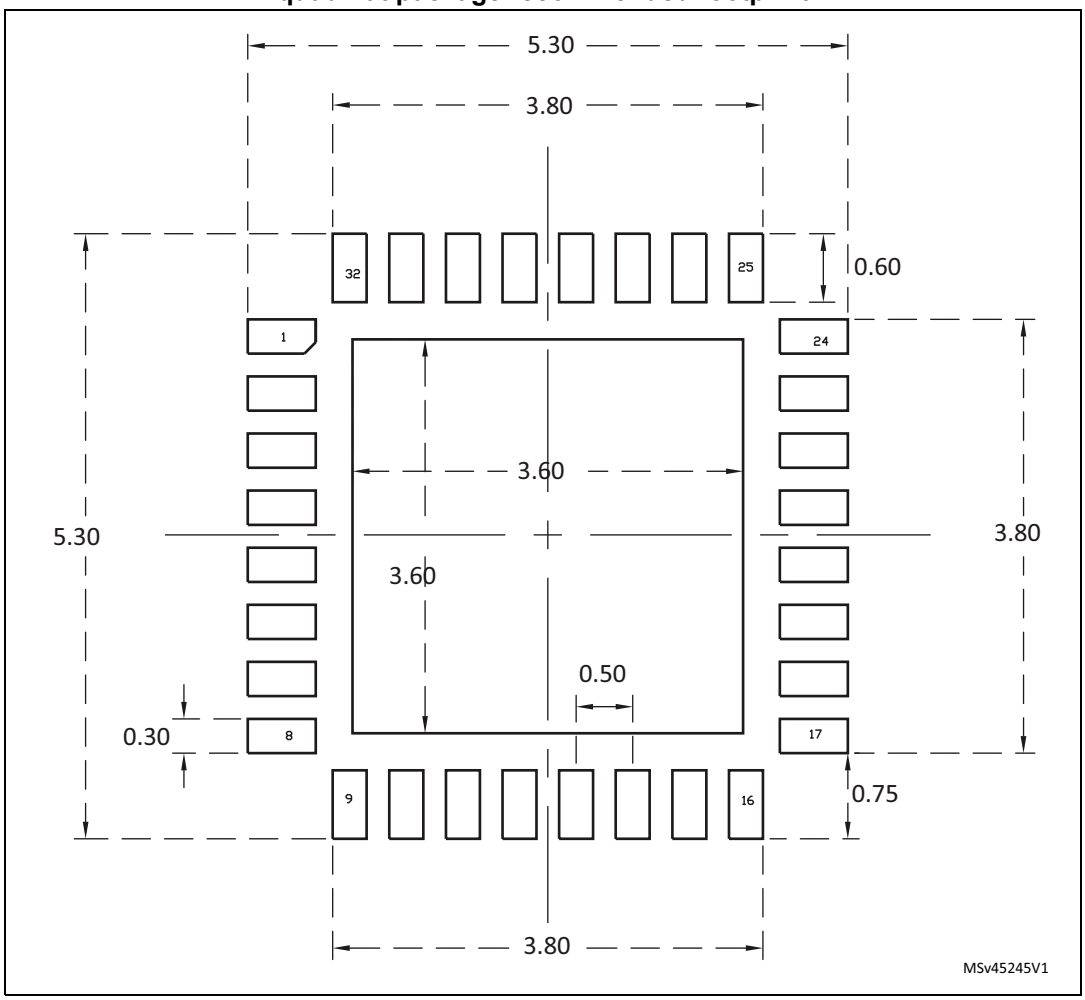

1. Drawing is not to scale.

**Table 64. VFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch very thin profile fine pitch quad flat package mechanical data**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | 0.800 | 0.900 | 1.000 | 0.0315 | 0.0354 | 0.0394 |
| A1 | 0.000 | 0.020 | 0.050 | 0.0000 | 0.0008 | 0.0020 |
| A3 | - | 0.200 | - | - | 0.0079 | - |
| b | 0.180 | 0.250 | 0.300 | 0.0071 | 0.0098 | 0.0118 |
| D | 4.850 | 5.000 | 5.150 | 0.1909 | 0.1969 | 0.2028 |
| D2 | 3.500 | 3.600 | 3.700 | 0.1378 | 0.1417 | 0.1457 |
| E | 4.850 | 5.000 | 5.150 | 0.1909 | 0.1969 | 0.2028 |
| E2 | 3.500 | 3.600 | 3.700 | 0.1378 | 0.1417 | 0.1457 |
| e | - | 0.500 | - | - | 0.0197 | - |
| L | 0.300 | 0.400 | 0.500 | 0.0118 | 0.0157 | 0.0197 |
| ddd | - | - | 0.050 | - | - | 0.0020 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 49. VFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch very thin profile fine pitch quad flat package recommended footprint**



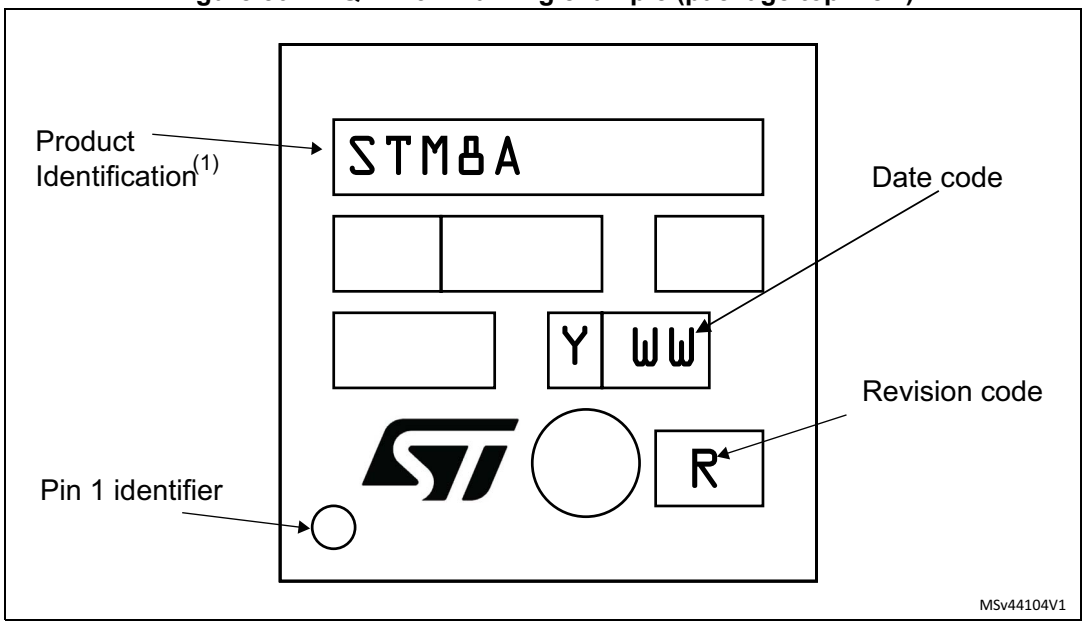

1. Dimensions are expressed in millimeters.

### Device marking for VFQFPN32

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

**Figure 50. VFQFPN32 marking example (package top view)**




1. Parts marked as “ES” or “E” are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

## 11.4 Thermal characteristics

The maximum chip junction temperature ($T_{Jmax}$) must never exceed the values given in *Table 27: General operating conditions*.

$T_{Jmax}$, in degrees Celsius, may be calculated using the following equation:

$$T_{Jmax} = T_{Amax} + (P_{Dmax} \times \Theta_{JA})$$

Where:

- $T_{Amax}$ is the maximum ambient temperature in °C
- $\Theta_{JA}$ is the package junction-to-ambient thermal resistance in ° C/W
- $P_{Dmax}$ is the sum of $P_{INTmax}$ and $P_{I/Omax}$ ($P_{Dmax} = P_{INTmax} + P_{I/Omax}$)
- $P_{INTmax}$ is the product of $I_{DD}$ and $V_{DD}$, expressed in Watts. This is the maximum chip internal power.
- $P_{I/Omax}$ represents the maximum power dissipation on output pins
  Where:
  $P_{I/Omax} = \Sigma (V_{OL}*I_{OL}) + \Sigma((V_{DD}-V_{OH})*I_{OH})$,
  taking into account the actual $V_{OL}/I_{OL}$ and $V_{OH}/I_{OH}$ of the I/Os at low and high level in the application.

**Table 65. Thermal characteristics(1)**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $\Theta_{JA}$ | Thermal resistance junction-ambient TSSOP20 - 4 x 4 mm | 110 | °C/W |
| | Thermal resistance junction-ambient LQFP 32 - 7 x 7 mm | 60 | |
| | Thermal resistance junction-ambient VFQFPN32 - 5 x 5 mm | TBD | |

1. Thermal resistances are based on JEDEC JESD51-2 with 4-layer PCB in a natural convection environment.

### 11.4.1 Reference document

JESD51-2 integrated circuits thermal test method environment conditions - natural convection (still air). Available from www.jedec.org.

### 11.4.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the order code (see *Section 12: Ordering information*).

The following example shows how to calculate the temperature range needed for a given application.

Assuming the following application conditions:

Maximum ambient temperature $T_{Amax}$= 75 °C (measured according to JESD51-2), $I_{DDmax}$ = 8 mA, $V_{DD}$ = 5 V

Maximum 20 I/Os used at the same time in output at low level with:
$I_{OL}$ = 8 mA, $V_{OL}$= 0.4 V

$P_{INTmax}$ = 8 mA x 5 V= 400 mW

$P_{IOmax}$ = 20 x 8 mA x 0.4 V = 64 mW

This gives: $P_{INTmax}$ = 400 mW and $P_{IOmax}$ 64 mW:

$P_{Dmax}$ = 400 mW + 64 mW

Thus: $P_{Dmax}$ = 464 mW.

Using the values obtained in *Table 65: Thermal characteristics on page 103* $T_{Jmax}$ is calculated as follows:

For LQFP32 60 °C/W

$T_{Jmax}$ = 75 °C + (60 °C/W x464 mW) = 75 °C + 27.8 °C = 102.8 °C

This is within the range of the suffix C version parts (-40 < $T_J$ < 125 °C).

Parts must be ordered at least with the temperature range suffix C.

# 12 Ordering information

**Table 66. STM8AF6213/13A/23/23A/26 ordering information scheme(1)**

| Example | STM8A | F | 62 | 2 | 3 | I | P | C | A | U |
|---|---|---|---|---|---|---|---|---|---|---|

**Product Class(2)**

8-bit automotive microcontroller

**Program memory type**

F = Flash + EEPROM

**Device family**

62 = LIN only

**Program memory size**

1 = 4 Kbyte
2 = 8 Kbyte

**Pin count**

3 = 20 pins
6 = 32 pins

**HSI accuracy**

Blank = ± 5%
I = ± 3%

**Package type**

T = LQFP
P = TSSOP
U = VFQFPN

**Temperature range**

A = -40 to 85 °C
C = -40 to 125 °C
D = -40 to 150 °C

**Number of ADC analog inputs**

Blank = 5 analog inputs
A = 7 analog inputs

**Packing**

Y = Tray
U = Tube
X = Tape and reel compliant with EIA 481-C

1. For a list of available options (e.g. memory size, package) and orderable part numbers or for further information on any aspect of this device, please go to *www.st.com* or contact the nearest ST Sales Office.
2. Qualified and characterized according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 and Q002 or equivalent.

# 13 STM8 development tools

Development tools for the STM8 microcontrollers include the full-featured STice emulation system supported by a complete software tool package including C compiler, assembler and integrated development environment with high-level language debugger. In addition, the STM8 is to be supported by a complete range of tools including starter kits, evaluation boards and a low-cost in-circuit debugger/programmer.

## 13.1 Emulation and in-circuit debugging tools

The STice emulation system offers a complete range of emulation and in-circuit debugging features on a platform that is designed for versatility and cost-effectiveness. In addition, the STM8 application development is supported by a low-cost in-circuit debugger/programmer.

The STice is the fourth generation of full-featured emulators from STMicroelectronics. It offers new advanced debugging capabilities including coverage to help detect and eliminate bottlenecks in application execution and dead code when fine tuning an application.

In addition, STice offers in-circuit debugging and programming of STM8A microcontrollers via the STM8 single wire interface module (SWIM), which allows non-intrusive debugging of an application while it runs on the target microcontroller.

For improved cost effectiveness, STice is based on a modular design that allows you to order exactly what you need to meet your development requirements and to adapt your emulation system to support existing and future ST microcontrollers.

### 13.1.1 STice key features

- Occurrence and time profiling and code coverage analysis (new features)
- Advanced breakpoints with up to 4 levels of conditions
- Data breakpoints
- Program and data trace recording up to 128 KB records
- Read/write on-the-fly of memory during emulation
- In-circuit debugging/programming via SWIM protocol
- 8-bit probe analyzer
- 1 input and 2 output triggers
- Power supply follower managing application voltages between 1.62 to 5.5 V
- Modularity that allows you to specify the components you need to meet your development requirements and adapt to future requirements.
- Supported by free software tools that include integrated development environment (IDE), programming software interface and assembler for STM8.

## 13.2 Software tools

STM8 development tools are supported by a complete, free software package from STMicroelectronics that includes ST visual develop (STVD) IDE and the ST visual programmer (STVP) software interface. STVD provides seamless integration of the Cosmic and Raisonance C compilers for STM8.

### 13.2.1 STM8 toolset

The STM8 toolset with STVD integrated development environment and STVP programming software is available for free download at www.st.com. This package includes:

#### ST visual develop

Full-featured integrated development environment from STMicroelectronics, featuring:

- Seamless integration of C and ASM toolsets
- Full-featured debugger
- Project management
- Syntax highlighting editor
- Integrated programming interface
- Support of advanced emulation features for STice such as code profiling and coverage

#### ST visual programmer (STVP)

Easy-to-use, unlimited graphical interface allowing read, write and verify of your STM8 microcontroller Flash program memory, data EEPROM and option bytes. STVP also offers project mode for saving programming configurations and automating programming sequences.

### 13.2.2 C and assembly toolchains

Control of C and assembly toolchains is seamlessly integrated into the STVD integrated development environment, making it possible to configure and control the building of the application directly from an easy-to-use graphical interface.

Available toolchains include:

#### Cosmic C compiler for STM8

All compilers are available in free version with a limited code size depending on the compiler. For more information, refer to www.cosmic-software.com, www.raisonance.com, and www.iar.com.

#### STM8 assembler linker

Free assembly toolchain included in the STM8 toolset, which allows the users to assemble and link your application source code.

## 13.3 Programming tools

During the development cycle, STice provides in-circuit programming of the STM8 Flash microcontroller on the user application board via the SWIM protocol. Additional tools include a low-cost in-circuit programmer as well as ST socket boards, which provide dedicated programming platforms with sockets for programming the STM8.

For production environments, programmers will include a complete range of gang and automated programming solutions from third-party tool developers already supplying programmers for the STM8 family.

# 14 Revision history

**Table 67. Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 11-Oct-2013 | 1 | Initial release. |
| 16-Dec-2013 | 2 | Changed the document status to Production data.<br>Updated *Figure: STM8AF6223PxAx TSSOP20 pinout* to add SPI_NSS to PD4, TLI to PD2, and change remap function on PB5 from TIM5_BKIn to TIM1_BKIN.<br>Updated *Table: STM8AF6223PxAx TSSOP20 pin description* to add SPI_NSS to PD4 and TLI to PD2.<br>Updated *Table: STM8AF6223 TSSOP20 pin description* and *Table: LQFP32 pin descriptio*n.<br>Updated AFR2 definition in *Table: STM8AF6223PxAx alternate function remapping bits [7:2] for 20-pin packages*.<br>Removed the remapping option on PA3 for AFR[1:0]=10 in *Table: STM8AF6223PxAx alternate function remapping bits [1:0] for 20-pin packages*.<br>Added note and removed remapping option on PA3 for AFR[1:0]=11 in *Table: STM8AF6223 alternate function remapping bits [1:0] for 20-pin packages*. Updated AFR2 definition in STM8AF6223 alternate function remapping bits [7:2] for 20-pin packages.<br>Added the note below *Table: STM8AF6226T alternate function remapping bits [1:0] for 32-pin packages*.<br>Updated *Table: I2C characteristics* to modify $t_{h(SDA)}$ and add $t_{SP}$.<br>Updated *Section: C assembly toolchains*. |
| 03-Apr-2014 | 3 | Replaced STM8AF6226T by STM8AF6226 part number. Added STM8AF6223A part number to cover STM8AF6223PxAx order codes.<br>Removed LINUART alternate function for PA3 in *Table: STM8AF6223PxAx TSSOP20 pin description*.<br>Removed note 3 for $I_{DD(AH)}$ in *Table: Total current consumption in active halt mode at VDD = 5 V*.<br>Updated the remapping option on PA3 for AFR[1:0]=11 in *Table: STM8AF6223 alternate function remapping bits [1:0] for 20-pin packages*.<br>Updated notes related to $t_{RET}$ minimum value in *Table: Data memory*.<br>Updated *Table: ESD absolute maximum ratings*.<br>Added notes related to protrusions and gate burrs for D and E1 dimensions in *Table: 20-pin, 4.40 mm body, 0.65 mm pitch mechanical data*. |

**Table 67. Document revision history (continued)**

| Date | Revision | Changes |
|---|---|---|
| 10-Jul-2014 | 4 | Extended the applicability to STM8AF6213 devices.<br>Updated the program memory feature, the power management, and the clock management features on the cover page.<br>Added the table in *Section: Memory map*.<br>Updated the *Figure: $f_{CPUmax}$ versus $V_{DD}$* in *Section: Operating conditions.*<br>Updated *Section: Ordering information*. |
| 26-Jun-2015 | 5 | Added:<br>– the footnote about the inrush current below *Table 28: Operating conditions at power-up/power-down*,<br>– *Figure 47: LQFP32 marking example (package top view)*,<br>– *Figure 44: TSSOP20 marking example (package top view)*.<br>Updated<br>– LIN standard version,<br>– the register label for LINUART block in *Table 11: General hardware register map*,<br>– the power dissipation in *Table 27: General operating conditions*,<br>– *Table 42: HSI oscillator characteristics* for HSI oscillator accuracy,<br>– the standard for EMI in *Electromagnetic interference (EMI)*,<br>– *Figure 48: STM8AF6213/23/23A/26 ordering information scheme*(1) (2) to add HSI accuracy.<br>Moved *Section 11.4: Thermal characteristics* to *Section 11: Package information*. |

**Table 67. Document revision history (continued)**

| Date | Revision | Changes |
|---|---|---|
| 28-Mar-2017 | 6 | Updated *Table 6: STM8AF6213/STM8AF6223 TSSOP20 pin description*<br>Added VFQFPN32 (5x5 mm) package information updating:<br>– *Section : Features* on the cover page: added VFQFPN32 (5x5 mm) figure<br>– Added *Section 11.2: LQFP32 package information*:<br>– Updated *Table 27: General operating conditions*<br>– Updated *Table 65: Thermal characteristics*<br>– Updated *Section 5.2: LQFP32/VFQPN32 pinout and pin description*<br>– Updated *Section 12: Ordering information*<br>Additional updates (not related to VFQFPN32):<br>– Table footnotes on *Section 10: Electrical characteristics*<br>– Updated *Section : Device marking for LQFP32 on page 98*, *Section : Device marking for TSSOP20 on page 95* and *Section : Device marking for VFQFPN32 on page 102*<br>– *Section 10.2: Absolute maximum ratings* |
| 07-Dec-2017 | 7 | Added:<br>– STMAF6213A RPN to the whole document<br>– Footnote (2) on *Table 66: STM8AF6213/13A/23/23A/26 ordering information scheme*<br>Updated:<br>– All document to add STMAF6213A reference where applicable<br>– *Table 1: STM8AF6213/13A/23/23A/26 features*<br>– Titles of sections *Device marking for LQFP32*, *Device marking for TSSOP20* and *Device marking for VFQFPN32* |
| 19-Mar-2019 | 8 | Added *Section 9: Unique ID*<br>Updated order of package figures on cover page and order of subsections on *Section 11: Package information* |
| 01-Apr-2020 | 9 | Updated: *Table 42: HSI oscillator characteristics* |

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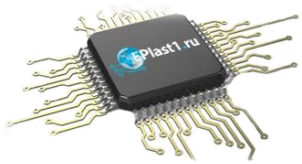


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