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# LC74900

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CMOS IC

## Silicon gate LCD PROCESSOR LSI for small size display

### Overview

LC74900 is a highly integrated multi-purpose LCD Panel (up to WVGA) controller processing analog and digital video signal.

It contains A/D converter, video decoder, De-interlacer/Scaler, and picture improvement.

### Features

(1) Video Input/Output

- Analog input: 4ch CVBS (NTSC, PAL, and SECAM) with 1ch 10bit A/D converter
- Digital input: 24bit RGB and YCbCr, 16bit YCbCr (4:2:2), and 8bit YC (BT.656)
- Digital output: 8bit video decoder output (BT.656)

(2) YC separation video decoder

- Adaptive 3line comb filter, automatic gain and chrominance control

(3) De-interlacer and Scaler

- Horizontal and vertical programmable scaler separately, and supports panels up to WVGA resolutions

(4) Picture Improvements

- CDEX (Color Depth Expander): high quality expansion for low-resolution graphics
- Dynamic gamma correction: picture adapted automatic luminance control
- Sharpness control, LTI and CTI: peaking enhancement without glares
- Color exciter: 6 phases RGBYMC gain control separately

(5) Panel interface

- 24bit RGB output and 18bit RGB output with dithering process
- Pulse Width Modulation for automatic LED backlight control
- Timing controller for LCD driver with horizontal or vertical reversing signals
- Pin swapping : replace output pin assignment of the RGB channel or bit

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## (6) On Screen Display

- Built-in OSD controller with integrated font ROM, which contains 501 fonts, and font RAM, which contains 8 fonts
- Character Numbers displayed on the screen: 24 characters by 8 rows, 24 characters by 10 rows, or 32 characters by 8 rows
- Character Size: 16 pixels wide by 20 pixels high
- Character Colors: 8 font colors for each character, 8 back colors for each character, and 8 font border colors for each row
- Inverting font colors and back colors each character, Blinking fonts each character, and Fringing each row
- Pin assignment for an optional external OSD controller: 24bit, 18bit, 12bit, and 6bit RGB

## (7) EEPROM booting

- Quick boot from an external EEPROM in power on sequence before starting a system controller
- Waiting timer between data transfers
- Verifying boot datas
- EEPROM Size: Up to 512K bits with I<sup>2</sup>C or SPI interface

## (8) Parallel data outputs, panel interface and video decoder output

- Reentering video decoder outputs, which are processed by an external graphic engine as digital inputs

## (9) System Controller Interface

- SPI (Max 1Mbit/s) or I<sup>2</sup>C bus (100Kbit/s or 400Kbit/s)

## LSI Specification

- Supply voltage: 1.5V (core), 3.3V (IO)
- Maximum operation frequency: 60MHz (video processing)
- Package: 120pin TQFP

## Applications

- For mediam or small size LCD Panel
- Automobile use: car TV, portable navigation, etc.
- Home use: Photo Frame, Portable DVD, Door Phone, etc.

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## Specifications

**Absolute Maximum Ratings** at  $T_a = 25^\circ\text{C}$ ,  $DV_{SS} = 0\text{V}$ ,  $ADC0AV_{SS} = 0\text{V}$ ,  $ADC1AV_{SS} = 0\text{V}$ ,  $PLLAV_{SS} = 0\text{V}$ ,  $XV_{SS} = 0\text{V}$

| Parameter                       | Symbol   | Conditions  | Ratings                   | unit             |
|---------------------------------|--|---|---------------------------|------------------|
| Maximum supply voltage (I/O)    | $DV_{DD33}$<br>$XV_{DD33}$<br>$DV_{DD3318}$          |   | -0.3 to +3.96             | V                |
| Maximum supply voltage (Analog) | $ADC0AV_{DD33}$<br>$ADC1AV_{DD33}$<br>$PLLAV_{DD33}$ |   | -0.3 to +3.96             | V                |
| Maximum supply voltage (Core)   | $DV_{DD15}$  |   | -0.3 to +1.8              | V                |
| Digital input voltage           | $V_I$  |   | -0.3 to $DV_{DD33}+0.3$   | V                |
|                                 | $V_I$ (5V Tolerant)                                  |   | -0.3 to $DV_{DD3318}+0.3$ |                  |
| Digital output voltage          | $V_O$  |   | -0.3 to $DV_{DD33}+0.3$   | V                |
|                                 |  |   | -0.3 to $DV_{DD3318}+0.3$ |                  |
| Maximum allowable loss          | $P_d \text{ max}$                                    | $T_a = 85^\circ\text{C}$ , With evaluation board* | 0.7                       | W                |
| Operating temperature           | $T_{opr}$  |   | -40 to +85                | $^\circ\text{C}$ |
| Storage temperature             | $T_{stg}$  |   | -55 to +125               | $^\circ\text{C}$ |

\*: Board size: 150mm × 150mm × 1.6mm, FR-4, 6layers

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

**Allowable Operation Ranges** at  $T_a = -40$  to  $+85^\circ\text{C}$ ,  $DV_{SS} = 0\text{V}$ ,  $ADC0AV_{SS} = 0\text{V}$ ,  $ADC1AV_{SS} = 0\text{V}$ ,  $PLLAV_{SS} = 0\text{V}$ ,  $XV_{SS} = 0\text{V}$

| Parameter                         | Symbol   | Conditions | min  | typ | max                          | unit |
|-----------------------------------|--|------------|------|-----|------------------------------|------|
| Supply voltage (I/O)              | $DV_{DD33}$<br>$XV_{DD33}$                           |            | 3.15 | 3.3 | 3.45                         | V    |
|                                   | $DV_{DD3318}$  |            | 3.15 | 3.3 | 3.45                         | V    |
|                                   |  |            |      | 1.7 | 1.8                          | 1.9  |
| Supply voltage (Analog)           | $ADC0AV_{DD33}$<br>$ADC1AV_{DD33}$<br>$PLLAV_{DD33}$ |            | 3.15 | 3.3 | 3.45                         | V    |
| Supply voltage (Core)             | $DV_{DD15}$  |            | 1.4  | 1.5 | 1.6                          | V    |
| Input voltage range               | $V_{IN}$   |            | 0    |     | $DV_{DD33}$<br>$DV_{DD3318}$ | V    |
| Input voltage range (5V Tolerant) | $V_{IN5}$  |            | 0    |     | 5.5                          | V    |

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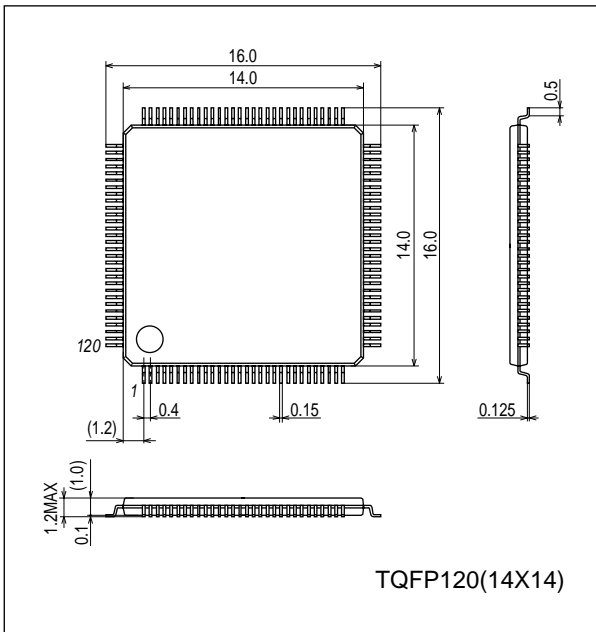
**DC Characteristics** at  $T_a = -40$  to  $+85^\circ\text{C}$ ,  $DV_{SS} = 0\text{V}$ ,  $ADC0AV_{SS} = 0\text{V}$ ,  $ADC1AV_{SS} = 0\text{V}$ ,  $PLLAV_{SS} = 0\text{V}$ ,  $XV_{SS} = 0\text{V}$ ,  $DV_{DD33} = 3.15\text{V}$  to  $3.45\text{V}$ ,  $DV_{DD3318} = 3.15\text{V}$  to  $3.45\text{V}$  or  $1.7\text{V}$  to  $1.9\text{V}$ ,  $DV_{DD15} = 1.42\text{V}$  to  $1.58\text{V}$ ,  $XV_{DD33} = 3.15\text{V}$  to  $3.45\text{V}$ ,  $ADC0AV_{DD} = 3.15\text{V}$  to  $3.45\text{V}$ ,  $ADC1AV_{DD} = 3.15\text{V}$  to  $3.45\text{V}$ ,  $PLLAV_{DD} = 3.15\text{V}$  to  $3.45\text{V}$

| Parameter                 | Symbol     | Conditions   | min                                | typ | max                                | unit          |
|---------------------------|------------|--|------------------------------------|-----|------------------------------------|---------------|
| Input high-level voltage  | $V_{IH}$   | CMOS level inputs  | $0.7DV_{DD33}$<br>$0.7DV_{DD3318}$ |     |                                    | V             |
|                           |            | CMOS level Schmitt inputs  | $0.7DV_{DD33}$                     |     |                                    | V             |
| Input low-level voltage   | $V_{IL}$   | CMOS level inputs  | 0                                  |     | $0.3DV_{DD33}$<br>$0.3DV_{DD3318}$ | V             |
|                           |            | CMOS level Schmitt inputs  | 0                                  |     | $0.3DV_{DD33}$                     | V             |
| Input high-level current  | $I_{IH}$   | $V_I = DV_{DD33}$  |                                    |     |                                    | $\mu\text{A}$ |
|                           |            | $V_I = DV_{DD3318}$  |                                    |     |                                    | $\mu\text{A}$ |
| Input low-level current   | $I_{IL}$   | $V_I = DV_{SS}$  |                                    |     |                                    | $\mu\text{A}$ |
| Output high-level voltage | $V_{OH}$   | Type B: $I_{OH} = -4\text{mA}$<br>Type G: $I_{OH} = -6\text{mA}$   | $DV_{DD33}-0.6$                    |     |                                    | V             |
|                           |            | $DV_{DD3318} = 3.15\text{V}$ to $3.45\text{V}$<br>Type J: $I_{OH} = -4\text{mA}$<br>Type K: $I_{OH} = -6\text{mA}$   | $DV_{DD3318}-0.6$                  |     |                                    | V             |
|                           |            | $DV_{DD3318} = 1.7\text{V}$ to $1.9\text{V}$<br>Type J: $I_{OH} = -3\text{mA}$<br>Type K: $I_{OH} = -5\text{mA}$   | $DV_{DD3318}-0.4$                  |     |                                    | V             |
| Output low-level voltage  | $V_{OL}$   | CMOS   |                                    |     | 0.4                                | V             |
| Output leakage current    | $I_{OZ}$   | When in high-impedance output mode   | -10                                |     | 10                                 | $\mu\text{A}$ |
| Operating current drain   | $I_{DDOP}$ | Output open, tck = 9MHz, 10steps<br>$T_a = 25^\circ\text{C}$ , $DV_{DD33} = 3.3\text{V}$ ,<br>$DV_{DD3318} = 3.3\text{V}$ , $XV_{DD} = 3.3\text{V}$ ,<br>$DV_{DD15} = 1.5\text{V}$ , $ADC0AV_{DD} = 3.3\text{V}$ ,<br>$ADC1AV_{DD} = 3.3\text{V}$ , $PLLAV_{DD} = 3.3\text{V}$         |                                    | 95  |                                    | mA            |
|                           |            | Output open, tck = 33MHz, 10steps<br>$T_a = 25^\circ\text{C}$ , $DV_{DD33} = 3.3\text{V}$ ,<br>$DV_{DD3318} = 3.3\text{V}$ , $XV_{DD} = 3.3\text{V}$ ,<br>$DV_{DD15} = 1.5\text{V}$ , $ADC0AV_{DD} = 3.3\text{V}$ ,<br>$ADC1AV_{DD} = 3.3\text{V}$ , $PLLAV_{DD} = 3.3\text{V}$        |                                    | 139 |                                    | mA            |
| Static current drain      | $I_{DDST}$ | Output open, tck: stop<br>$V_I = DV_{SS}$ , $T_a = 25^\circ\text{C}$ , $DV_{DD33} = 3.3\text{V}$ ,<br>$DV_{DD3318} = 1.8\text{V}$ , $XV_{DD} = 3.3\text{V}$ ,<br>$DV_{DD15} = 1.5\text{V}$ , $ADC0AV_{DD} = 3.3\text{V}$ ,<br>$ADC1AV_{DD} = 3.3\text{V}$ , $PLLAV_{DD} = 3.3\text{V}$ |                                    | 34  |                                    | $\mu\text{A}$ |

Package Dimensions

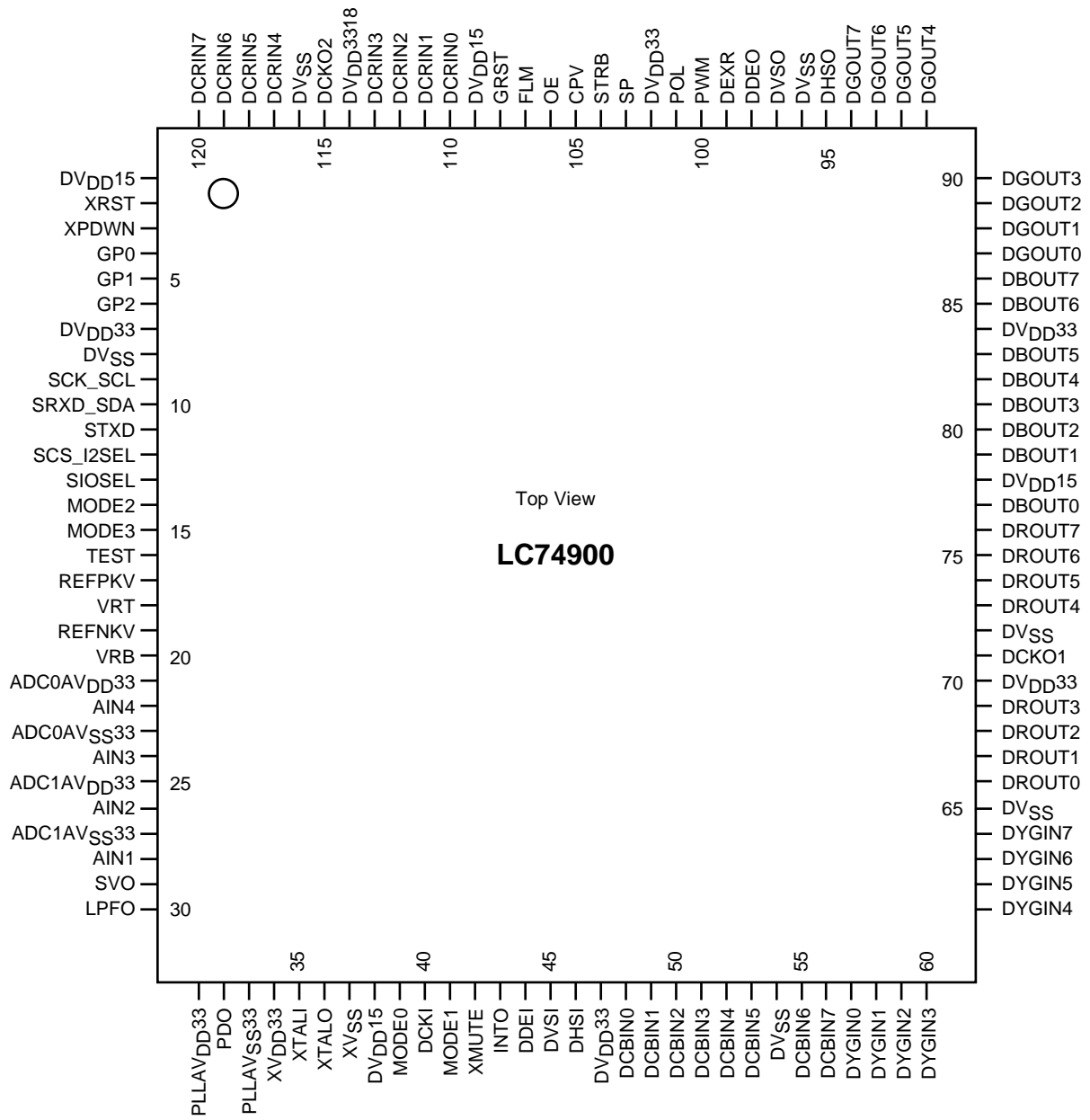
unit : mm (typ)

3257A



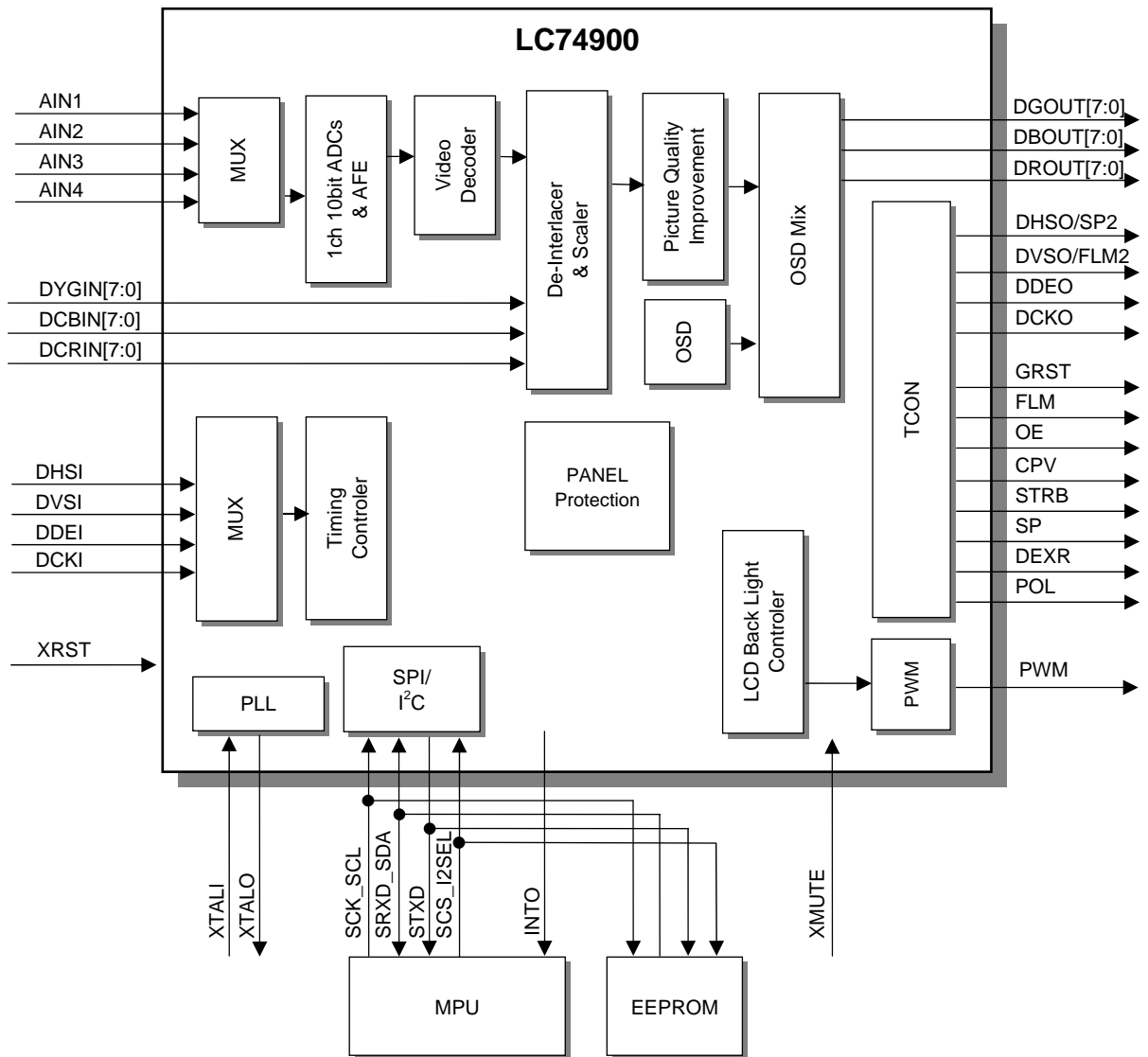
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## Pin Assignment



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## Block Diagram



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## Pin Functions

| Pin No. | Pin symbol              | I/O format |        | Connected to   |         | Digital IO power supply | Remarks   |
|---------|-------------------------|------------|--------|----------------|---------|-------------------------|---|
|         |                         | I/O        | Format |                |         |                         |   |
| 1       | DV <sub>DD</sub> 15     | P          | -      | Core voltage   | Digital |                         | Power supply for core (1.5V)  |
| 2       | XRST                    | I          | A      | CMOS           | Digital | DV <sub>DD</sub> 33     | Reset pin (active at a low voltage level)   |
| 3       | XPDOWN                  | I          | A      | CMOS           | Digital | DV <sub>DD</sub> 33     | Fixed at a high voltage level   |
| 4       | GP0                     | I/O        | B      | CMOS           | Digital | DV <sub>DD</sub> 33     | Input: Digital input/OSD enable (pull down if not used)<br>Output: Global port/Video decoder Vsync  |
| 5       | GP1                     | I/O        | B      | CMOS           | Digital | DV <sub>DD</sub> 33     | Input: Digital input/OSD halftone (pull down if not used)<br>Output: Global Port/Video DecoderHsync |
| 6       | GP2                     | I/O        | B      | CMOS           | Digital | DV <sub>DD</sub> 33     | Global port output  |
| 7       | DV <sub>DD</sub> 33     | P          | -      | IO voltage     | Digital |                         | Power supply for IO (3.3V)  |
| 8       | DV <sub>SS</sub>        | P          | -      | GND            | Digital |                         | GND for digital   |
| 9       | SCK_SCL                 | I/O        | C      | CMOS           | Digital | DV <sub>DD</sub> 33     | I <sup>2</sup> C: I <sup>2</sup> C Clock inout, SPI: Clock input                                    |
| 10      | SRXD_SDA                | I/O        | C      | CMOS           | Digital | DV <sub>DD</sub> 33     | I <sup>2</sup> C: data inout, SPI: data input   |
| 11      | STXD                    | I/O        | B      | CMOS           | Digital | DV <sub>DD</sub> 33     | SPI: data output  |
| 12      | SCS_I2SEL               | I          | A      | CMOS           | Digital | DV <sub>DD</sub> 33     | I <sup>2</sup> C: Select I <sup>2</sup> C slave address, SPI: Chip select                           |
| 13      | SIOSEL                  | I          | D      | CMOS           | Digital | DV <sub>DD</sub> 33     | Select CPU I/F, "L": I <sup>2</sup> C, "H": SPI   |
| 14      | MODE2                   | I          | D      | CMOS           | Digital | DV <sub>DD</sub> 33     | Operation mode control  |
| 15      | MODE3                   | I          | D      | CMOS           | Digital | DV <sub>DD</sub> 33     | Operation mode control  |
| 16      | TEST                    | I          | D      | CMOS           | Digital | DV <sub>DD</sub> 33     | For production test (Fixed at a low voltage level)  |
| 17      | REFPKV                  | I          | E      |                | Analog  |                         | Top reference level Buffer-AMP input for ADC  |
| 18      | VRT                     | I          | E      |                | Analog  |                         | Top reference level for ADC   |
| 19      | REFNKV                  | I          | E      |                | Analog  |                         | Bottom reference level Buffer-AMP input for ADC   |
| 20      | VRB                     | I          | E      |                | Analog  |                         | Bottom reference level for ADC  |
| 21      | ADC0AV <sub>DD</sub> 33 | P          | -      | Analog voltage | Analog  |                         | Power supply for ADC (3.3V)   |
| 22      | AIN4                    | I          | E      |                | Analog  |                         | CVBS input 4  |
| 23      | ADC0AV <sub>SS</sub> 33 | P          | -      | GND            | Analog  |                         | GND for ADC   |
| 24      | AIN3                    | I          | E      |                | Analog  |                         | CVBS input 3  |
| 25      | ADC1AV <sub>DD</sub> 33 | P          | -      | Analog voltage | Analog  |                         | Power supply for ADC (3.3V)   |
| 26      | AIN2                    | I          | E      |                | Analog  |                         | CVBS input 2  |
| 27      | ADC1AV <sub>SS</sub> 33 | P          | -      | GND            | Analog  |                         | GND for ADC   |
| 28      | AIN1                    | I          | E      |                | Analog  |                         | CVBS input 1  |
| 29      | SVO                     | O          | E      |                | Analog  |                         | AFE output  |
| 30      | LPFO                    | O          | E      |                | Analog  |                         | External AGC control level  |
| 31      | PLLAV <sub>DD</sub> 33  | P          | -      | Analog voltage | Analog  |                         | Power supply for PLL (3.3V)   |
| 32      | PDO                     | O          | -      |                | Analog  |                         | Test port for PLL (Open)  |
| 33      | PLLAV <sub>SS</sub> 33  | P          | -      | GND            | Analog  |                         | GND for PLL   |
| 34      | XV <sub>DD</sub> 33     | P          | -      | IO voltage     | Digital |                         | Power supply for 27MHz X'tal (3.3V)   |
| 35      | XTALI                   | I          | F      | CMOS           | Digital | XV <sub>DD</sub> 33     | 27MHz X'tal input   |
| 36      | XTALO                   | O          | F      | CMOS           | Digital | XV <sub>DD</sub> 33     | 27MHz X'tal output  |
| 37      | XV <sub>SS</sub>        | P          | -      | GND            | Digital |                         | GND for 27MHz X'tal   |
| 38      | DV <sub>DD</sub> 15     | P          | -      | Core voltage   | Digital |                         | Power supply for core (1.5V)  |
| 39      | MODE0                   | I          | D      | CMOS           | Digital | DV <sub>DD</sub> 33     | Operation mode control  |
| 40      | DCKI                    | I          | D      | CMOS           | Digital | DV <sub>DD</sub> 33     | Digital video clock   |
| 41      | MODE1                   | I          | D      | CMOS           | Digital | DV <sub>DD</sub> 33     | Operation mode control  |
| 42      | XMUTE                   | I          | A      | CMOS           | Digital | DV <sub>DD</sub> 33     | Mute control (active at a low voltage level)  |
| 43      | INTO                    | I/O        | B      | CMOS           | Digital | DV <sub>DD</sub> 33     | Interrupt output  |
| 44      | DDEI                    | I          | D      | CMOS           | Digital | DV <sub>DD</sub> 33     | Digital video enable/OSD enable   |
| 45      | DVSI                    | I          | D      | CMOS           | Digital | DV <sub>DD</sub> 33     | Digital video Vsync/OSD half tone   |
| 46      | DHSI                    | I          | D      | CMOS           | Digital | DV <sub>DD</sub> 33     | Digital video Hsync   |
| 47      | DV <sub>DD</sub> 33     | P          | -      | IO voltage     | Digital |                         | Power supply for IO (3.3V)  |
| 48      | DCBIN0                  | I          | D      | CMOS           | Digital | DV <sub>DD</sub> 33     | Digital video input/OSD input (pull down if not used)   |
| 49      | DCBIN1                  | I          | D      | CMOS           | Digital | DV <sub>DD</sub> 33     | Digital video input/OSD input (pull down if not used)   |
| 50      | DCBIN2                  | I          | D      | CMOS           | Digital | DV <sub>DD</sub> 33     | Digital video input/OSD input (pull down if not used)   |

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| Pin No. | Pin symbol         | I/O format |        | Connected to |         | Digital IO power supply | Remarks  |
|---------|--------------------|------------|--------|--------------|---------|-------------------------|--|
|         |                    | I/O        | Format |              |         |                         |  |
| 51      | DCBIN3             | I          | D      | CMOS         | Digital | DV <sub>DD33</sub>      | Digital video input/OSD input (pull down if not used)  |
| 52      | DCBIN4             | I          | D      | CMOS         | Digital | DV <sub>DD33</sub>      | Digital video input/OSD input (pull down if not used)  |
| 53      | DCBIN5             | I          | D      | CMOS         | Digital | DV <sub>DD33</sub>      | Digital video input/OSD input (pull down if not used)  |
| 54      | DV <sub>SS</sub>   | P          |        | GND          | Digital |                         | GND for digital  |
| 55      | DCBIN6             | I          | D      | CMOS         | Digital | DV <sub>DD33</sub>      | Digital video input/OSD input (pull down if not used)  |
| 56      | DCBIN7             | I          | D      | CMOS         | Digital | DV <sub>DD33</sub>      | Digital video input/OSD input (pull down if not used)  |
| 57      | DYGIN0             | I          | D      | CMOS         | Digital | DV <sub>DD33</sub>      | Digital video input/OSD input (pull down if not used)  |
| 58      | DYGIN1             | I          | D      | CMOS         | Digital | DV <sub>DD33</sub>      | Digital video input/OSD input (pull down if not used)  |
| 59      | DYGIN2             | I          | D      | CMOS         | Digital | DV <sub>DD33</sub>      | Digital video input/OSD input (pull down if not used)  |
| 60      | DYGIN3             | I          | D      | CMOS         | Digital | DV <sub>DD33</sub>      | Digital video input/OSD input (pull down if not used)  |
| 61      | DYGIN4             | I          | D      | CMOS         | Digital | DV <sub>DD33</sub>      | Digital video input/OSD input (pull down if not used)  |
| 62      | DYGIN5             | I          | D      | CMOS         | Digital | DV <sub>DD33</sub>      | Digital video input/OSD input (pull down if not used))   |
| 63      | DYGIN6             | I          | D      | CMOS         | Digital | DV <sub>DD33</sub>      | Digital video input/OSD input (pull down if not used)  |
| 64      | DYGIN7             | I          | D      | CMOS         | Digital | DV <sub>DD33</sub>      | Digital video input/OSD input (pull down if not used)  |
| 65      | DV <sub>SS</sub>   | P          |        | GND          | Digital |                         | GND for digital  |
| 66      | DROUT0             | I/O        | B      | CMOS         | Digital | DV <sub>DD33</sub>      | Panel R output (LSB) (input port in test mode)   |
| 67      | DROUT1             | I/O        | B      | CMOS         | Digital | DV <sub>DD33</sub>      | Panel R output (input port in test mode)   |
| 68      | DROUT2             | I/O        | B      | CMOS         | Digital | DV <sub>DD33</sub>      | Panel R output (input port in test mode)   |
| 69      | DROUT3             | I/O        | B      | CMOS         | Digital | DV <sub>DD33</sub>      | Panel R output (input port in test mode)   |
| 70      | DV <sub>DD33</sub> | P          |        | IO voltage   | Digital |                         | Power supply for IO (3.3V)   |
| 71      | DCKO1              | O          | G      | CMOS         | Digital | DV <sub>DD33</sub>      | Panel clock output   |
| 72      | DV <sub>SS</sub>   | P          |        | GND          | Digital |                         | GND for digital  |
| 73      | DROUT4             | I/O        | B      | CMOS         | Digital | DV <sub>DD33</sub>      | Panel R output (input port in test mode)   |
| 74      | DROUT5             | I/O        | B      | CMOS         | Digital | DV <sub>DD33</sub>      | Panel R output (input port in test mode)   |
| 75      | DROUT6             | I/O        | B      | CMOS         | Digital | DV <sub>DD33</sub>      | Panel R output (input port in test mode)   |
| 76      | DROUT7             | I/O        | B      | CMOS         | Digital | DV <sub>DD33</sub>      | Panel R output (MSB) (input port in test mode)   |
| 77      | DBOUT0             | I/O        | B      | CMOS         | Digital | DV <sub>DD33</sub>      | Panel B output (LSB) (input port in test mode)   |
| 78      | DV <sub>DD15</sub> | P          |        | Core voltage | Digital |                         | Power supply for core (1.5V)   |
| 79      | DBOUT1             | I/O        | B      | CMOS         | Digital | DV <sub>DD33</sub>      | Panel B output (input port in test mode)   |
| 80      | DBOUT2             | I/O        | B      | CMOS         | Digital | DV <sub>DD33</sub>      | Panel B output (input port in test mode)   |
| 81      | DBOUT3             | I/O        | B      | CMOS         | Digital | DV <sub>DD33</sub>      | Panel B output (input port in test mode)   |
| 82      | DBOUT4             | I/O        | B      | CMOS         | Digital | DV <sub>DD33</sub>      | Panel B output (input port in test mode)   |
| 83      | DBOUT5             | I/O        | B      | CMOS         | Digital | DV <sub>DD33</sub>      | Panel B output (input port in test mode)   |
| 84      | DV <sub>DD33</sub> | P          |        | IO voltage   | Digital |                         | Power supply for IO (3.3V)   |
| 85      | DBOUT6             | I/O        | B      | CMOS         | Digital | DV <sub>DD33</sub>      | Panel B output (input port in test mode)   |
| 86      | DBOUT7             | I/O        | B      | CMOS         | Digital | DV <sub>DD33</sub>      | Panel B output (MSB) (input port in test mode)   |
| 87      | DGOUT0             | I/O        | B      | CMOS         | Digital | DV <sub>DD33</sub>      | Panel G output (LSB) (input port in test mode)   |
| 88      | DGOUT1             | I/O        | B      | CMOS         | Digital | DV <sub>DD33</sub>      | Panel G output (input port in test mode)   |
| 89      | DGOUT2             | I/O        | B      | CMOS         | Digital | DV <sub>DD33</sub>      | Panel G output (input port in test mode)   |
| 90      | DGOUT3             | I/O        | B      | CMOS         | Digital | DV <sub>DD33</sub>      | Panel G output (input port in test mode)   |
| 91      | DGOUT4             | I/O        | B      | CMOS         | Digital | DV <sub>DD33</sub>      | Panel G output (input port in test mode)   |
| 92      | DGOUT5             | I/O        | B      | CMOS         | Digital | DV <sub>DD33</sub>      | Panel G output (input port in test mode)   |
| 93      | DGOUT6             | I/O        | B      | CMOS         | Digital | DV <sub>DD33</sub>      | Panel G output (input port in test mode)   |
| 94      | DGOUT7             | I/O        | B      | CMOS         | Digital | DV <sub>DD33</sub>      | Panel G output (MSB) (input port in test mode)   |
| 95      | DHSO               | I/O        | B      | CMOS         | Digital | DV <sub>DD33</sub>      | Panel Hsync/Start pulse for source driver/<br>Video decoder Vsync output (input port in test mode) |
| 96      | DV <sub>SS</sub>   | P          |        | GND          | Digital |                         | GND for digital  |
| 97      | DVSO               | I/O        | B      | CMOS         | Digital | DV <sub>DD33</sub>      | Panel Vsync/Start pulse for gate driver/<br>Video decoder Vsync output (input port in test mode)   |
| 98      | DDEO               | I/O        | B      | CMOS         | Digital | DV <sub>DD33</sub>      | Panel enable output (input port in test mode)  |
| 99      | DEXR               | I/O        | B      | CMOS         | Digital | DV <sub>DD33</sub>      | Invert control signal for DTR/<br>Video decoder output 1[7](BT.656) (input port in test mode)      |

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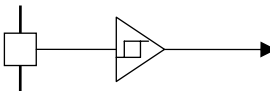
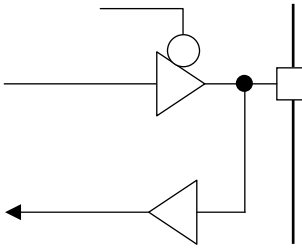
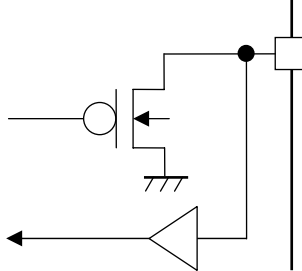
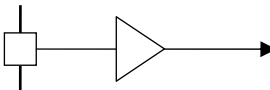
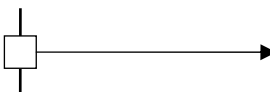
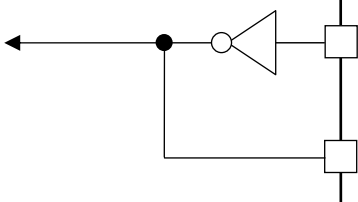
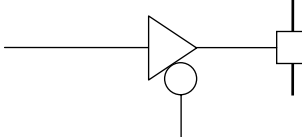
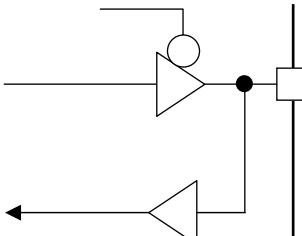
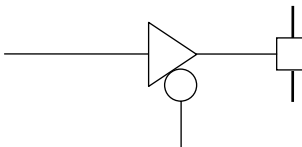
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| Pin No. | Pin symbol            | I/O format |        | Connected to |         | Digital IO power supply | Remarks  |
|---------|-----------------------|------------|--------|--------------|---------|-------------------------|--|
|         |                       | I/O        | Format |              |         |                         |  |
| 100     | PWM                   | I/O        | B      | CMOS         | Digital | DV <sub>DD</sub> 33     | Pulse width modulation (input port in test mode)   |
| 101     | POL                   | I/O        | B      | CMOS         | Digital | DV <sub>DD</sub> 33     | Polarity control for source driver/<br>Video decoder output 1[6] (BT.656) (input port in test mode)        |
| 102     | DV <sub>DD</sub> 33   | P          |        | IO voltage   | Digital |                         | Power supply for IO (3.3V)   |
| 103     | SP                    | I/O        | B      | CMOS         | Digital | DV <sub>DD</sub> 33     | Start pulse for source driver/<br>Video decoder output 1[5] (BT.656) (input port in test mode)             |
| 104     | STRB                  | I/O        | B      | CMOS         | Digital | DV <sub>DD</sub> 33     | Data stroboscope for source driver/<br>Video decoder output 1[4] (BT.656) (input port in test mode)        |
| 105     | CPV                   | I/O        | B      | CMOS         | Digital | DV <sub>DD</sub> 33     | Clock for gate driver/<br>Video decoder output 1[3] (BT.656) (input port in test mode)                     |
| 106     | OE                    | I/O        | B      | CMOS         | Digital | DV <sub>DD</sub> 33     | Output enable for gate driver/<br>Video decoder output 1[2] (BT.656) (input port in test mode)             |
| 107     | FLM                   | I/O        | B      | CMOS         | Digital | DV <sub>DD</sub> 33     | Start pulse for gate driver/<br>Video decoder output 1[1] (BT.656) (input port in test mode)               |
| 108     | GRST                  | I/O        | B      | CMOS         | Digital | DV <sub>DD</sub> 33     | Reset for gate driver/<br>Video decoder output 1[0] (BT.656) (input port in test mode)                     |
| 109     | DV <sub>DD</sub> 15   | P          |        | Core voltage | Digital |                         | Power supply for core (1.5V)   |
| 110     | DCRIN0                | I/O        | H      | CMOS         | Digital | DV <sub>DD</sub> 3318   | Input: Digital video input/OSD input (pull down if not used)<br>Output: Video decoder output 2[0] (BT.656) |
| 111     | DCRIN1                | I/O        | H      | CMOS         | Digital | DV <sub>DD</sub> 3318   | Input: Digital video input/OSD input (pull down if not used)<br>Output: Video decoder output 2[1] (BT.656) |
| 112     | DCRIN2                | I/O        | H      | CMOS         | Digital | DV <sub>DD</sub> 3318   | Input: Digital video input/OSD input (pull down if not used)<br>Output: Video decoder output 2[2] (BT.656) |
| 113     | DCRIN3                | I/O        | H      | CMOS         | Digital | DV <sub>DD</sub> 3318   | Input: Digital video input/OSD input (pull down if not used)<br>Output: Video decoder output 2[3] (BT.656) |
| 114     | DV <sub>DD</sub> 3318 | P          | -      | IO voltage   | Digital |                         | Power supply for IO (3.3V/1.8V)  |
| 115     | DCKO2                 | O          | J      | CMOS         | Digital | DV <sub>DD</sub> 3318   | Video decoder clock output   |
| 116     | DV <sub>SS</sub>      | P          | -      | GND          | Digital |                         | GND for digital  |
| 117     | DCRIN4                | I/O        | H      | CMOS         | Digital | DV <sub>DD</sub> 3318   | Input: Digital video input/OSD input (pull down if not used)<br>Output: Video decoder output 2[4] (BT.656) |
| 118     | DCRIN5                | I/O        | H      | CMOS         | Digital | DV <sub>DD</sub> 3318   | Input: Digital video input/OSD input (pull down if not used)<br>Output: Video decoder output 2[5] (BT.656) |
| 119     | DCRIN6                | I/O        | H      | CMOS         | Digital | DV <sub>DD</sub> 3318   | Input: Digital video input/OSD input (pull down if not used)<br>Output: Video decoder output 2[6] (BT.656) |
| 120     | DCRIN7                | I/O        | H      | CMOS         | Digital | DV <sub>DD</sub> 3318   | Input: Digital video input/OSD input (pull down if not used)<br>Output: Video decoder output 2[7] (BT.656) |

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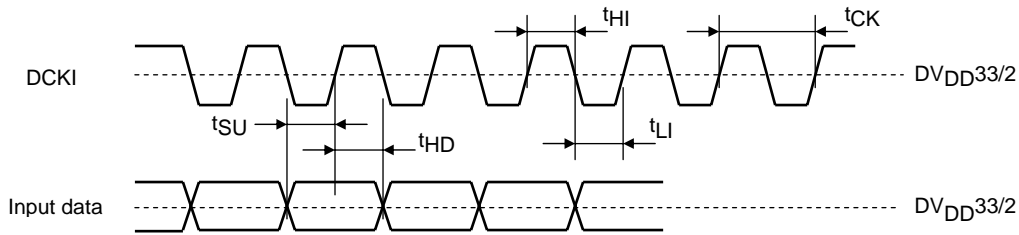
## Pin Type

| I/O type | Function  | Equivalent circuit  | Applicable pins   |
|----------|---|---|---|
| A        | Schmitt trigger<br>CMOS input                           |    | XRST, XPDWN, SCS_I2SEL, XMUTE   |
| B        | 8mA<br>3-STATE drive<br>CMOS I/O                        |    | GP0, GP1, GP2, STXD, INTO,<br>DROUT0, DROUT1, DROUT2, DROUT3,<br>DROUT4, DROUT5, DROUT6, DROUT7,<br>DBOUT0, DBOUT1, DBOUT2, DBOUT3,<br>DBOUT4, DBOUT5, DBOUT6, DBOUT7,<br>DGOUT0, DGOUT1, DGOUT2, DGOUT3,<br>DGOUT4, DGOUT5, DGOUT6, DGOUT7<br>DVSO, DHSO, DDEO, DEXR,<br>PWM, POL, SP, STRB,<br>CPV, OE, FLM, GRST |
| C        | 8mA<br>OpenDrain output<br>CMOS input*                  |    | SCK_SCL, SRXD_SDA   |
| D        | CMOS input  |   | SIOSEL, MODE2, MODE3, TEST, MODE0,<br>DCKI, MODE1, DDEI, DVSI, DHSI,<br>DCBIN0, DCBIN1, DCBIN2, DCBIN3,<br>DCBIN4, DCBIN5, DCBIN6, DCBIN7,<br>DYGIN0, DYGIN1, DYGIN2, DYGIN3,<br>DYGIN4, DYGIN5, DYGIN6, DYGIN7   |
| E        | Analog I/O  |  | REFPKV, VRT, REFNKV, VRB, AIN4,<br>AIN3, AIN2, AIN1, SVO, LPFO  |
| F        | Oscillator circuit I/O                                  |  | XTALI, XTALO  |
| G        | 12mA<br>3-STATE drive<br>CMOS output                    |  | DCKO1   |
| H        | 3.3V: 8mA<br>1.8V: 3mA<br>3-STATE drive<br>CMOS I/O     |  | DCRIN0, DCRIN1, DCRIN2, DCRIN3,<br>DCRIN4, DCRIN5, DCRIN6, DCRIN7   |
| J        | 3.3V: 12mA<br>1.8V: 5mA<br>3-STATE drive<br>CMOS output |  | DCKO2   |

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## I/O Data Timing

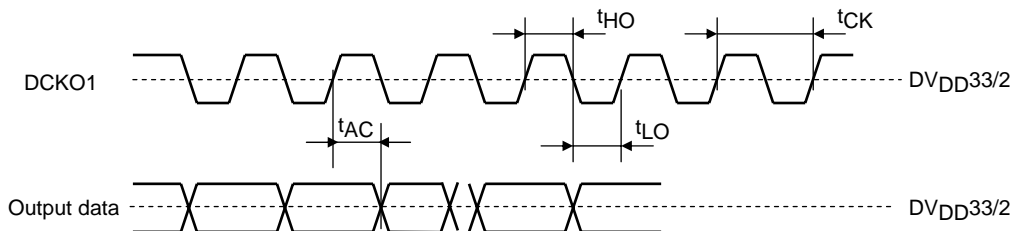
### (1) Input data timing



| Pin name                                       | Parameter   | Symbol   | min  | typ | max | unit |
|--|---|----------|------|-----|-----|------|
| DCKI   | Clock cycle   | $t_{CK}$ | 16.7 |     |     | ns   |
|  | Duty  |          |      | 50  |     | %    |
| DCRIN*, DYGIN*,<br>DCBIN*, DVSI, DHSI,<br>DDEI | Input data setup time<br>( $DV_{DD33} = 3.15V$ to $3.45V$ )<br>( $DV_{DD3318} = 3.15V$ to $3.45V$ ) | $t_{SU}$ | 3    |     |     | ns   |
|  | Input data hold time<br>( $DV_{DD33} = 3.15V$ to $3.45V$ )<br>( $DV_{DD3318} = 3.15V$ to $3.45V$ )  | $t_{HD}$ | 2    |     |     | ns   |

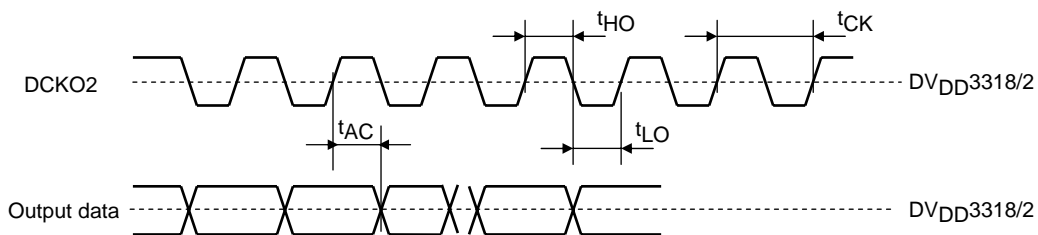
\* The recommended duty ratio of input clock is 50%

### (2) Output data timing



| Pin name   | Parameter  | Symbol   | min  | typ | max | unit |
|--|--|----------|------|-----|-----|------|
| DCKO1  | Clock cycle  | $t_{CK}$ | 16.7 |     |     | ns   |
|  | Duty   |          |      | 50  |     | %    |
| DROUT*, DGOUT*, DBOUT*<br>DVSO, DHSO, DDEO, DEXR, POL,<br>SP, STRB, CPV, OE, FLM, GRST | Output data delay time<br>$DV_{DD33} = 3.15V$ to $3.45V$ | $t_{AC}$ | -3   |     | 3   | ns   |

\* DCKO1 output is not inverted. Output capacitance: 15pF



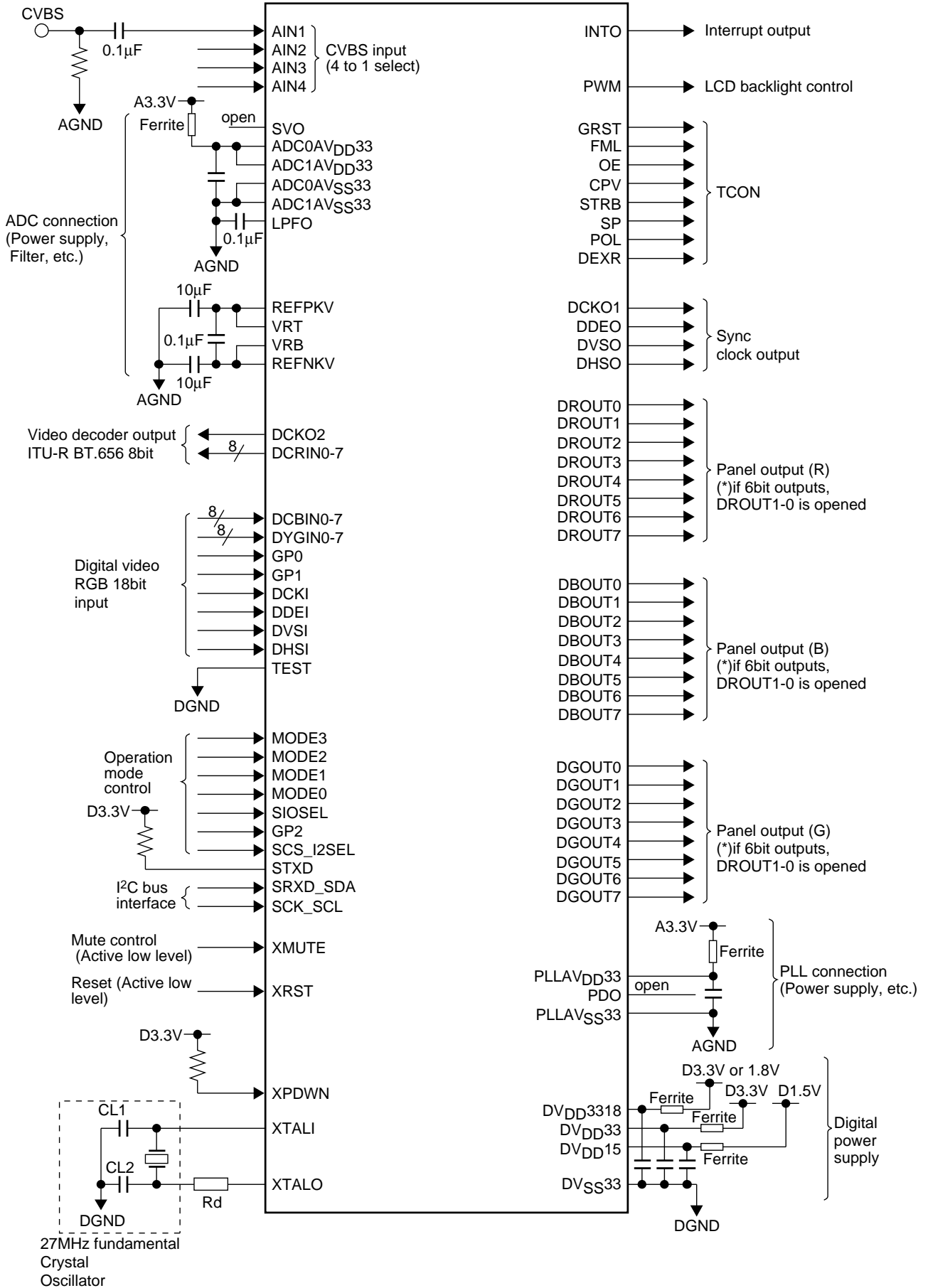
| Pin name   | Parameter  | Symbol   | min | typ | max | unit |
|--|--|----------|-----|-----|-----|------|
| DCKO2  | Clock cycle  | $t_{CK}$ | 37  |     |     | ns   |
|  | Duty   |          |     | 50  |     | %    |
| DCRIN*, DEXR, POL, SP<br>STRB, CPV, OE, FLM, GRST,<br>GP0, GP1, DVSO, DHSO | Output data delay time<br>$DV_{DD3318} = 3.15V$ to $3.45V$<br>$DV_{DD33} = 3.15V$ to $3.45V$ | $t_{AC}$ | -3  |     | 3   | ns   |
| DCRIN*   | Output data delay time<br>$DV_{DD3318} = 1.7V$ to $1.9V$                                     | $t_{AC}$ | -6  |     | 6   | ns   |

\* DCKO1 output is not inverted. Output capacitance: 15pF

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## Connection Example of Parallel Output Mode (Panel/Video Decoder)

\* For details, see Application Note.



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- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



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