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LC709202F

CMOS LSI

1-Cell Li+ (lithium-ion)

Battery Monitor IC

Overview

The LC709202F is an IC that measures the remaining power level of 1-cell lithium-ion (Li+) batteries used for a portable equipment etc.

This product is able to reduce a fuel gauge errors by implementing its unique correction technology for measurement value of battery temperature and voltage.

It is possible for this to realize high precision for measurement in battery power measurement IC that does not need a current sensing resistor. ($\pm 3\%$ under certain conditions)

Applications

- Wireless Handsets
- Smartphones/PDA devices
- MP3 players
- digital cameras
- Portable Game Players
- USB-related devices

Features

- Accuracy of remaining battery power level measurement
- $\pm 3\%$ (at an ambient operating temperature of 0°C to 50°C)

Note: The accuracy above is the value of an experiment using the evaluation board.

- Precision $\pm 7.5\text{mV/Cell}$ Voltage Measurement

- A current sensing resistor is unnecessary.

- Alert function

- Interface

- I²C Interface (up to 400 kHz supported)

- Low power consumption

- Normal Mode : $15\mu\text{A}$
- Sleep Mode : $0.1\mu\text{A}$

- Corresponding battery

- Model to be used depending on the material of the electrode of the battery pack + is different.

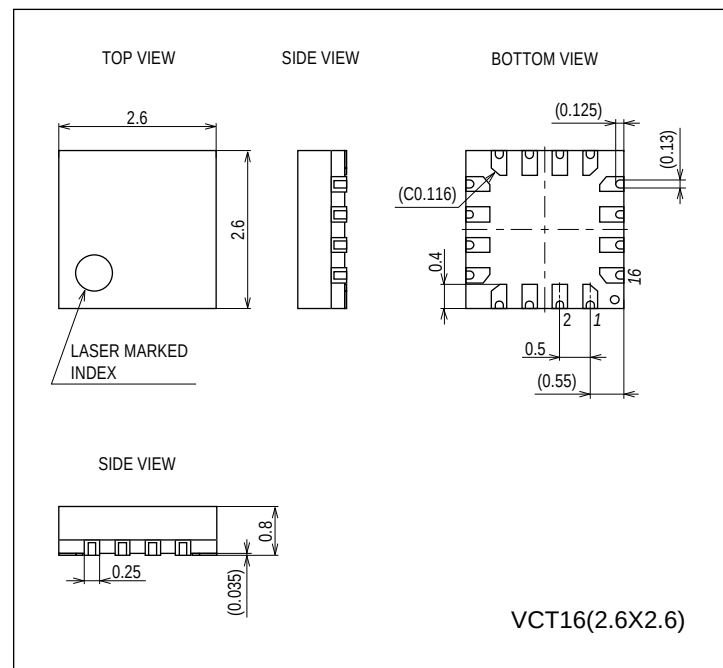
LC709202F-01: ternary system

LC709202F-02: nickelic acid

Package Dimensions

unit : mm (typ)

3318



* I²C Bus is a trademark of Philips Corporation.

LC709202F

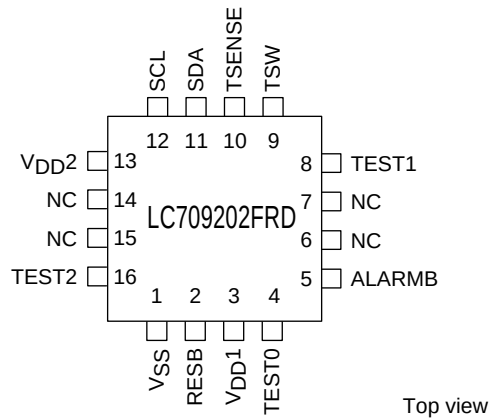
■ Ports

- I²C communication pin 2 (SDA, SCL)
- Battery temperature reading control pin 1 (TSW)
- Analog voltage input pin for battery temperature 1 (TSENSE)
- External alarm / Interrupt for Low-Battery warning 1 (ALARMB)
- Reset pin 1 (RESB)
- TEST pin 3 (TEST0, TEST1, TEST2)
- Power supply pin 3 (VSS, VDD1, VDD2)

■ Package form

- VCT16 (2.6×2.6) : Lead-free type

Pin Assignment

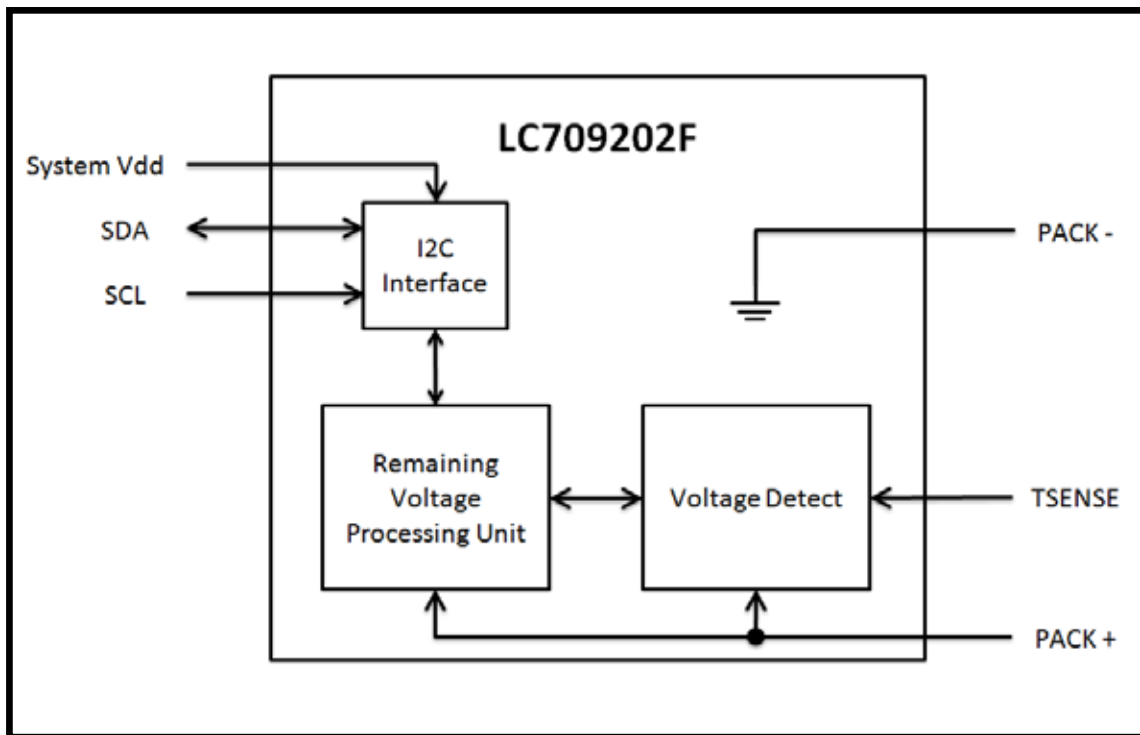


VCT16 (2.6×2.6) “Lead-free Type”

Pin Function

VCT16	Pin Name	I/O	Description
1	VSS	-	Connect to the - terminal of the battery.
2	RESB	I	Reset pin
3	VDD1	-	Connect to the + terminal of the battery.
4	TEST0	I	Test pin *Connect to VSS.
5	ALARMB	O	Alert indication. An active low output used to indicate specified condition thresholds have been met. *When you do not use an alert function, please connect with VSS.
8	TEST1	O	Set “OPEN”
9	TSW	O	Battery temperature reading control pin *Set high when reading in the temperature, held low at other times.
10	TSENSE	I	Battery temperature analog voltage input pin
11	SDA	I/O	I ² C data pin
12	SCL	I/O	I ² C clock pin
13	VDD2	-	+ power pin for I ² C-Bus communication pin(SDA,SCL)
16	TEST2	O	Set “OPEN”

Block Diagram



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Absolute Maximum Ratings at Ta=25°C, V_{SS}=0V

Parameter	Symbol	Pin/Remarks	Conditions	V _{DD} [V]	Specification			Unit
					min	typ	max	
Maximum supply voltage	V _{DD} max	V _{DD1} , V _{DD2}			-0.3		+6.5	V
Input voltage	V _I (1)	RESB, TSENSE			-0.3		V _{DD1} +0.3	
Output voltage	V _O (1)	TSW			-0.3		V _{DD1} +0.3	
	V _O (2)	ALARMB			-0.3			
Input/output voltage	V _{IO} (1)	SDA, SCL			-0.3		+5.5	
Allowable power dissipation	P _d max	VCT16	Ta=-40 to+85°C				55	mW
Operating ambient temperature	T _{opr}				-40		+85	°C
Storage ambient temperature	T _{stg}				-55		+125	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Allowable Operating Conditions at Ta= -40 to +85°C, V_{SS}=0V

Parameter	Symbol	Pin/Remarks	Conditions	V _{DD} [V]	Specification			unit
					min	typ	max	
Operating supply voltage	V _{DD} (1)	V _{DD1}			2.5		4.5	V
High level input voltage	V _{IH} (1)	TSENSE		2.5 to 4.5	0.70V _{DD1}		V _{DD1}	
	V _{IH} (2)	RESB		2.5 to 4.5	0.75V _{DD1}		V _{DD1}	
	V _{IH} (3)	SDA, SCL	V _{DD2} =1.6V to 5.5V	2.5 to 4.5	0.70V _{DD2}		V _{DD2}	
Low level input voltage	V _{IL} (1)	TSENSE		2.5 to 4.5	V _{SS}		0.25V _{DD1}	
	V _{IL} (2)	RESB		2.5 to 4.5	V _{SS}		0.25V _{DD1}	
	V _{IL} (3)	SDA, SCL	V _{DD2} =1.6V to 5.5V	2.5 to 4.5	V _{SS}		0.30V _{DD2}	

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Electrical Characteristics at Ta= -40 to +85°C, VSS=0V

Parameter	Symbol	Pin/Remarks	Conditions	Specification			Unit
				VDD[V]	min	typ	max
High level input current	I _{IH} (1)	RESB	V _{IN} =V _{DD1} (including output transistor off leakage current)	2.5 to 4.5			1
	I _{IH} (2)	SDA, SCL	V _{IN} =V _{DD2} V _{DD2} =1.6V to 5.5V (including output transistor off leakage current)	2.5 to 4.5			1
Low level input current	I _{IL} (1)	RESB	V _{IN} =V _{SS} (including output transistor off leakage current)	2.5 to 4.5	-1		
	I _{IL} (2)	SDA, SCL	V _{IN} =V _{SS} V _{DD2} =1.6V to 5.5V (including output transistor off leakage current)	2.5 to 4.5	-1		
High level output voltage	V _{OH} (1)	TSW	I _{OH} =-0.4 mA	3.0 to 4.5	V _{DD} -0.4		
	V _{OH} (2)		I _{OH} =-0.2 mA	2.5 to 4.5	V _{DD} -0.4		
Low level output voltage	V _{OL} (1)	TSW, ALARMB, SDA, SCL	I _{OL} =3.0 mA	3.0 to 4.5			0.4
	V _{OL} (2)		I _{OL} =1.3 mA	2.5 to 4.5			0.4
Hysteresis voltage	V _{HYS} (1)	RESB		2.5 to 4.5		0.1V _{DD1}	
	V _{HYS} (2)	SDA, SCL		2.5 to 4.5		0.1V _{DD2}	
Pin capacitance	CP	All pins	Pins other than the pin under test V _{IN} =V _{SS} Ta=25°C	2.5 to 4.5		10	pF
Consumption current (Note 1)	I _{DD} (1)	V _{DD1}	Normal Mode	2.5 to 4.5		15	26
	I _{DD} (2)		Auto Mode	2.5 to 4.5		2 to 15	4 to 26
	I _{DD} (3)		Sleep Mode	2.5 to 4.5		0.1	5
Voltage measurement accuracy	V _{ME} (1)	V _{DD1}	Ta= +25°C	3.6	-7.5		+7.5
	V _{ME} (2)		Ta= -20°C to +70°C	2.5 to 4.5	-20		+20

Note 1: Consumption current is a value in the range of -20°C to +70°C

I²C Slave Characteristics at Ta=-40 to+85°C, V_{SS}=0V

Parameter	Symbol	Pin/Remarks	Conditions	V _{DD} [V]	Specification		unit
					min	max	
Clock frequency	TSCL	SCL		2.5 to 4.5		400	kHz
Bus free time between STOP condition and START condition	TBUF	SCL, SDA	See Fig. 1.		1.3		μs
Hold time (repeated) START condition First clock pulse is generated after this interval	THD:STA	SCL, SDA	See Fig. 1.		0.6		μs
Repeated START condition setup time	TSU:STA	SCL, SDA	See Fig. 1.		0.6		μs
STOP condition setup time	TSU:STO	SCL, SDA	See Fig. 1.		0.6		μs
Data hold time	THD:DAT	SCL, SDA	See Fig. 1.		0	0.9	μs
Data setup time	TSU:DAT	SCL, SDA	See Fig. 1.		100		ns
Clock low period	TLOW	SCL			1.3		μs
Clock high period	THIGH	SCL			0.6		μs
Clock/data fall time	TF	SCL, SDA			20 + 0.1C _B	300	ns
Clock/data rise time	TR	SCL, SDA			20 + 0.1C _B	300	ns

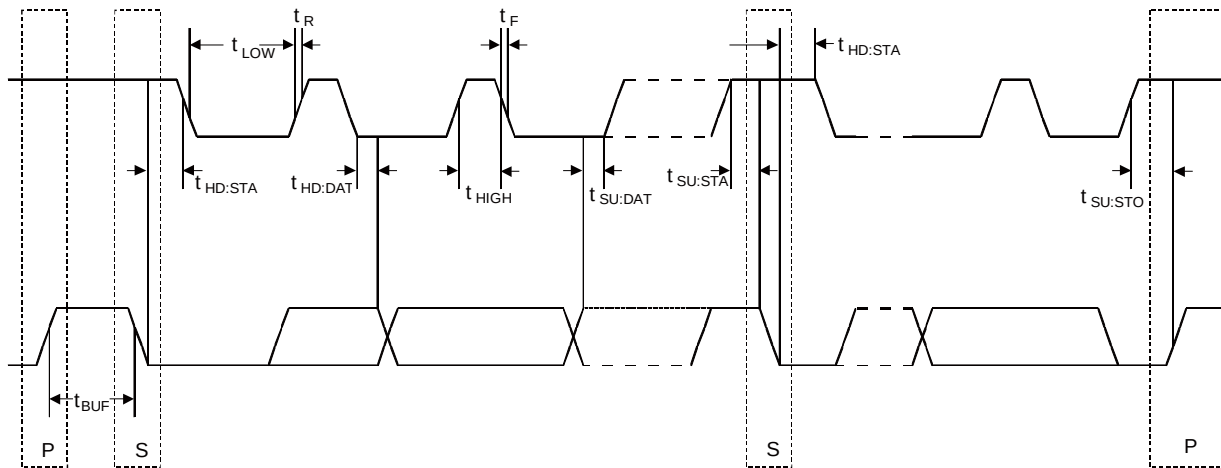


Figure 1 I²C Timing

Discharge Characteristics

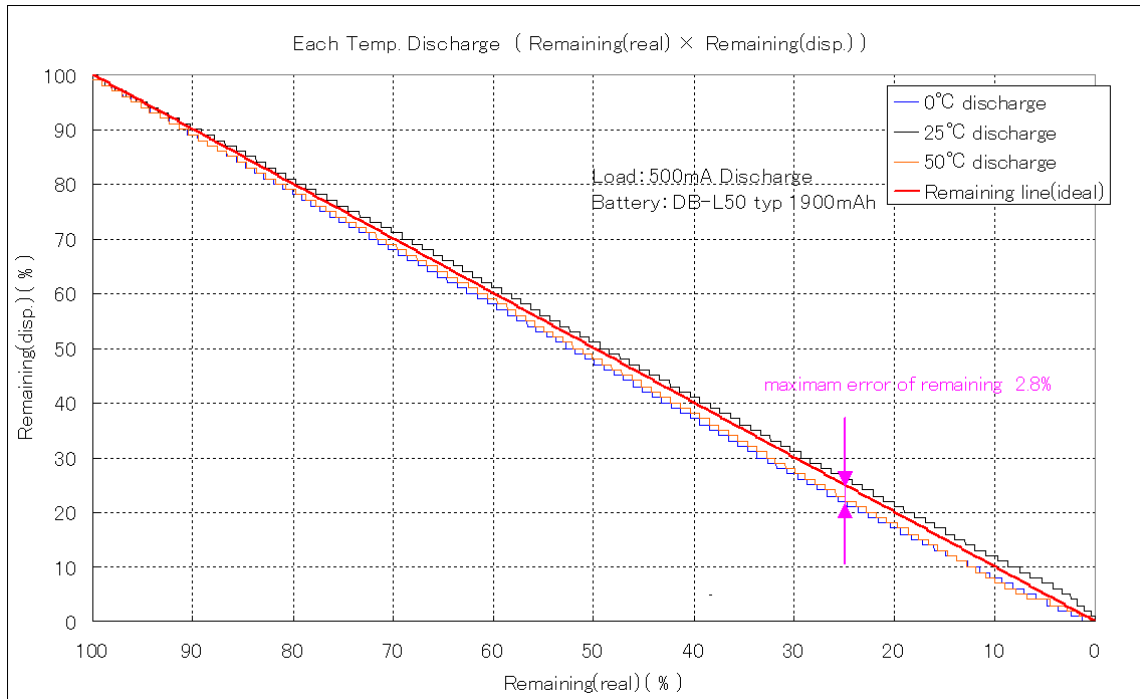


Figure 2 Discharge Characteristics by Temperature Change

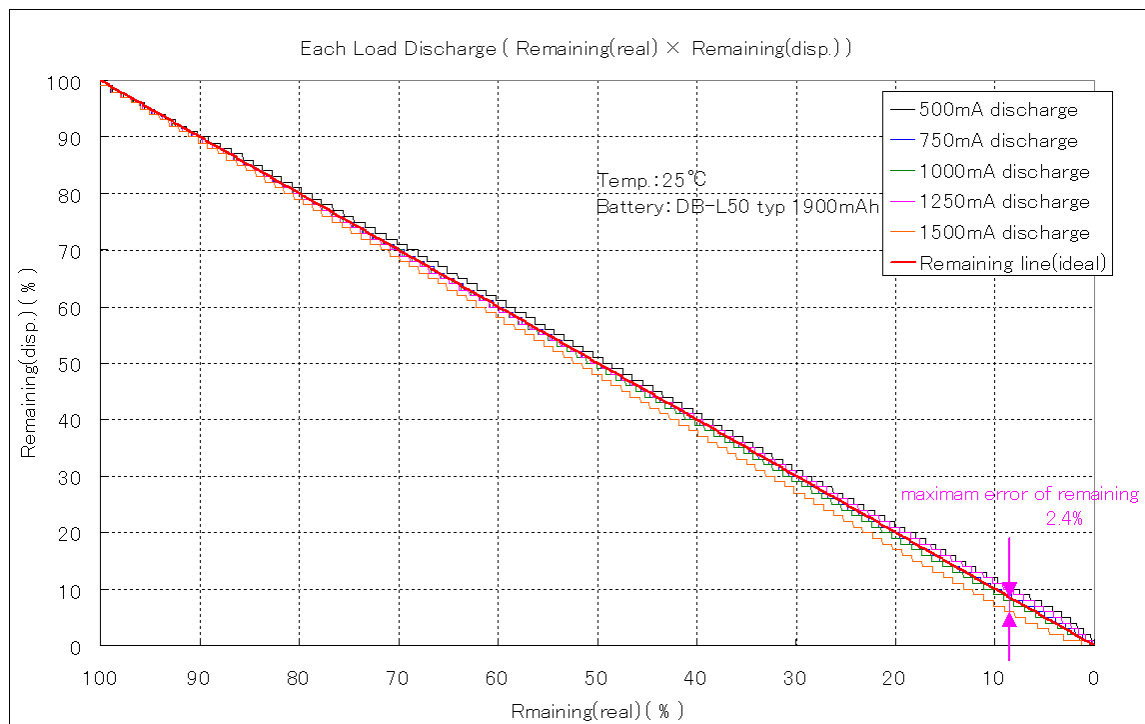


Figure 3 Discharge Characteristics by Load Change

Communication Protocol

Communication protocol type: I²C

Frequency: 400 kHz

Address: 0x16

Bus Protocols

S	:	Start Condition
Sr	:	Repeated Start Condition
Rd	:	Read (bit value of 1)
Wr	:	Write (bit value of 0)
A	:	ACK (bit value of 0)
N	:	NACK (bit value of 1)
P	:	Stop Condition
CRC-8	:	Slave Address to Last Data (CRC-8-ATM: ex.3778mV: 0x16,0x09,0x17,0xC2,0x0E □ 0x86)
	:	Master-to-Slave
	:	Slave-to-Master
...	:	Continuation of protocol

Read Word Protocol

S	Slave Address	Wr	A	Command Code	A	...
Sr	Slave Address	Rd	A	Data Byte Low	A	Data Byte High ...
A	CRC-8	N	P			

Write Word Protocol

S	Slave Address	Wr	A	Command Code	A	...
	Data Byte Low	A	Data Byte High	A	CRC-8	A P

Access	Slave Functions	Command Code	Range	Unit
Read	Cell Temperature	0x08	0 to 65535	0.1°K (0.0°C= 2732)
	Cell Voltage	0x09	0 to 65535	mV
	Current	0x0A	-32768 to 32767	mA
	Adjustment Pack 8	0x0B	0 to 255	Value
	Relative State Of Charge	0x0D	0 to 100	%
	Remaining Capacity	0x0F	0 to 1000	mAh
	Full Charge Capacity	0x10	1000	mAh
	IC Version	0x11	0 to 65535	Version
	Adjustment Thermistor	0x12	0 to 255	Value
	Hot Start Sleep Mode Auto Mode	0x13	bit 0 bit 1 bit 2	disable: 0 or enable: 1
	Alarm Low Battery	0x14	High : 0 to 250 Low : 0 to 100	20mV %
	Adjustment B	0x15	0 to 65535	B
	System Mode	0x16	bit 0to3 : bit 4to7 : data 0 to 6	Nomal Mode Sleep Mode Auto Mode Auto deep
Write	Adjustment Pack 0	0x00	0 to 32767	Value
	Adjustment Pack 1	0x01	0 to 32767	Value
	Adjustment Pack 2	0x02	0 to 32767	Value
	Adjustment Pack 3	0x03	0 to 32767	Value
	Adjustment Pack 4	0x04	0 to 32767	Value
	Adjustment Pack 5	0x05	0 to 32767	Value
	Set Relative State Of Charge	0x08	High : 0xA5 Low : 0 to 100	- %
	Adjustment Pack 8		High : 0x5A Low : 0 to 255	- Value
	Adjustment Thermistor		High : 0xAA Low : 0 to 255	- Value
	Hot Start Sleep Mode Auto Mode		High : 0x55 Low : bit 0 bit 1 bit 2	disable: 0 or enable: 1
	Initial Relative State Of Charge		0xAA55	-
	Alarm Low Battery	0x0A	High : 0 to 250 Low : 0 to 100	20mV(activate under) %(activate under)
	Adjustment B	0x0B	0 to 65535	B
	Cell Temperature	0x0C	2532 to 3332 (I2C Write Mode) 0xAA55 (Thermistor Mode)	0.1°K (0.0°C= 2732) -

The schematic diagram illustrates the electrical connections for the LC709202F VCT16(2.6x2.6) sensor module. The module is a central component with various pins and test points. It is connected to a Battery Pac (PACK-, PACK+) and a System Vdd/Vss supply. The module includes an I2C Bus Master interface (SCL, SDA) and an Interrupt Input. The module also features pins for VDD2, VSS, TEST1, TEST2, TEST0, TEST3, and various test points (TSENSE, TSW, TSENSE, TSW). The module is connected to a Battery Pac (PACK-, PACK+) and a System Vdd/Vss supply. The module includes an I2C Bus Master interface (SCL, SDA) and an Interrupt Input. The module also features pins for VDD2, VSS, TEST1, TEST2, TEST0, TEST3, and various test points (TSENSE, TSW, TSENSE, TSW).

The schematic diagram illustrates the electrical connections for the LC709202F VCT16(2.6x2.6) sensor module. The module is a square component with pins labeled SCL, SDA, TSENSE, TSW, VDD2, NC, TEST1, NC, NC, TEST2, VSS, RESB, VDD1, TEST0, and ALARMB. The connections are as follows:

- Battery Pac:** The T pin is connected to the TSENSE pin. The VDD2 pin is connected to the positive terminal of the Battery Pac. The VSS pin is connected to the negative terminal of the Battery Pac. The PACK- and PACK+ pins are also connected to the Battery Pac terminals.
- ASIC:** The ALARMB pin is connected to the Interrupt Input of the ASIC. The VDD1 pin is connected to the VDD pin of the ASIC. The VSS pin is connected to the VSS pin of the ASIC.
- System Vdd/Vss:** The VDD1 pin is connected to the System Vdd rail. The VSS pin is connected to the System Vss rail.
- Resistors:** A 10kΩ resistor is connected between the TSENSE pin and the System Vdd rail. A 100kΩ resistor is connected between the TSW pin and the System Vdd rail. A 10kΩ resistor is connected between the ALARMB pin and the System Vss rail.
- Capacitors:** A 0.1μF capacitor is connected between the VDD2 pin and the System Vdd rail. A 1μF capacitor is connected between the VDD1 pin and the System Vdd rail. A 0.1μF capacitor is connected between the VSS pin and the System Vss rail.

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