

1. General description

Planar passivated high commutation three quadrant triac in a SOT54 (TO-92) plastic package. This "series D" triac balances the requirements of commutation performance and gate sensitivity and is intended for interfacing with low power drivers and logic ICs including microcontrollers.

2. Features and benefits

- 3Q technology for improved noise immunity
- Direct gate triggering from low power drivers and logic ICs
- High commutation capability with very sensitive gate
- High voltage capability
- Planar passivated for voltage ruggedness and reliability
- Triggering in three quadrants only
- Very sensitive gate for easy logic level triggering

3. Applications

- Low power motor controls
- Small inductive loads e.g. solenoids, door locks, water valves
- Small loads in large white goods

4. Quick reference data

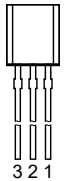
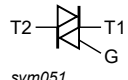
Table 1. Quick reference data

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------------------------|--------------------------------------|---|------|-----|------|--------------------|
| V_{DRM} | repetitive peak off-state voltage | | - | - | 1000 | V |
| $I_{\text{T(RMS)}}$ | RMS on-state current | full sine wave; $T_{\text{lead}} \leq 70\text{ }^{\circ}\text{C}$; Fig. 1 ; Fig. 2 ; Fig. 3 | - | - | 0.8 | A |
| I_{TSM} | non-repetitive peak on-state current | full sine wave; $T_{\text{j(init)}} = 25\text{ }^{\circ}\text{C}$; $t_{\text{p}} = 20\text{ ms}$; Fig. 4 ; Fig. 5 | - | - | 9 | A |
| | | full sine wave; $T_{\text{j(init)}} = 25\text{ }^{\circ}\text{C}$; $t_{\text{p}} = 16.7\text{ ms}$ | - | - | 9.9 | A |
| T_{j} | junction temperature | | - | - | 125 | $^{\circ}\text{C}$ |
| Static characteristics | | | | | | |
| I_{GT} | gate trigger current | $V_{\text{D}} = 12\text{ V}$; $I_{\text{T}} = 0.1\text{ A}$; T2+ G+; $T_{\text{j}} = 25\text{ }^{\circ}\text{C}$; Fig. 7 | 0.25 | - | 5 | mA |
| | | $V_{\text{D}} = 12\text{ V}$; $I_{\text{T}} = 0.1\text{ A}$; T2+ G-; $T_{\text{j}} = 25\text{ }^{\circ}\text{C}$; Fig. 7 | 0.25 | - | 5 | mA |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------------------|---------------------------------------|--|------|-----|-----|------------------|
| | | $V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2- G-; $T_j = 25\text{ }^\circ\text{C}$; Fig. 7 | 0.25 | - | 5 | mA |
| I_H | holding current | $V_D = 12\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 9 | - | - | 10 | mA |
| V_T | on-state voltage | $I_T = 0.85\text{ A}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 10 | - | 1.3 | 1.6 | V |
| Dynamic characteristics | | | | | | |
| dV_D/dt | rate of rise of off-state voltage | $V_{DM} = 670\text{ V}$; $T_j = 125\text{ }^\circ\text{C}$; ($V_{DM} = 67\%$ of V_{DRM}); exponential waveform; gate open circuit | - | 150 | - | V/ μs |
| dI_{com}/dt | rate of change of commutating current | $V_D = 400\text{ V}$; $T_j = 125\text{ }^\circ\text{C}$; $I_{T(RMS)} = 0.8\text{ A}$; $dV_{com}/dt = 10\text{ V}/\mu\text{s}$; gate open circuit | 0.5 | - | - | A/ms |
| | | $V_D = 400\text{ V}$; $T_j = 125\text{ }^\circ\text{C}$; $I_{T(RMS)} = 0.8\text{ A}$; $dV_{com}/dt = 1\text{ V}/\mu\text{s}$; gate open circuit | 1 | - | - | A/ms |

5. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|-----|--------|-----------------|--|---|
| 1 | T2 | main terminal 2 |  TO-92 (SOT54) |  sym051 |
| 2 | G | gate | | |
| 3 | T1 | main terminal 1 | | |

6. Ordering information

Table 3. Ordering information

| Type number | Package | | |
|---------------|---------|---|---------|
| | Name | Description | Version |
| BTA2008-1000D | TO-92 | plastic single-ended leaded (through hole) package; 3 leads | SOT54 |

7. Marking

Table 4. Marking codes

| Type number | Marking code |
|---------------|--------------|
| BTA2008-1000D | 200810D |

8. Limiting values

Table 5. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---------------------|--------------------------------------|--|-----|------|------------------|
| V _{DRM} | repetitive peak off-state voltage | | - | 1000 | V |
| I _{T(RMS)} | RMS on-state current | full sine wave; T _{lead} ≤ 70 °C; Fig. 1; Fig. 2; Fig. 3 | - | 0.8 | A |
| I _{TSM} | non-repetitive peak on-state current | full sine wave; T _{j(init)} = 25 °C; t _p = 20 ms; Fig. 4; Fig. 5 | - | 9 | A |
| | | full sine wave; T _{j(init)} = 25 °C; t _p = 16.7 ms | - | 9.9 | A |
| I ² t | I ² t for fusing | t _p = 10 ms; sine-wave pulse | - | 0.41 | A ² s |
| di _T /dt | rate of rise of on-state current | I _G = 20 mA | - | 100 | A/μs |
| I _{GM} | peak gate current | | - | 1 | A |
| P _{GM} | peak gate power | | - | 2 | W |
| P _{G(AV)} | average gate power | over any 20 ms period | - | 0.1 | W |
| T _{stg} | storage temperature | | -40 | 150 | °C |
| T _j | junction temperature | | - | 125 | °C |

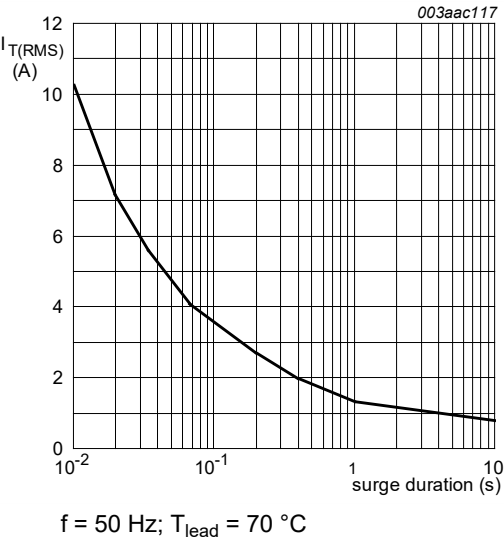


Fig. 1. RMS on-state current as a function of surge duration; maximum values

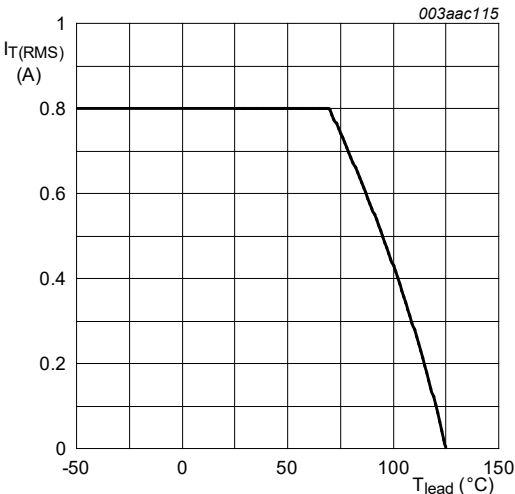


Fig. 2. RMS on-state current as a function of lead temperature; maximum values

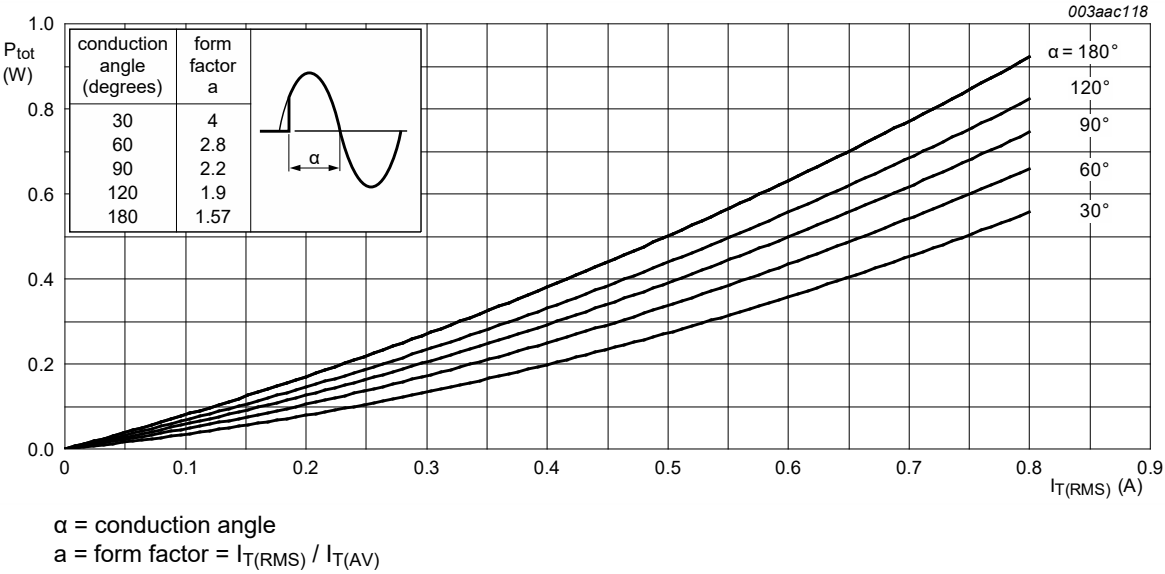


Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values

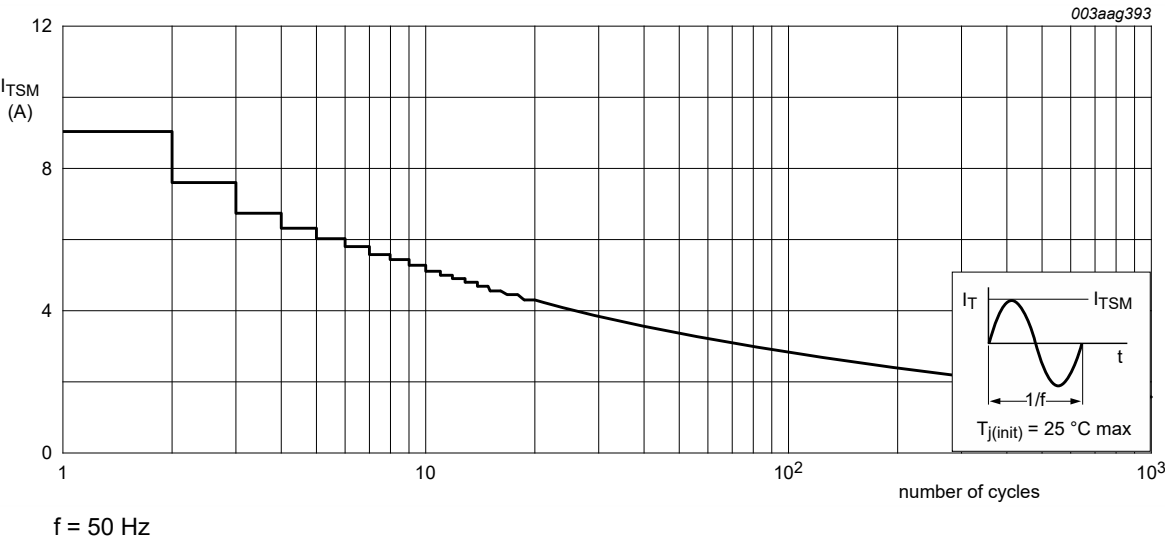
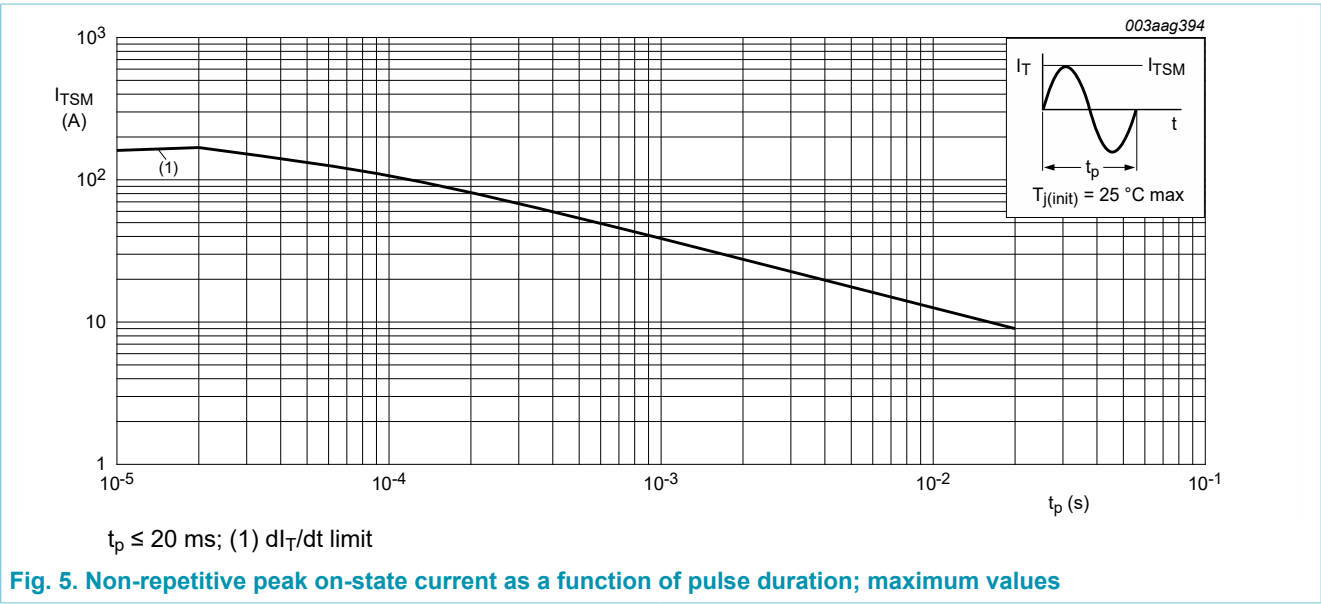


Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values



9. Thermal characteristics

Table 6. Thermal characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------|--|---|-----|-----|-----|------|
| $R_{th(j-lead)}$ | thermal resistance from junction to lead | full cycle; Fig. 6 | - | - | 60 | K/W |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient free air | printed circuit board mounted: lead length = 4 mm | - | 150 | - | K/W |

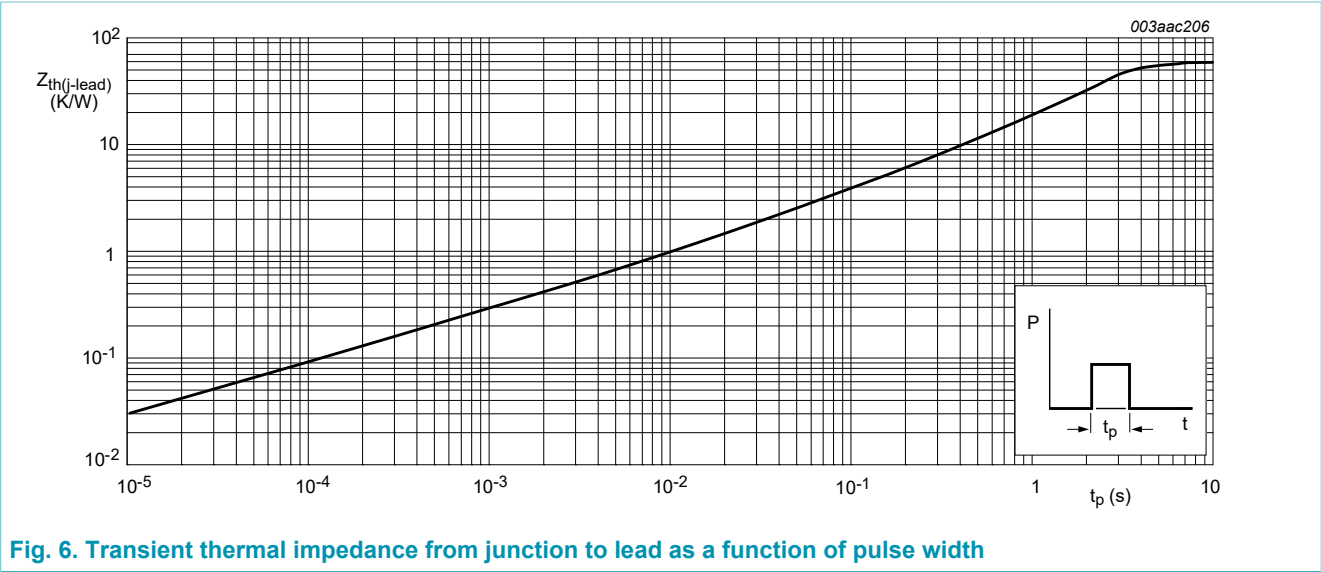
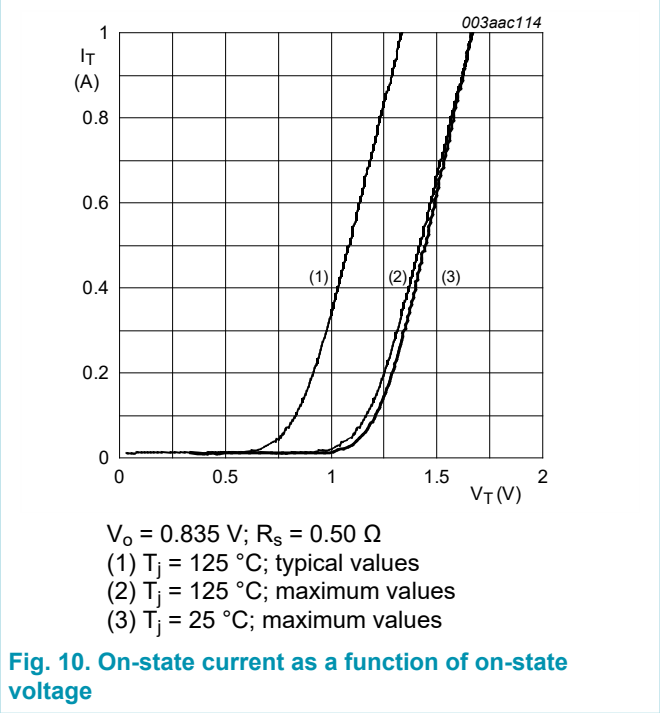
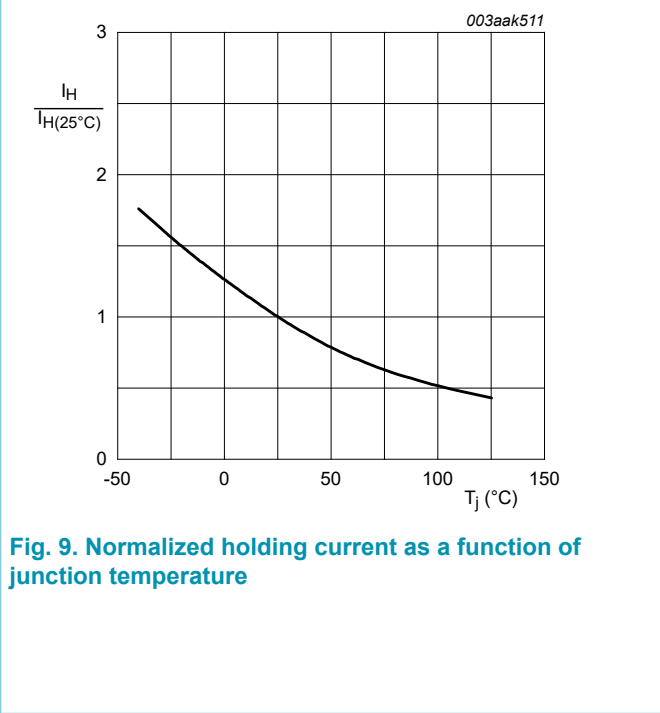
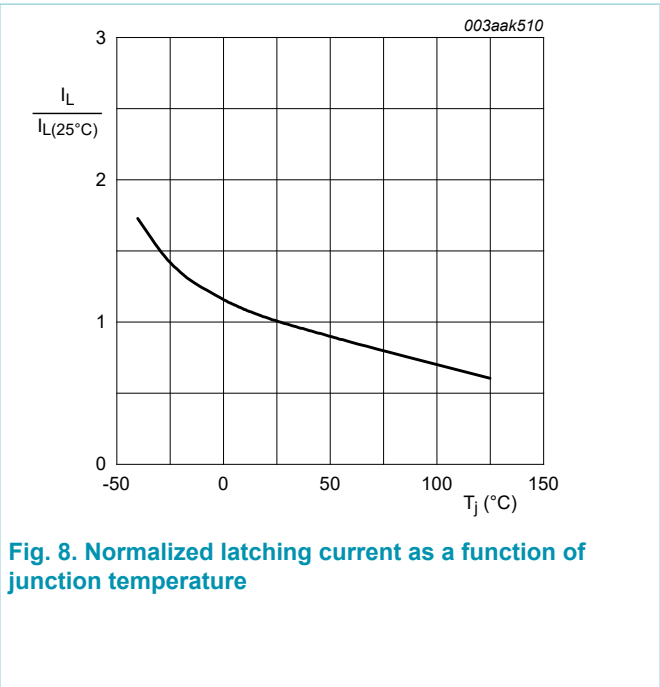
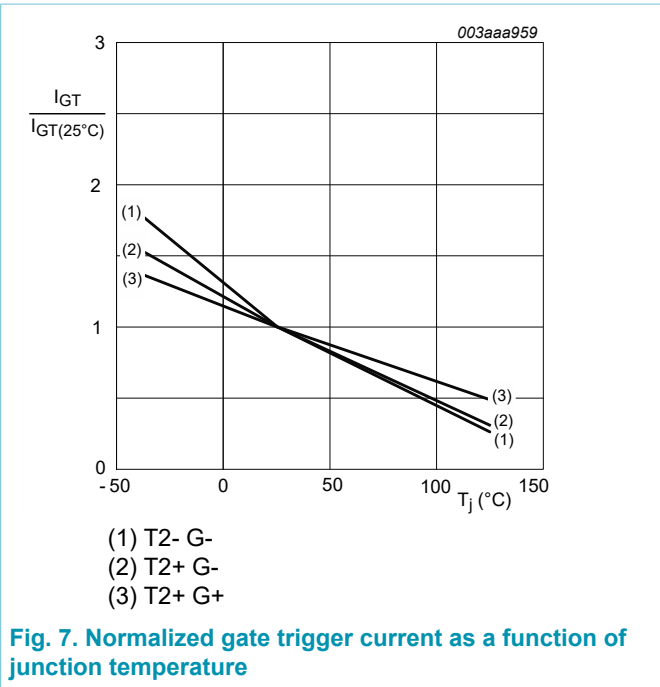


Fig. 6. Transient thermal impedance from junction to lead as a function of pulse width

10. Characteristics

Table 7. Characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------------------|---------------------------------------|--|------|------|-----|------------------|
| Static characteristics | | | | | | |
| I_{GT} | gate trigger current | $V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G+; $T_j = 25\text{ }^\circ\text{C}$; Fig. 7 | 0.25 | - | 5 | mA |
| | | $V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G-; $T_j = 25\text{ }^\circ\text{C}$; Fig. 7 | 0.25 | - | 5 | mA |
| | | $V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2- G-; $T_j = 25\text{ }^\circ\text{C}$; Fig. 7 | 0.25 | - | 5 | mA |
| I_L | latching current | $V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; T2+ G+; $T_j = 25\text{ }^\circ\text{C}$; Fig. 8 | - | - | 10 | mA |
| | | $V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; T2+ G-; $T_j = 25\text{ }^\circ\text{C}$; Fig. 8 | - | - | 20 | mA |
| | | $V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; T2- G-; $T_j = 25\text{ }^\circ\text{C}$; Fig. 8 | - | - | 10 | mA |
| I_H | holding current | $V_D = 12\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 9 | - | - | 10 | mA |
| V_T | on-state voltage | $I_T = 0.85\text{ A}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 10 | - | 1.3 | 1.6 | V |
| V_{GT} | gate trigger voltage | $V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 11 | - | 0.85 | 1 | V |
| | | $V_D = 400\text{ V}$; $I_T = 0.1\text{ A}$; $T_j = 125\text{ }^\circ\text{C}$; Fig. 11 | 0.2 | 0.3 | - | V |
| I_D | off-state current | $V_D = 1000\text{ V}$; $T_j = 125\text{ }^\circ\text{C}$ | - | 0.1 | 0.5 | mA |
| Dynamic characteristics | | | | | | |
| dV_D/dt | rate of rise of off-state voltage | $V_{DM} = 670\text{ V}$; $T_j = 125\text{ }^\circ\text{C}$; ($V_{DM} = 67\%$ of V_{DRM}); exponential waveform; gate open circuit | - | 150 | - | V/ μs |
| dI_{com}/dt | rate of change of commutating current | $V_D = 400\text{ V}$; $T_j = 125\text{ }^\circ\text{C}$; $I_{T(RMS)} = 0.8\text{ A}$; $dV_{com}/dt = 10\text{ V}/\mu\text{s}$; gate open circuit | 0.5 | - | - | A/ms |
| | | $V_D = 400\text{ V}$; $T_j = 125\text{ }^\circ\text{C}$; $I_{T(RMS)} = 0.8\text{ A}$; $dV_{com}/dt = 1\text{ V}/\mu\text{s}$; gate open circuit | 1 | - | - | A/ms |



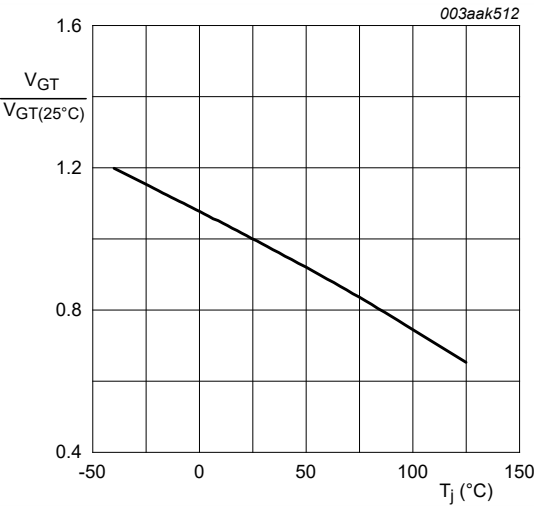


Fig. 11. Normalized gate trigger voltage as a function of junction temperature

11. Package outline

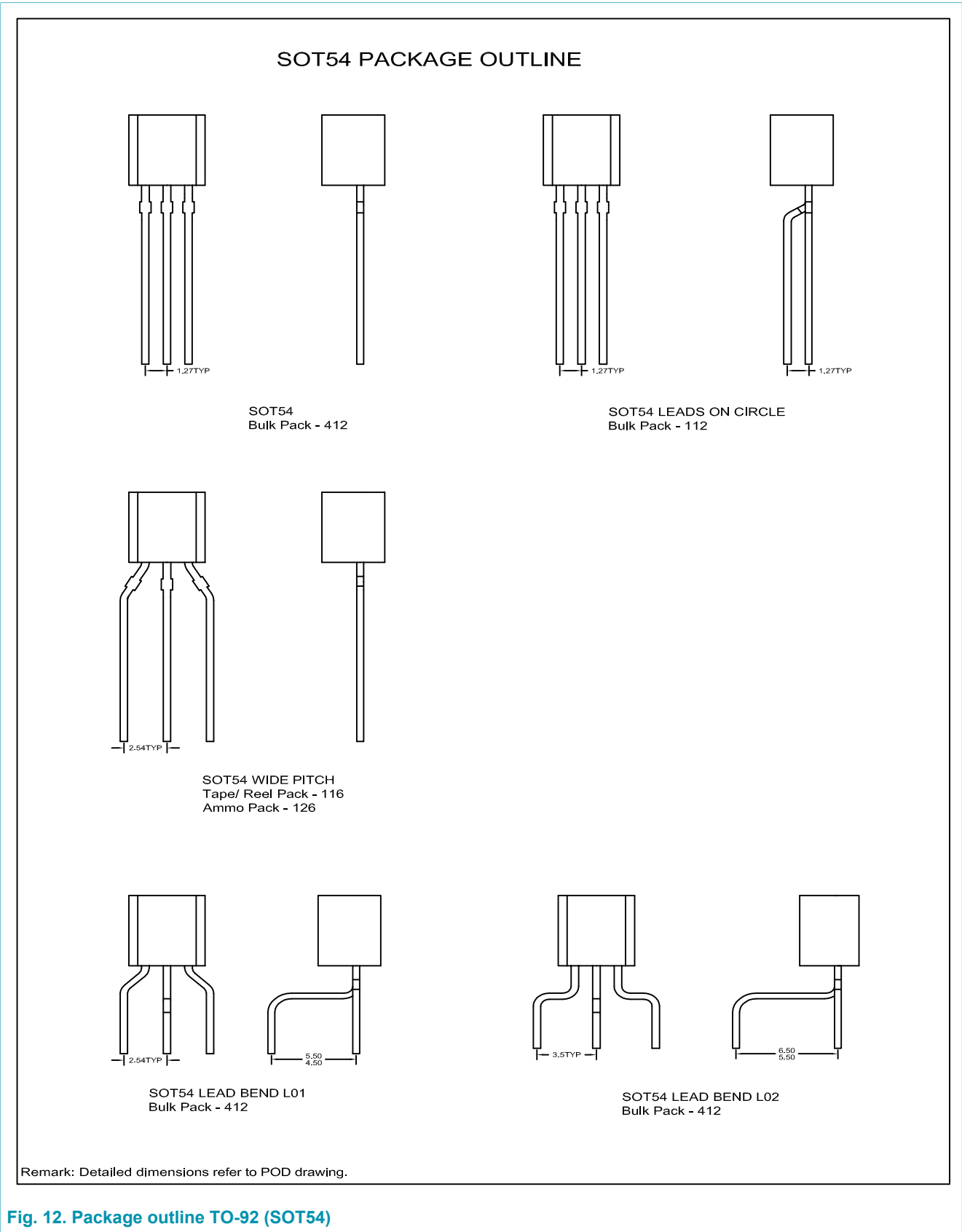


Fig. 12. Package outline TO-92 (SOT54)

12. Legal information

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| Document status [1][2] | Product status [3] | Definition |
|--------------------------------|--------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
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| Product [short] data sheet | Production | This document contains the product specification. |

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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13. Contents

1. General description..... 1

2. Features and benefits..... 1

3. Applications..... 1

4. Quick reference data..... 1

5. Pinning information.....2

6. Ordering information.....2

7. Marking.....2

8. Limiting values..... 3

9. Thermal characteristics..... 6

10. Characteristics.....7

11. Package outline..... 10

12. Legal information..... 11

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Date of release: 28 September 2016



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