ZL30316

Combined Synchronous Ethernet and IEEE1588 Timing over Packet Technology

Data Sheet

October 2012

Features

- Supports Hybrid Mode (using SyncE for frequency synchronization and IEEE 1588 for phase alignment)
- Recovers and transmits network synchronization over Ethernet, IP and MPLS Networks
- Simultaneously supports both the Synchronous Ethernet and the IEEE1588 industry standard timing protocols
- Capable of server, client and boundary clock operationIntegrates two separate digital phase locked loops, with hitless switching between packet and electrical clock references
- Targeted for synchronization distribution to better than ITU-T G.8261, G.823, G.824 and ANSI T1.101 synchronization interface standards
- Average frequency accuracy better than ±10 ppb
- Aligns to a low frequency input signal at server (e.g., 1 Hz) with targeted accuracy better than ±1 µs
- Recovers clocks from two independent servers, with hitless switching between packet streams for redundancy
- Supports holdover if the server stream is lost
- Accepts eight input references, and up to three associated low frequency alignment or framing pulses

Ordering Information

ZL30316GKG	256 TEPBGA, 17 x 17 mm
ZL30316GKG2*	256 TEPBGA, 17 x 17 mm

* Pb Free Tin/Silver/Copper

-40°C to +85°C

- Generates up to four separate output clocks at frequencies between 8 kHz and 100 MHz
- Generates two separate Synchronous Ethernet clocks to drive industry standard Ethernet PHY devices at either 25 MHz or 125 MHz
- Fully configurable solution, enabling performance to be tailored to application/network requirements
- Two independently configurable MAC interfaces, supporting MII, RMII, GMII and TBI standards
- Wire-speed Ethernet Bridge pass through function between the MAC interfaces
- Synchronous serial control interface
- Full demonstration & evaluation platform available

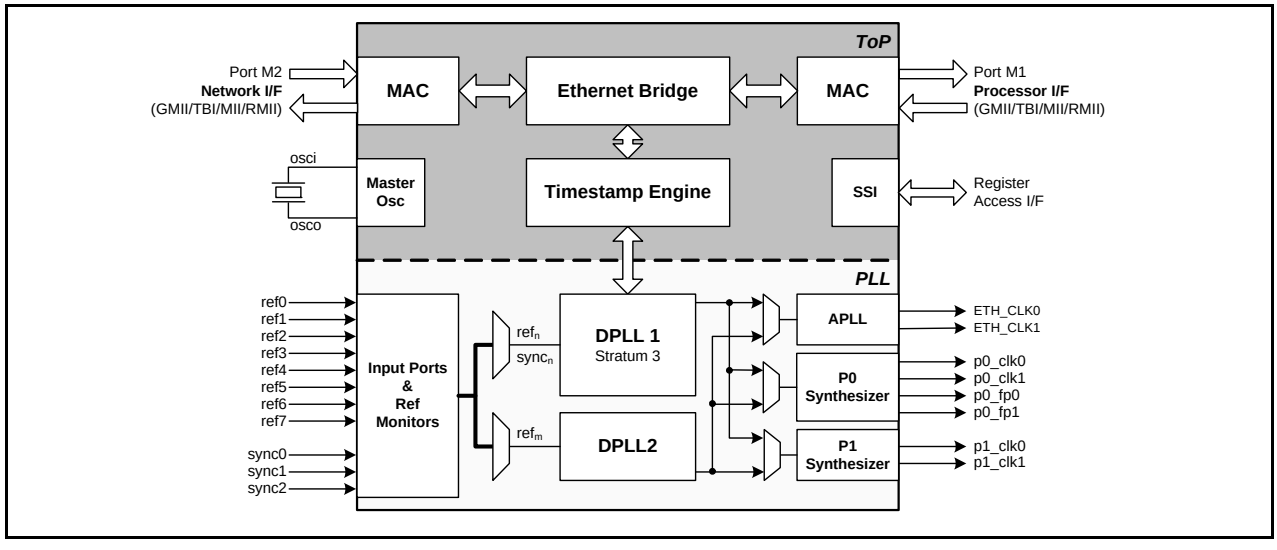


Figure 1 - ZL30316 Functional Block Diagram

Applications

- IEEE 1588 and Synchronous Ethernet timing
- GSM and UMTS air interface synchronization over a packet network
- Circuit Emulation Services over Packets
- IP-PBX and VoIP Gateways
- Video Conferencing
- Broadband Video Distribution

Description

Network infrastructures are gradually converging onto a packet-based architecture. With this convergence, there are a significant number of synchronous applications that require accurate timing to be distributed over the packet networks. Examples of precision timing sensitive applications that need the transport of synchronization over packet networks include transport of TDM over packet networks, connections to 2 G and 3 G cellular base stations, Voice over IP, IP PBXs, video-conferencing and broadband video.

There are two main ways to enable synchronization over a packet network, synchronizing the packet network itself, as in the Synchronous Ethernet approach, or distributing the timing using the packets as in Microsemi's Timing over Packet (ToP) technology. The two techniques can also be combined to provide a very powerful hybrid solution. Synchronous Ethernet delivers a very accurate frequency reference, but doesn't address phase and time synchronization. ToP can be used to supplement the excellent frequency distribution of Synchronous Ethernet with accurate phase and time information. Alternatively, ToP can be used to extend the reach of the Synchronous Ethernet reference across an asynchronous network, such as a LAN connected to a synchronous WAN.

Microsemi has combined both methods into a single device. The ZL30316 incorporates an extremely low-jitter frequency synthesizer, capable of generating all the frequencies required for Synchronous Ethernet operation, together with Microsemi's patent-pending Timing over Packet (ToP) technology based on the industry-standard IEEE1588™ "PTP" (Precision Time Protocol). Not only can it function as a fully-featured Digital PLL, it also supports the distribution of time, phase and frequency across both layer 2 and layer 3 networks, using both Synchronous Ethernet and IEEE1588 protocols, either alone or in combination.

The ZL30316 is a member of a family of footprint-compatible devices offering the full range of features required for timing and synchronization across the packet network. These devices facilitate design of a flexible card that can be upgraded as required by simply placing another member of the same family.

The family members include:

ZL30310	Combined IEEE1588™ ToP and Synchronous Ethernet, coupled with a GR-1244 Stratum 3E/3/4/4E and GR-253 SONET and G.813 quality phase locked loop for timing card applications, plus a second independent PLL for rate conversion or generation of additional derived clocks.
ZL30312	Combined IEEE1588™ ToP and Synchronous Ethernet, coupled with a GR-1244 Stratum 3/4/4E and GR-253 SEONET and G.813 quality phase locked loop for timing card applications, plus a second independent PLL for rate conversion or generation of additional derived clocks.
ZL30314	Combined IEEE1588™ ToP and Synchronous Ethernet, coupled with a GR1244 Stratum 3/4/4E and G.813 Option 1 quality phase locked loop for timing card applications, plus a second independent PLL for rate conversion or generation of additional derived clocks.
ZL30316	Combined IEEE1588™ ToP and Synchronous Ethernet, coupled with two independent, flexible phase locked loops for line card applications
ZL30320	Combined IEEE1588™ ToP and Synchronous Ethernet for line card applications
ZL30321	Synchronous Ethernet line card device in a ToP compatible footprint, containing two independent DPLLs

The Microsemi device offers the following clock routing options:

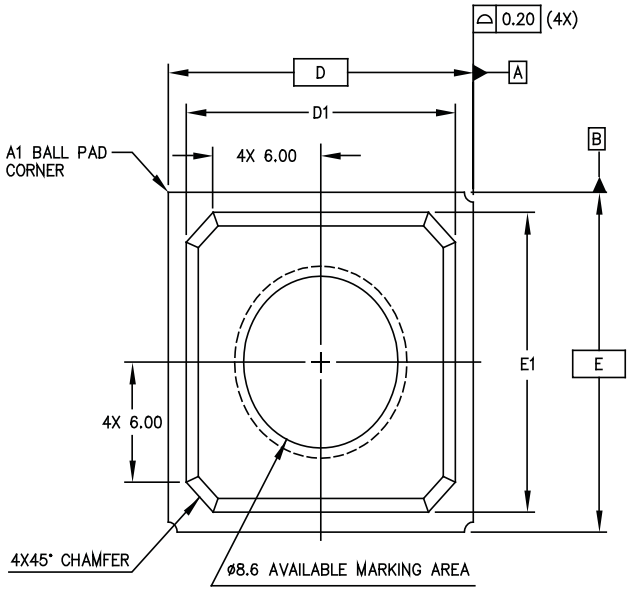
Input	Output	Description
clock reference	clock	conventional PLL behaviour, *e.g., Synchronous Ethernet node*
clock reference	packet stream	server behaviour, *e.g., IEEE1588 server*
clock reference	clock and/or packet stream	conventional PLL behaviour coupled with packet time server, *e.g., combined Synchronous Ethernet and IEEE1588 server*
packet reference	clock	client behaviour, *e.g., IEEE1588 client*
clock and/or packet reference	clock	conventional PLL behaviour, coupled with packet time client, either as fail-over from one to the other, or in combination *e.g., combined Synchronous Ethernet and IEEE1588 client*
packet reference	clock and/or packet stream	combination of client and boundary clock behaviour, *e.g., IEEE1588 boundary clock*

When operating as a server, the Microsemi device locks onto the incoming clock reference as a conventional PLL, filtering any jitter that may be present. It also synchronizes to any low-frequency alignment signal, e.g., an 8 kHz TDM frame pulse, or a 1 Hz alignment input. The device delivers streams of packets, each containing a timestamp indicating the precise time that the packet was launched into the network, relative to the acquired reference. It also receives packets from clients, and returns a message indicating the exact time that the client message was received at the server. Using this information, clients are able to align their own timebase with that of the server.

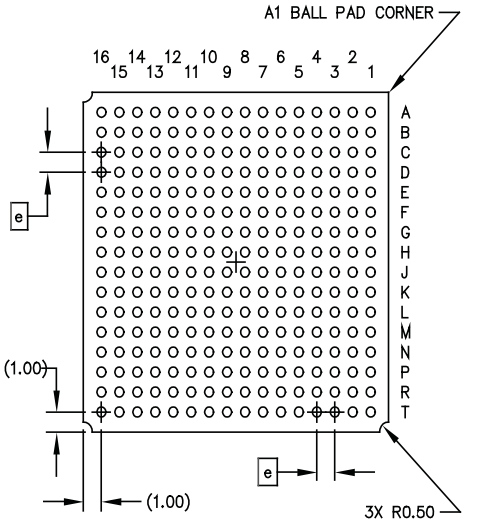
As a client, the Microsemi device can track two independent servers, and determine which one is providing the best time reference. If either the primary reference or the network between the server and client fails, the device can switch to the alternative reference without introducing a phase discontinuity. Alternatively, the client can switch to a conventional clock reference.

The solution timing recovery algorithm continuously tracks the frequency offset and phase drift between the clocks located at the server and the client nodes connected via the packet switched network. The algorithm is tolerant of lost packets, and of packet delay variation caused by packet queuing, route changes and other effects. In the event of a failure in the packet network, or the advent of severe congestion preventing or seriously delaying the delivery of timing packets, the device will put the recovered clocks into holdover until the flow of timing packets is restored. When the device is in holdover mode the drift of the local oscillator directly affects the accuracy of the output clocks.

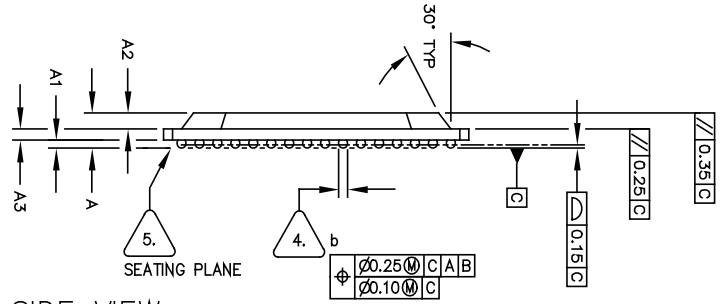
When using ToP technology, the device is designed to meet ANSI standard T1.101 and ITU-T standards G.823 and G.824 for synchronization distribution. It maintains a mean frequency accuracy of better than ±10 ppb and time alignment of better than ±1 μs when operated over a suitable network.



TOP VIEW



BOTTOM VIEW



SIDE VIEW

DIMENSION	MIN	Nom	MAX
A	1.55	1.76	1.97
A1	0.30	0.40	0.50
A2	0.75	0.80	0.85
A3	0.50	0.56	0.62
D	16.80	17.00	17.20
D1	14.95	15.00	15.35
E	16.80	17.00	17.20
E1	14.95	15.00	15.35
b	0.40	0.50	0.60
e		1.00	
N		256	
Conforms to JEDEC MS-034/B except dimension 'b JEDEC "b" 0.6 +/- 0.1mm			

5. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

4. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL, DIAMETER PARALLEL TO PRIMARY DATUM C.

3. N IS NUMBER OF SOLDER BALLS

2. NOT TO SCALE.

1. ALL DIMENSIONS IN MM AND TOLERANCES CONFORM TO. ASME Y14.5M-1994.

NOTES: UNLESS OTHERWISE SPECIFIED

ISSUE	1	2		
ACN	CDCA			
DATE	24Aug06			
APPRD.				

Microsemi

Previous package codes

N/A

Package Code GK

Package Outline for 256ball, 17x17mm, 1.0mm Pitch TEBGA-2

119347

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TECHNICAL DOCUMENTATION – NOT FOR RESALE

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- Поставка более 17-ти миллионов наименований электронных компонентов;
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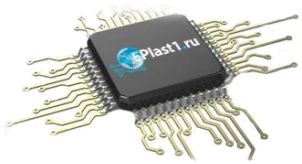
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

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