

## ADD-A-PAK Generation VII Power Modules Thyristor/Thyristor, 105 A



ADD-A-PAK

PRODUCT SUMMARY	
$I_{T(AV)}$	105 A
Type	Modules - Thyristor, Standard

### MECHANICAL DESCRIPTION

The ADD-A-PAK generation VII, new generation of ADD-A-PAK module, combines the excellent thermal performances obtained by the usage of exposed direct bonded copper substrate, with advanced compact simple package solution and simplified internal structure with minimized number of interfaces.

### FEATURES

- High voltage
- Industrial standard package
- UL approved file E78996
- Low thermal resistance
- Designed and qualified for industrial level
- Material categorization: For definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT

### BENEFITS

- Excellent thermal performances obtained by the usage of exposed direct bonded copper substrate
- Up to 1600 V
- High surge capability
- Easy mounting on heatsink

### ELECTRICAL DESCRIPTION

These modules are intended for general purpose high voltage applications such as high voltage regulated power supplies, lighting circuits, temperature and motor speed control circuits, UPS and battery charger.

MAJOR RATINGS AND CHARACTERISTICS			
SYMBOL	CHARACTERISTICS	VALUES	UNITS
$I_{T(AV)}$	85 °C	105	A
$I_{T(RMS)}$		165	
$I_{TSM}$	50 Hz	2000	
	60 Hz	2094	
$I^2t$	50 Hz	20	kA <sup>2</sup> s
	60 Hz	18.26	
$I^2\sqrt{t}$		200	kA <sup>2</sup> √s
$V_{RRM}$	Range	400 to 1600	V
$T_{Stg}$		-40 to 130	°C
$T_J$		-40 to 130	°C



**ELECTRICAL SPECIFICATIONS**

VOLTAGE RATINGS					
TYPE NUMBER	VOLTAGE CODE	V <sub>RRM</sub> , MAXIMUM REPETITIVE PEAK REVERSE VOLTAGE V	V <sub>RSM</sub> , MAXIMUM NON-REPETITIVE PEAK REVERSE VOLTAGE V	V <sub>DRM</sub> , MAXIMUM REPETITIVE PEAK OFF-STATE VOLTAGE, GATE OPEN CIRCUIT V	I <sub>RRM</sub> , I <sub>DRM</sub> AT 130 °C mA
VS-VSK.105	04	400	500	400	15
	08	800	900	800	
	12	1200	1300	1200	
	16	1600	1700	1600	

ON-STATE CONDUCTION						
PARAMETER	SYMBOL	TEST CONDITIONS			VALUES	UNITS
Maximum average on-state current	I <sub>T(AV)</sub>	180° conduction, half sine wave, T <sub>C</sub> = 85 °C			105	A
Maximum continuous RMS on-state current	I <sub>T(RMS)</sub>	DC			165	
		T <sub>C</sub>			78	°C
Maximum peak, one-cycle non-repetitive on-state current	I <sub>TSM</sub>	t = 10 ms	No voltage reappplied	Sinusoidal half wave, initial T <sub>J</sub> = T <sub>J</sub> maximum	2000	A
		t = 8.3 ms			2094	
		t = 10 ms	100 % V <sub>RRM</sub> reappplied		1682	
		t = 8.3 ms			1760	
Maximum I <sup>2</sup> t for fusing	I <sup>2</sup> t	t = 10 ms	No voltage reappplied	Initial T <sub>J</sub> = T <sub>J</sub> maximum	20	kA <sup>2</sup> s
		t = 8.3 ms			18.26	
		t = 10 ms	100 % V <sub>RRM</sub> reappplied		14.14	
		t = 8.3 ms			12.91	
Maximum I <sup>2</sup> √t for fusing	I <sup>2</sup> √t (1)	t = 0.1 ms to 10 ms, no voltage reappplied T <sub>J</sub> = T <sub>J</sub> maximum			200	kA <sup>2</sup> √s
Maximum value of threshold voltage	V <sub>T(TO)</sub> (2)	Low level (3)	T <sub>J</sub> = T <sub>J</sub> maximum		0.98	V
		High level (4)			1.12	
Maximum value of on-state slope resistance	r <sub>t</sub> (2)	Low level (3)	T <sub>J</sub> = T <sub>J</sub> maximum		2.7	mΩ
		High level (4)			2.34	
Maximum on-state voltage drop	V <sub>TM</sub>	I <sub>TM</sub> = π × I <sub>T(AV)</sub>	T <sub>J</sub> = 25 °C		1.8	V
Maximum non-repetitive rate of rise of turned on current	dI/dt	T <sub>J</sub> = 25 °C, from 0.67 V <sub>DRM</sub> , I <sub>TM</sub> = π × I <sub>T(AV)</sub> , I <sub>g</sub> = 500 mA, t <sub>r</sub> < 0.5 μs, t <sub>p</sub> > 6 μs			150	A/μs
Maximum holding current	I <sub>H</sub>	T <sub>J</sub> = 25 °C, anode supply = 6 V, resistive load, gate open circuit			250	mA
Maximum latching current	I <sub>L</sub>	T <sub>J</sub> = 25 °C, anode supply = 6 V, resistive load			400	

**Notes**

- (1) I<sup>2</sup>t for time t<sub>x</sub> = I<sup>2</sup>√t × √t<sub>x</sub>
- (2) Average power = V<sub>T(TO)</sub> × I<sub>T(AV)</sub> + r<sub>t</sub> × (I<sub>T(RMS)</sub>)<sup>2</sup>
- (3) 16.7 % × π × I<sub>AV</sub> < I < π × I<sub>AV</sub>
- (4) I > π × I<sub>AV</sub>



TRIGGERING					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum peak gate power	$P_{GM}$			12	W
Maximum average gate power	$P_{G(AV)}$			3.0	
Maximum peak gate current	$I_{GM}$			3.0	A
Maximum peak negative gate voltage	$-V_{GM}$			10	V
Maximum gate voltage required to trigger	$V_{GT}$	$T_J = -40\text{ °C}$	Anode supply = 6 V resistive load	4.0	
		$T_J = 25\text{ °C}$		2.5	
		$T_J = 125\text{ °C}$		1.7	
Maximum gate current required to trigger	$I_{GT}$	$T_J = -40\text{ °C}$	Anode supply = 6 V resistive load	270	mA
		$T_J = 25\text{ °C}$		150	
		$T_J = 125\text{ °C}$		80	
Maximum gate voltage that will not trigger	$V_{GD}$	$T_J = 125\text{ °C}$ , rated $V_{DRM}$ applied		0.25	V
Maximum gate current that will not trigger	$I_{GD}$	$T_J = 125\text{ °C}$ , rated $V_{DRM}$ applied		6	mA

BLOCKING					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum peak reverse and off-state leakage current at $V_{RRM}$ , $V_{DRM}$	$I_{RRM}$ , $I_{DRM}$	$T_J = 130\text{ °C}$ , gate open circuit		20	mA
Maximum RMS insulation voltage	$V_{INS}$	50 Hz		3000 (1 min) 3600 (1 s)	V
Maximum critical rate of rise of off-state voltage	$dV/dt$	$T_J = 130\text{ °C}$ , linear to $0.67 V_{DRM}$		1000	V/ $\mu$ s

THERMAL AND MECHANICAL SPECIFICATIONS						
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS	
Junction operating and storage temperature range	$T_J, T_{Stg}$			-40 to 130	°C	
Maximum internal thermal resistance, junction to case per leg	$R_{thJC}$	DC operation		0.22	°C/W	
Typical thermal resistance, case to heatsink per module	$R_{thCS}$	Mounting surface flat, smooth and greased		0.1		
Mounting torque $\pm 10\%$	to heatsink	A mounting compound is recommended and the torque should be rechecked after a period of 3 hours to allow for the spread of the compound.		4	Nm	
	busbar			3		
Approximate weight					75	g
					2.7	oz.
Case style			JEDEC®	AAP GEN VII (TO-240AA)		

$\Delta R$ CONDUCTION PER JUNCTION											
DEVICES	SINE HALF WAVE CONDUCTION					RECTANGULAR WAVE CONDUCTION					UNITS
	180°	120°	90°	60°	30°	180°	120°	90°	60°	30°	
VSK.105..	0.04	0.048	0.063	0.085	0.125	0.033	0.052	0.067	0.088	0.127	°C/W

**Note**

- Table shows the increment of thermal resistance  $R_{thJC}$  when devices operate at different conduction angles than DC



Fig. 1 - Current Ratings Characteristics



Fig. 4 - On-State Power Loss Characteristics



Fig. 2 - Current Ratings Characteristics

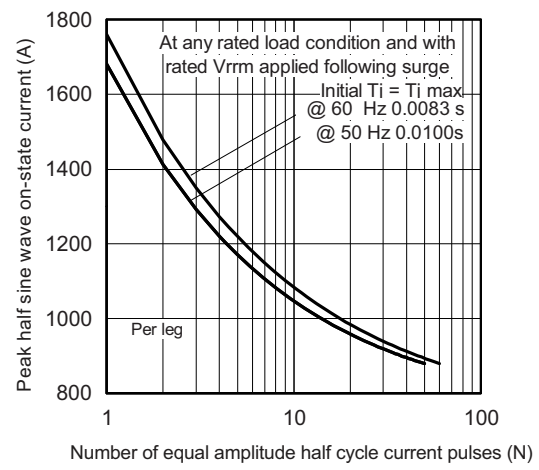


Fig. 5 - Maximum Non-Repetitive Surge Current



Fig. 3 - On-State Power Loss Characteristics



Fig. 6 - Maximum Non-Repetitive Surge Current



Fig. 7 - On-State Power Loss Characteristics



Fig. 8 - On-State Power Loss Characteristics



Fig. 9 - On-State Voltage Characteristics



Fig. 10 - Thermal Impedance  $Z_{thJC}$  Characteristics



Fig. 11 - Gate Characteristics

## ORDERING INFORMATION TABLE

Device code	<b>VS-VS</b>	<b>K</b>	<b>U</b>	<b>105</b>	<b>/</b>	<b>16</b>
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1    
 2    
 3    
 4    
 5

- 1 - Vishay Semiconductors product
- 2 - Module type
- 3 - Circuit configuration (see Circuit Configuration table)
- 4 - Current code (105 A)
- 5 - Voltage code (see Voltage Ratings table)

### Note

- To order the optional hardware go to [www.vishay.com/doc?95172](http://www.vishay.com/doc?95172)



CIRCUIT CONFIGURATION		
CIRCUIT DESCRIPTION	CIRCUIT CONFIGURATION CODE	CIRCUIT DRAWING
Two SCRs common cathodes	U	<p>VSKU</p>
Two SCRs common anodes	V	<p>VSKV</p>
LINKS TO RELATED DOCUMENTS		
Dimensions	<a href="http://www.vishay.com/doc?95368">www.vishay.com/doc?95368</a>	

## ADD-A-PAK Generation VII - Thyristor

**DIMENSIONS** in millimeters (inches)







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#### Как с нами связаться

**Телефон:** 8 (812) 309 58 32 (многоканальный)

**Факс:** 8 (812) 320-02-42

**Электронная почта:** [org@eplast1.ru](mailto:org@eplast1.ru)

**Адрес:** 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.