**MAXIM**

# 1% Accurate, Quad-/Hex-/Octal-Voltage µP Supervisors

## General Description

The MAX16060/MAX16061/MAX16062 are 1% accurate, quad-/hex-/octal-voltage µP supervisors in a small thin QFN package. These devices provide supervisory functions for complex multivoltage systems. The MAX16060 monitors four voltages, the MAX16061 monitors six voltages, and the MAX16062 monitors eight voltages.

These devices offer independent outputs for each monitored voltage along with a reset output that asserts whenever any of the monitored voltages fall below their respective thresholds (down to 0.4V) or the manual reset input is asserted. The reset output remains asserted for the reset timeout after all voltages are above their respective thresholds and the manual reset input is deasserted. The minimum reset timeout is internally set to 140ms or can be adjusted with an external capacitor.

All open-drain outputs have internal 30µA pullups that eliminate the need for external pullup resistors. However, each output can be driven with an external voltage up to 5.5V. Other features offered include a manual reset input, a tolerance pin for selecting 5% or 10% input thresholds, and a margin enable function for deasserting the outputs during margin testing.

An additional feature is a watchdog timer that asserts $\overline{RESET}$ when the watchdog timeout period (1.6s typ) is exceeded. The watchdog timer can be disabled by leaving WDI unconnected.

These devices are offered in 16-, 20-, and 24-pin thin QFN packages (4mm x 4mm) and are fully specified from -40°C to +125°C.

## Features

♦ **Fixed Thresholds for 3.3V, 2.5V, and 1.8V Systems**
♦ **Adjustable Thresholds Monitor Low Voltages (Down to 0.4V)**
♦ **1% Accurate over Temperature**
♦ **Open-Drain Outputs with Internal Pullups Reduce the Number of External Components**
♦ **Fixed 140ms (min) or Capacitor-Adjustable Reset Timeout**
♦ **Manual Reset, Margin Enable, and Tolerance Select Inputs**
♦ **Watchdog Timer**
   **1.6s (typ) Timeout Period**
   **54s Startup Delay After Reset**
♦ **Monitors Four (MAX16060), Six (MAX16061), or Eight (MAX16062) Voltages**
♦ **RESET Output Indicates All Voltages Present**
♦ **Independent Voltage Monitors**
♦ **Guaranteed to Remain Asserted Down to $V_{CC}$ = 1V**
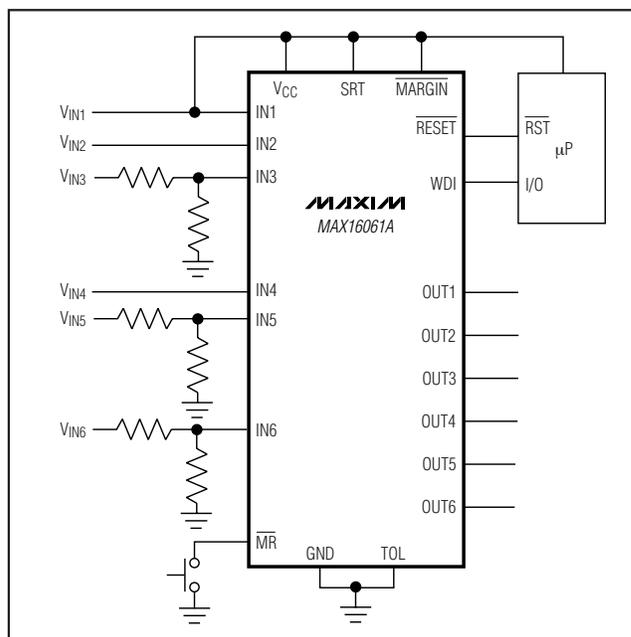♦ **Small (4mm x 4mm) Thin QFN Package**

## Applications

| | |
|---|---|
| Storage Equipment | Multivoltage ASICs |
| Servers | Automotive |
| Networking/Telecommunication Equipment | |

## Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE |
|---|---|---|
| **MAX16060_TE+** | -40°C to +125°C | 16 TQFN-EP* |
| **MAX16061_TP+** | -40°C to +125°C | 20 TQFN-EP* |
| **MAX16062_TG+** | -40°C to +125°C | 24 TQFN-EP* |

**Note:** The "_" is a placeholder for the input voltage threshold. See Table 1. The MAX16060/MAX16061/MAX16062 are available in factory-preset thresholds/configuration combinations. Choose the desired combination and complete part number from Table 1.
+Denotes a lead-free package.
For tape-and-reel, add a "T" after the "+." Tape-and-reel are offered in 2.5k increments.
*EP = Exposed pad.

## Typical Operating Circuit



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*For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.*

**MAX16060/MAX16061/MAX16062**

## ABSOLUTE MAXIMUM RATINGS

V$_{CC}$, OUT_, IN_, $\overline{\text{RESET}}$ to GND ..............................-0.3V to +6V
TOL, MARGIN, $\overline{\text{MR}}$, SRT, WDI to GND ...........-0.3V to V$_{CC}$ + 0.3
Input/Output Current ($\overline{\text{RESET}}$, MARGIN,
    SRT, $\overline{\text{MR}}$, TOL, OUT_, WDI).........................................±20mA
Continuous Power Dissipation (T$_A$ = +70°C)
    16-Pin TQFN (derate 16.9mW/°C above +70°C) ......1349mW
    20-Pin TQFN (derate 16.9mW/°C above +70°C) ......1355mW
    24-Pin TQFN (derate 16.9mW/°C above +70°C) ......1666mW

Operating Temperature Range .........................-40°C to +125°C
Junction Temperature  ....................................................+150°C
Storage Temperature Range .............................-65°C to +150°C
Lead Temperature (soldering, 10s) .................................+300°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## ELECTRICAL CHARACTERISTICS

(V$_{CC}$ = 2.0V to 5.5V, T$_A$ = -40°C to +125°C, unless otherwise specified. Typical values are at V$_{CC}$ = 3.3V, T$_A$ = +25°C.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Operating Voltage Range | V$_{CC}$ | (Note 2) | 1.0 | | 5.5 | V |
| Supply Current (Note 3) | I$_{CC}$ | V$_{CC}$ = 3.3V, OUT_, $\overline{\text{RESET}}$ not asserted | | 45 | 65 | µA |
| | | V$_{CC}$ = 5V, OUT_, $\overline{\text{RESET}}$ not asserted | | 50 | 70 | |
| UVLO (Undervoltage Lockout) | V$_{UVLO}$ | V$_{CC}$ rising | 1.62 | 1.80 | 1.98 | V |
| UVLO Hysteresis | V$_{UVLO\_HYS}$ | | | 65 | | mV |
| **IN_ (See Table 1)** | | | | | | |
| Threshold Voltages (IN_ Falling) | V$_{TH}$ | 3.3V threshold, TOL = GND | 3.069 | 3.102 | 3.135 | V |
| | | 3.3V threshold, TOL = V$_{CC}$ | 2.904 | 2.937 | 2.970 | |
| | | 2.5V threshold, TOL = GND | 2.325 | 2.350 | 2.375 | |
| | | 2.5V threshold, TOL = V$_{CC}$ | 2.200 | 2.225 | 2.250 | |
| | | 1.8V threshold, TOL = GND | 1.674 | 1.692 | 1.710 | |
| | | 1.8V threshold, TOL = V$_{CC}$ | 1.584 | 1.602 | 1.620 | |
| Adjustable Threshold (IN_ Falling) | V$_{TH}$ | TOL = GND | 0.390 | 0.394 | 0.398 | V |
| | | TOL = V$_{CC}$ | 0.369 | 0.373 | 0.377 | |
| IN_ Hysteresis | V$_{TH\_HYS}$ | IN_ rising | | 0.5 | | % V$_{TH}$ |
| IN_ Input Current | | Fixed thresholds | | 3 | 16 | µA |
| | | Adjustable thresholds | -100 | | +100 | nA |

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## ELECTRICAL CHARACTERISTICS (continued)

($V_{CC}$ = 2.0V to 5.5V, $T_A$ = -40°C to +125°C, unless otherwise specified. Typical values are at $V_{CC}$ = 3.3V, $T_A$ = +25°C.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **RESET** | | | | | | |
| Reset Timeout | $t_{RP}$ | SRT = $V_{CC}$ | 140 | 200 | 280 | ms |
| | | $C_{SRT}$ = 1500pF (Note 4) | 2.43 | 3.09 | 3.92 | |
| | | $C_{SRT}$ = 100pF | | 0.206 | | |
| | | $C_{SRT}$ = open | | 50 | | µs |
| SRT Ramp Current | $I_{SRT}$ | $V_{SRT}$ = 0V | 460 | 600 | 740 | nA |
| SRT Threshold | | | 1.173 | 1.235 | 1.293 | V |
| SRT Hysteresis | | | | 100 | | mV |
| IN_ to Reset Delay | $t_{RD}$ | IN_ falling | | 20 | | µs |
| $\overline{RESET}$ Output-Voltage Low | $V_{OL}$ | $V_{CC}$ = 3.3V, $I_{SINK}$ = 10mA, $\overline{RESET}$ asserted | | | 0.3 | V |
| | | $V_{CC}$ = 2.5V, $I_{SINK}$ = 6mA, $\overline{RESET}$ asserted | | | 0.3 | |
| | | $V_{CC}$ = 1.2V, $I_{SINK}$ = 50µA, $\overline{RESET}$ asserted | | | 0.3 | |
| $\overline{RESET}$ Output-Voltage High | $V_{OH}$ | $V_{CC}$ ≥ 2.0V, $I_{SOURCE}$ = 6µA, $\overline{RESET}$ deasserted | 0.8 x $V_{CC}$ | | | V |
| $\overline{MR}$ Input-Voltage Low | $V_{IL}$ | | | | 0.3 x $V_{CC}$ | V |
| $\overline{MR}$ Input-Voltage High | $V_{IH}$ | | 0.7 x $V_{CC}$ | | | V |
| $\overline{MR}$ Minimum Pulse Width | | | 1 | | | µs |
| $\overline{MR}$ Glitch Rejection | | | | 100 | | ns |
| $\overline{MR}$ to Reset Delay | | | | 200 | | ns |
| $\overline{MR}$ Pullup Resistance | | Pulled up to $V_{CC}$ | 12 | 20 | 28 | kΩ |
| **OUTPUTS (OUT_ )** | | | | | | |
| OUT_ Output-Voltage Low | $V_{OL}$ | $V_{CC}$ = 3.3V, $I_{SINK}$ = 2mA | | | 0.3 | V |
| | | $V_{CC}$ = 2.5V, $I_{SINK}$ = 1.2mA | | | 0.3 | |
| OUT_ Output-Voltage High | $V_{OH}$ | $V_{CC}$ ≥ 2.0V, $I_{SOURCE}$ = 6µA | 0.8 x $V_{CC}$ | | | V |
| IN_ to OUT_ Propagation Delay | $t_D$ | ($V_{TH}$ + 100mV) to ($V_{TH}$ - 100mV) | | 20 | | µs |

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## ELECTRICAL CHARACTERISTICS (continued)

($V_{CC}$ = 2.0V to 5.5V, $T_A$ = -40°C to +125°C, unless otherwise specified. Typical values are at $V_{CC}$ = 3.3V, $T_A$ = +25°C). (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **WATCHDOG TIMER** | | | | | | |
| WDI Input-Voltage Low | $V_{IL}$ | | | | 0.3 x $V_{CC}$ | V |
| WDI Input-Voltage High | $V_{IH}$ | | 0.7 x $V_{CC}$ | | | V |
| WDI Pulse Width | | (Note 5) | 50 | | | ns |
| Watchdog Timeout Period | $t_{WDI}$ | | 1.12 | 1.60 | 2.40 | s |
| Watchdog Startup Period | | | 35 | 54 | 72 | s |
| Watchdog Input Current | | $V_{WDI}$ = 0 to $V_{CC}$ (Note 5) | -1 | | +1 | µA |
| **DIGITAL LOGIC** | | | | | | |
| TOL Input-Voltage Low | $V_{IL}$ | | | | 0.3 x $V_{CC}$ | V |
| TOL Input-Voltage High | $V_{IH}$ | | 0.7 x $V_{CC}$ | | | V |
| TOL Input Current | | TOL = $V_{CC}$ | | | 100 | nA |
| $\overline{MARGIN}$ Input-Voltage Low | $V_{IL}$ | | | | 0.3 x $V_{CC}$ | V |
| $\overline{MARGIN}$ Input-Voltage High | $V_{IH}$ | | 0.7 x $V_{CC}$ | | | V |
| $\overline{MARGIN}$ Pullup Resistance | | Pulled up to $V_{CC}$ | 12 | 20 | 28 | kΩ |
| $\overline{MARGIN}$ Delay Time | $t_{MD}$ | Rising or falling (Note 6) | | 50 | | µs |

**Note 1:** Devices are tested at $T_A$ = +25°C and guaranteed by design for $T_A$ = $T_{MIN}$ to $T_{MAX}$.
**Note 2:** The outputs are guaranteed to remain asserted down to $V_{CC}$ = 1V.
**Note 3:** Measured with WDI, $\overline{MARGIN}$, and $\overline{MR}$ unconnected.
**Note 4:** The minimum and maximum specifications for this parameter are guaranteed by using the worst case of the SRT ramp current and SRT threshold specifications.
**Note 5:** Guaranteed by design and not production tested.
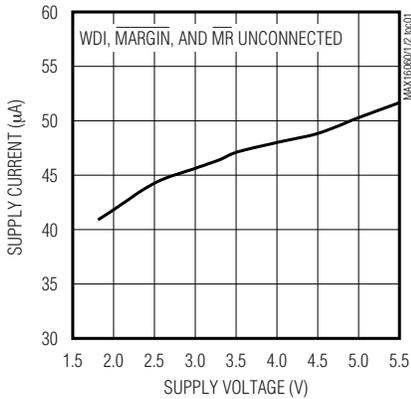**Note 6:** Amount of time required for logic to lock/unlock outputs from margin testing.

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## Typical Operating Characteristics
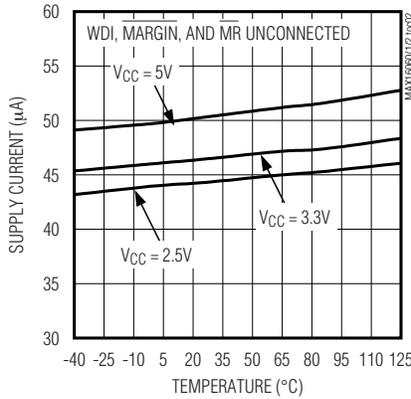
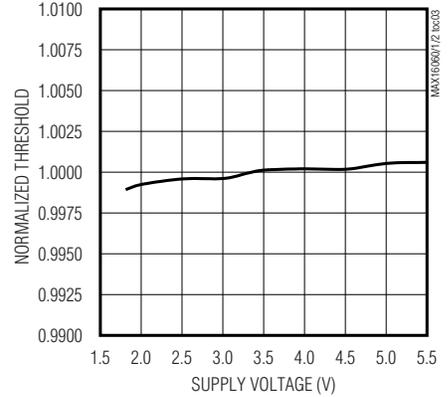($V_{CC}$ = 3.3V, $T_A$ = +25°C, unless otherwise noted.)
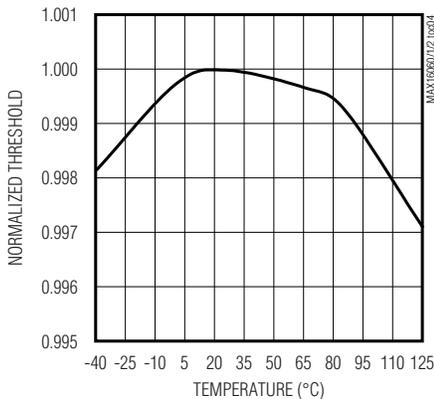
SUPPLY CURRENT vs. SUPPLY VOLTAGE
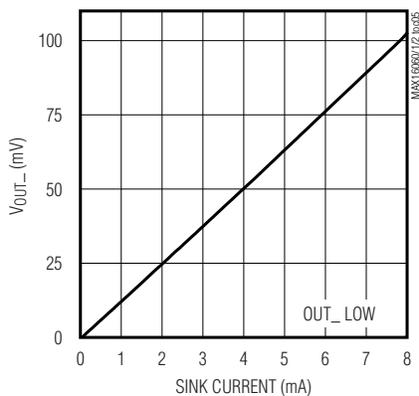


SUPPLY CURRENT vs. TEMPERATURE



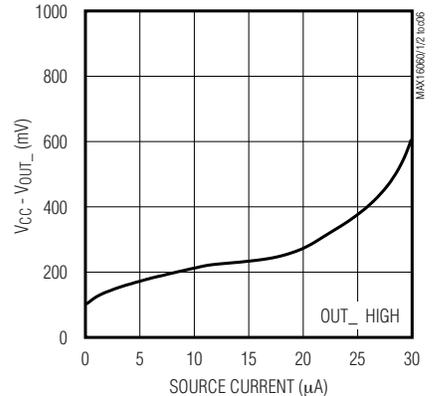NORMALIZED THRESHOLD vs. SUPPLY VOLTAGE



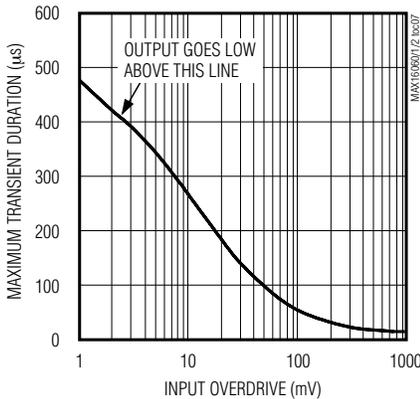NORMALIZED THRESHOLD vs. TEMPERATURE
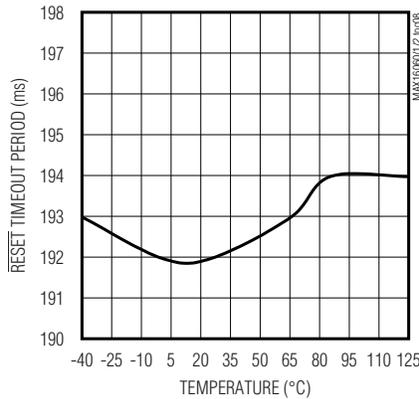


OUTPUT VOLTAGE vs. SINK CURRENT



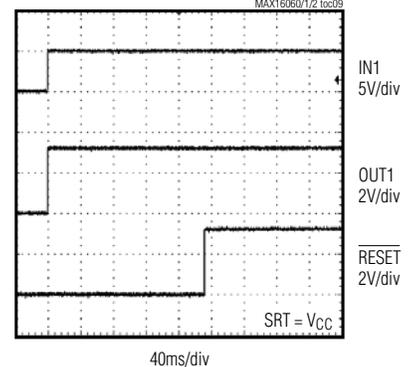OUTPUT VOLTAGE vs. SOURCE CURRENT



MAXIMUM TRANSIENT DURATION vs. INPUT OVERDRIVE
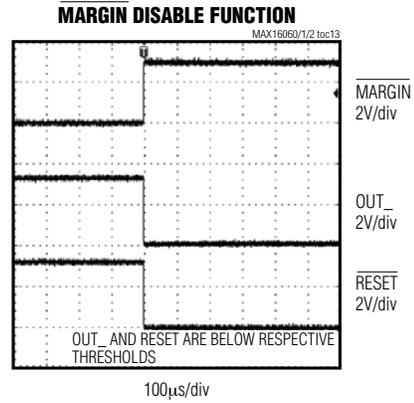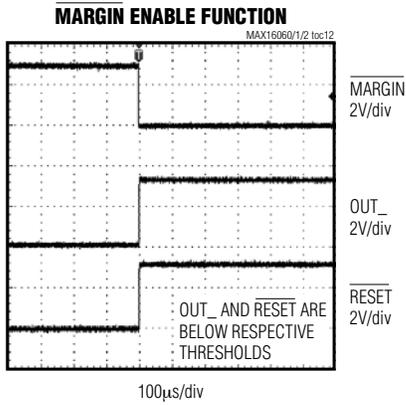


RESET TIMEOUT PERIOD vs. TEMPERATURE



RESET TIMEOUT DELAY



**MAX16060/MAX16061/MAX16062**

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(V$_{CC}$ = 3.3V, T$_A$ = +25°C, unless otherwise noted.)
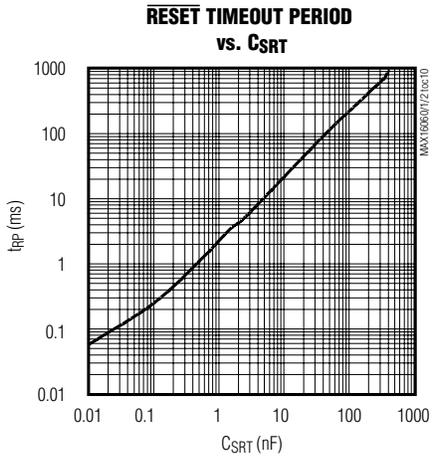
**RESET TIMEOUT PERIOD vs. C$_{SRT}$**



**WATCHDOG TIMEOUT PERIOD vs. TEMPERATURE**



**MARGIN ENABLE FUNCTION**



OUT_ AND RESET ARE BELOW RESPECTIVE THRESHOLDS

100µs/div

**MARGIN DISABLE FUNCTION**



OUT_ AND RESET ARE BELOW RESPECTIVE THRESHOLDS

100µs/div

**MAX16060/MAX16061/MAX16062**

## Pin Description (MAX16060)

| PIN | NAME | FUNCTION |
|---|---|---|
| 1 | IN3 | Monitored Input Voltage 3. See Table 1 for the input voltage threshold. |
| 2 | IN4 | Monitored Input Voltage 4. See Table 1 for the input voltage threshold. |
| 3 | WDI | Watchdog Timer Input. If WDI remains low or high for longer than the watchdog timeout period, $\overline{RESET}$ is asserted. The timer clears whenever a reset is asserted or a rising or falling edge on WDI is detected. The watchdog timer enters a startup period that allows 54s for the first transition to occur before a reset. Leave WDI unconnected to disable the watchdog timer. The WDI unconnected-state detector uses a small 400nA current. Therefore, do not connect WDI to anything that will source or sink more than 200nA. Note that the leakage current specification for most three-state drivers exceeds 200nA. |
| 4 | GND | Ground |
| 5 | V$_{CC}$ | Unmonitored Power-Supply Input |
| 6 | OUT3 | Output 3. When the voltage at IN3 falls below its threshold, OUT3 goes low and stays low until the voltage at IN3 exceeds its threshold. The open-drain output has a 30µA internal pullup to V$_{CC}$. |
| 7 | OUT4 | Output 4. When the voltage at IN4 falls below its threshold, OUT4 goes low and stays low until the voltage at IN4 exceeds its threshold. The open-drain output has a 30µA internal pullup to V$_{CC}$. |
| 8 | $\overline{MR}$ | Active-Low Manual Reset Input. Pull $\overline{MR}$ low to assert $\overline{RESET}$ low. $\overline{RESET}$ remains low for the reset timeout period after $\overline{MR}$ is deasserted. $\overline{MR}$ is pulled up to V$_{CC}$ through a 20kΩ resistor. |
| 9 | SRT | Set Reset Timeout Input. Connect a capacitor from SRT to GND to set the reset timeout period. The reset timeout period can be calculated as follows: Reset Timeout (s) = 2.06 x 10$^6$ (Ω) x C$_{SRT}$ (F). For the internal timeout period of 140ms (min), connect SRT to V$_{CC}$. |
| 10 | $\overline{MARGIN}$ | Active-Low Manual Deassert Input. Pull $\overline{MARGIN}$ low to deassert all outputs (go into high state), regardless of the voltage at any monitored input. |
| 11 | OUT2 | Output 2. When the voltage at IN2 falls below its threshold, OUT2 goes low and stays low until the voltage at IN2 exceeds its threshold. The open-drain output has a 30µA internal pullup to V$_{CC}$. |
| 12 | OUT1 | Output 1. When the voltage at IN1 falls below its threshold, OUT1 goes low and stays low until the voltage at IN1 exceeds its threshold. The open-drain output has a 30µA internal pullup to V$_{CC}$. |
| 13 | $\overline{RESET}$ | Active-Low Reset Output. $\overline{RESET}$ asserts low when any of the monitored voltages falls below its respective threshold or $\overline{MR}$ is asserted. $\overline{RESET}$ remains asserted for the reset timeout period after all monitored voltages exceed their respective thresholds and $\overline{MR}$ is deasserted. This open-drain output has a 30µA internal pullup. |
| 14 | IN1 | Monitored Input Voltage 1. See Table 1 for the input voltage threshold. |
| 15 | IN2 | Monitored Input Voltage 2. See Table 1 for the input voltage threshold. |
| 16 | TOL | Threshold Tolerance Input. Connect TOL to GND to select 5% threshold tolerance. Connect TOL to V$_{CC}$ to select 10% threshold tolerance. |
| — | EP | Exposed Pad. EP is internally connected to GND. Connect EP to the ground plane to provide a low thermal resistance path from the IC junction to the PCB. Do not use as the electrical connection to GND. |

# 1% Accurate, Quad-/Hex-/Octal-Voltage µP Supervisors

| PIN | NAME | FUNCTION |
|-----|------|----------|
| 1 | IN4 | Monitored Input Voltage 4. See Table 1 for the input voltage threshold. |
| 2 | IN5 | Monitored Input Voltage 5. See Table 1 for the input voltage threshold. |
| 3 | IN6 | Monitored Input Voltage 6. See Table 1 for the input voltage threshold. |
| 4 | WDI | Watchdog Timer Input. If WDI remains low or high for longer than the watchdog timeout period, $\overline{RESET}$ is asserted and the timer is cleared. The timer also clears whenever a reset is asserted or a rising or falling edge on WDI is detected. The watchdog timer enters a startup period that allows 54s for the first transition to occur before a reset. Leave WDI unconnected to disable the watchdog timer. The WDI unconnected-state detector uses a small 400nA current. Therefore, do not connect WDI to anything that will source or sink more than 200nA. Note that the leakage current specification for most three-state drivers exceeds 200nA. |
| 5 | GND | Ground |
| 6 | V$_{CC}$ | Unmonitored Power-Supply Input |
| 7 | OUT4 | Output 4. When the voltage at IN4 falls below its threshold, OUT4 goes low and stays low until the voltage at IN4 exceeds its threshold. The open-drain output has a 30µA internal pullup to V$_{CC}$. |
| 8 | OUT5 | Output 5. When the voltage at IN5 falls below its threshold, OUT5 goes low and stays low until the voltage at IN5 exceeds its threshold. The open-drain output has a 30µA internal pullup to V$_{CC}$. |
| 9 | OUT6 | Output 6. When the voltage at IN6 falls below its threshold, OUT6 goes low and stays low until the voltage at IN6 exceeds its threshold. The open-drain output has a 30µA internal pullup to V$_{CC}$. |
| 10 | $\overline{MR}$ | Active-Low Manual Reset Input. Pull $\overline{MR}$ low to assert $\overline{RESET}$ low. $\overline{RESET}$ remains low for the reset timeout period after $\overline{MR}$ is deasserted. $\overline{MR}$ is pulled up to V$_{CC}$ through a 20kΩ resistor. |
| 11 | SRT | Set Reset Timeout Input. Connect a capacitor from SRT to GND to set the reset timeout period. The reset timeout period can be calculated as follows: Reset Timeout (s) = 2.06 x 10$^6$ (Ω) x C$_{SRT}$ (F). For the internal timeout period of 140ms (min), connect SRT to V$_{CC}$. |
| 12 | $\overline{MARGIN}$ | Manual Deassert Input. Pull $\overline{MARGIN}$ low to deassert all outputs (go into high state), regardless of the voltage at any monitored input. |
| 13 | OUT3 | Output 3. When the voltage at IN3 falls below its threshold, OUT3 goes low and stays low until the voltage at IN3 exceeds its threshold. The open-drain output has a 30µA internal pullup to V$_{CC}$. |
| 14 | OUT2 | Output 2. When the voltage at IN2 falls below its threshold, OUT2 goes low and stays low until the voltage at IN2 exceeds its threshold. The open-drain output has a 30µA internal pullup to V$_{CC}$. |
| 15 | OUT1 | Output 1. When the voltage at IN1 falls below its threshold, OUT1 goes low and stays low until the voltage at IN1 exceeds its threshold. The open-drain output has a 30µA internal pullup to V$_{CC}$. |
| 16 | $\overline{RESET}$ | Active-Low Reset Output. $\overline{RESET}$ asserts low when any of the monitored voltages falls below its respective threshold or $\overline{MR}$ is asserted. $\overline{RESET}$ remains asserted for the reset timeout period after all monitored voltages exceed their respective thresholds and $\overline{MR}$ is deasserted. This open-drain output has a 30µA internal pullup. |
| 17 | IN1 | Monitored Input Voltage 1. See Table 1 for the input voltage threshold. |
| 18 | IN2 | Monitored Input Voltage 2. See Table 1 for the input voltage threshold. |
| 19 | IN3 | Monitored Input Voltage 3. See Table 1 for the input voltage threshold. |
| 20 | TOL | Threshold Tolerance Input. Connect TOL to GND to select 5% threshold tolerance. Connect TOL to V$_{CC}$ to select 10% threshold tolerance. |
| — | EP | Exposed Pad. EP is internally connected to GND. Connect EP to the ground plane to provide a low thermal resistance path from the IC junction to the PCB. Do not use as the electrical connection to GND. |

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### Pin Description (MAX16062)

| PIN | NAME | FUNCTION |
|---|---|---|
| 1 | IN5 | Monitored Input Voltage 5. See Table 1 for the input voltage threshold. |
| 2 | IN6 | Monitored Input Voltage 6. See Table 1 for the input voltage threshold. |
| 3 | IN7 | Monitored Input Voltage 7. See Table 1 for the input voltage threshold. |
| 4 | IN8 | Monitored Input Voltage 8. See Table 1 for the input voltage threshold. |
| 5 | WDI | Watchdog Timer Input. If WDI remains low or high for longer than the watchdog timeout period, $\overline{RESET}$ is asserted and the timer is cleared. The timer also clears whenever a reset is asserted or a rising or falling edge on WDI is detected. The watchdog timer enters a startup period that allows 54s for the first transition to occur before a reset. Leave WDI unconnected to disable the watchdog timer. The WDI unconnected state detector uses a small 400nA current. Therefore, do not connect WDI to anything that will source or sink more than 200nA. Note that the leakage current specification for most three-state drivers exceeds 200nA. |
| 6 | GND | Ground |
| 7 | $V_{CC}$ | Unmonitored Power-Supply Input |
| 8 | OUT5 | Output 5. When the voltage at IN5 falls below its threshold, OUT5 goes low and stays low until the voltage at IN5 exceeds its threshold. The open-drain output has a 30µA internal pullup to $V_{CC}$. |
| 9 | OUT6 | Output 6. When the voltage at IN6 falls below its threshold, OUT6 goes low and stays low until the voltage at IN6 exceeds its threshold. The open-drain output has a 30µA internal pullup to $V_{CC}$. |
| 10 | OUT7 | Output 7. When the voltage at IN7 falls below its threshold, OUT7 goes low and stays low until the voltage at IN7 exceeds its threshold. The open-drain output has a 30µA internal pullup to $V_{CC}$. |
| 11 | OUT8 | Output 8. When the voltage at IN8 falls below its threshold, OUT8 goes low and stays low until the voltage at IN8 exceeds its threshold. The open-drain output has a 30µA internal pullup to $V_{CC}$. |
| 12 | $\overline{MR}$ | Active-Low Manual Reset Input. Pull $\overline{MR}$ low to assert $\overline{RESET}$ low. $\overline{RESET}$ remains low for the reset timeout period after $\overline{MR}$ is deasserted. $\overline{MR}$ is pulled up to $V_{CC}$ through a 20kΩ resistor. |
| 13 | SRT | Set Reset Timeout Input. Connect a capacitor from SRT to GND to set the reset timeout period. The reset timeout period can be calculated as follows:<br>Reset Timeout (s) = $2.06 \times 10^6 (\Omega) \times C_{SRT}$ (F). For the internal timeout period of 140ms (min), connect SRT to $V_{CC}$. |
| 14 | $\overline{MARGIN}$ | Margin Disable Input. Pull $\overline{MARGIN}$ low to deassert all outputs (go into high state), regardless of the voltage at any monitored input. |
| 15 | OUT4 | Output 4. When the voltage at IN4 falls below its threshold, OUT4 goes low and stays low until the voltage at IN4 exceeds its threshold. The open-drain output has a 30µA internal pullup to $V_{CC}$. |
| 16 | OUT3 | Output 3. When the voltage at IN3 falls below its threshold, OUT3 goes low and stays low until the voltage at IN3 exceeds its threshold. The open-drain output has a 30µA internal pullup to $V_{CC}$. |
| 17 | OUT2 | Output 2. When the voltage at IN2 falls below its threshold, OUT2 goes low and stays low until the voltage at IN2 exceeds its threshold. The open-drain output has a 30µA internal pullup to $V_{CC}$. |
| 18 | OUT1 | Output 1. When the voltage at IN1 falls below its threshold, OUT1 goes low and stays low until the voltage at IN1 exceeds its threshold. The open-drain output has a 30µA internal pullup to $V_{CC}$. |
| 19 | $\overline{RESET}$ | Active-Low Reset Output. $\overline{RESET}$ asserts low when any of the monitored voltages falls below its respective threshold or $\overline{MR}$ is asserted. $\overline{RESET}$ remains asserted for the reset timeout period after all monitored voltages exceed their respective thresholds and $\overline{MR}$ is deasserted. This open-drain output has a 30µA internal pullup. |
| 20 | IN1 | Monitored Input Voltage 1. See Table 1 for the input voltage threshold. |
| 21 | IN2 | Monitored Input Voltage 2. See Table 1 for the input voltage threshold. |
| 22 | IN3 | Monitored Input Voltage 3. See Table 1 for the input voltage threshold. |
| 23 | IN4 | Monitored Input Voltage 4. See Table 1 for the input voltage threshold. |
| 24 | TOL | Threshold Tolerance Input. Connect TOL to GND to select 5% threshold tolerance. Connect TOL to $V_{CC}$ to select 10% threshold tolerance. |
| — | EP | Exposed Pad. EP is internally connected to GND. Connect EP to the ground plane to provide a low thermal resistance path from the IC junction to the PCB. Do not use as the electrical connection to GND. |

# 1% Accurate, Quad-/Hex-/Octal-Voltage µP Supervisors

## Table 1. Input-Voltage-Threshold Selector

| PART | IN1 | IN2 | IN3 | IN4 | IN5 | IN6 | IN7 | IN8 |
|------|-----|-----|-----|-----|-----|-----|-----|-----|
| MAX16060A | 3.3 | 2.5 | ADJ | 1.8 | — | — | — | — |
| MAX16060B | 3.3 | ADJ | ADJ | 1.8 | — | — | — | — |
| MAX16060C | ADJ | 2.5 | ADJ | 1.8 | — | — | — | — |
| MAX16060D | 3.3 | 2.5 | ADJ | ADJ | — | — | — | — |
| MAX16060E | ADJ | ADJ | ADJ | ADJ | — | — | — | — |
| MAX16061A | 3.3 | 2.5 | ADJ | 1.8 | ADJ | ADJ | — | — |
| MAX16061B | 3.3 | ADJ | ADJ | 1.8 | ADJ | ADJ | — | — |
| MAX16061C | 3.3 | 2.5 | ADJ | ADJ | ADJ | ADJ | — | — |
| MAX16061D | ADJ | 2.5 | ADJ | 1.8 | ADJ | ADJ | — | — |
| MAX16061E | ADJ | ADJ | ADJ | ADJ | ADJ | ADJ | — | — |
| MAX16062A | 3.3 | 2.5 | ADJ | 1.8 | ADJ | ADJ | ADJ | ADJ |
| MAX16062B | 3.3 | ADJ | ADJ | 1.8 | ADJ | ADJ | ADJ | ADJ |
| MAX16062C | 3.3 | 2.5 | ADJ | ADJ | ADJ | ADJ | ADJ | ADJ |
| MAX16062D | ADJ | 2.5 | ADJ | 1.8 | ADJ | ADJ | ADJ | ADJ |
| MAX16062E | ADJ | ADJ | ADJ | ADJ | ADJ | ADJ | ADJ | ADJ |

**Note:** *Other fixed thresholds may be available. Contact factory for availability.*

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MAX16060/MAX16061/MAX16062



Figure 1. MAX16060D Functional Diagram

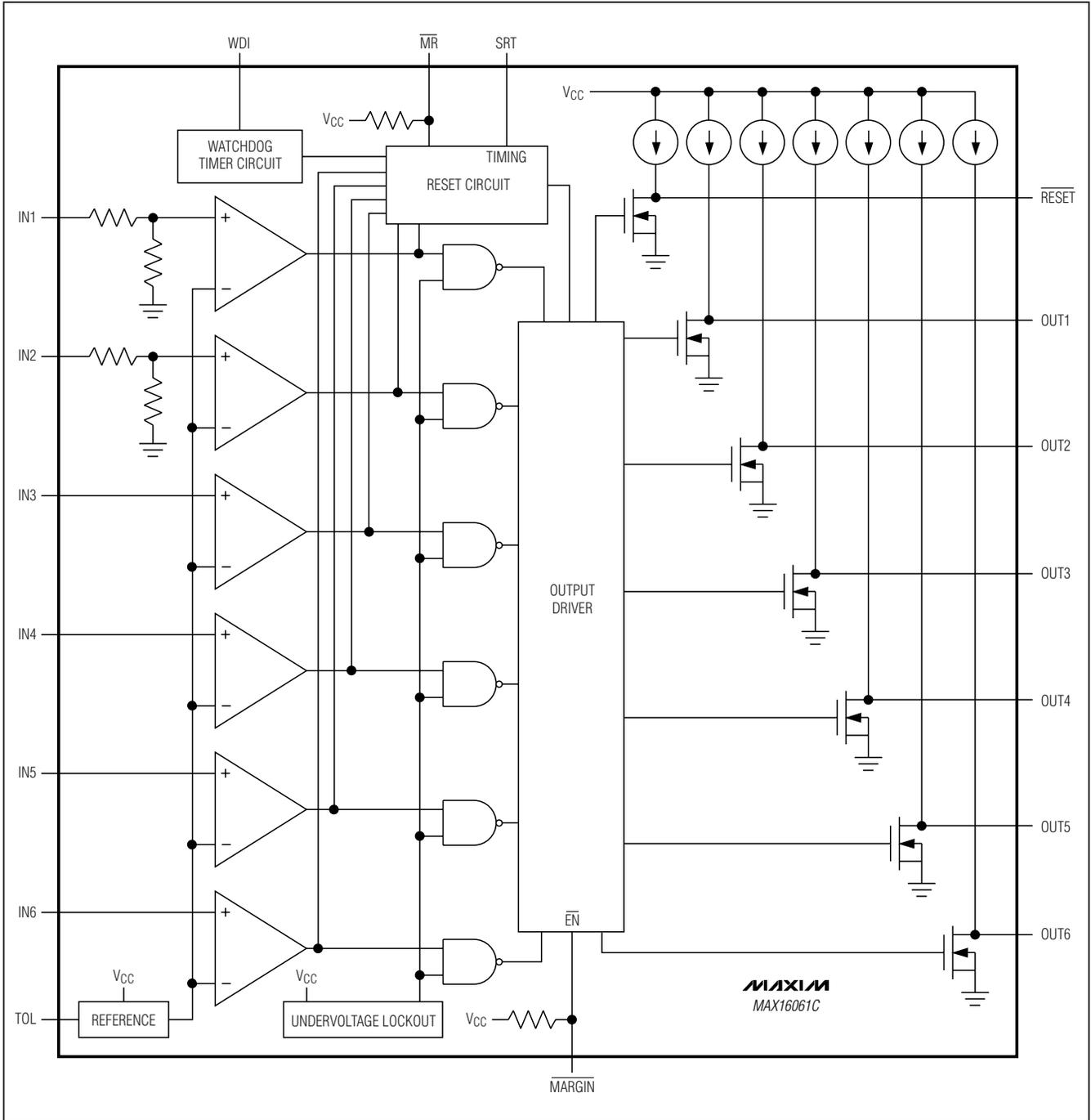# 1% Accurate, Quad-/Hex-/Octal-Voltage
# µP Supervisors

MAX16060/MAX16061/MAX16062



Figure 2. MAX16061C Functional Diagram

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# 1% Accurate, Quad-/Hex-/Octal-Voltage µP Supervisors

**MAX16060/MAX16061/MAX16062**



Figure 3. MAX16062C Functional Diagram

## Detailed Description

The MAX16060/MAX16061/MAX16062 are 1% accurate low-voltage, quad-/hex-/octal-voltage µP supervisors in a small thin QFN package. These devices provide supervisory functions for complex multivoltage systems. The MAX16060 monitors four voltages; the MAX16061 monitors six voltages; and the MAX16062 monitors eight voltages.

These supervisors offer independent outputs for each monitored voltage along with a reset output that asserts whenever any of the monitored voltages fall below their respective thresholds or the manual reset input is asserted. The reset output remains asserted for the reset timeout after all voltages are above their respective thresholds and the manual reset input is deasserted. The minimum reset timeout is internally set to 140ms or can be adjusted with an external capacitor.

All open-drain outputs have internal 30µA pullups that eliminate the need for external pullup resistors. However, each output can be driven with an external voltage up to 5.5V. Other features offered include a manual reset input, a tolerance pin for selecting 5% or 10% input thresholds, and a margin enable function for deasserting the outputs during margin testing.

An additional feature is a watchdog timer that asserts RESET when the watchdog timeout period (1.6s typ) is exceeded. The watchdog timer can be disabled by leaving WDI unconnected.

## Applications Information

### Undervoltage-Detection Circuit

The open-drain outputs of the MAX16060/ MAX16061/MAX16062 can be configured to detect an undervoltage condition. Figure 4 shows a configuration where an LED turns on when the comparator output is low, indicating an undervoltage condition. These devices can also be used in applications such as system supervisory monitoring, multivoltage level detection, and $V_{CC}$ bar-graph monitoring (Figure 5).

### Tolerance (TOL)

The MAX16060/MAX16061/MAX16062 feature a pin-selectable threshold tolerance. Connect TOL to GND to select 5% threshold tolerance. Connect TOL to $V_{CC}$ to select 10% threshold tolerance.

### Window Detection

A window detector circuit uses two inputs in the configuration shown in Figure 6. External resistors set the two threshold voltages of the window detector circuit. External logic gates create the OUT signal. The window detection width is the difference between the threshold voltages (Figure 7).
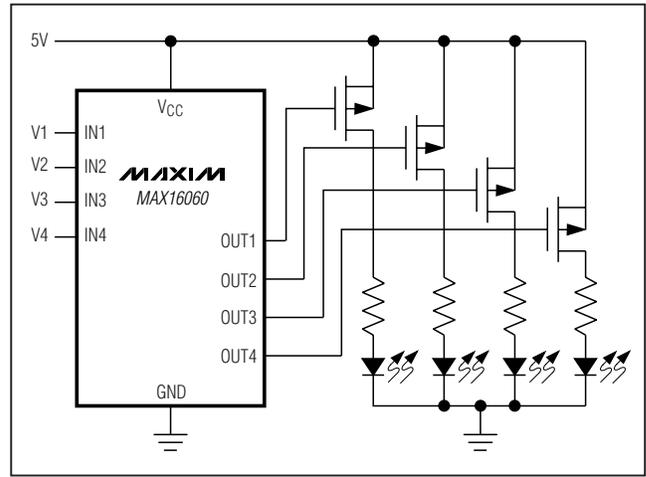


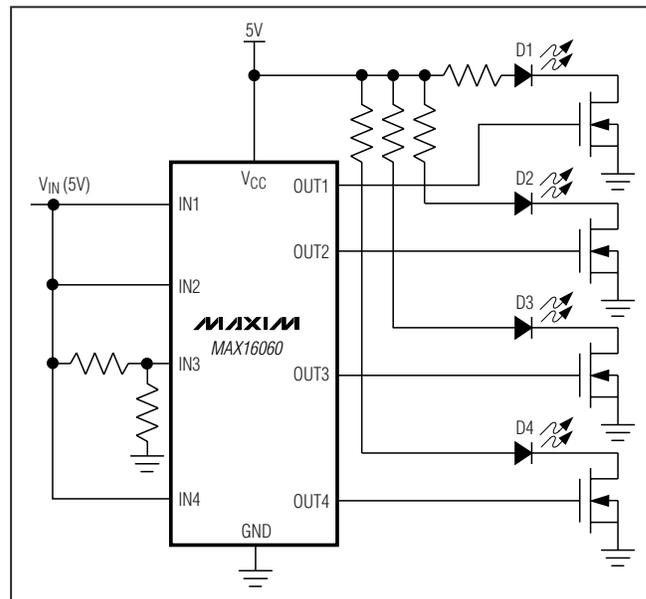Figure 4. Quad Undervoltage Detector with LED Indicators



Figure 5. $V_{CC}$ Bar-Graph Monitoring

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$$V_{TH1} = \left(1 + \frac{R1}{R2}\right)\left(V_{TH} + V_{TH\_HYS}\right)$$
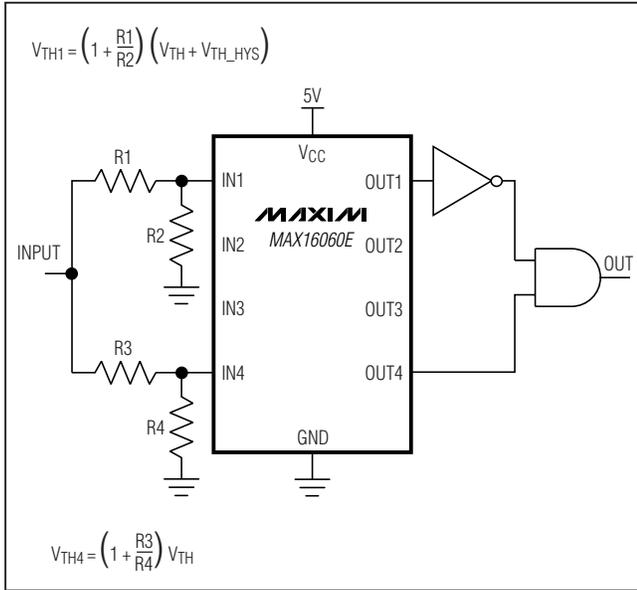


$$V_{TH4} = \left(1 + \frac{R3}{R4}\right)V_{TH}$$

Figure 6. Window Detection



Figure 7. Output Response of Window Detector Circuit



Figure 8. Setting the Adjustable Input

$$R1 = R2\left(\frac{V_{INTH}}{V_{TH}} - 1\right)$$
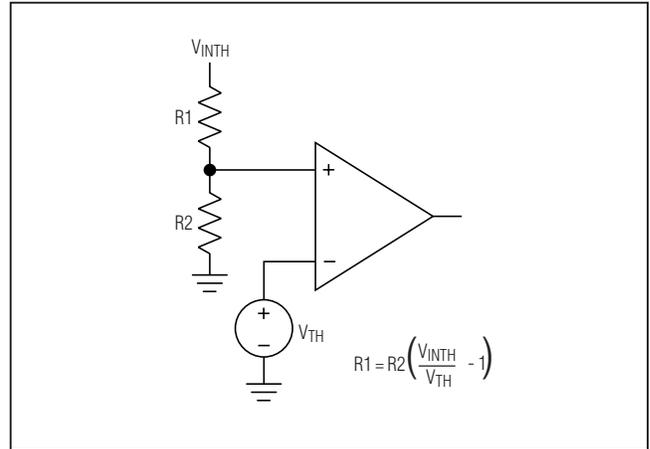
### Adjustable Input

These devices offer several monitor options with adjustable input thresholds (see Table 1). The threshold voltage at each adjustable IN_ input is typically 0.394V (TOL = GND) or 0.373V (TOL = $V_{CC}$). To monitor a voltage $V_{INTH}$, connect a resistive-divider network to the circuit as shown in Figure 8.

$$V_{INTH} = V_{TH}\left((R1/R2) + 1\right)$$

$$R1 = R2\left((V_{INTH}/V_{TH}) - 1\right)$$

Large resistors can be used to minimize current through the external resistors. For greater accuracy, use lower-value resistors.

### Unused Inputs

Connect any unused IN_ inputs to a voltage above its threshold.

### OUT_ Outputs

The OUT_ outputs go low when their respective IN_ inputs drop below their specified thresholds. The output is open drain with a 30µA internal pullup to $V_{CC}$. For many applications, no external pullup resistor is required to interface with other logic devices. An external pullup resistor to any voltage from 0 to 5.5V overrides the internal pullup if interfacing to different logic supply voltages. Internal circuitry prevents reverse current flow from the external pullup voltage to $V_{CC}$ (Figure 9).

# 1% Accurate, Quad-/Hex-/Octal-Voltage
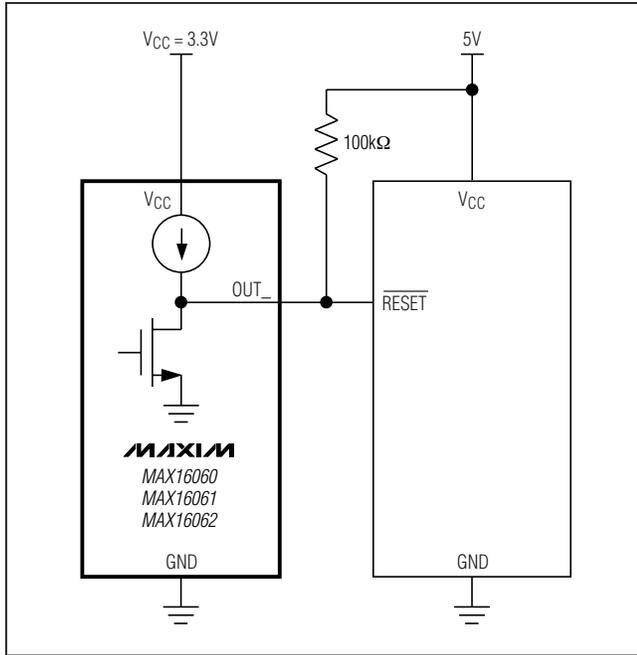# µP Supervisors



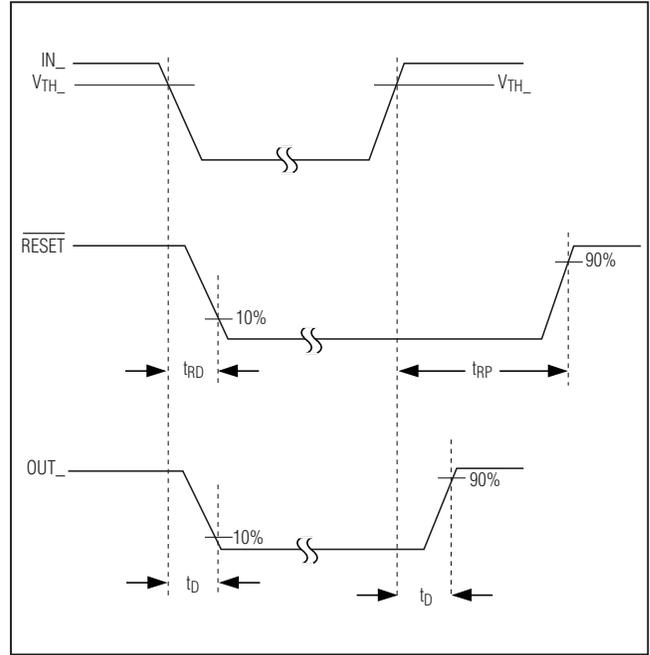Figure 9. Interfacing to a Different Logic Supply Voltage



Figure 10. Output Timing Diagram

## $\overline{RESET}$ Output

$\overline{RESET}$ asserts low when any of the monitored voltages fall below their respective thresholds or $\overline{MR}$ is asserted. $\overline{RESET}$ remains asserted for the reset timeout period after all monitored voltages exceed their respective thresholds and $\overline{MR}$ is deasserted (see Figure 10). This open-drain output has a 30µA internal pullup. An external pullup resistor to any voltage from 0 to 5.5V overrides the internal pullup if interfacing to different logic supply voltages. Internal circuitry prevents reverse current flow from the external pullup voltage to $V_{CC}$ (Figure 9).

## Reset Timeout Capacitor

The reset timeout period can be adjusted to accommodate a variety of µP applications. Adjust the reset timeout period ($t_{RP}$) by connecting a capacitor ($C_{SRT}$) between SRT and GND. Calculate the reset timeout capacitor as follows:

$$C_{SRT}(F) = \frac{t_{RP}(s) \times I_{SRT}}{V_{TH\_SRT}}$$

Connect SRT to $V_{CC}$ for a factory-programmed reset timeout of 140ms (min).

## Manual Reset Input ($\overline{MR}$)

Many µP-based products require manual reset capability, allowing the operator, a test technician, or external logic circuitry to initiate a reset. A logic-low on $\overline{MR}$ asserts $\overline{RESET}$ low. $\overline{RESET}$ remains asserted while $\overline{MR}$ is low, and during the reset timeout period (140ms min) after $\overline{MR}$ returns high. The $\overline{MR}$ input has an internal 20kΩ pullup resistor to $V_{CC}$, so it can be left unconnected if not used. $\overline{MR}$ can be driven with TTL or CMOS-logic levels, or with open-drain/collector outputs. Connect a normally open momentary switch from $\overline{MR}$ to GND to create a manual reset function. External debounce circuitry is not required. If $\overline{MR}$ is driven from long cables or if the device is used in a noisy environment, connecting a 0.1µF capacitor from $\overline{MR}$ to GND provides additional noise immunity.

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### Margin Output Disable ($\overline{MARGIN}$)

$\overline{MARGIN}$ allows system-level testing while power supplies are adjusted from their nominal voltages. Drive $\overline{MARGIN}$ low to force $\overline{RESET}$ and OUT_ high, regardless of the voltage at any monitored input. The state of each output does not change while $\overline{MARGIN}$ = GND. The watchdog timer continues to run when $\overline{MARGIN}$ is low, and if a timeout occurs, $\overline{RESET}$ will assert $t_{MD}$ after $\overline{MARGIN}$ is deasserted.

The $\overline{MARGIN}$ input is internally pulled up to $V_{CC}$. Leave $\overline{MARGIN}$ unconnected or connect to $V_{CC}$ if unused.

### Undervoltage Lockout (UVLO)

The MAX16060/MAX16061/MAX16062 feature a $V_{CC}$ undervoltage lockout (UVLO) that preserves a reset status even if $V_{CC}$ falls as low as 1V. The undervoltage lockout circuitry monitors the voltage at $V_{CC}$. If $V_{CC}$ falls below the UVLO falling threshold (typically 1.735V), $\overline{RESET}$ is asserted and all OUT_ are asserted low. This eliminates an incorrect $\overline{RESET}$ or OUT_ output state as $V_{CC}$ drops below the normal $V_{CC}$ operational voltage range of 1.98V to 5.5V.

During power-up as $V_{CC}$ rises above 1V, $\overline{RESET}$ is asserted and all OUT_ are asserted low until $V_{CC}$ exceeds the UVLO threshold. As $V_{CC}$ exceeds the UVLO threshold, all inputs are monitored and the correct output state appears at all the outputs. This also ensures that $\overline{RESET}$ and all OUT_ are in the correct state once $V_{CC}$ reaches the normal $V_{CC}$ operational range.
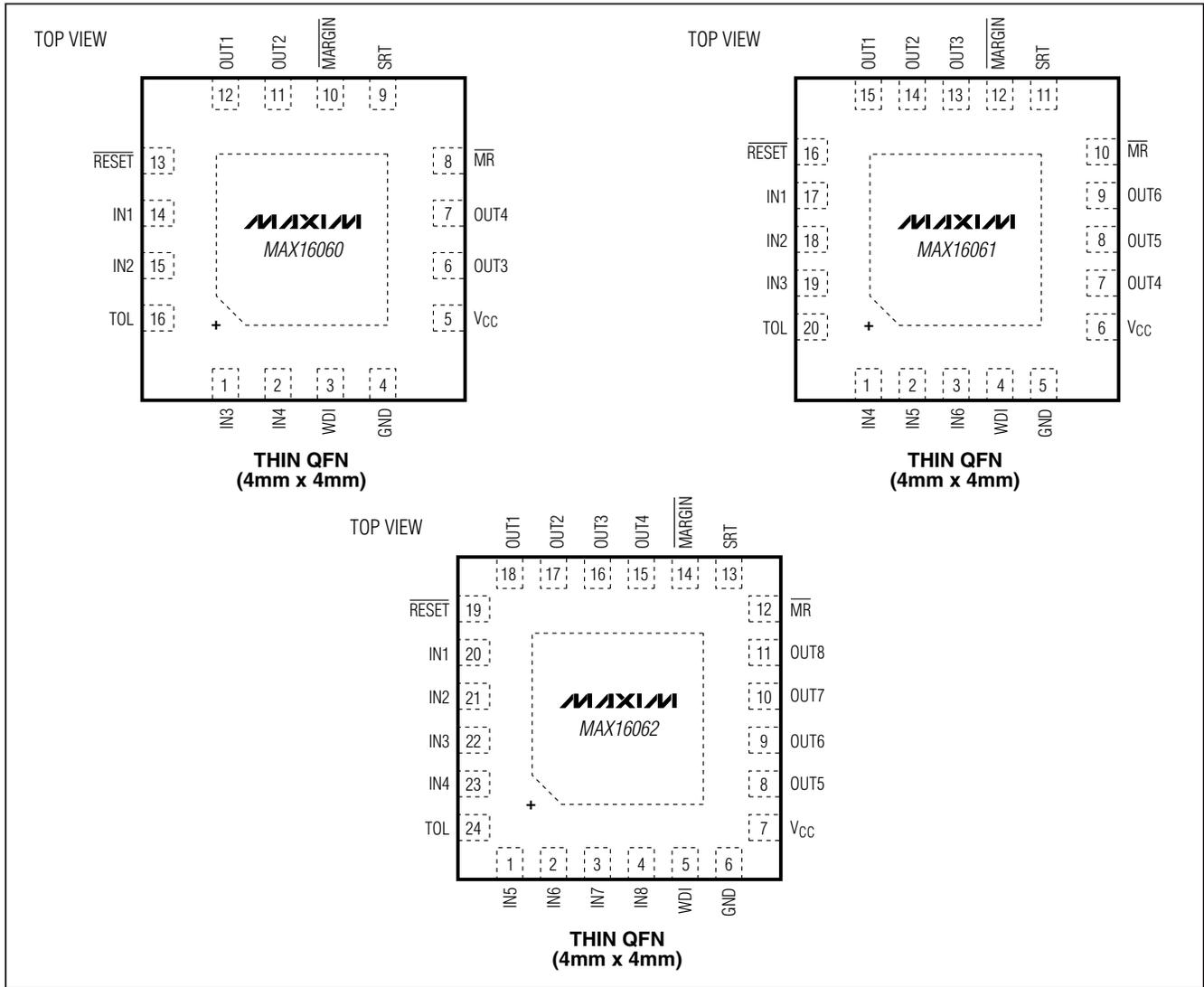
### Power-Supply Bypassing

In noisy applications, bypass $V_{CC}$ to ground with a 0.1µF capacitor as close to the device as possible. The additional capacitor improves transient immunity. For fast-rising $V_{CC}$ transients, additional capacitance may be required.

# 1% Accurate, Quad-/Hex-/Octal-Voltage
# µP Supervisors

**MAX16060/MAX16061/MAX16062**



TOP VIEW

MAX16060

**THIN QFN**
**(4mm x 4mm)**

TOP VIEW

MAX16061

**THIN QFN**
**(4mm x 4mm)**

TOP VIEW

MAX16062

**THIN QFN**
**(4mm x 4mm)**

_____**Chip Information**

PROCESS: BiCMOS

_____**Package Information**

For the latest package outline information, go to
**www.maxim-ic.com/packages**.

| PACKAGE TYPE | PACKAGE CODE | DOCUMENT NO. |
|---|---|---|
| 16 TQFN | T1644-4 | **21-0139** |
| 20 TQFN | T2044-3 | **21-0139** |
| 24 TQFN | T2444-4 | **21-0139** |

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