

MC74HCT595A

8-Bit Serial-Input/Serial or Parallel-Output Shift Register with Latched 3-State Outputs and LSTTL Compatible Inputs

High-Performance Silicon-Gate CMOS

The MC74HCT595A consists of an 8-bit shift register and an 8-bit D-type latch with three-state parallel outputs. The shift register accepts serial data and provides a serial output. The shift register also provides parallel data to the 8-bit latch. The shift register and latch have independent clock inputs. This device also has an asynchronous reset for the shift register.

The HCT595A directly interfaces with the SPI serial data port on CMOS MPUs and MCUs. The device inputs are compatible with standard CMOS or LSTTL outputs.

Features

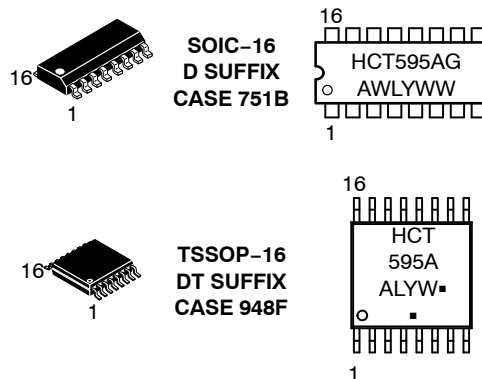
- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1.0 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 328 FETs or 82 Equivalent Gates
- Improvements over HC595 / HCT595
 - Improved Propagation Delays
 - 50% Lower Quiescent Power
 - Improved Input Noise and Latchup Immunity
- Pb-Free Packages are Available*



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MARKING DIAGRAMS



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G, ■ = Pb-Free Package

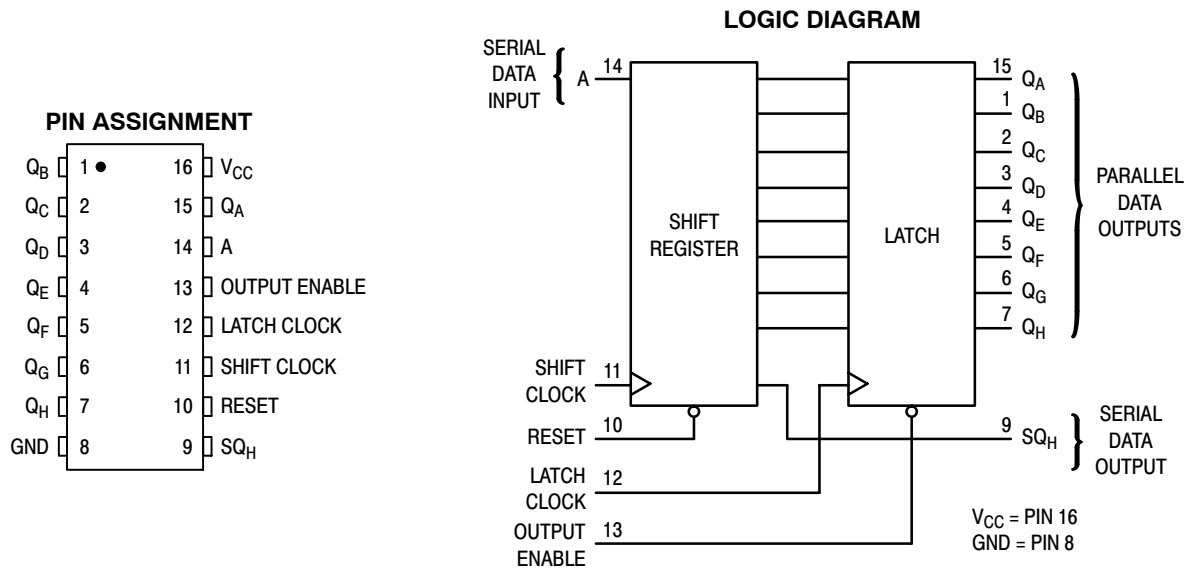
(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MC74HCT595A



ORDERING INFORMATION

Device	Package	Shipping†
MC74HCT595ADG	SOIC-16 (Pb-Free)	48 Units / Rail
MC74HCT595ADR2G	SOIC-16 (Pb-Free)	2500 Tape & Reel
MC74HCT595ADTG	TSSOP-16*	96 Units / Rail
MC74HCT595ADTR2G	TSSOP-16* (Pb-Free)	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*This package is inherently Pb-Free.

MC74HCT595A

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	- 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	- 0.5 to $V_{CC} + 0.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	- 0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, SOIC Package† TSSOP Package†	500 450	mW
T_{stg}	Storage Temperature	- 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP, SOIC or TSSOP Package)	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

†Derating — SOIC Package: - 7 mW/°C from 65° to 125°C
TSSOP Package: - 6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature Range, All Package Types	- 55	+ 125	°C
t_r, t_f	Input Rise/Fall Time (Figure 1)	0	500	ns

MC74HCT595A

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				- 55 to 25°C	≤ 85°C	≤ 125°C	
V _{IH}	Minimum High-Level Input Voltage	V _{out} = 0.1 V or V _{CC} - 0.1 V I _{out} ≤ 20 μA	4.5 to 5.5	2.0	2.0	2.0	V
V _{IL}	Maximum Low-Level Input Voltage	V _{out} = 0.1 V or V _{CC} - 0.1 V I _{out} ≤ 20 μA	4.5 to 5.5	0.8	0.8	0.8	V
V _{OH}	Minimum High-Level Output Voltage, Q _A - Q _H	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA	4.5	4.4	4.4	4.4	V
		V _{in} = V _{IH} or V _{IL} I _{out} ≤ 6.0 mA	4.5	3.98	3.84	3.7	
V _{OL}	Maximum Low-Level Output Voltage, Q _A - Q _H	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA	4.5	0.1	0.1	0.1	V
		V _{in} = V _{IH} or V _{IL} I _{out} ≤ 6.0 mA	4.5	0.26	0.33	0.4	
V _{OH}	Minimum High-Level Output Voltage, SQ _H	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA	4.5	4.4	4.4	4.4	V
		V _{in} = V _{IH} or V _{IL} I _{out} ≤ 4.0 mA	4.5	3.98	3.84	3.7	
V _{OL}	Maximum Low-Level Output Voltage, SQ _H	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA	4.5	0.1	0.1	0.1	V
		V _{in} = V _{IH} or V _{IL} I _{out} ≤ 4.0 mA	4.5	0.26	0.33	0.4	
I _{in}	Maximum Input Leakage Current	V _{in} = V _{CC} or GND	5.5	± 0.1	± 1.0	± 1.0	μA
I _{oz}	Maximum Three-State Leakage Current, Q _A - Q _H	Output in High-Impedance State V _{in} = V _{IL} or V _{IH} V _{out} = V _{CC} or GND	5.5	± 0.5	± 5.0	± 10	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{in} = V _{CC} or GND I _{out} = 0 μA	5.5	4.0	40	160	μA
ΔI _{CC}	Additional Quiescent Supply Current	V _{in} = 2.4V, Any One Input V _{in} = V _{CC} or GND, Other Inputs I _{out} = 0 μA	5.5	≥ -55°C	25 to 125°C		mA
				2.9	2.4		

MC74HCT595A

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6.0$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			-55 to 25°C	≤ 85°C	≤ 125°C	
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 7)	4.5 to 5.5	30	24	20	MHz
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Shift Clock to SQ _H (Figures 1 and 7)	4.5 to 5.5	28	35	42	ns
t_{PHL}	Maximum Propagation Delay, Reset to SQ _H (Figures 2 and 7)	4.5 to 5.5	29	36	44	ns
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Latch Clock to Q _A - Q _H (Figures 3 and 7)	4.5 to 5.5	28	35	42	ns
t_{PLZ} , t_{PHZ}	Maximum Propagation Delay, Output Enable to Q _A - Q _H (Figures 4 and 8)	4.5 to 5.5	30	38	45	ns
t_{PZL} , t_{PZH}	Maximum Propagation Delay, Output Enable to Q _A - Q _H (Figures 4 and 8)	4.5 to 5.5	27	34	41	ns
t_{TLH} , t_{THL}	Maximum Output Transition Time, Q _A - Q _H (Figures 3 and 7)	4.5 to 5.5	12	15	18	ns
t_{TLH} , t_{THL}	Maximum Output Transition Time, SQ _H (Figures 1 and 7)	4.5 to 5.5	15	19	22	ns
C _{in}	Maximum Input Capacitance	—	10	10	10	pF
C _{out}	Maximum Three-State Output Capacitance (Output in High-Impedance State), Q _A - Q _H	—	15	15	15	pF

C _{PD}	Power Dissipation Capacitance (Per Package)*	Typical @ 25°C, V _{CC} = 5.0 V			pF
		300			

* Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

TIMING REQUIREMENTS (Input $t_r = t_f = 6.0$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t_{su}	Minimum Setup Time, Serial Data Input A to Shift Clock (Figure 5)	4.5 to 5.5	10	13	15	ns
t_{su}	Minimum Setup Time, Shift Clock to Latch Clock (Figure 6)	4.5 to 5.5	15	19	22	ns
t_h	Minimum Hold Time, Shift Clock to Serial Data Input A (Figure 5)	4.5 to 5.5	5.0	5.0	5.0	ns
t_{rec}	Minimum Recovery Time, Reset Inactive to Shift Clock (Figure 2)	4.5 to 5.5	10	13	15	ns
t_w	Minimum Pulse Width, Reset (Figure 2)	4.5 to 5.5	12	15	18	ns
t_w	Minimum Pulse Width, Shift Clock (Figure 1)	4.5 to 5.5	10	13	15	ns
t_w	Minimum Pulse Width, Latch Clock (Figure 6)	4.5 to 5.5	10	13	15	ns
t_r , t_f	Maximum Input Rise and Fall Times (Figure 1)	4.5 to 5.5	500	500	500	ns

MC74HCT595A

FUNCTION TABLE

Operation	Inputs					Resulting Function			
	Reset	Serial Input A	Shift Clock	Latch Clock	Output Enable	Shift Register Contents	Latch Register Contents	Serial Output SQ _H	Parallel Outputs Q _A - Q _H
Reset shift register	L	X	X	L, H, ↓	L	L	U	L	U
Shift data into shift register	H	D	↑	L, H, ↓	L	D → SR _A ; SR _N → SR _{N+1}	U	SR _G → SR _H	U
Shift register remains unchanged	H	X	L, H, ↓	L, H, ↓	L	U	U	U	U
Transfer shift register contents to latch register	H	X	L, H, ↓	↑	L	U	SR _N → LR _N	U	SR _N
Latch register remains unchanged	X	X	X	L, H, ↓	L	*	U	*	U
Enable parallel outputs	X	X	X	X	L	*	**	*	Enabled
Force outputs into high impedance state	X	X	X	X	H	*	**	*	Z

SR = shift register contents
LR = latch register contents

D = data (L, H) logic level
U = remains unchanged

↑ = Low-to-High
↓ = High-to-Low

* = depends on Reset and Shift Clock inputs
** = depends on Latch Clock input

PIN DESCRIPTIONS

INPUTS A (Pin 14)

Serial Data Input. The data on this pin is shifted into the 8-bit serial shift register.

CONTROL INPUTS Shift Clock (Pin 11)

Shift Register Clock Input. A low-to-high transition on this input causes the data at the Serial Input pin to be shifted into the 8-bit shift register.

Reset (Pin 10)

Active-low, Asynchronous, Shift Register Reset Input. A low on this pin resets the shift register portion of this device only. The 8-bit latch is not affected.

Latch Clock (Pin 12)

Storage Latch Clock Input. A low-to-high transition on this input latches the shift register data.

Output Enable (Pin 13)

Active-low Output Enable. A low on this input allows the data from the latches to be presented at the outputs. A high on this input forces the outputs (Q_A-Q_H) into the high-impedance state. The serial output is not affected by this control unit.

OUTPUTS Q_A - Q_H (Pins 15, 1, 2, 3, 4, 5, 6, 7)

Noninverted, 3-state, latch outputs.

SQ_H (Pin 9)

Noninverted, Serial Data Output. This is the output of the eighth stage of the 8-bit shift register. This output does not have three-state capability.

MC74HCT595A

SWITCHING WAVEFORMS

($V_I = 0$ to 3 V, $V_M = 1.3$ V)

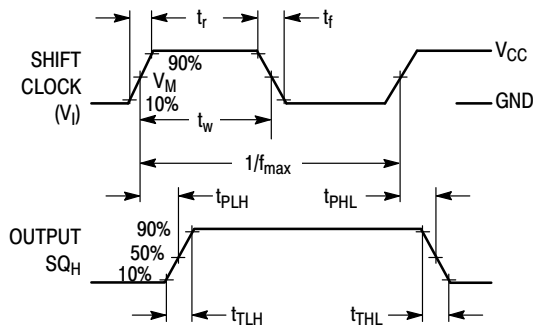


Figure 1.

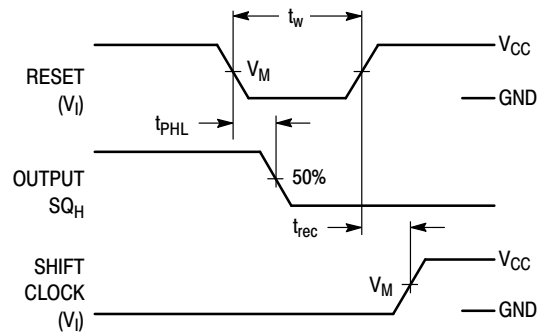


Figure 2.

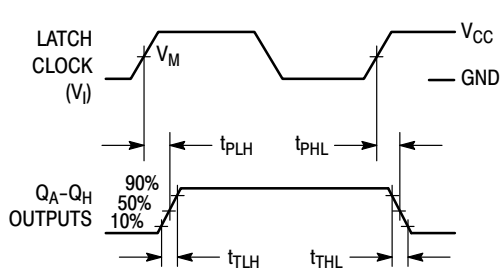


Figure 3.

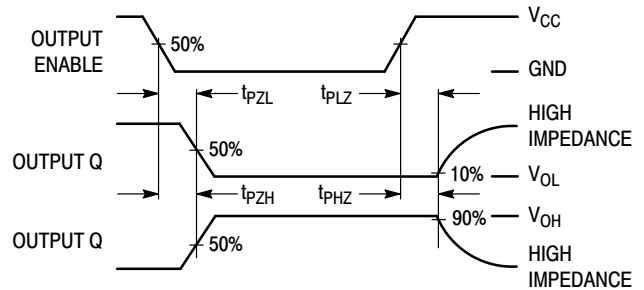


Figure 4.

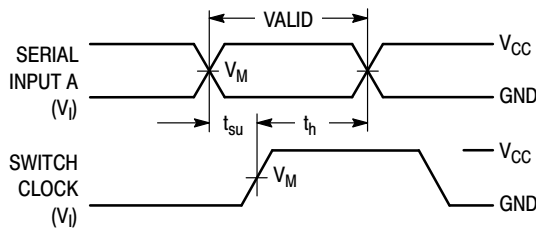


Figure 5.

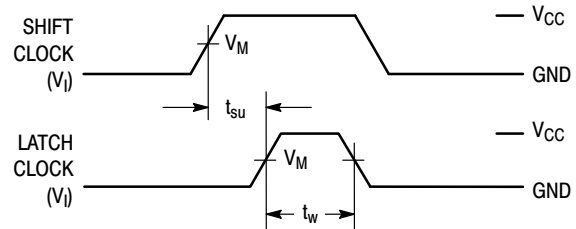
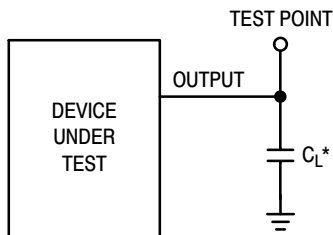


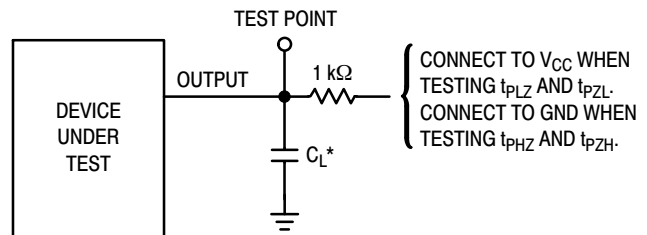
Figure 6.

TEST CIRCUITS



*Includes all probe and jig capacitance

Figure 7.

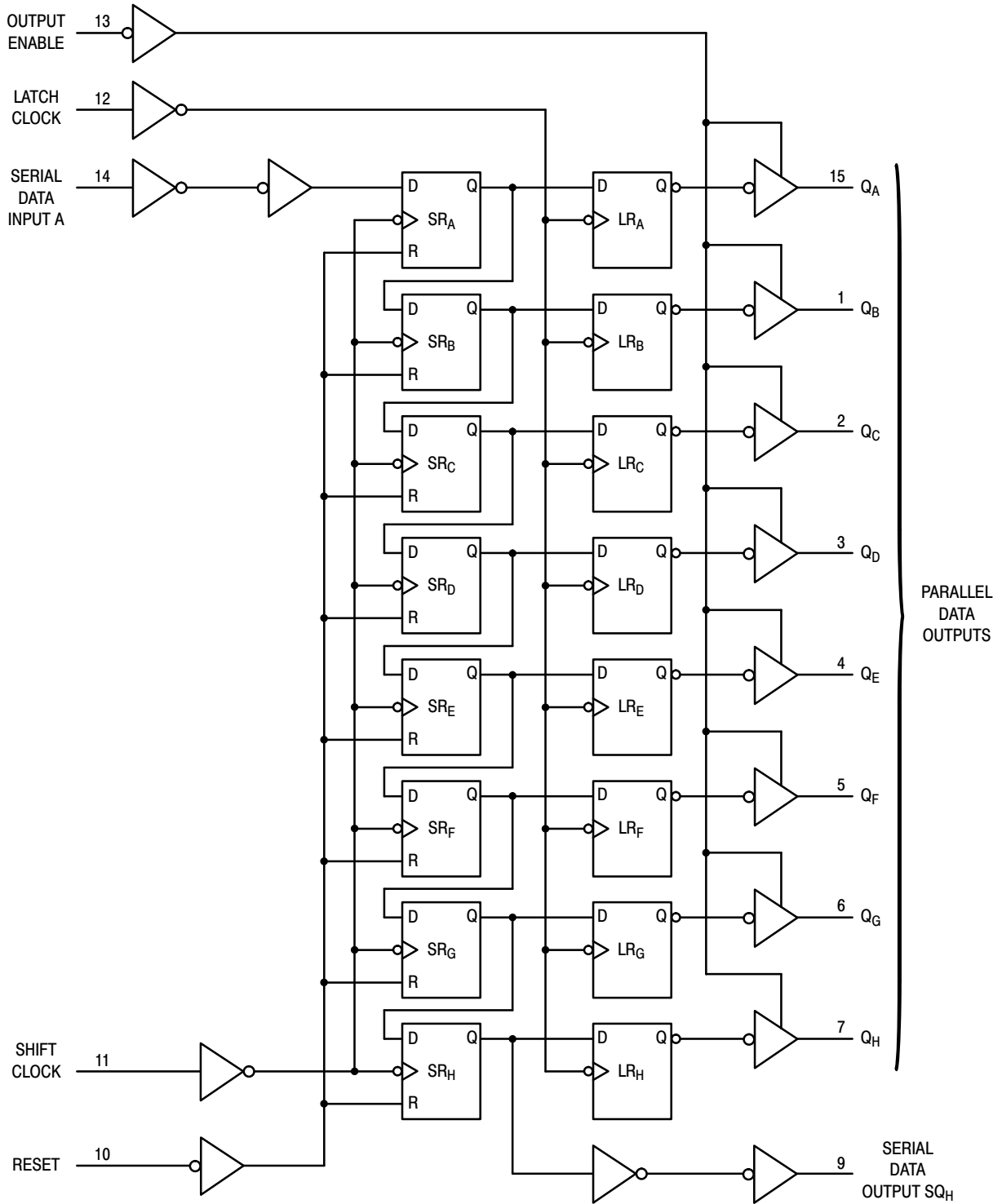


*Includes all probe and jig capacitance

Figure 8.

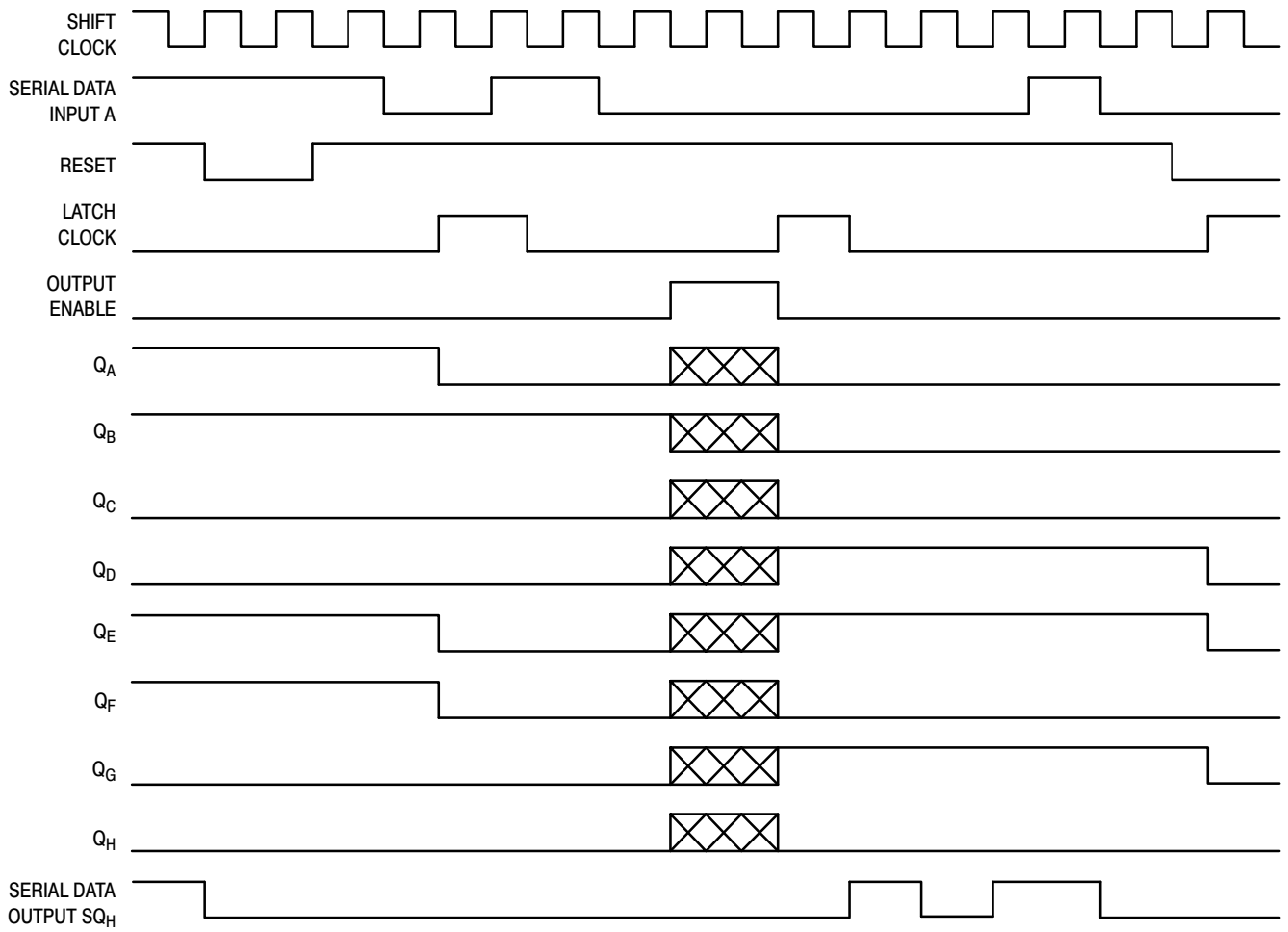
MC74HCT595A


EXPANDED LOGIC DIAGRAM



MC74HCT595A

TIMING DIAGRAM

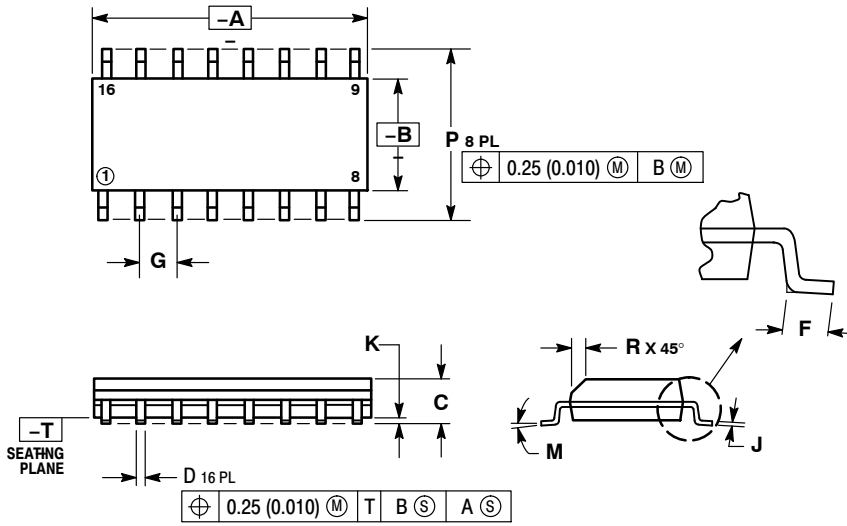


NOTE:  implies that the output is in a high-impedance state.

MC74HCT595A

PACKAGE DIMENSIONS

SOIC-16
D SUFFIX
CASE 751B-05
ISSUE J

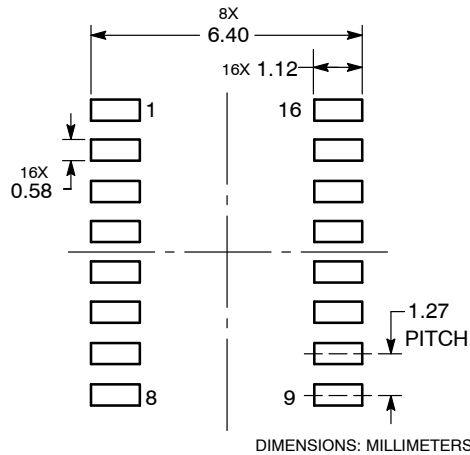


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

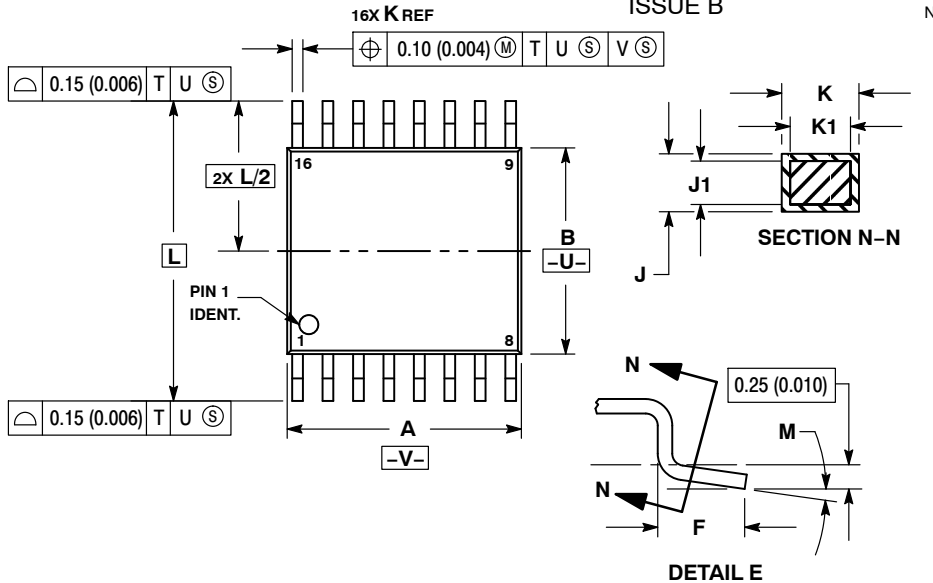
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MC74HCT595A

PACKAGE DIMENSIONS

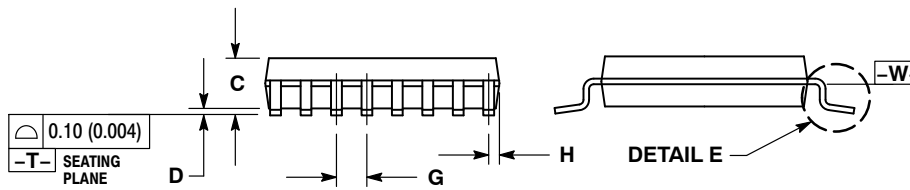
TSSOP-16
DT SUFFIX
CASE 948F-01
ISSUE B



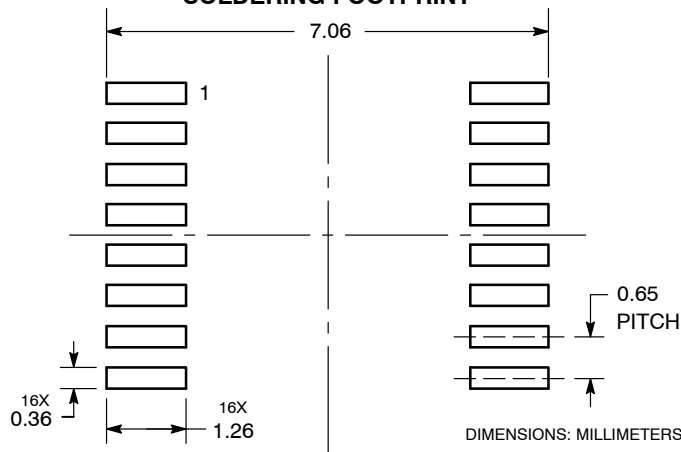
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°



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