An Ultra-small, 4 mΩ, 5 A Integrated Power Switch with PG Output

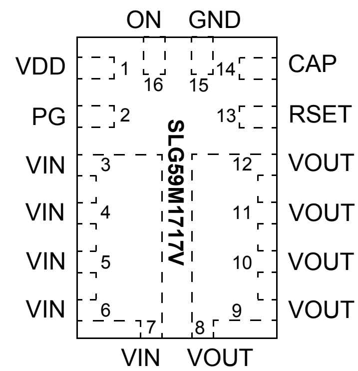
General Description

Operating from a 2.5 V to 5.5 V power supply and fully specified over the -40 °C to 85 °C Industrial temperature range, the SLG59M1717V is a high-performance 4 mΩ, 5 A single-channel nFET integrated power switch designed for all 0.8 V to 5.5 V power rail applications. The SLG59M1717V features adjustable inrush current control which is achieved by adjusting the V_{OUT} slew rate with an external capacitor. Using a proprietary MOSFET design, the SLG59M1717V achieves a stable 4 mΩ RDS_{ON} across a wide input/supply voltage range. The SLG59M1717V also incorporates resistor-adjustable current limiting as well as thermal protection. Using Silego's proprietary CuFET™ technology for high-current operation, the SLG59M1717V is packaged in a space-efficient, low thermal resistance, RoHS-compliant 1.6mm x 2.5 mm STQFN package.

Features

- Low Typical RDS_{ON} nFET Block: 4 mΩ
- Maximum Continuous Switch Current: Up to 5 A
- Supply Voltage: 2.5 V ≤ V_{DD} ≤ 5.5 V
- Wide Input Voltage Range: 0.8 V ≤ V_{IN} ≤ V_{DD}
- Capacitor adjustable Start-up and In-rush Current Control
- Two-stage Overcurrent Protection:
  - Resistor-adjustable Active Current Limit
  - Fixed 1.6 A Short-circuit Current Limit
- Thermal Shutdown Protection
- Open-drain PG Signaling
- Operating Temperature: -40 °C to 85 °C
- Low θ_{JA}, 16-pin 1.6 mm x 2.5 mm STQFN
  - Pb-Free / Halogen-Free / RoHS compliant

Pin Configuration

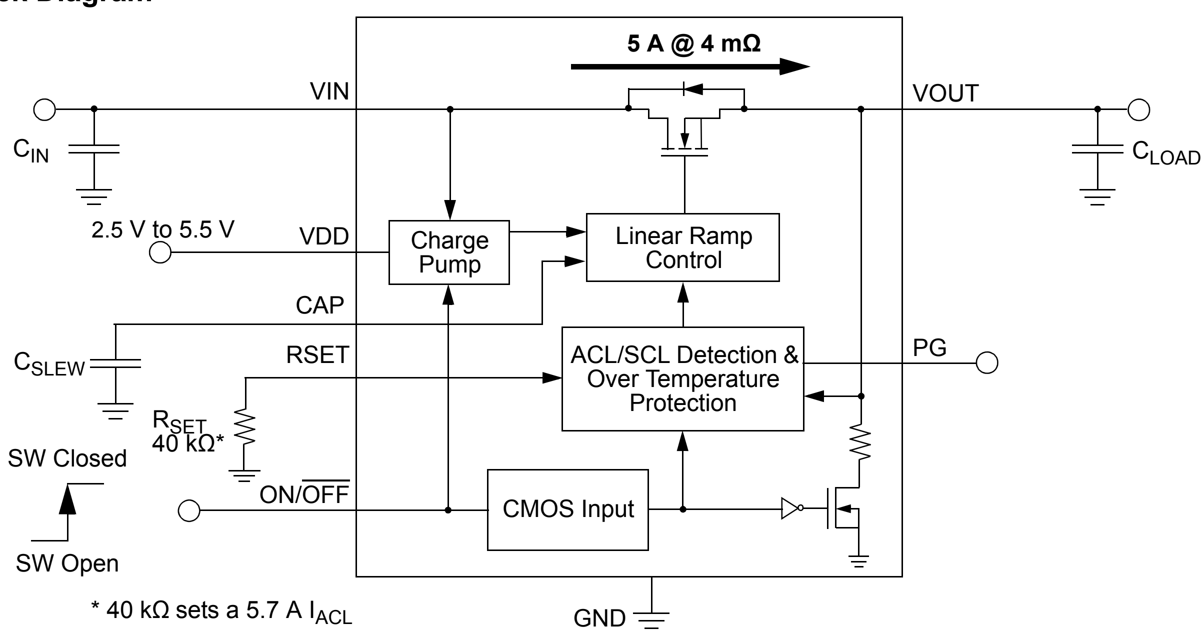


16-pin FC-STQFN
(Top View)

Applications

- Notebook Power Rail Switching
- Tablet Power Rail Switching
- Smartphone Power Rail Switching

Block Diagram



Pin Description

Pin #	Pin Name	Type	Pin Description
1	VDD	Power	With an internal 1.9 V UVLO threshold, VDD supplies the power for the operation of the power switch and internal control circuitry where its range is 2.5 V ≤ V_{DD} ≤ 5.5 V. Bypass the VDD pin to GND with a 0.1 µF (or larger) capacitor
2	PG	Output	An open drain output. PG is asserted when V_{OUT} reaches 90% of V_{IN}. Connect an external 10-kΩ resistor from the PG pin to local system logic supply.
3-7	VIN	MOSFET	Drain terminal of Power MOSFET (Pins 3-7 fused together). Connect a 10 µF (or larger) low ESR capacitor from this pin to GND. Capacitors used at VIN should be rated at 10 V or higher.
8-12	VOUT	MOSFET	Source terminal of Power MOSFET (Pins 8-12 fused together). Connect a capacitor (up to 600 µF) from this pin to GND. Capacitors used at VOUT should be rated at 10 V or higher.
13	RSET	Input	A 1%-tolerance, metal-film resistor between 38 kΩ and 80 kΩ sets the IPS's active current limit. A 38 kΩ resistor sets the SLG59M1717V's active current limit to 6 A and a 80 kΩ resistor sets the active current limit to 2.85 A.
14	CAP	Input	A capacitor connected from CAP pin to GND sets the VOUT slew rate and overall turn-on time of the SLG59M1717V. For best performance, the range for C_{SLEW} values are 2 nF ≤ C_{SLEW}. Capacitors used at the CAP pin should be rated at 10 V or higher.
15	GND	GND	Ground
16	ON	Input	A low-to-high transition on this pin closes the power switch. ON is an asserted-HIGH, level-sensitive CMOS input with V_{IL} < 0.3 V and V_{IH} > 0.85 V. Connect this pin to the output of a general-purpose output (GPO) from a microcontroller or other application processor. While there is an internal pull down circuit to ground (~4 MΩ), do not allow this pin to be open-circuited.

Ordering Information

Part Number	Type	Production Flow
SLG59M1717V	STQFN 16L	Industrial, -40 °C to 85 °C
SLG59M1717VTR	STQFN 16L (Tape and Reel)	Industrial, -40 °C to 85 °C

Absolute Maximum Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Power Supply Pin to GND		--	--	6	V
V_{IN} to GND	Power Switch Input Voltage to GND		-0.3	--	6	V
V_{OUT} to GND	Power Switch Output Voltage to GND		-0.3	--	V_{IN}	V
ON, RSET, CAP, and to PG GND	ON, RSET, CAP, and PG Pin Voltages to GND		-0.3	--	6	V
T_S	Storage Temperature		-65	--	150	°C
ESD_{HBM}	ESD Protection	Human Body Model	2000	--	--	V
ESD_{CDM}	ESD Protection	Charged Device Model	500	--	--	V
MSL	Moisture Sensitivity Level		1			
θ_{JA}	Package Thermal Resistance, Junction-to-Ambient	1.6mm x 2.5mm STQFN; Determined using 1 in^2, 1.2 oz. copper pads under each VIN and VOUT on FR4 pcb material, with airflow	--	35	--	°C/W
W_{DIS}	Package Power Dissipation		--	--	1.2	W
IDS_{MAX}	Max Continuous Switch Current		--	--	5	A
MOSFET IDS_{PK}	Peak Current from Drain to Source	Maximum pulsed switch current, pulse width < 1 ms, 1% duty cycle	--	--	6	A

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Electrical Characteristics

T_A = -40 °C to 85 °C (unless otherwise stated)

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Power Supply Voltage		2.5	--	5.5	V
$V_{DD(UVLO)}$	V_{DD} Undervoltage Lockout Threshold	V_{DD} ↑	1.6	1.9	2.2	V
		V_{DD} ↓	1.5	1.8	2.2	V
I_{DD}	Power Supply Current when OFF	$V_{DD} = V_{IN}$ = 5.5 V; ON = 0	--	--	1	μA
	Power Supply Current, ON (Steady State)	$V_{DD} = V_{IN}$ = ON = 5.5 V; No Load, R_{SET} = 80 kΩ	--	160	200	μA
RDS_{ON}	ON Resistance	T_A 25°C MOSFET @100 mA; $V_{DD} = V_{IN}$ = 5 V	--	4	5.5	mΩ
		T_A 85°C MOSFET @100 mA; $V_{DD} = V_{IN}$ = 5 V	--	5	6.8	mΩ
		T_A 85°C MOSFET @ 5 A; V_{DD} = 5 V, V_{IN} = 1 V[2]	--	5.1	7.0	mΩ
MOSFET IDS	Current from V_{IN} to V_{OUT}	Continuous	--	--	5	A
I_{FET_OFF}	MOSFET OFF Leakage Current	$V_{DD} = V_{IN}$ = 5.5 V; V_{OUT} = 0 V; ON = 0 V	--	0.1	2	μA
V_{IN}	Drain Voltage		0.8	--	V_{DD}	V

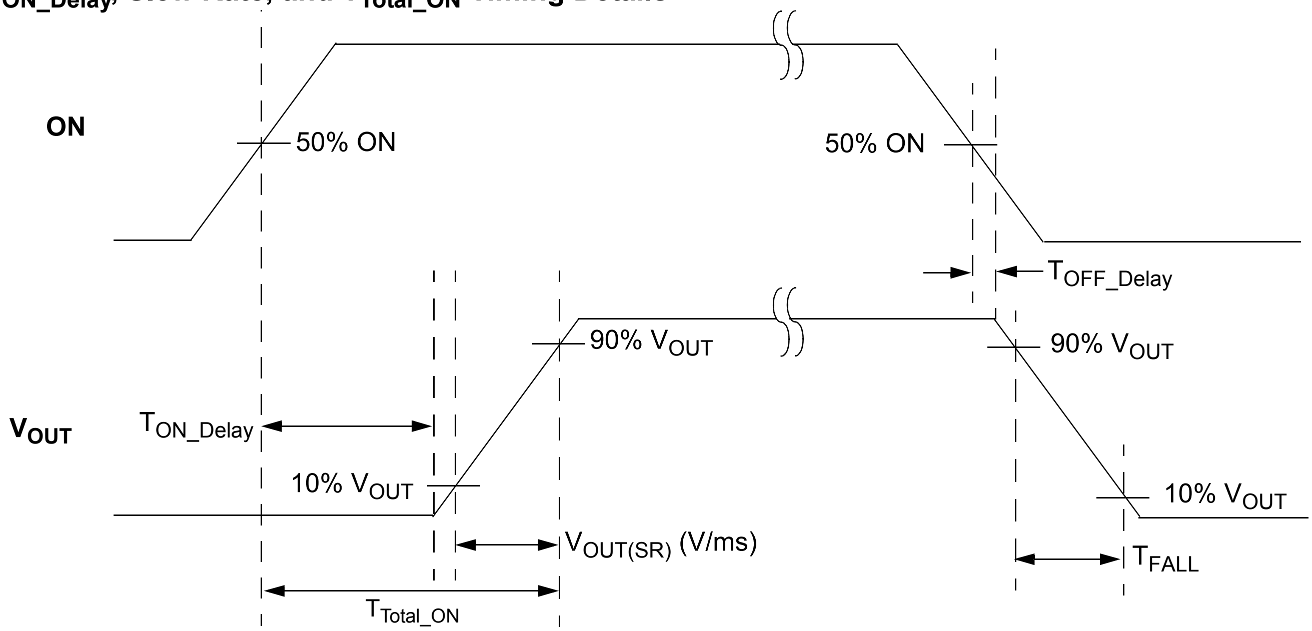
Electrical Characteristics (continued)

T_A = -40 °C to 85 °C (unless otherwise stated)

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
T_{ON_Delay}	ON pin Delay Time	50% ON to Ramp Begin, V_{DD} = V_{IN} = 5 V; C_{SLEW} = 12 nF; R_{LOAD} = 20 Ω, C_{LOAD} = 10 µF	--	200	--	µs
$V_{OUT(SR)}$	V_{OUT} Slew Rate[3]	10% V_{OUT} to 90% V_{OUT} ↑;	Set by External C_{SLEW}[1]			V/ms
		Example: C_{SLEW} = 12 nF; V_{DD} = V_{IN} = 5 V; R_{LOAD} = 20 Ω, C_{LOAD} = 10 µF	0.8	1	1.2	V/ms
T_{Total_ON}	Total Turn-on Time	50% ON to 90% V_{OUT} ↑;	Set by External C_{SLEW}[1]			ms
		Example: C_{SLEW} = 12 nF; V_{DD} = V_{IN} = 5 V, R_{LOAD} = 20 Ω, C_{LOAD} = 10 µF	--	4.7	--	ms
T_{OFF_Delay}	OFF Delay Time	50% ON to V_{OUT} Fall Start; V_{DD} = V_{IN} = 5 V, R_{LOAD} = 20 Ω, no C_{LOAD}	--	8	15	µs
C_{LOAD}	Output Load Capacitance	C_{LOAD} connected from VOUT to GND	1	10	600	µF
I_{LIMIT}	Active Current Limit (I_{ACL})[2]	V_{OUT} > 0.25 V; R_{SET} = 80 kΩ	2.28	2.85	3.42	A
	Short-circuit Current Limit (I_{SCL})[3]	V_{OUT} < 0.25 V	--	1.6	--	A
PG_{VOH}	Power Good Pull-up Voltage	Open Drain Output Buffer	--	--	5.5	V
PG	Power Good level	V_{OUT} reaches 90% of V_{IN}	87	90	93	%
PG_{HYS}	Power Good Hysteresis	V_{OUT} below V_{PG} level 5%	--	5	--	%
ON_V_{IH}	High Input Voltage on ON pin		0.85	--	V_{DD}	V
ON_V_{IL}	Low Input Voltage on ON pin		-0.3	0	0.3	V
$R_{DISCHRG}$	Output Discharge Resistance	V_{DD} = 5 V, V_{OUT} = 0.4 V, ON = 0 V	70	93	150	Ω
$THERM_{ON}$	Thermal shutoff turn-on temperature		--	150	--	°C
$THERM_{OFF}$	Thermal shutoff turn-off temperature		--	130	--	°C

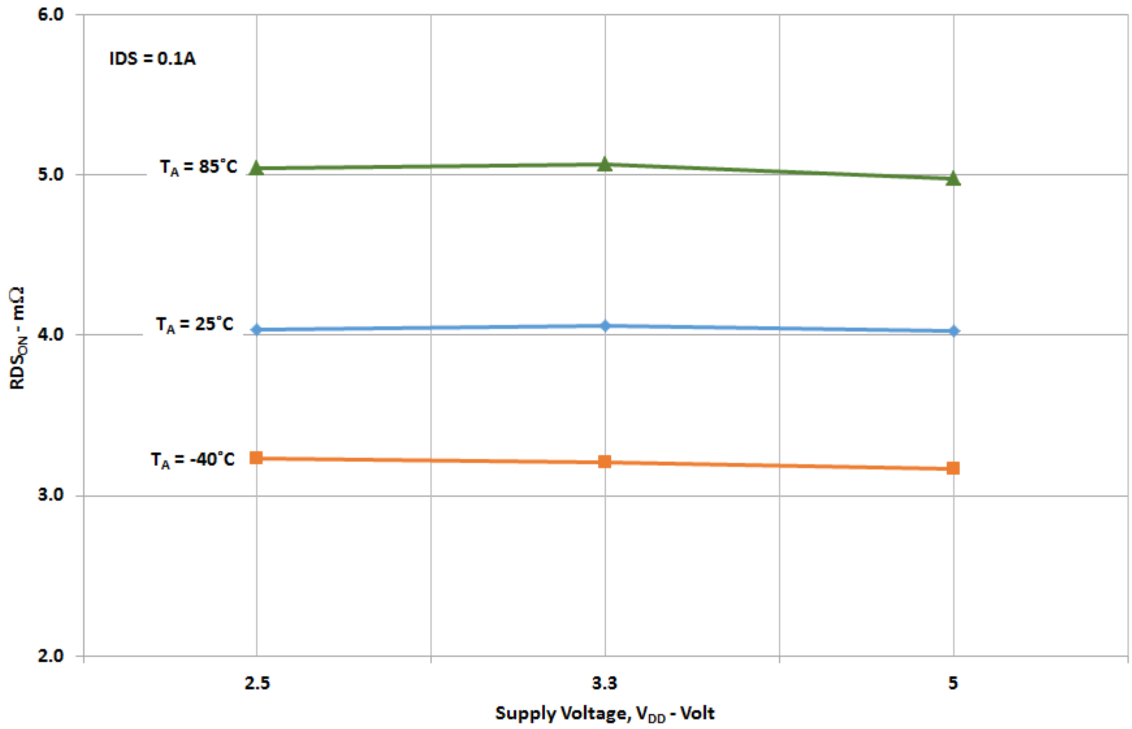
Notes:
1. Refer to typical Timing Parameter vs. C_{SLEW} performance charts for additional information when available.
2. Based on bench characterization
3. Please consult SLG59M1717V Start-up Inrush Current Considerations with Capacitive Loads section starting on Page 14.

T_{ON_Delay}, Slew Rate, and T_{Total_ON} Timing Details

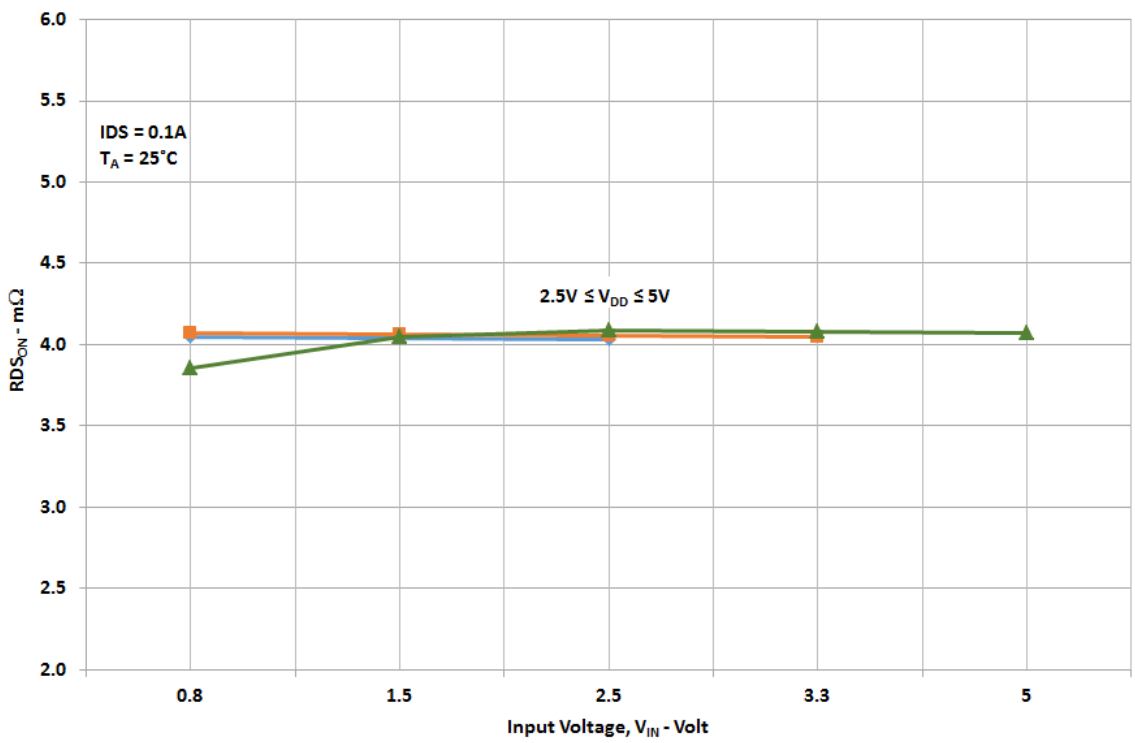


Typical Performance Characteristics

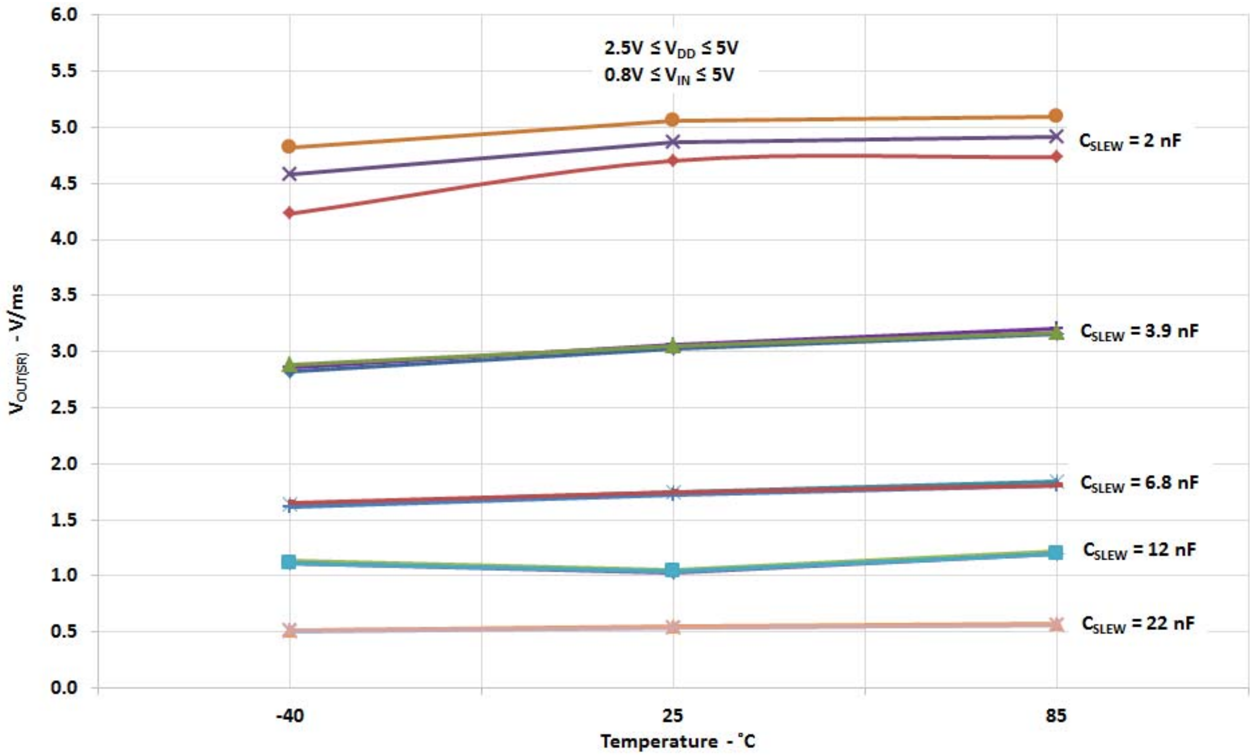
RDS_{ON} vs. V_{DD}, and Temperature



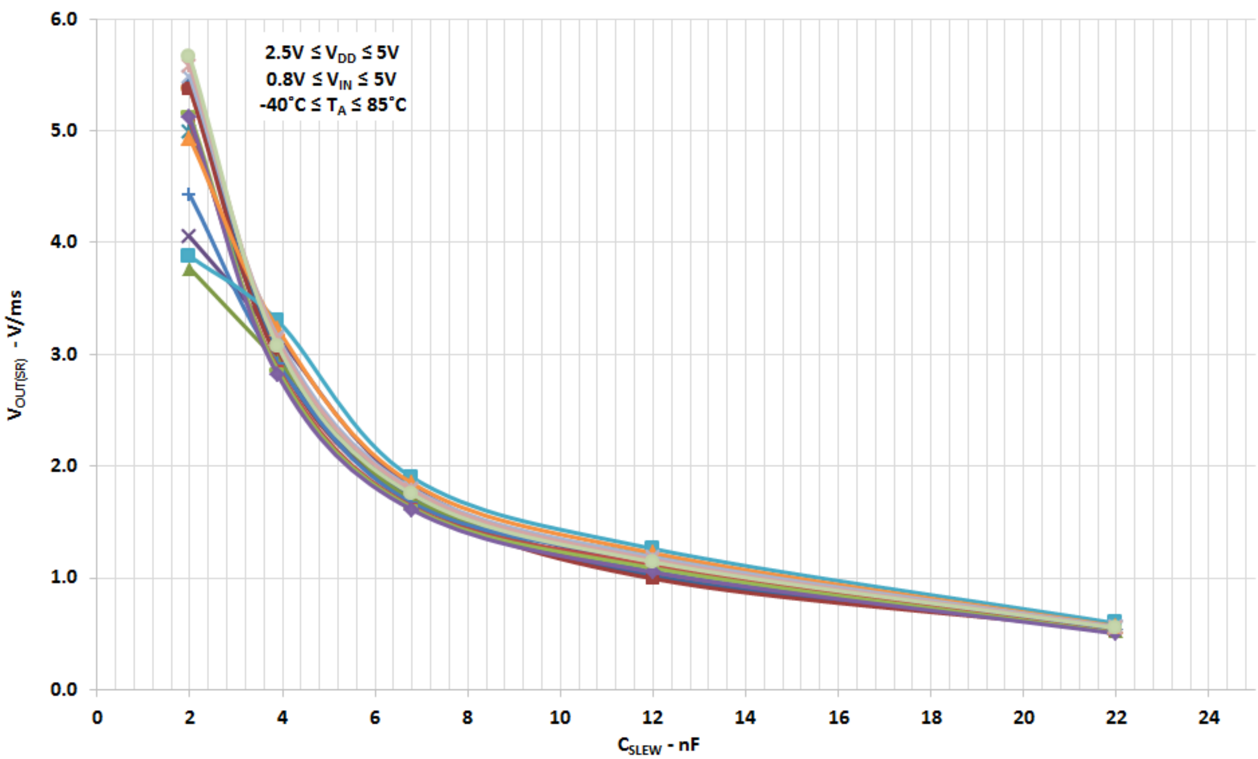
RDS_{ON} vs. V_{IN} and V_{DD}



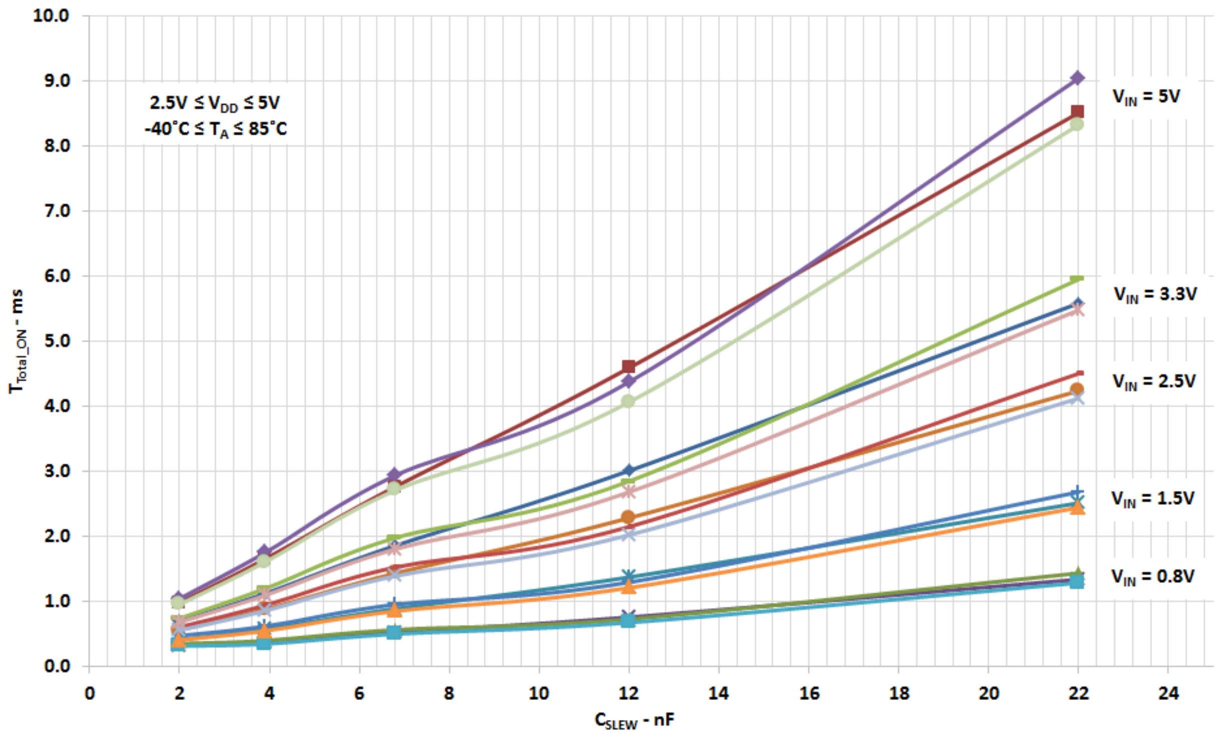
$V_{OUT(SR)}$ vs. Temperature, V_{IN}, V_{DD}, and C_{SLEW}



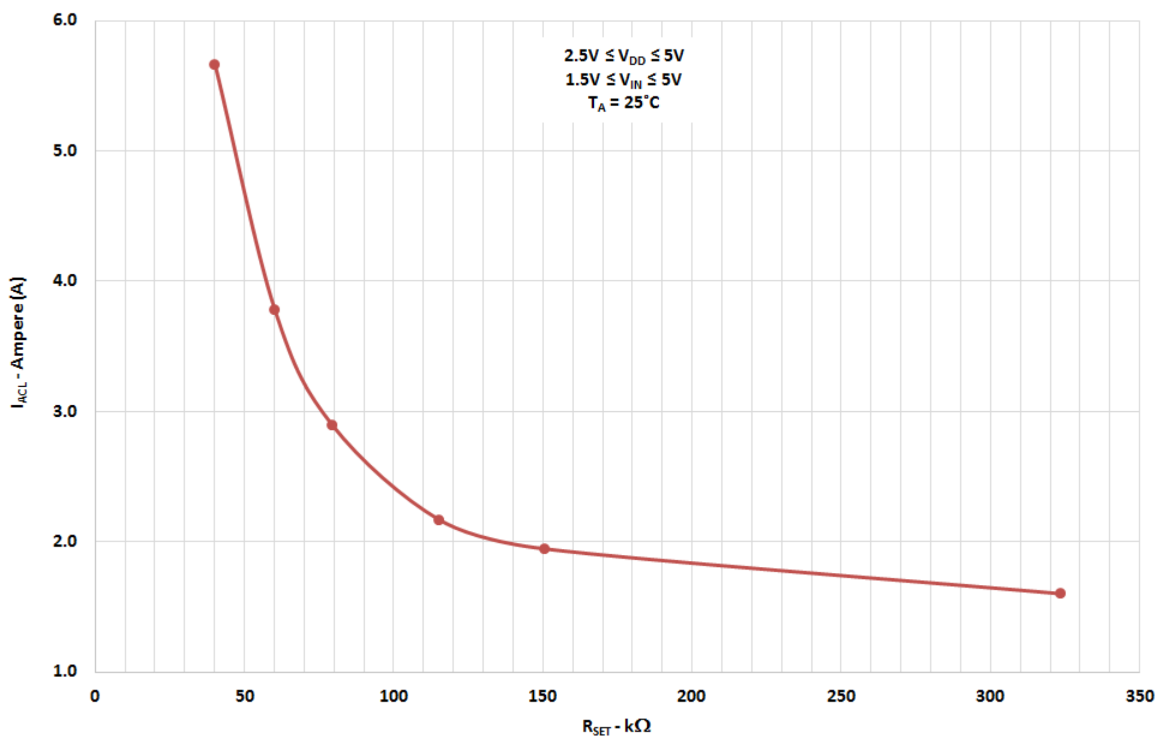
$V_{OUT(SR)}$ vs. C_{SLEW}, V_{IN}, V_{DD}, and Temperature



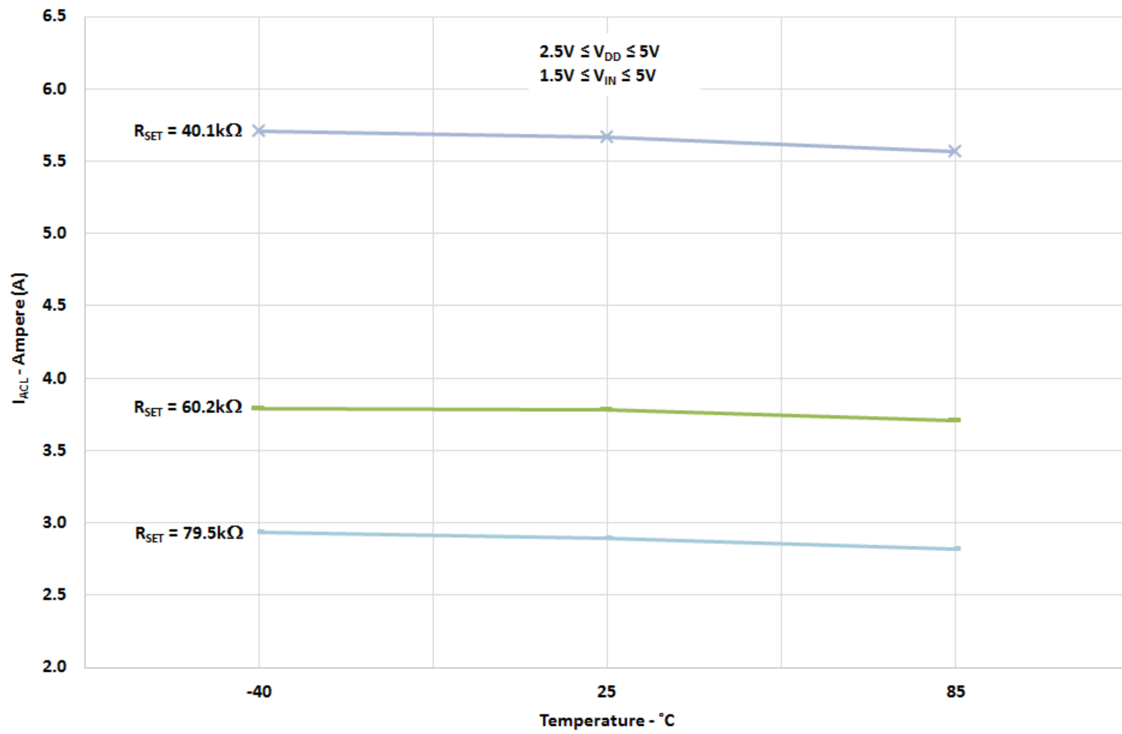
T_{Total_ON} vs. C_{SLEW}, V_{IN}, V_{DD}, and Temperature



I_{ACL} vs. R_{SET}, V_{DD}, and V_{IN}



I_{ACL} vs. Temperature, V_{DD}, and V_{IN}



Typical Turn-on Waveforms - V_{DD} = V_{IN} = 5 V

ON

V_{OUT}

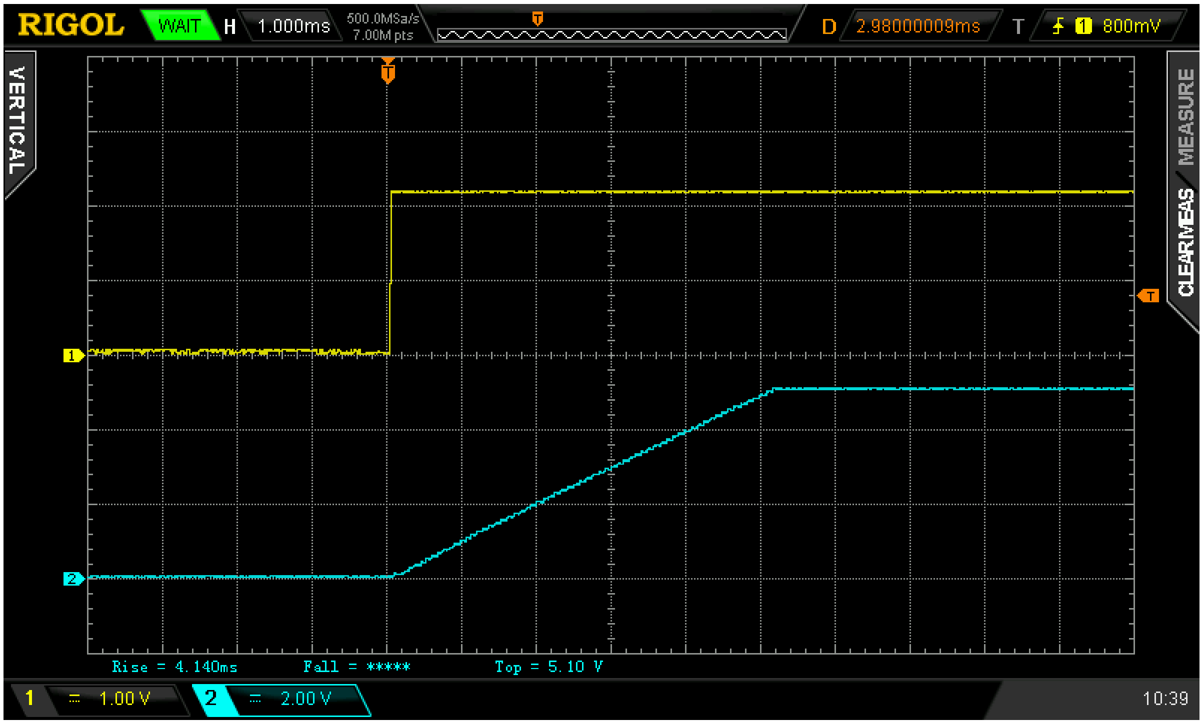


Figure 1. Typical Turn ON operation waveform for V_{DD} = V_{IN} = 5 V, C_{SLEW} = 12 nF, C_{LOAD} = 10 μF, R_{LOAD} = 20 Ω

ON

V_{OUT}

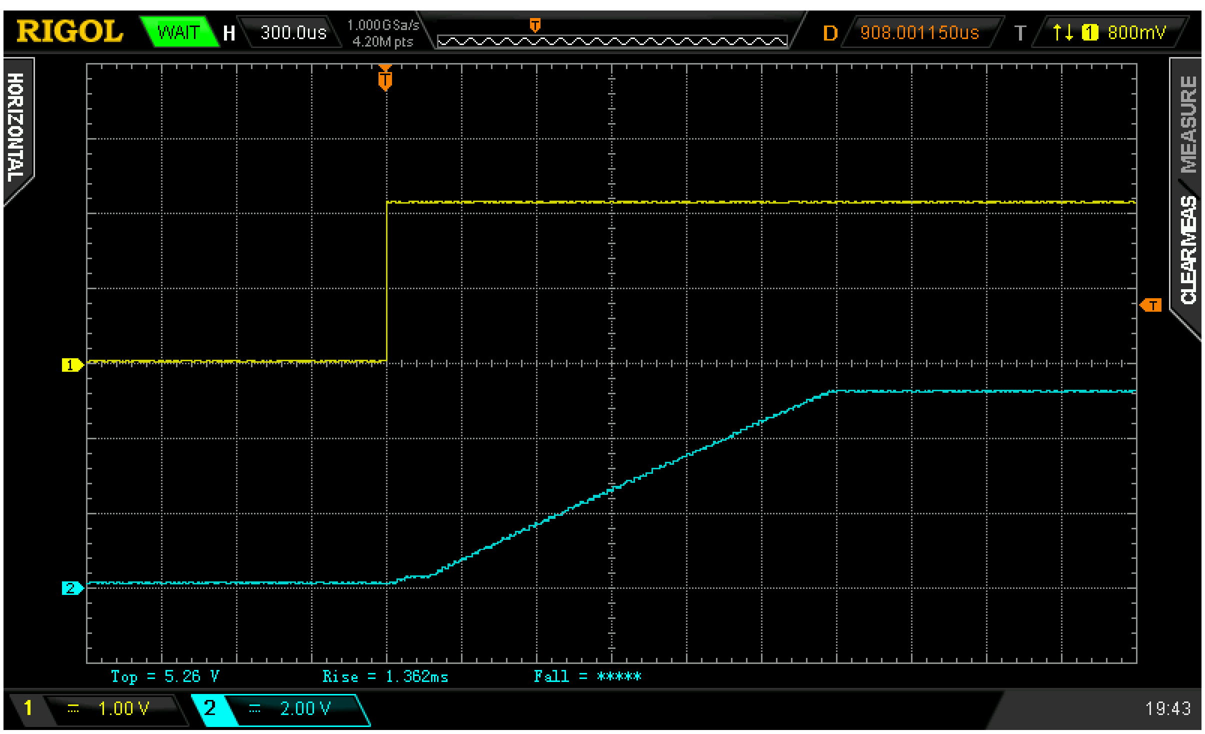


Figure 2. Typical Turn ON operation waveform for V_{DD} = V_{IN} = 5 V, C_{SLEW} = 4 nF, C_{LOAD} = 10 μF, R_{LOAD} = 20 Ω

Typical Turn-off Waveforms - $V_{DD} = V_{IN} = 5$ V

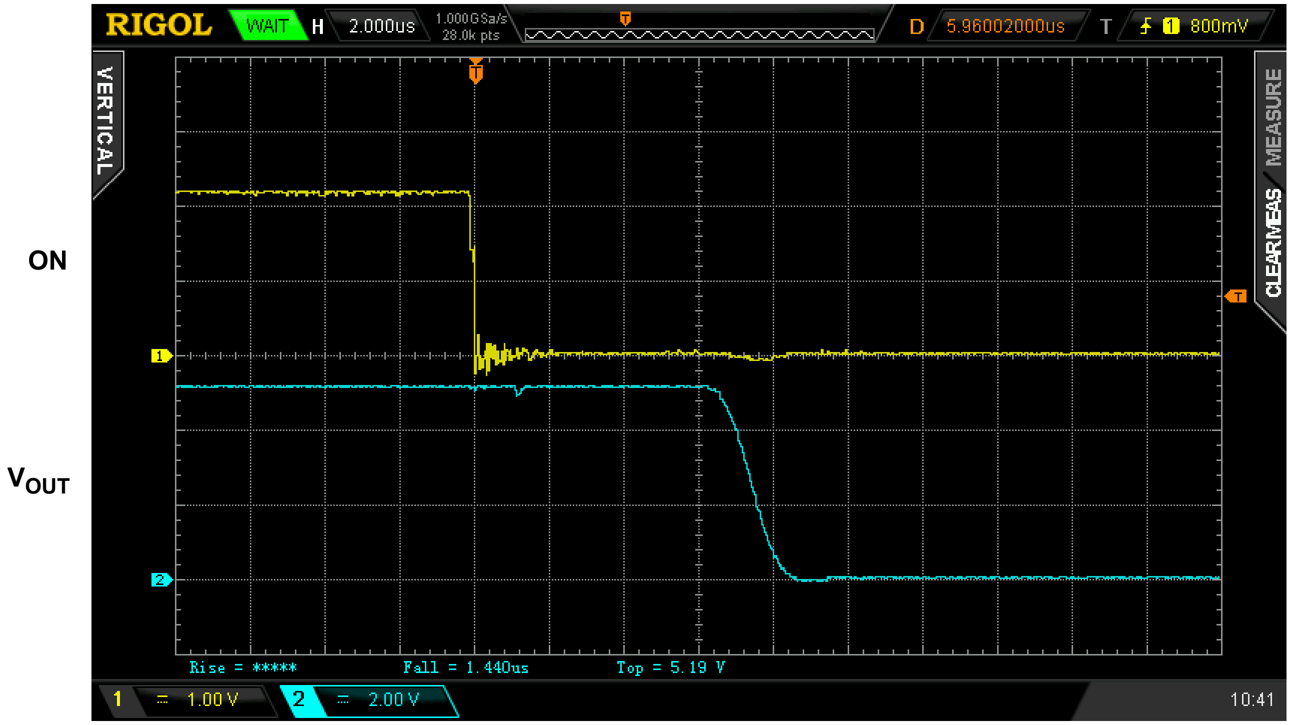


Figure 3. Typical Turn OFF operation waveform for $V_{DD} = V_{IN} = 5$ V, $C_{SLEW} = 12$ nF, no C_{LOAD}, $R_{LOAD} = 20\ \Omega$

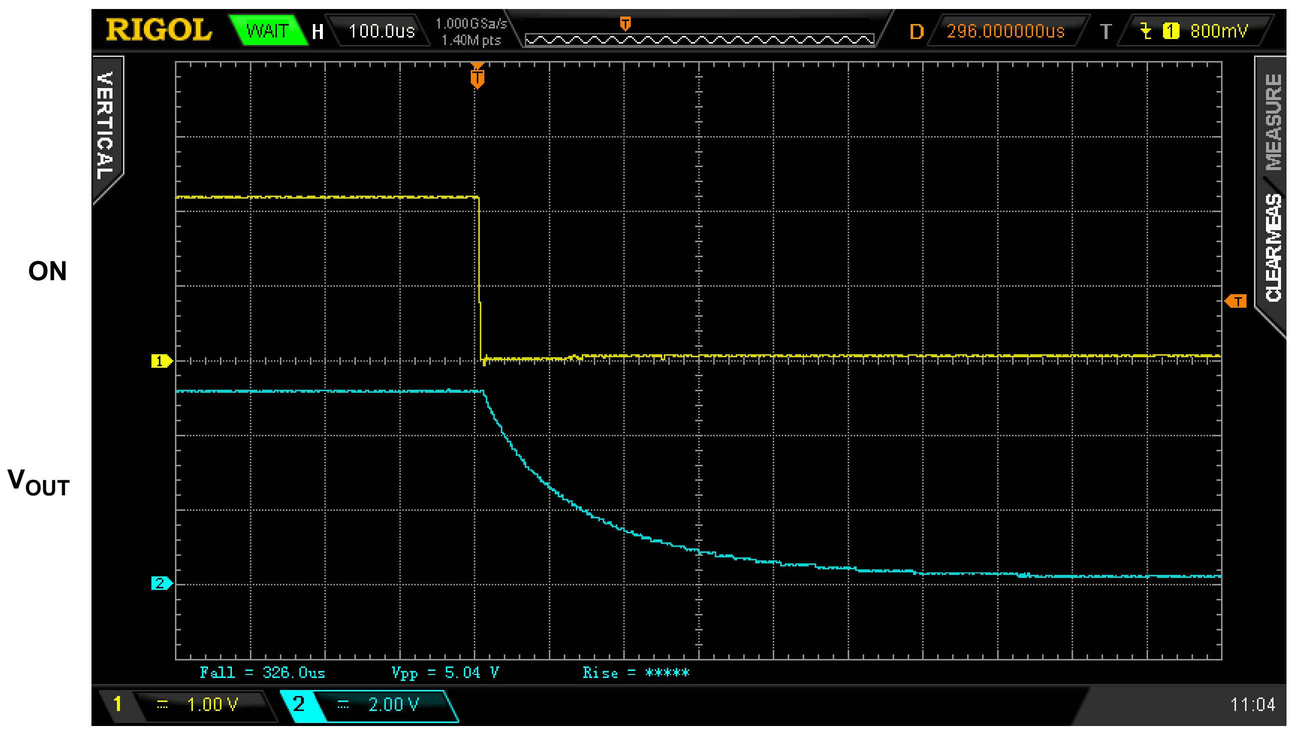
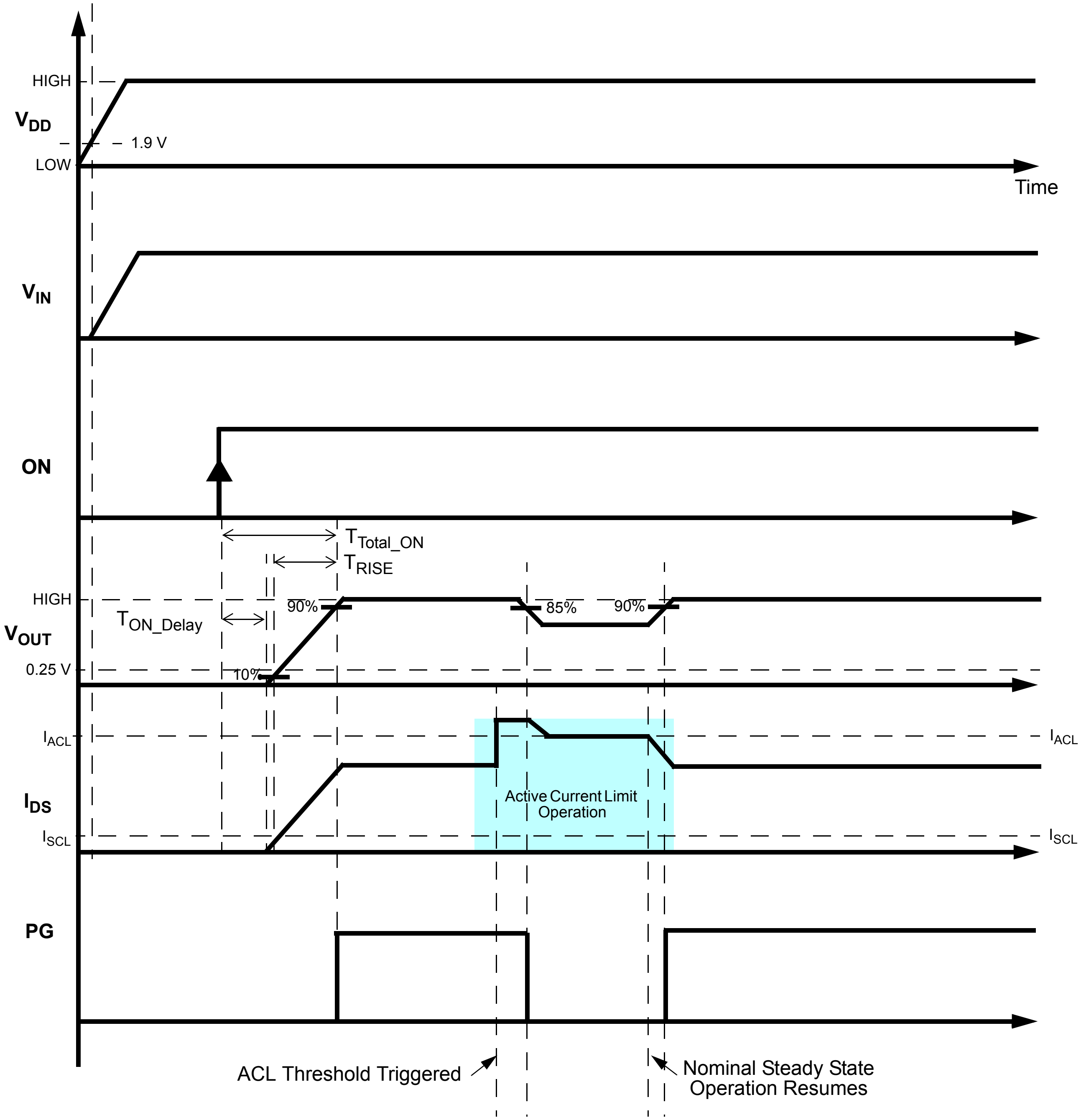
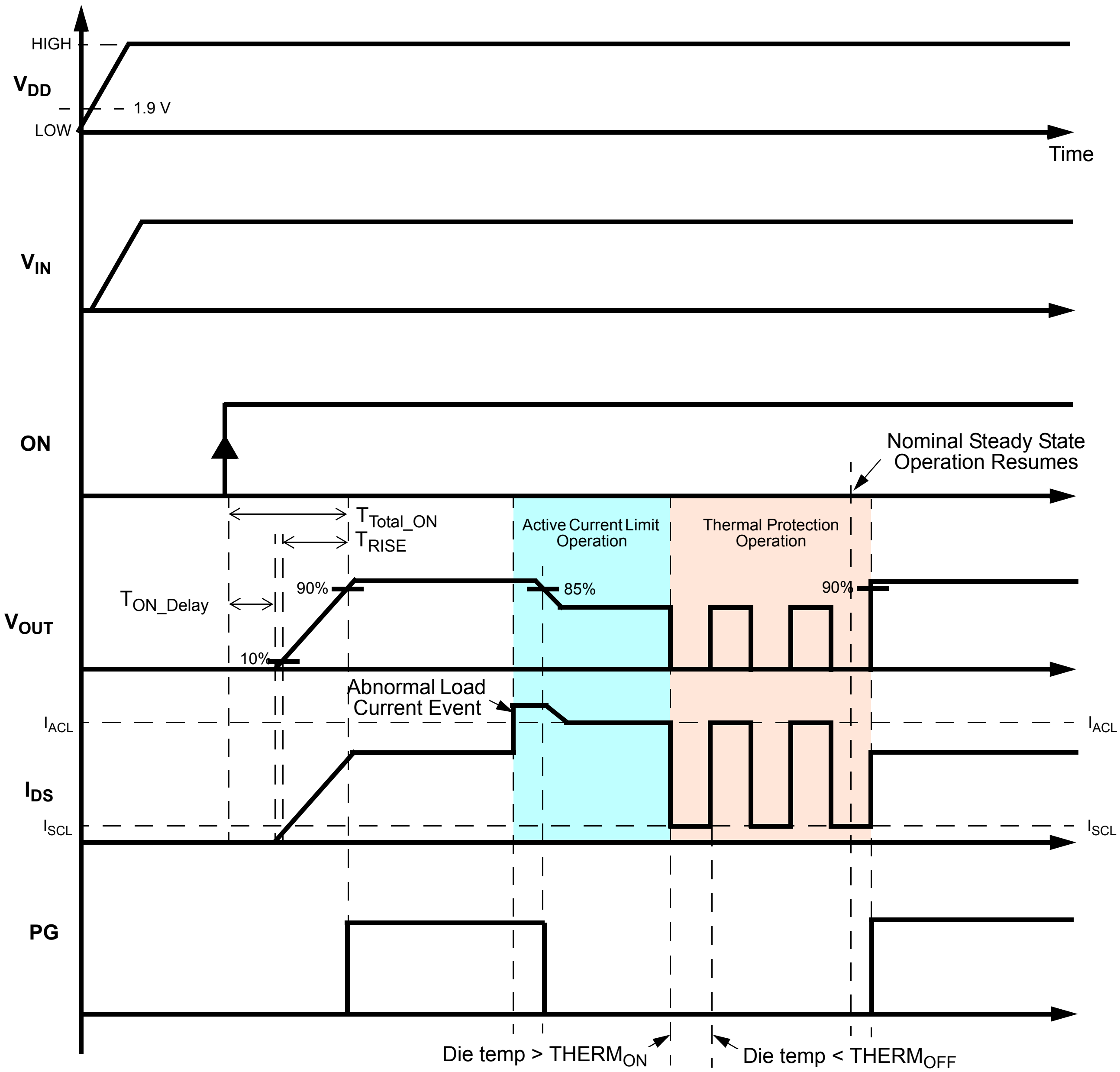


Figure 4. Typical Turn OFF operation waveform for $V_{DD} = V_{IN} = 5$ V, $C_{SLEW} = 12$ nF, $C_{LOAD} = 10$ μF, $R_{LOAD} = 20\ \Omega$

Timing Diagram - Basic Operation including Active Current Limit Protection



Timing Diagram - Active Current Limit & Thermal Protection Operation



SLG59M1717V Power-Up/Power-Down Sequence Considerations

To ensure glitch-free power-up under all conditions, apply V_{DD} first, followed by V_{IN} after V_{DD} exceeds 1.9 V. Then allow V_{IN} to reach 90% of its max value before toggling the ON pin from Low-to-High. Likewise, power-down in reverse order.

If V_{DD} and V_{IN} need to be powered up simultaneously, glitching can be minimized by having a suitable load capacitor. A 10 µF C_{LOAD} will prevent glitches for rise times of V_{DD} and V_{IN} less than 2 ms.

If the ON pin is toggled HIGH before V_{DD} and V_{IN} have reached their steady-state values, the IPS timing parameters may differ from datasheet specifications.

The slew rate of output V_{OUT} follows a linear ramp set by a capacitor connected to the CAP pin. A larger capacitor value at the CAP pin produces a slower ramp, reducing inrush current from capacitive loads.

SLG59M1717V Current Limiting Operation

The SLG59M1717V has two types of current limiting triggered by the output V_{OUT} voltage.

1. Standard Current Limiting Mode (with Thermal Shutdown Protection)

When the V_{OUT} voltage > 250 mV, the output current is initially limited to the Active Current Limit (I_{ACL}) specification listed in the Electrical Characteristics table. The ACL monitor's response time is very fast and is triggered within a few microseconds to sudden (transient) changes in load current. When a load current overload is detected, the ACL monitor increases the FET resistance to keep the current from exceeding the power switch's I_{ACL} threshold. During active current-limit operation, V_{OUT} is also reduced by I_{ACL} x $RDS_{ON(ACL)}$. This observed behavior is illustrated in the timing diagrams on Pages 12 and 13.

However, if a load-current overload condition persists where the die temperature rises because of the increased FET resistance, the power switch's internal Thermal Shutdown Protection circuit can be activated. If the die temperature exceeds the listed $THERM_{ON}$ specification, the FET is shut OFF completely, thereby allowing the die to cool. When the die cools to the listed $THERM_{OFF}$ temperature threshold, the FET is allowed to turn back on. This process may repeat as long as the output current overload condition persists.

2. Short Circuit Current Limiting Mode (with Thermal Shutdown Protection)

When the V_{OUT} voltage < 250 mV (which is the case with a hard short, such as a solder bridge on the power rail), the power switch's internal Short-circuit Current Limit (SCL) monitor limits the FET current to approximately 1.6 A (the I_{SCL} threshold). While the internal Thermal Shutdown Protection circuit remains enabled and since the I_{SCL} threshold is much lower than the I_{ACL} threshold, thermal shutdown protection may become activated only at higher ambient temperatures.

SLG59M1717V Start-up Inrush Current Considerations with Capacitive Loads

In distributed power applications, the SLG59M1717V is generally implemented on the outboard or downstream side of switching regulator dc/dc converters with internal overcurrent protection. As an adjustable output voltage slew-rate, integrated power switch, it is important to understand the start-up operation of the SLG59M1717V with capacitive loads. An equivalent circuit of the SLG59M1717V's slew-rate control loop with capacitors at its VIN and VOUT pins is shown in *Figure 1*:

SLG59M1717V Start-up Inrush Current Considerations with Capacitive Loads (continued)

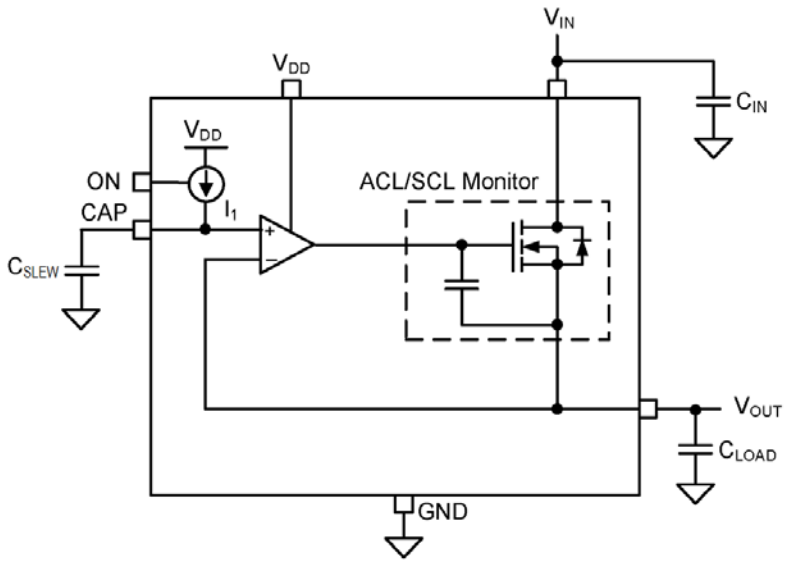


Figure 1. SLG59M1717V's Equivalent Slew-rate Control Loop Circuit.

For a desired V_{OUT} slew-rate ($V_{OUT(SR)}$), a corresponding C_{SLEW} value is selected. At the VOUT pin and with ON = LOW, the internal FET is OFF, V_{OUT} is initially at 0V, and there is no stored charge on C_{LOAD}. When a low-to-high transition is applied to the IC's ON pin, an internal current source (I_1) is enabled which, in turn, charges the external slew-rate capacitor, C_{SLEW}. The SLG59M1717V's internal micropower op amp sets the circuit's $V_{OUT(SR)}$ based on the slew rate of the nodal voltage at its non-inverting pin (the voltage at the CAP pin).

As a function of $V_{OUT(SR)}$ and C_{LOAD}, a 1st-order expression for the circuit's FET current (and inrush current) when a low-to-high transition on the ON pin is applied becomes:

$$\text{Start-up Current } I_{DS} \text{ or } I_{INRUSH} = V_{OUT(SR)} \times C_{LOAD}$$

From the expression above and for a given $V_{OUT(SR)}$, C_{LOAD} determines the magnitude of the inrush current; that is, for large values of C_{LOAD}, large inrush currents can result. If the inrush currents are large enough to trigger the overcurrent protection of an upstream dc/dc converter, the system can be shut down.

In applications where the desired $V_{OUT(SR)}$ is fast and C_{LOAD} is very large (>200µF), there is a secondary effect on the observed $V_{OUT(SR)}$ attributed to the SLG59M1717V's internal short-circuit current limit monitor (its SCL monitor). If the resultant inrush current is larger than the IC's I_{SCL} threshold, the SCL current monitor limits the inrush current and the current to charge C_{LOAD} until the SCL OFF threshold is crossed (~0.25V). During the time the SCL monitor's been activated, the inrush current profile may exhibit an observable reduction in $V_{OUT(SR)}$ as shown in *Figure 2* where C_{SLEW} was set to 4nF and 470µF was chosen for C_{LOAD}.

SLG59M1717V Start-up Inrush Current Considerations with Capacitive Loads (continued)

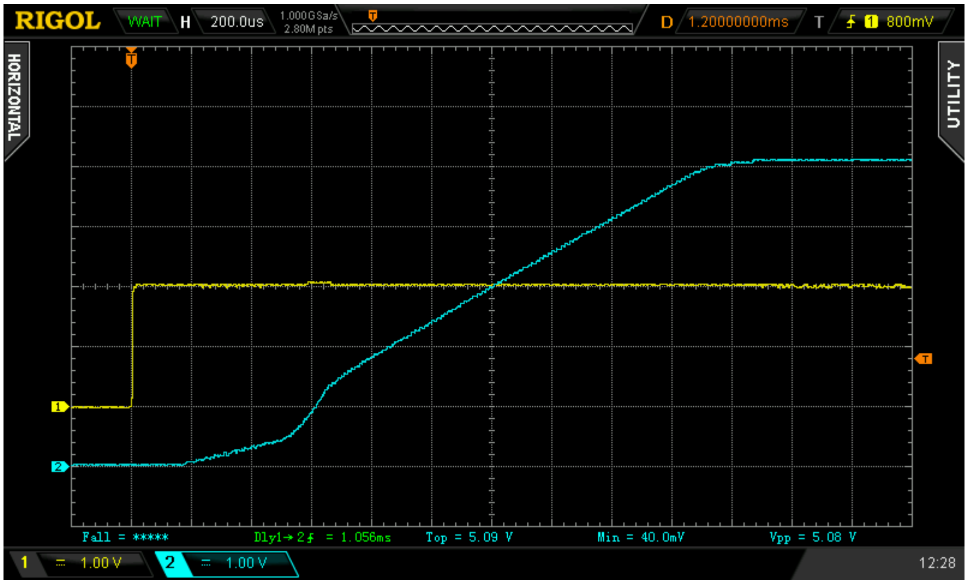


Figure 2. A SLG59M1717V with C_{SLEW} set to 4nF and 470µF for C_{LOAD}. C_{LOAD}-to-C_{SLEW} ratio is greater than 33,600. Note that the internal SCL monitor's been triggered and $V_{OUT(SR)}$ is reduced until V_{OUT} reaches ~0.25V.

A closer analysis of the IC's internal slew-control large-scale yields the following:

$$\frac{I_{SCL}}{C_{LOAD}} = M_{SR} \times \frac{I_1}{C_{SLEW}}$$

where

I_{SCL} = IC's short-circuit current limit threshold, typically 1.6 A;
M_{SR} = An internal slew-rate multiplier from the IC's CAP pin to the VOUT pin;
I_1 = An internal current source to charge the external C_{SLEW}.

Rearranging the equation to isolate both C_{LOAD} and C_{SLEW} yields the following:

$$\frac{C_{LOAD}}{C_{SLEW}} = \frac{I_{SCL}}{I_1 \times M_{SR}}$$

For the SLG59M1717V device, the right-hand side of the expression is approximately 33,600 after taking into account part-to-part variations because of process, voltage, and temperature.

Referring to the configuration of *Figure 2*'s scope capture, the C_{LOAD}-to-C_{SLEW} ratio is 117,500 (470µF/4nF) where it is evident that the SCL monitor circuit is charging C_{LOAD} shortly after a low-to-high ON transition. If it is desired to avoid a reduction in $V_{OUT(SR)}$, the choices are decreasing C_{LOAD} and/or increasing C_{SLEW} so that the ratio is always less than 33,600 including taking into account external capacitor tolerances for initial accuracy and temperature.

As shown in *Figure 3*, it was chosen to reduce $V_{OUT(SR)}$ by increasing C_{SLEW} to 15nF while keeping C_{LOAD} at 470µF. With this configuration, the ratio of C_{LOAD} to C_{SLEW} is about 31,333 (smaller than 33,600). Upon a low-to-high transition on the ON pin, the V_{OUT} increases smoothly with no evidence of SCL monitor's interaction.

SLG59M1717V Start-up Inrush Current Considerations with Capacitive Loads (continued)

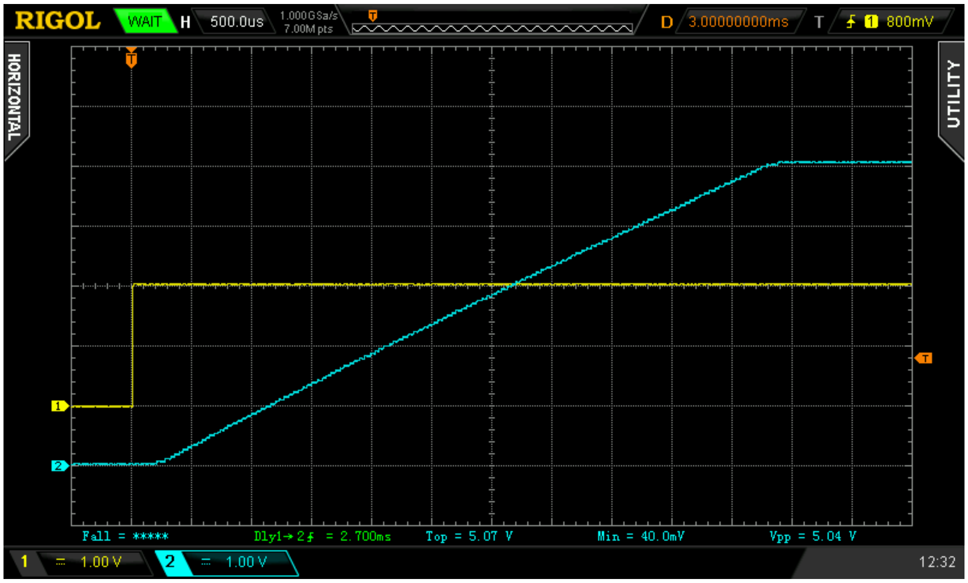


Figure 3. A SLG59M1717V with C_{SLEW} set to 15nF and 470µF retained for C_{LOAD}. C_{LOAD}-to-C_{SLEW} ratio is smaller than 33,600. Note smooth V_{OUT} transition.

Setting the SLG59M1717V Output Current Limit with R_{SET}

The current-limit operation of the SLG59M1717V begins by choosing the appropriate ±1%-tolerance R_{SET} value for the application. The recommended range for R_{SET} is:

$$38\ k\Omega \leq R_{SET} \leq 80\ k\Omega$$

which corresponds to an output constant current limit in the following range:

$$2.85\ A \leq I_{ACL} \leq 6\ A$$

Table 1: Setting Current Limit Threshold vs. R_{SET}

Constant Current Limit	R_{SET}
2.85 A	80 kΩ
3.8 A	60 kΩ
6 A	38 kΩ

Power Dissipation

The junction temperature of the SLG59M1717V depends on different factors such as board layout, ambient temperature, and other environmental factors. The primary contributor to the increase in the junction temperature of the SLG59M1717V is the power dissipation of its power MOSFET. Its power dissipation and the junction temperature in nominal operating mode can be calculated using the following equations:

$$PD = RDS_{ON} \times I_{DS}^2$$

where:
PD = Power dissipation, in Watts (W)
RDS_{ON} = Power MOSFET ON resistance, in Ohms (Ω)
I_{DS} = Output current, in Amps (A)

and

$$T_J = PD \times \theta_{JA} + T_A$$

where:
T_J = Junction temperature, in Celsius degrees (°C)
θ_{JA} = Package thermal resistance, in Celsius degrees per Watt (°C/W)
T_A = Ambient temperature, in Celsius degrees (°C)

During active current-limit operation, the SLG59M1717V's power dissipation can be calculated by taking into account the voltage drop across the power switch (V_{IN} - V_{OUT}) and the magnitude of the output current in active current-limit operation (I_{ACL}):

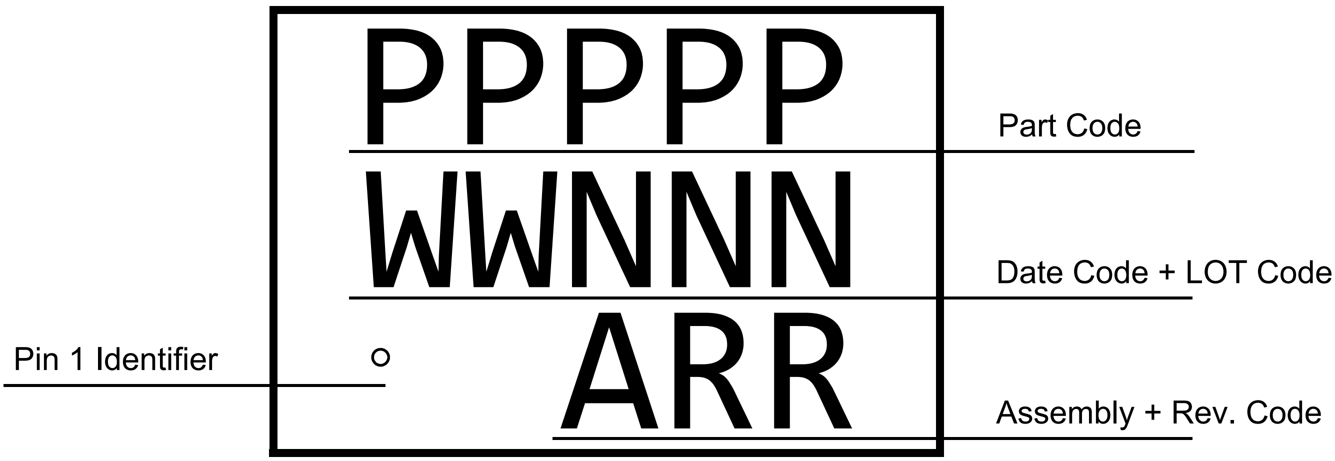
$$PD = (V_{IN} - V_{OUT}) \times I_{ACL} \text{ or}$$

$$PD = (V_{IN} – (R_{LOAD} \times I_{ACL})) \times I_{ACL}$$

where:

PD = Power dissipation, in Watts (W)
V_{IN} = Input Voltage, in Volts (V)
R_{LOAD} = Load Resistance, in Ohms (Ω)
I_{ACL} = Output limited current, in Amps (A)
$V_{OUT} = R_{LOAD} \times I_{ACL}$

Package Top Marking System Definition

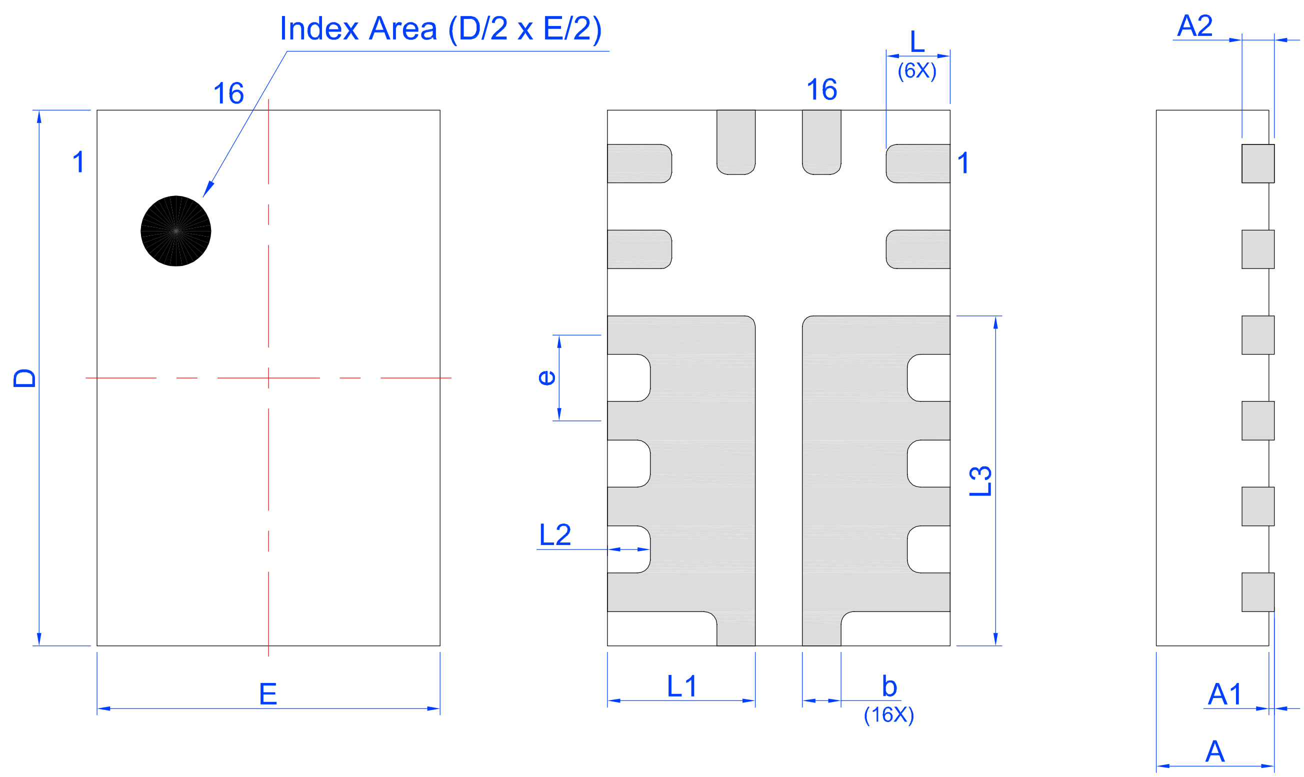


PPPPP - Part ID Field
WW - Date Code Field[1]
NNN - Lot Traceability Code Field[1]
A - Assembly Site Code Field [2]
RR - Part Revision Code Field[2]

Note 1: Each character in code field can be alphanumeric A-Z and 0-9
Note 2: Character in code field can be alphabetic A-Z

Package Drawing and Dimensions

16 Lead STQFN Package 1.6 mm x 2.5 mm (Fused Lead)



Top View BTM View Side View

Unit: mm

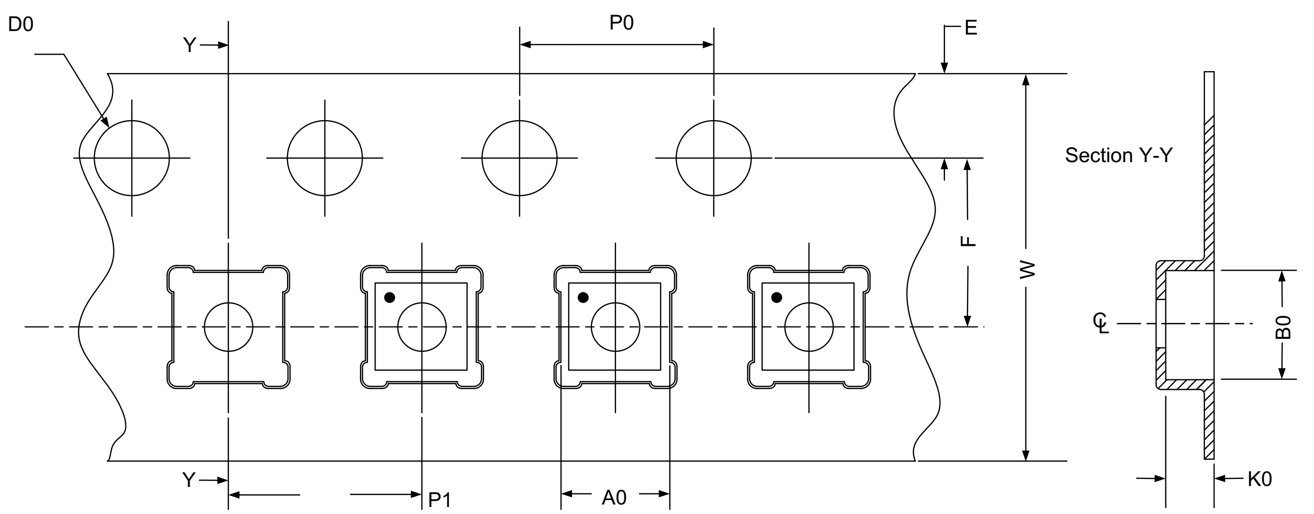
Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	2.45	2.50	2.55
A1	0.005	-	0.05	E	1.55	1.60	1.65
A2	0.10	0.15	0.20	L	0.25	0.30	0.35
b	0.13	0.18	0.23	L1	0.64	0.69	0.74
e	0.40 BSC			L2	0.15	0.20	0.25
				L3	1.49	1.54	1.59

Tape and Reel Specifications

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STQFN 16L 1.6x2.5mm 0.4P FCA Green	16	1.6x2.5x 0.55mm	3000	3000	178/60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

Package Type	PocketBTM Length	PocketBTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 16L 1.6x2.5mm 0.4P FCA Green	1.8	2.8	0.7	4	4	1.55	1.75	3.5	8



Refer to EIA-481 specification

Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 2.2 mm^3 (nominal). More information can be found at www.jedec.org.

Revision History

Date	Version	Change
2/23/2017	1.00	Production Release

Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits,General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.

Как с нами связаться

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