MAX77818

Dual Input, Power Path, 3A Switching Mode Charger with FG

General Description

The MAX77818 is a high-performance companion PMIC for the latest smartphones and tablet computers. The PMIC includes a dual input, smart power path 3.0A switch mode charger with reverse boost capability and adapter input protection up to $16V_{DC}$ withstand, proprietary ModelGauge™ (mg5) fuel gauge technology.

The switch mode battery charger's operating frequency is 4MHz and includes integrated, low-loss switches to provide the industry's smallest L/C size, lowest heat, and fastest battery charging programmable up to 3.0A. The charger has two inputs that accept adapter/USB (CHIN) and/or wireless type inputs (WCIN). The wireless input can simultaneously charge the battery while powering USB-OTG type accessories. The USB-OTG output provides true-load disconnect and is protected by an adjustable output current limit.

The battery charger includes smart power path and I^2C adjustable settings to accommodate a wide range of battery sizes and system loads. When external power is applied from either input, battery charging is enabled. With a valid input power source (adapter or wireless charger), the BYP pin voltage is equal to the input voltage minus resistive voltage drop. During battery-only reverse boost operation, the BYP output can be regulated with the reverse boost feature and provides up to 5V at 1.5A and requires no additional inductor, allowing the MAX77818 to power USB OTG accessories.

The switching charger is designed with a special CC, CV, and die temperature regulation algorithm. ModelGauge (mg5) provides accurate battery fuel gauging without calibration and operates with extremely low battery current.

The safeout LDO drive system USB interface devices.

The MAX77818 features a I^2C revision 3.0-compatible serial interface that comprises a bidirectional serial data line (SDA) and a serial clock line (SCL).

Applications

- Smartphones and Tablets
- Other Handheld Devices

Benefits and Features

- Dual Input Switchmode Battery Charger
  - Adapter/USB Input
    - Up to 13.4V Adapter Charging
    - Up to 4.0A rated, Input Current Protection (Programmable)
  - Wireless Charging Input
    - Up to 5.9V Wireless Charging
    - Up to 1.26A, Input Current Protection (Programmable)
    - Support USB-OTG Accessories
  - Battery Charge Current, Up to 3.0A
    - No Sense Resistor
    - CC, CV, and Die Temperature Control
    - Integrated Battery True-Disconnect FET
    - $R_{DS}(ON)$ = 12.8mΩ
    - Rated Up to $4.5A_{RMS}$, Discharge Current Limit (Programmable)
  - Reverse Boost Capability
    - Supports USB-OTG Accessories
    - Up to 5.1V/1.5A
    - Adjustable OCP
- ModelGauge (mg5) Battery Fuel Gauge
  - ±1% SOC Accuracy, No Calibration Cycles, Very Low I_Q
  - Time-to-Empty and Time-to-Full Prediction
- Two Safeout LDOs
- I^2C Serial Interface
- 72-Bump. 3.867mm x 3.608mm WLP with 0.4mm Pitch

***Ordering Information* appears at end of data sheet.**

19-6902; Rev 0; 6/15

Absolute Maximum Ratings

Switching Charger
CHGIN to GND ....-0.3V to +16V
BYP to GND ....-0.3V to +16V
WCIN, PVL, AVL, BAT_SP, BATT, SYS,
DETBATB to GND ....-0.3V to +6V
BST to PVL..-0.3V to +16V
BST to CHGLX ....-0.3V to +6V
WCINOKB, INOKB to GND ....-0.3V to SYS+0.3V
BAT_SN, CHGPG to GND ....-0.3V to +0.3V
CHGLX, CHGPG Continuous Current ....$3.5A_{RMS}$
SYS, BATT Continuous Current ....$4.5A_{RMS}$
CHGIN, BYP Continuous Current ....$4.0A_{RMS}$
WCIN Continuous Current..$1.5A_{RMS}$
Fuel Gauge
V_{BFG}, to GND ....-0.3V to +2.2V
THMB, THM to GND .... -0.3V to V_{AVL} + 0.3V

Safeout LDOs
SAFEOUT1, SAFEOUT2 to GND ....-0.3V to 6V
SAFEOUT1, SAFEOUT2 Continuous Current 100mA
I²C and Interface Logic
V_{IO} to GND...-0.3V to +6V
SDA, SCL to GND ....-0.3V to V_{IO}+0.3V
INTB to GND ....-0.3V to V_{SYS_A} + 0.3V
TEST_, V_{CCTEST}, SYS_ to GND...........................-0.3V to +6V
GND_ to GND ....-0.3V to +0.3V
Thermal Ratings
Operating Temperature Range.......................... -40°C to +85°C
Junction Temperature...+150°C
Storage Temperature Range .... -65°C to +150°C
Soldering Temperature (reflow).....................................+260°C
Continuous Power Dissipation (T_A = +70°C)
(derate 28.9mW/°C with 4L board, above 70°C)...........2.31W

CHGLX has internal clamp diodes to CHGPG and BYP. Applications that forward bias these diodes should take care not to exceed the IC's package power dissipation limits.

Package Thermal Characteristics (Note 1)

WLP
Junction-to-Ambient Thermal Resistance ($θ_{JA}$) ....34.6°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

General Electrical Characteristics

(V_{SYS} = +3.7V, C_{HGIN} = 0V , V_{IO} = 1.8V, T_A =-40°C to +85°C, unless otherwise noted. Limits are 100% production tested at T_A = +25°C . Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Shutdown Supply Current (BATT)		All circuits off V_{BATT} = 3.6V		23	50	µA
No Load Supply Current (BATT)		Fuel gauge is on All other circuits off, V_{BATT} = 3.6V		50	100	µA
SYS INPUT RANGE						
SYS Operating Voltage		Guaranteed by $V_{SYSUVLO}$ and $V_{SYSOVLO}$	2.8		5	V
SYS Undervoltage Lockout Threshold		V_{SYS} falling, 200mV hysteresis	2.45	2.5	2.55	V
SYS Overvoltage Lockout Threshold		V_{SYS} rising, 200mV hysteresis	5.2	5.36	5.52	V

Electrical Characteristics (continued)

General Electrical Characteristics

(V_{SYS} = +3.7V, C_{HGIN} = 0V , V_{IO} = 1.8V, T_A =-40°C to +85°C, unless otherwise noted. Limits are 100% production tested at T_A = +25°C . Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC AND CONTROL INPUT						
SCL, SDA Input Low Level		T_A = +25°C			0.3 x V_{IO}	V
SCL, SDA Input High Level		T_A = +25°C	0.7 x V_{IO}			V
SCL, SDA Input Hysteresis		T_A = +25°C		0.05 x V_{IO}		V
SCL, SDA Logic Input Current		V_{IO} = 3.6V	-10		+10	µA
SCL, SDA Input capacitance				10		pF
SDA Output Low Voltage		Sinking 20mA			0.4	V
Output Low Voltage INTB		I_{SINK} = 1mA			0.4	V
I^2C-COMPATIBLE INTERFACE TIMING FOR STANDARD, FAST, AND FAST-MODE PLUS (Note 2)						
Clock Frequency	f_{SCL}				1000	kHz
Hold Time (Repeated) START Condition	$t_{HD;STA}$		0.26			µs
CLK Low Period	t_{LOW}		0.5			µs
CLK High Period	t_{HIGH}		0.26			µs
Setup Time Repeated START Condition	$t_{SU;STA}$		0.26			µs
DATA Hold Time	$t_{HD:DAT}$		0			µs
DATA Valid Time	$t_{VD:DAT}$				0.45	µs
DATA Valid Acknowledge Time	$t_{VD:ACK}$				0.45	µs
DATA Setup Time	$t_{SU;DAT}$		50			ns
Setup Time for STOP Condition	$t_{SU;STO}$		0.26			µs
Bus Free Time Between STOP and START	t_{BUF}		0.5			µs
Pulse Width of Spikes that Must Be Suppressed by the Input Filter		(Note 3)		50		ns

Electrical Characteristics (continued)

General Electrical Characteristics

(V_{SYS} = +3.7V, C_{HGIN} = 0V , V_{IO} = 1.8V, T_A =-40°C to +85°C, unless otherwise noted. Limits are 100% production tested at T_A = +25°C . Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.)

PARAMETER	SYMBOL	CONDITIONS	C_B = 100pF			UNITS
			MIN	TYP	MAX	
I²C-COMPATIBLE INTERFACE TIMING FOR HS MODE (Note 2)						
Clock Frequency	f_{SCL}				3.4	MHz
Setup Time Repeated START Condition	$t_{SU;STA}$		160			ns
Hold Time (Repeated) START Condition	$t_{HD;STA}$		160			ns
CLK Low Period	t_{LOW}		160			ns
CLK High Period	t_{HIGH}		60			ns
DATA Setup time	$t_{SU;DAT}$		10			ns
DATA Hold Time	$t_{HD:DAT}$		0			ns
SCL Rise Time	t_{RCL}	T_A = +25°C	10		40	ns
Rise Time of SCL Signal After a Repeated START condition and After an Acknowledge Bit	t_{RCL1}	T_A = +25°C	10		80	ns
SCL Fall Time	t_{FCL}	T_A = +25°C	10		40	ns
SDA Rise Time	t_{RDA}	T_A = +25°C	10		80	ns
SDA Fall Time	t_{FDA}	T_A = +25°C			80	ns
Setup Time for STOP Condition	$t_{SU;STO}$		160			ns
Pulse Width of Spikes that Must be Suppressed by the Input Filter				10		ns

Switching Charger Electrical Characteristics

(V_{CHGIN} = 5V, V_{BATT} = 4.2V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = 25°C. Fast-charge current is set for 1.5A, done current is set for 150mA. Limits are 100% production tested at T_A = +25°C . Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CHGIN INPUT						
CHGIN Operating Voltage Range		Operating voltage	3.2		V_{OVLO}	V
WCIN Operating Voltage Range		Operating voltage	3.2		V_{OVLO}	V
CHGIN Overvoltage Threshold (Note 4)	$V_{CHGIN-OVLO}$	V_{CHGIN} rising	13.4	13.7	14	V
WCIN Overvoltage Threshold (Note 4)	$V_{WCIN-OVLO}$	V_{WCIN} rising	5.9		6	V
WCIN Overvoltage Threshold Hysteresis	$V_{WCINH-OVLO}$	V_{WCIN} falling		100		mV
CHGIN Overvoltage Threshold Hysteresis	$V_{CHGINH-OVLO}$	V_{CHGIN} falling		300		mV
WCIN/CHGIN Overvoltage Delay	T_{D-OVLO}	V_{WCIN/BUS_DET} rising, 100mV overdrive, not production tested		10		us
		V_{WCIN/BUS_DET} falling, 100mV overdrive, not production tested		20		us
WCIN/CHGIN to GND Minimum Turn-On Threshold Range (Note 4)	$V_{WCIN/CHGIN\_UVLO}$	V_{CHGIN} rising, 100mV hysteresis, programmable at 4.5V, 4.9V, 5.0V, 5.1V, WCIN input is disabled when valid CHGIN input is detected	4.5		5.1	V
WCIN/CHGIN to GND Minimum Turn-On Threshold Accuracy	$V_{WCIN/CHGIN\_UVLO}$	$V_{WCIN/CHGIN}$ rising, 4.5V setting	4.4	4.5	4.6	V
WCIN/CHGIN to SYS Minimum Turn-On Threshold (Note 4)	$V_{WCIN/CHGIN2SYS}$	V_{CHGIN} rising, 50mV hysteresis, WCIN input is disabled when valid CHGIN input is detected	V_{SYS} + 0.12	V_{SYS} + 0.20	V_{SYS} + 0.28	V
WCIN/CHGIN Turn-On Threshold Delay	T_{D-UVLO}	Not production tested		10		us
WCIN/CHGIN Adaptive Current Regulation Threshold Range (Note 5)	$V_{WCIN/CHGIN\_REG}$	Programmable at 4.3V, 4.7V, 4.8V, 4.9V	4.3		4.9	V
WCIN/CHGIN Adaptive Voltage Regulation Threshold Accuracy	$V_{WCIN/CHGIN\_REG}$	4.9V setting	4.8	4.9	5	V
CHGIN Current-Limit Range		Programmable, 500mA default, factory programmable option of 100mA, production tested at 100mA, 500mA, 1000mA, 1800mA, 4000mA settings only	0.1		4	A
WCIN Current-Limit Range		Programmable, 500mA default, factory programmable option of 100mA, production tested at 100mA, 250mA, 500mA, 1000mA settings only	0.06		1.26	A

Switching Charger Electrical Characteristics (continued)

(V_{CHGIN} = 5V, V_{BATT} = 4.2V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = 25°C. Fast-charge current is set for 1.5A, done current is set for 150mA. Limits are 100% production tested at T_A = +25°C . Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
WCIN or CHGIN Supply Current	I_{IN}	$V_{WCIN/CHGIN}$ = 2.4V, the input is undervoltage and R_{INSD} is the only loading		0.075		mA
		$V_{WCIN/CHGIN}$ = 5.0V, charger disabled		0.17	0.5	
		$V_{WCIN/CHGIN}$ = 5.0V, charger enabled, V_{SYS} = V_{BATT} = 4.5V, (no switching, battery charged)		2.7	4	
VWCIN or VCHGIN Input Current Limit	$I_{INLIMIT}$	V_{WCIN} or V_{CHGIN} = 5.0V, charger enabled, V_{BATT} = 3.8V, 100mA input current setting, T_A = +25°C	90	102	108	mA
		V_{WCIN} or V_{CHGIN} = 5.0V, charger enabled, V_{BATT} = 3.8V, 500mA Input current setting, T_A = +25°C	462.5	487.5	500	
		V_{WCIN} or V_{CHGIN} = 5.0V, charger enabled, V_{BATT} = 3.8V, 1000mA Input current setting, T_A = +25°C	950	975	1000	
		V_{WCIN} or V_{CHGIN} = 5.0V, charger enabled, V_{BATT} = 3.8V, 1000mA input current setting, T_A = 0°C to +85°C	926	975	1024	
VCHGIN Input Current Limit	$I_{INLIMIT}$	V_{CHGIN} = 5.0V, charger enabled, V_{BATT} = 3.8V, 1800mA input current setting, T_A = +25°C	1710	1755	1800	mA
		V_{CHGIN} = 5.0V, charger enabled, V_{BATT} = 3.8V, 1800mA input current setting, T_A = 0°C to +85°C	1667	1755	1843	
		V_{CHGIN} = 5.0V, charger enabled, V_{BATT} = 3.8V, 4000mA input current setting, T_A = +25°C	3800	3900	4000	
		V_{CHGIN} = 5.0V, charger enabled, V_{BATT} = 3.8V, 4000mA input current setting, T_A = 0°C to +85°C	3705	3900	4095	
WCIN, CHGIN Self-Discharge Down to UVLO Time	t_{INSD}	Time required for the charger input to cause a 10µF input capacitor to decay from 6.0V to 4.3V.		100		ms
WCIN, CHGIN Input Self-Discharge Resistance	R_{INSD}	For CHGIN, this resistor is disconnected from the CHGIN pin during MUIC microphone mode		35		kΩ
WCINOK/CHGINOK to Start Switching	t_{START}			150		ms

Switching Charger Electrical Characteristics (continued)

(V_{CHGIN} = 5V, V_{BATT} = 4.2V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = 25°C. Fast-charge current is set for 1.5A, done current is set for 150mA. Limits are 100% production tested at T_A = +25°C . Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SWITCH IMPEDANCES AND LEAKAGE CURRENTS							
CHGIN to BYP Resistance	R_{IN2BYP}	Bidirectional			0.0144	0.04	Ω
WCIN to BYP Resistance	$R_{WCIN2BYP}$				0.093	0.26	Ω
CHGLX High-Side Resistance	R_{HS}				0.0327	0.1	Ω
CHGLX Low-Side Resistance	R_{LS}				0.0543	0.14	Ω
BATT to SYS Dropout Resistance	$R_{BAT2SYS}$				0.0128	0.04	Ω
CHGIN to BATT Dropout Resistance	R_{IN2BAT}	Calculation estimates a 0.04Ω inductor resistance (R_L) $R_{IN2BAT} = R_{IN2BYP} + R_{HS} + R_L + R_{BAT2SYS}$			0.0999		Ω
CHGLX Leakage Current		CHGLX = CHGPG or BYP	T_A = +25°C		0.01	10	µA
			T_A = +85°C		1		µA
BST Leakage Current		V_{BST} = 5.5V	T_A = +25°C		0.01	10	µA
			T_A = +85°C		1		µA
BYP Leakage Current		V_{BYP} = 5.5V, V_{CHGIN} = 0V, V_{CHGLX} = 0V, charger disabled	T_A = +25°C		0.01	10	µA
			T_A = +85°C		1		µA
WCIN Leakage Current		V_{BYP} = 0V, V_{CHGIN} = 0V, V_{WCIN} = 5.5V	T_A = +25°C		0.01		µA
			T_A = +85°C		1		µA
SYS Leakage Current		V_{SYS} = 0V, V_{BATT} = 4.2V, charger disabled	T_A = +25°C		0.01	10	µA
			T_A = +85°C		1		µA

Switching Charger Electrical Characteristics (continued)

(V_{CHGIN} = 5V, V_{BATT} = 4.2V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = 25°C. Fast-charge current is set for 1.5A, done current is set for 150mA. Limits are 100% production tested at T_A = +25°C . Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
BATT Quiescent Current (I_{SYS} = 0A, I_{BYP} = 0A)	I_{MBAT}	V_{CHGIN} = 0V, V_{SYS} = 0V, V_{BATT} = 4.2V, QBAT is off	T_A = +25°C		20	30	µA
			T_A = +85°C		20		µA
		V_{CHGIN} = 0V, V_{BATT} = 4.2V, QBAT is on, main-battery overcurrent protection disabled	T_A = +25°C		15.3		µA
			T_A = +85°C		15.3		µA
		V_{CHGIN} = 0V, V_{BATT} = 4.2V, QBAT is on, main-battery overcurrent protection enabled	T_A = +25°C		20		µA
			T_A = +85°C		20		µA
		V_{SYS} = 4.2V, V_{BATT} = 0V, charger disabled	T_A = +25°C		0.01	10	µA
			T_A = +85°C		1		µA
	I_{MBDN}	V_{CHGIN} = 5V, V_{BATT} = 4.2V, QBAT is off, main-battery overcurrent protection disabled, Charger is enabled but in its done mode	T_A = +25°C		3	10	µA
			T_A = +85°C		3		µA
CHARGER DC-DC BUCK							
Minimum On-Time	$t_{ON\text{-}MIN}$				75		ns
Minimum Off-Time	t_{OFF}				75		ns
Current Limit (Note 6)	I_{LIM}	T_A = 0°C to +85°C I_{ND} = 0 (0.47µH inductor option) Production tested at I_{LIM} = 00 setting (Note 7)	I_{LIM} = 00 (3.00A out)	4.15	5.05	5.95	A
			I_{LIM} = 01 (2.75A out)		4.75		
			I_{LIM} = 10 (2.50A out)		4.45		
			I_{LIM} = 11 (2.25A out)		4.15		
		T_A = 0°C to +85°C I_{ND} = 1 (1.0µH inductor option) Production tested at I_{LIM} = 11 setting (Note 7)	I_{LIM} = 00 (3.00A out)		4.60		A
			I_{LIM} = 01 (2.75A out)		4.30		
			I_{LIM} = 10 (2.50A out)		4.00		
			I_{LIM} = 11 (2.25A out)	3.00	3.70	4.40	

Switching Charger Electrical Characteristics (continued)

(V_{CHGIN} = 5V, V_{BATT} = 4.2V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = 25°C. Fast-charge current is set for 1.5A, done current is set for 150mA. Limits are 100% production tested at T_A = +25°C . Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
REVERSE BOOST							
BYP Voltage Adjustment Range		2.5V < V_{BATT} < 4.5V. Adjustable from 3V to 5.75V, production tested at 3V, 5.0V and 5.75V settings		3		5.75	V
Reverse Boost Quiescent Current	I_{BYP}	Not switching: output forced 200mV above its target regulation voltage			1150		µA
Reverse Boost BYP Voltage in OTG Mode	$V_{BYP.OTG}$	5.1V setting		4.94	5.1	5.26	V
CHGIN Voltage in OTG Mode	$V_{CHGIN.OTG}$	Mode = 0x05 or 0x0F, WCIN switch is on, VCHGIN_REG = 4.9V, RIN2WCIN + RDSCHGIN < 300ml, OTG load current ≤ 450mA		4.75			V
CHGIN Output Current Limit	$I_{CHGIN.OTG.LIM}$	3.4V < V_{BATT} < 4.5V, T_A = +25°C	OTG_ILIM = 00	500		550	mA
			OTG_ILIM = 01	900		990	mA
			OTG_ILIM = 10	1200		1320	mA
			OTG_ILIM=11	1500		1650	mA
Reverse Boost Output Voltage Ripple		Discontinuous inductor current (i.e., skip mode)			±150		mV
		Continuous inductor current			±150		mV
CHARGER							
BATT Regulation Voltage Range	$V_{BATTREG}$	Programmable in 25mV steps (4 bits), production tested at 3.65V and 4.4V only.		3.65		4.7	V
BATT Regulation Voltage Accuracy		3.65V and 4.7V settings	T_A = +25°C	-0.75		+0.75	%
			T_A = 0°C to +85°C	-1		+1	%
Fast-Charge Current Program Range		0A to 3.0A in 50mA steps, production tested at 500,1000, 2000 and 3000mA settings		0		3	A
Fast-Charge Current Accuracy		Programmed currents ≥ 500mA, V_{BATT} > V_{SYSMIN} (short mode), production tested at 500mA, 800mA, 1000mA, 2000mA, 3000mA settings	T_A = +25°C	-2.5		+2.5	%
			T_A = 0°C to +85°C	-5		+5	%
		Programmed currents ≥ 500mA, V_{BATT} < V_{SYSMIN} (LDO mode), production test at 800mA		-10		+10	%

Switching Charger Electrical Characteristics (continued)

(V_{CHGIN} = 5V, V_{BATT} = 4.2V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = 25°C. Fast-charge current is set for 1.5A, done current is set for 150mA. Limits are 100% production tested at T_A = +25°C . Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Fast-Charge Currents	I_{FC}	T_A = +25°C, V_{BATT} > V_{SYSMIN}	Programmed for 3.0A	2925	3000	3075	mA
			Programmed for 2.0A	1950	2000	2050	mA
			Programmed for 1.0A	975	1000	1025	mA
			Programmed for 0.5A	487.5	500	512.5	mA
Low-Battery Prequalification Threshold	V_{PQLB}	V_{BATT} rising		2.8	2.9	3	V
Dead-Battery Prequalification Threshold	V_{PQDB}	V_{BATT} rising		1.9	2	2.1	V
Prequalification Threshold Hysteresis	V_{PQ-H}	Applies to both V_{PQLB} and V_{PQDB}			100		mV
Low-Battery Prequalification Charge Current	I_{PQLB}	Default setting = disabled		75	100	140	mA
Dead-Battery Prequalification Charge Current	I_{PQDB}			40	55	80	mA
Charger Restart Threshold Range	V_{RSTRT}	Adjustable, 100, 150, and 200; it can also be disabled		100	150	200	mV
Charger Restart Deglitch Time		10mV overdrive, 100ns rise time			130		ms
Top-Off Current Program Range		Programmable from 100 to 350mA in 8 steps.		100		350	mA
Top-Off Current Accuracy (Note 8)		Gain				5	%
		Offset				20	mA
Charge Termination Deglitch Time	t_{TERM}	2mV overdrive, 100ns rise/fall time			30		ms
Charger State Change Interrupt Deglitch Time	t_{SCIDG}	Excludes transition to timer fault state, watchdog timer state			30		ms
Charger Soft-Start Time	t_{SS}				1.5		ms

Switching Charger Electrical Characteristics (continued)

(V_{CHGIN} = 5V, V_{BATT} = 4.2V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = 25°C. Fast-charge current is set for 1.5A, done current is set for 150mA. Limits are 100% production tested at T_A = +25°C . Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SMART POWER SELECTOR							
BATT to SYS Reverse Regulation Voltage	V_{BSREG}	I_{BATT} = 10mA			30		mV
		I_{BATT} = 1A			60		mV
		Load regulation during the reverse regulation mode			30		mV/A
Minimum SYS Voltage Accuracy	V_{SYSMIN}	Programmable from 3.4V to 3.7V in 100mV steps, V_{BATT} = 2.8V, tested at 3.4V and 3.7V settings		-3		3	%
Maximum SYS Voltage	V_{SYSMAX}	The maximum system voltage: V_{SYSMAX} = V_{BATREG} + $R_{BAT2SYS}$ x I_{BATT}	V_{BATREG} = 4.2V, I_{BATT} = 3.0A		4.245	4.32	V
		The maximum system voltage: V_{SYSMAX} = V_{BATREG} + $R_{BAT2SYS}$ x I_{BATT}.	V_{BATREG} = 4.7V, I_{BATT} = 3.0A		4.745	4.82	V
WATCHDOG TIMER							
Watchdog Timer Period	t_{WD}			80			s
Watchdog Timer Accuracy				-20	0	+20	%
CHARGE TIMER							
Prequalification Time	t_{PQ}	Applies to both low-battery prequalification and dead-battery prequalification modes			35		min
Fast-Charge Constant Current + Fast-Charge Constant Voltage Time	t_{FC}	Adjustable from 4hrs to 16hrs in 2 hour steps including a disable setting			8		hrs
Top-Off Time	t_{TO}	Adjustable from 0min to 70min in 10min steps			30		min
Timer Accuracy				-20		+20	%
AVL FILTER							
Internal AVL Filter Resistance					12.5		Ω

Switching Charger Electrical Characteristics (continued)

(V_{CHGIN} = 5V, V_{BATT} = 4.2V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = 25°C. Fast-charge current is set for 1.5A, done current is set for 150mA. Limits are 100% production tested at T_A = +25°C . Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
THERMAL FOLDBACK						
Junction Temperature Thermal Regulation Loop Setpoint Program Range	T_{JREG}	Junction temperature when charge current is reduced. Programmable from +85°C to +130°C in 15°C steps, default value is +100°C	85		130	°C
Thermal Regulation Gain	A_{TJREG}	The charge current is decreased 6.7% of the fast charge current setting for every degree that the junction temperature exceeds the thermal regulation temperature. This slope ensures that the full-scale current of 3.0A is reduced to 0A by the time the junction temperature is 20°C above the programmed loop set point. For lower programmed charge currents such as 500mA, this slope is valid for charge current reductions down to 100mA; below 100mA the slope becomes shallower but the charge current still reduced to 0A if the junction temperature is 20°C above the programmed loop set point.		-150		mA/°C
BATTERY OVERCURRENT PROTECTION						
Battery Overcurrent Threshold Range	I_{BOVCR}	Programmable from 3.0A to 4.5A in 0.25A steps, can be disabled	3		4.5	A
Battery Overcurrent Debounce Time	t_{BOVRC}	This is the response time for generating the overcurrent interrupt flag	3	6	10	ms
Battery Overcurrent Protection Quiescent Current	I_{BOVRC}			3 + I_{BATT} /22000		µA
System Power-Up Current	I_{SYSPU}		35	50	80	mA
System Power-Up Voltage	V_{SYSPU}	V_{SYS} rising, 100mV hysteresis	2	2.1	2.2	V
System Power-Up Response Time	t_{SYSPU}	Time required for circuit to activate from an unpowered state (i.e., main-battery hot insertion)		1		µs
SYSTEM SELF DISCHARGE WITH NO POWER						
BATT Self-Discharge Resistor				600		Ω
SYS Self-Discharge Resistor				600		Ω
Self-Discharge Latch Time				300		ms

Switching Charger Electrical Characteristics (continued)

(V_{CHGIN} = 5V, V_{BATT} = 4.2V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = 25°C. Fast-charge current is set for 1.5A, done current is set for 150mA. Limits are 100% production tested at T_A = +25°C . Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DETBATB, INOKB, WCINOKB							
DETBATB Logic Threshold	V_{IH}	4% hysterisis			0.8 x V_{IO}		V
Logic Input Leakage Current	$I_{DETBATB}$				0.1	1	µA
Output Low Voltage INOKB, WCINOKB		I_{SINK} = 1mA				0.4	V
Output High Leakage INOKB, WCINOKB		V_{SYS} = 5.5V	T_A = +25°C	-1	0	+1	µA
			T_A = +85°C		0.1		µA

Safeout LDOs Electrical Characteristics

(V_{SYS} = 2.8V to 4.5V, T_A = -40°C to 85°C, typical values are at T_A = +25°C, unless otherwise noted. Limits are 100% production tested at T_A = +25°C . Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SAFEOUT1						
Output Voltage (Default On)		5V < V_{CHGIN} < 5.5V, I_{OUT} = 10mA, SAFEOUT1 = 01 (default)	4.8	4.9	5	V
		SAFEOUT1 = 00		4.85		V
		SAFEOUT1 = 10		4.95		V
		SAFEOUT1 = 11		3.3		V
Maximum Output Current			60			mA
Output Current Limit			60	150	320	mA
Dropout Voltage		V_{CHGIN} = 5V, I_{OUT} = 60mA		120		mV
Load Regulation		V_{CHGIN} = 5.5V, 30µA < I_{OUT} < 30mA		50		mV
Quiescent Supply Current		Not production tested		72		µA
Output Capacitor for Stable Operation (Note 9)		0µA < I_{OUT} < 30mA, MAX ESR = 50mΩ		1		µF
Minimum Output Capacitor for Stable Operation (Note 9)		0µA < I_{OUT} < 30mA, MAX ESR = 50mΩ		0.7		µF
Internal Off-Discharge Resistance				1200		Ω

Safeout LDOs Electrical Characteristics (continued)

(V_{SYS} = 2.8V to 4.5V, T_A = -40°C to 85°C, typical values are at T_A = +25°C, unless otherwise noted. Limits are 100% production tested at T_A = +25°C . Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SAFEOUT2						
Output Voltage (Default Off)		5V < V_{CHGIN} < 5.5V, I_{OUT} = 10mA, SAFEOUT2 = 01 (default)	4.8	4.9	5	V
		SAFEOUT2 = 00		4.85		V
		SAFEOUT2 = 10		4.95		V
		SAFEOUT2 = 11		3.3		V
Maximum Output Current			60			mA
Output Current Limit			60	150	320	mA
Dropout Voltage		V_{CHGIN} = 5V, I_{OUT} = 60mA		120		mV
Load Regulation		V_{CHGIN} = 5.5V, 30µA < I_{OUT} < 30mA		50		mV
Quiescent Supply Current		Not production tested		72		µA
Output Capacitor for Stable Operation (Note 9)		0µA < I_{OUT} < 30mA, MAX ESR = 50mΩ		1		µF
Minimum Output Capacitor for Stable Operation (Note 9)		0FA < I_{OUT} < 30mA, MAX ESR = 50mΩ		0.7		µF
Internal Off-Discharge Resistance				1200		Ω

Note 9: Not production tested.

Fuel Gauge Electrical Characteristics

(V_{SYS} = 2.8V to 4.5V, T_A = -40°C to 85°C, typical values are at T_A = +25°C, unless otherwise noted. Limits are 100% production tested at T_A = +25°C . Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{DD0}	Fuel gauge shut down (Note 10)		0.5		µA
	I_{DD1}	Fuel gauge active, average with 7.5% ADC duty cycle (Note 10)		35	70	µA
ADC Duty Cycle	Duty			7.5		%
Parameter Capture Rate	t_{ACQ}	Period of ADC activation loop		0.1758		s
Regulator Output	V_{BFG}		1.5	1.8	1.98	V
VOLTAGE CHANNEL						
V_{BATT} Measurement Error	V_{GERR}	V_{BATT} = 2.8V to 4.5V, T_A = +25°C	-7.5		+7.5	mV
		T_A = -40°C to +85°C	-20		+20	mV
V_{BATT} Measurement Resolution	V_{LSB}			1.25		mV
V_{BATT} Measurement Range	V_{RANGE}		2.8		4.98	V

Fuel Gauge Electrical Characteristics (continued)

(V_{SYS} = 2.8V to 4.5V, T_A = -40°C to 85°C, typical values are at T_A = +25°C, unless otherwise noted. Limits are 100% production tested at T_A = +25°C . Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
CURRENT CHANNEL							
Current Measurement Resolution	I_{LSB}				1.25		mA
Current Measurement Range	I_{RANGE}			-3.6		+3.6	A
Current Measurement Offset	I_{OERR}	Long term average at zero input current			±0.25		mA
Current Measurement Symmetrical Error	I_{SERR}	(Notes 11, 12, 13)			2%		%
Current Measurement Asymmetrical Error	I_{AERR}	±3000mA	(Notes 12, 13, 14)	-150		+150	mA
		±1000mA		-20		+20	
		±300mA		-9.5		+9.5	
Linear Regulator Mode Current Measurement Error	I_{LRERR}	+1500mA	(Note 15)	-225		+225	mA
		+100mA		-40		+40	
Time-Base Accuracy	t_{ERR}	V_{SYS} = 3.7V at T_A = +25°C			±1		%
		T_A = -40°C to +85°C		-3.5		+3.5	
THERMAL CHANNEL							
Ratiometric Measurement Accuracy, THM	T_{GERR}	(Note 13)		-0.5		+0.5	% of full scale
Ratiometric Measurement Resolution, THM	T_{LSB}				0.0244		% of full scale
THMB Output Drive	V_{OH_THMB}	I_{OH_THMB} = -0.5mA		V_{AVL} - 0.1			V
THMB Precharge Time	t_{PRE_THMB}				12.7		ms
THMB Operating Range	V_{THMB}			2.8		V_{AVL}	V
THMB Input Leakage	I_{IN_THMB}	V_{THMB} = 5V		-1		+1	µA
THM Input leakage	I_{IN_THM}			-1		+1	µA

Electrical Characteristics (continued)

Note 2: Design guidance only, not tested during final test.
Note 3: Input filters on the SDA and SCL inputs suppress noise spikes of less than 50ns.
Note 4: The CHGIN input must be less than V_{OVLO} and greater than both V_{CHGIN_UVLO} and $V_{CHGIN2SYS}$ for the charger to turn-on.
Note 5: The input voltage regulation loop decreases the input current to regulate the input voltage at V_{CHGIN_REG}. If the input current is decreased to $I_{CHGIN\_REG\_OFF}$ and the input voltage is below V_{CHGIN_REG}, then the charger input is turned off.
Note 6: Production tested to ¼ of the threshold with LPM bit = 1 (¼ FET configuration).
Note 7: Production tested in charger DC-DC low-power mode (CHG_LPM bit = 1).
Note 8: Not production tested. **Note 10:** The total chip supply current includes the charger supply current in addition to the supply current for the fuel gauge.
Note 11: Symmetrical error is the sum of odd order errors in the measured values at two inputs symmetrical around zero; for example, ISERR_0.3A = (Error 0.3A - Error -0.3A)/2/0.3A x 100.
Note 12: Total current measurement error is the sum of the symmetrical and asymmetrical errors. Fuel gauge accuracy is sensitive to asymmetrical error but insensitive to symmetrical error.
Note 13: Current and ratiometric measurement errors are production tested at V_{SYS} = 3.7V and guaranteed by design at V_{SYS} = 2.8V and 4.5V.
Note 14: Asymmetrical error is the sum of even order errors in the measured values at two inputs symmetrical around zero; for example IAERR_0.3A = (Error 0.3A + Error -0.3A)/2.
Note 15: Total linear regulator mode current measurement error is simply the total error with respect to the input. This mode exists for a short duration when charging an empty battery, hence this error has limited consequence.

Pin Configuration

TOP VIEW
(BUMP SIDE DOWN)

MAX77818

	1	2	3	4	5	6	7	8	9
A	+ N.C.	TEST4	SDA	SCL	WCINOKB	GND_Q	WCIN	WCIN	N.C.
B	VCC_TEST	TEST3	TEST5	TEST6	VIO	DETBATB	SAFEOUT2	BYP	SAFEOUT1
C	TEST1	TEST2	INTB	N.C.	INOKB	N.C.	BYP	CHGIN	CHGIN
D	GND_A	GND_A	GND_A	GND_A	GND_A	AVL	BYP	CHGIN	CHGIN
E	SYS_A	N.C.	GND_D	N.C.	SYS	N.C.	PVL	BYP	BYP
F	VBFG	SYS_A	N.C.	N.C.	SYS	BAT_SN	BST	CHGLX	CHGLX
G	THMB	N.C.	BATT	BATT	SYS	BAT_SP	CHGR GSUB	CHGLX	CHGLX
H	N.C.	THM	BATT	BATT	SYS	SYS	CHGPG	CHGPG	CHGPG

WLP
(72 BUMPS WLP 9X8 BUMP ARRAY 0.4MM PITCH)

N/C PINS ARE FLOATING AND CAN BE CONNECTED AT BOARD-LEVEL IF NEEDED.

ALL TEST PINS (TEST1-6 AND VCCTEST) SHOULD BE GROUNDED IN THE END-USE APPLICATION.

*TOP VIEW = WAFER BACK-SIDE VIEW (BUMPS NOT VIEWABLE)

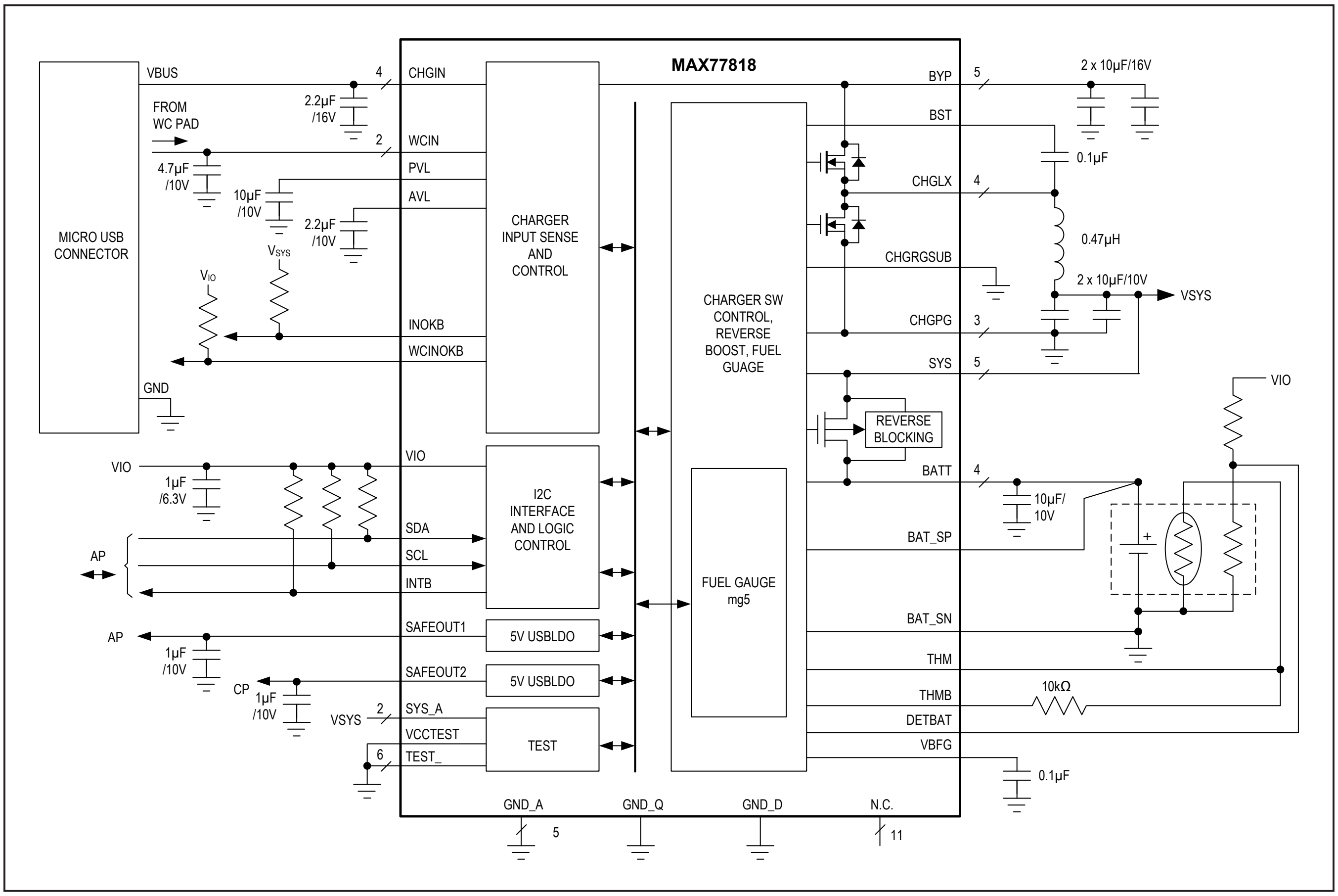
Pin Description

PIN	NAME	FUNCTION
A1, A9, C4, C6, E2, E4, E6, F3, F4, G2, H1	N.C.	No Connection
A2	TEST4	Test I/O Pin. Ground this pin in the application.
A3	SDA	I^2C Serial Data. Add an external 2.2kΩ pullup resistor to V_{IO}.
A4	SCL	I^2C Serial Clock. Add an external 2.2kΩ pullup resistor to V_{IO}.
A5	WCINOKB	Wireless Charger Input Valid, Active-Low Logic Output Flag. Open-drain, active-low output that indicates when valid voltage is present at WCIN and SYS.
A6	GND_Q	Quiet Ground. Short to GND_A and GND_D.
A7, A8	WCIN	Wireless Charger Input. $6V_{DC}$ protected input pin connected to Wireless charger power source. The wireless charger may be active during OTG mode, or disabled using the WCINSEL bit. Connect a 4.7µF/10V ceramic capacitor from WCIN to GND plane
B1	V_{CCTEST}	Test Mux Supply. Ground this pin in the application.
B2	TEST3	Test I/O. Ground this pin in the application.
B3	TEST5	Test I/O. Ground this pin in the application.
B4	TEST6	Test I/O. Ground this pin in the application.
B5	V_{IO}	Digital I/O Supply Input for I^2C Interface.
B6	DETBATB	Battery Detection Active-Low Input. Connect this pin to the ID pin on the battery pack. If DETBATB is pulled below 80% of the externally applied V_{IO} voltage, this is an indication that the battery is present and the charger starts when valid CHGIN and/or WCIN power is present. If DETBATB is driven high to VIO voltage or left unconnected, this is an indication that the battery is not present and the charger does not start. DETBATB is pulled high to V_{IO} pin through an off-chip pullup resistor.
B7	SAFEOUT2	Safeout LDO2 Output. Default off. Bypass with a 1µF ceramic capacitor to GND.
B8, C7, D7, E8, E9	BYP	CHGIN Bypass. This pin can see up to OVP limit. Output of adapter Input current Limit block and input to switching charger. BYP is also the boost converter output when the charger is operating in reverse boost mode. Bypass with 2x10µF/16V ceramic capacitors from BYP to CHGPG ground plane.
B9	SAFEOUT1	Safeout LDO1 Output. Default 4.9V and on when CHGIN power is valid. Bypass with a 1µF ceramic capacitor to GND.
C1	TEST1	Test I/O. Ground this pin in the application.
C2	TEST2	Test I/O. Ground this pin in the application.
C3	INTB	Interrupt Output. Active-low, open-drain output. Add a 200kΩ pullup resistor to V_{IO}.
C5	INOKB	Charger Input Valid, Active-Low Logic Output Flag. Open-drain output indicates when valid voltage is present at both CHGIN and SYS or WCIN and SYS.

Pin Description (continued)

PIN	NAME	FUNCTION
C8, C9, D8, D9	CHGIN	Charger Input. The adapter/USB charger input may be active, or disabled using the CHGINSEL bit. Connect a 2.2μF/16V ceramic capacitor from CHGIN to GND plane.
D1–D5	GND_A	Analog Ground. Short to GND_D and GND_Q.
E3	GND_D	Digital Ground. Short to GND_A and GND_Q.
D6	AVL	Analog Voltage Level. Output of on-chip 5V LDO used to power on-chip, low-noise circuits. Bypass with a 2.2μF/10V ceramic capacitor to GND. Powering external loads from AVL is not recommended, other than pulldown resistors.
E1, F2	SYS_A	Analog SYS Input
E5, F5, G5, H5, H6	SYS	System Power Connection. Connect system loads to this node. Bypass with 2x10μF ceramic capacitors from SYS to CHGPG ground plane.
E7	PVL	Internal Bias Regulator High-Current Output Bypass. Supports internal noisy and high-current gate drive loads. Bypass to PGND with a minimum 10μF/10V ceramic capacitor.
F1	V_{BFG}	1.8V power supply output for Fuel Gauge. Bypass V_{BFG} with a 0.1μF ceramic capacitor, V_{BFG} is not intended to power external circuitry.
F6	BAT_SN	Battery Negative Differential Sense Connection. Connect to the negative or ground terminal close to the battery.
F7	BST	High-Side FET Driver Supply. Bypass BST to LX with a 0.1μF ceramic capacitor.
F8, F9, G8, G9	CHGLX	Charger Switching Node. Connect the inductor between CHGLX and SYS.
G1	THMB	Pullup Voltage for THM Pin Pullup Resistor. Can be switched to save power.
G3, G4, H3, H4	BATT	Battery Power Connection. Connect to the positive terminal of a single-cell (or parallel cell) Li Ion battery. Bypass BATT to CHGPG ground plane with a 10μF ceramic capacitor.
G6	BAT_SP	Battery Positive Differential Sense Connection. Connect to the positive terminal close to the battery.
G7	CHGRGSUB	Substrate Charger Ground Connection. Connect with GND_A.
H2	THM	Thermistor Connection. Determines battery temperature using ratiometric measurement.
H7–H9	CHGPG	Charger Power Ground Connection

Block Diagram



Detailed Description

System Faults

MAX77818 monitors the system for the following faults:

V_{SYS} undervoltage lockout

V_{SYS} overvoltage lockout

V_{SYS} Fault

The system monitors the V_{SYS} node for undervoltage and overvoltage. The following describes the IC behavior if any of these events is to occur.

V_{SYS} Undervoltage Lockout (VSYSUVLO)

When charger input is valid and SYS node falls below SYS UVLO, all charger and fuel gauge O type registers are reset and following happen:

when DEADBAT < SYS < UVLO (= 2.5V), QBAT is on and SYS is shorted to BAT.

when 0 < SYS < DEADBAT (= 2.0V), QBAT is off, but the charger pulls up SYS from BAT with a constant current of 50mA.

when charger input is invalid and battery is present.

when DEADBAT < SYS < UVLO (= 2.5V), QBAT is on and SYS is shorted to BAT.

when 0 < SYS < DEADBAT (= 2.0V), QBAT is off.

V_{SYS} Overvoltage Lockout (VSYSUVLO)

The absolute maximum ratings state that the SYS node withstands up to 6V. The SYS OVLO threshold is set to 5.36V (typ). Ideally, V_{SYS} should not exceed the battery charge termination threshold. Systems must be designed so that V_{SYS} never exceeds 4.8V (transient and steady-state). If the V_{SYS} should exceed $V_{SYSOVLO}$ during a fault, the MAX77818 resets the charger and fuel gauge O type registers.

INTB

The MAX77818 uses one interrupt pin: INTB. The interrupt is meant to indicate to the application processor that the status of MAX77818 has changed. The INTB signal is asserted whenever one or more interrupts are toggled, and those interrupts are not masked. The application processor reads the interrupts in two steps. First, the AP reads the INTSRC register. This is a read-only register that indicates which functional block is generating the interrupt (i.e., charger and FG). Depending on the result of the read, the next step is to read the actual interrupt registers pertaining to the functional block.

For example, if the application processor reads 0x02 from INTSRC register, it means the top-level MAX77818 block has an interrupt generated. The next step is to read the related interrupt register of the MAX77818 functional block.

The INTB pin becomes high (cleared) as soon as the read sequence of the last INT_ register that contains an active interrupt starts. FG interrupts are cleared by setting new threshold values. All interrupts can be masked to prevent the INTB from being asserted for masked interrupts. A mask bit in the INTM register implements masking. The INTSRC register can still provide the actual interrupt status of the masked interrupts, but the INTB pin is not asserted.

Charger, Safeout LDO, and Charger Type Detection Interaction

The charger type detection circuit performs charger type detection and gates whether or not the charger is enabled. The charger type detection circuit allows the charger to be enabled once charge detection is complete, depending on the type of charger detected and whether or not it is USB 2.0 compliant. A manual override bit allows the user to enable the charger regardless of the charger type detection circuit charger detection status.

SAFEOUT1 is enabled by default once charger detection is complete and CHGIN is valid regardless of DETBATB. SAFEOUT2 can also be enabled once the same conditions are met, and the user sets the ENSAFEOUT2 register bit.

Switching Mode Charger

Features:

- Complete Li+/Li-poly battery charger
- Prequalification, constant current, constant voltage
- 55mA dead-battery prequalification
- 100mA low-battery prequalification current
- Adjustable constant current charge
  - 0A to 3.0A in 50mA steps
  - ±5% accuracy
- Adjustable charge termination threshold
  - 100mA to 200mA in 25mA steps and 200mA to 350mA in 50mA steps
  - ±5% accuracy
- Adjustable battery regulation voltage
  - 3.625V to 4.700V in 25mV steps
  - ±0.5% accuracy at T = +25°C
  - ±1% accuracy
  - Remote differential sensing
- Synchronous switch-mode design
- Reverse boost mode with adjustable V_{BYP} from 3.0V to 5.8V
- Smart Power Selector™
  - Optimally distributes power between charge adapter, system, and main battery
  - When powered by a charge adapter, the main battery can provide supplemental current to the system
  - The charge adapter and can support the system without a main battery
- No external MOSFETs required
- Dual input
  - Reverse leakage protection prevents the battery leaking current to the inputs
  - 4.0A adapter input
    - 16V withstand, 14V operating
    - Adjustable input current limit (100mA to 4.0A in 33.3mA steps (CHGIN_ILIM), 500mA default)
    - Support AC-to-DC wall warts and USB adapters
  - 1.26A wireless charger input
    - 6V fault tolerant
    - Adjustable input current limit (60mA to 1.26A in 20mA steps (WCIN_ILIM), 500mA default)

Smart Power Selector is a trademark of Maxim Integrated Products, Inc.

- Charge safety timer
  - Selectable: 4hr to 16hr in 2hr steps plus a disable setting
- Die temperature monitor with thermal foldback loop
  - Selectable die temperature thresholds (°C): 70, 85,100, and 115
- Input voltage dropout control allows operation from high-impedance sources. Charge current is reduced so input is not pulled below 4.3V.
- BATT to SYS switch is 12.8mΩ (typ).
- Dead battery detection
- Short-circuit protection
  - Programmable BAT to SYS overcurrent threshold from 3.0A to 4.5A in 0.25A steps plus a disable setting
  - DISIBS bit allows the host to disable the battery to system discharge path to protect against a short-circuit
  - SYS short to ground
    - BUCK current is limited by by the ILIM current limit. BATT currents above the programmed by B2SOVRC threshold generate an interrupt. The host can then disable the battery to system discharge path by setting DISIBS.

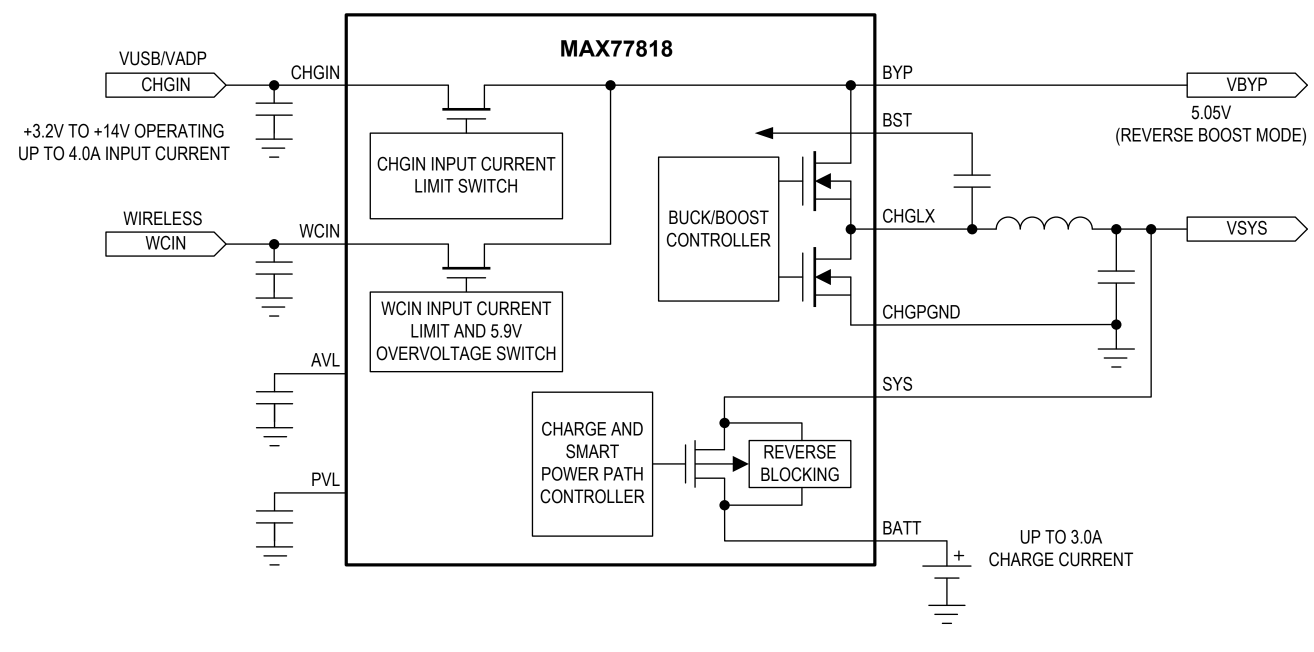


Figure 1. Simplified Functional Diagram

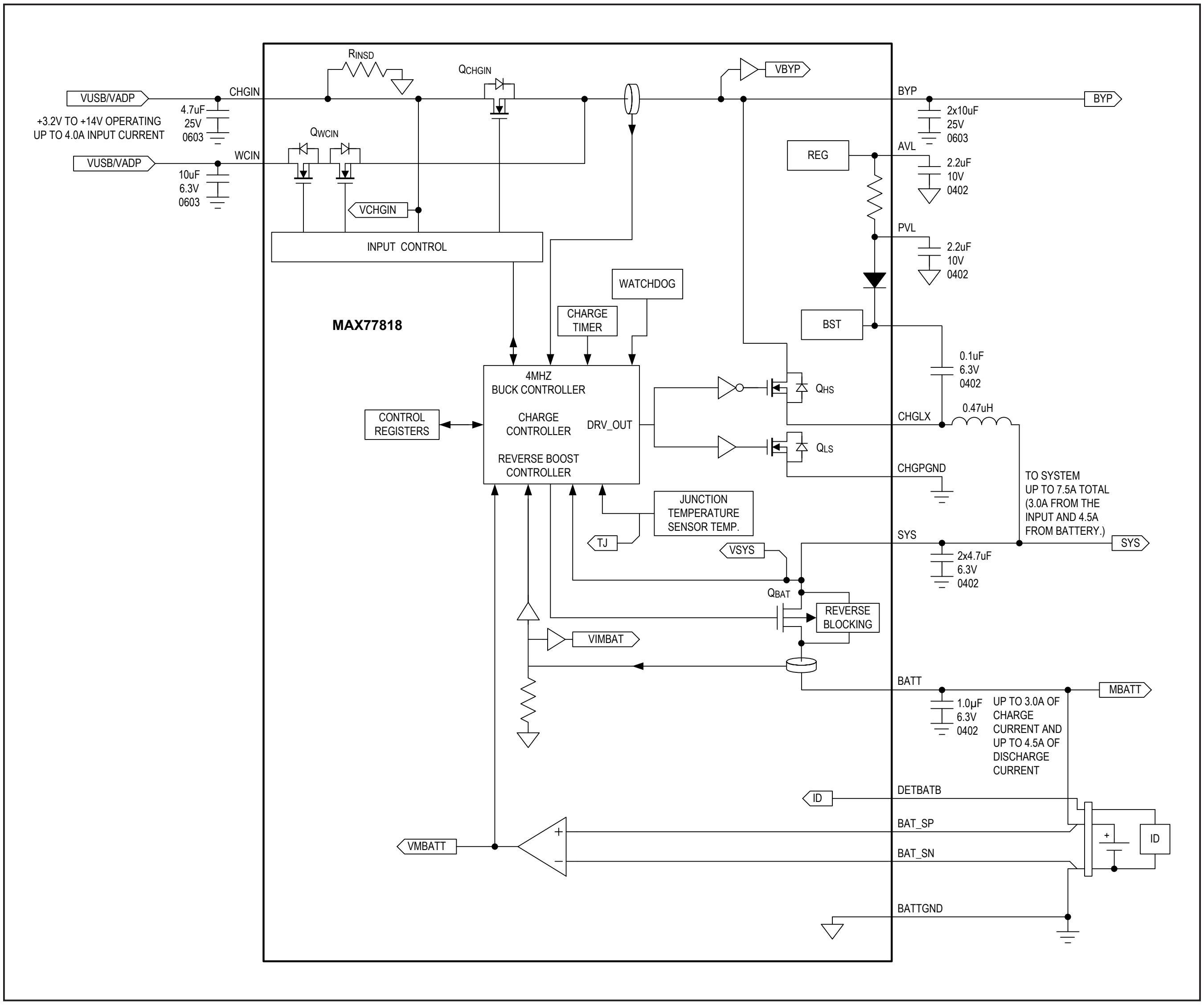


Figure 2. Main Battery Charger Detailed Functional Diagram

Detailed Description

The MAX77818 includes a full-featured switch-mode charger for a one-cell lithium ion (Li+) or lithium polymer (Li-poly) battery. As shown in Figure 2, the current limit for CHGIN input is independently programmable from 0 to 3.0A in 33.3mA steps allowing the flexibility for connection to either an AC-to-DC wall charger or a USB port. CHGIN current limit default is set between 100mA and 500mA with 500mA being the programmed default.

The synchronous switch-mode DC-DC converter utilizes a high 4.0MHz switching frequency which is ideal for portable devices because it allows the use of small components while eliminating excessive heat generation. The DC-DC has both a buck and a boost mode of operation. When charging the main battery the converter operation as a buck. The DC-DC buck operates from a 3.2V to 14V source and delivers up to 3.0A to the battery. Battery charge current is programmable from 0A to 3.0A. As a boost converter, the DC-DC uses energy from the main battery to boost the voltage at BYP. The boosted BYP voltage is useful to provide the supply the USB OTG voltage.

Maxim's Smart Power Selector architecture makes the best use of the limited adapter power and the battery's power at all times to supply up to 3.0A continuous (4A peak) from the buck to the system. Additionally, supplement mode provides additional current from the battery to the system up to $4.5A_{RMS}$. Adapter power that is not used for the system goes to charging the battery. All power switches for charging and switching the system load between battery and adapter power are included on chip. No external MOSFETs are required.

Maxim's proprietary process technology allows for low-R_{DSON} devices in a small solution size. The total dropout resistance from adapter power input to the battery is 0.0999Ω (typ) assuming that the inductor has 0.04Ω of ESR. This 0.0999Ω typical dropout resistance allows for charging a battery up to 3.0A from a 5V supply. The resistance from the BATT to SYS node is 0.0128Ω, allowing for low power dissipation and long battery life.

A multitude of safety features ensures reliable charging. Features include a charge timer, watchdog, junction thermal regulation, over/undervoltage protection, and short-circuit protection.

The BATT to SYS switch has overcurrent protection. See the *Main battery Overcurrent Protection* section for more information.

Smart Power Selector

The Smart Power Selector architecture is a network of internal switches and control loops that distributes energy between an external power source CHGIN, BYP, SYS, and BATT.

Figure 1 shows a simplified arrangement for the smart power selector's power steering switches. Figure 2 shows a more detailed arrangement of the smart power selector switches and gives them the following names: Q_{CHGIN}, Q_{HS}, Q_{LS}, and Q_{BAT}.

Switch and Control Loop Descriptions

Input Switch: Q_{CHGIN} provides the input current limit. The input switch is completely on and does not provide forward blocking. As shown in Figure 2, there are SPS control loops that monitor the current through the input switches as well as the input voltage.

DC-DC Switches: Q_{HS} and Q_{LS} are the DC-DC switches that can operate as a buck (step-down) or a boost (step-up). When operating as a buck, energy is moved from BYP to SYS. When operating as a boost, energy is moved from SYS to BYP. SPS control loops monitor the DC-DC switch current, the SYS voltage, and the BYP voltage.

Battery-to-System Switch: Q_{BAT} controls the battery charging and discharging. Additionally Q_{BAT} allows the battery to be isolated from the system (SYS). An SPS control loop monitors the Q_{BAT} current.

Control Bits

MODE configures the Smart Power Selector.

MINVSYS sets the minimum system voltage.

VBYPSET sets the BYP regulation voltage target.

B2SOVRC configures the main battery overcurrent protection.

Energy Distribution Priority:

With a valid external power source:

The external power source is the primary source of energy.

The main battery is the secondary source of energy.

Energy delivery to BYP is the highest priority.

Energy delivery to SYS is the second priority.

Any energy that is not required by BYP or SYS is available to the main battery charger.

With no power source available at CHGIN:

The main battery is the primary source of energy.

Energy delivery to BYP is the highest priority.

BYP includes the CHGIN if they are asked to supply energy in a USB OTG type of application.

Energy delivery to SYS is the second priority.

BYP Regulation Voltage

When the DC-DC is enabled in boost only mode (MODE = 0x08), the voltage from BYP to ground (V_{BYP}) is regulated to VBYPSET.

When the DC-DC is enabled in one of its USB OTG modes (MODE = 0x09 or MODE = 0x0A), V_{BYP} is set for 5.1V ($V_{BYP.ORG}$).

When the DC-DC is off or in one of its buck modes (MODE = 0x00 or MODE = 0x04 or MODE = 0x05) and there is a valid power source at CHGIN, $V_{BYP} = V_{CHGIN} - I_{CHGIN} \times R_{QCHGIN}$ When the DC-DC is off and there is no valid power source at CHGIN, BYP is connected to SYS with an internal 200Ω resistor. This 200Ω resistor keeps BYP biased as SYS and allows for the system to draw very light loads from BYP. IF the system loading on BYP is more than 1.0mA then the DC-DC should be operated in boost mode. Note that the inductor and the high-side switch's body diode are in parallel with the 200Ω from SYS to BYP.

SYS Regulation Voltage

When the DC-DC is enabled as a buck and the charger is disabled (MODE = 0x04), V_{SYS} is regulated to V_{BATREG} (CHG_CV_PRM) and Q_{BAT} is off.

When the DC-DC is enabled as a buck and the charger enabled but in a non-charging state such as done, watchdog suspend or timer fault (MODE = 0x05 and not charging), V_{SYS} is regulated to V_{BATREG} (CHG_CV_PRM) and Q_{BAT} is off.

When the DC-DC is enabled as a buck and charging in prequalification, fast-charge, or top-off modes (MODE = 0x05 and charging), V_{SYS} is regulated to V_{SYSMIN} when the $V_{BATT} < V_{SYSMIN}$; in this mode the Q_{BAT} switch acts like a linear regulator and dissipates power [$P = (V_{SYSMIN} - V_{BATT}) \times I_{BATT}$]. When $V_{BATT} > V_{SYSMIN}$, then $V_{SYS} = V_{BATT} - I_{BATT} \times R_{BAT2SYS}$; in this mode the Q_{BAT} switch is closed.

In all of the above modes, if the combined SYS and BYP loading exceed the input current limit, then V_{SYS} drops to $V_{BATT} - V_{BSREG}$ and the battery provides supplemental current. If the fuel gauge requests main battery information (voltage and current) during this supplement mode, then the Q_{BAT} switch is closed ($V_{SYS} = V_{BATT} - I_{BATT} \times R_{BAT2SYS}$) during the fuel gauge sample. If the fuel gauge wants requests continuous samples from the main battery during supplement mode, then the Q_{BAT} switch eventually opens when I_{BATT} decreases below 40mA.

When the DC-DC is enabled as a boost (MODE = 0x08 or 0x09 or 0x0A), then the QBAT switch is closed and $V_{SYS} = V_{BATT} - I_{BATT} \times R_{BAT2SYS}$

Battery Detect Input Pin (DETBATB)

DETBATB is tied to the ID pin of the battery pack. If DETBATB is pulled below 80% of V_{IO} pin voltage, this is an indication that the main battery is present and the battery charger starts upon valid CHGIN. If DETBATB is left unconnected or equal to V_{IO} voltage, this indicates that the battery is not present and the charger does not start upon valid CHGIN, see Figure 3. The DETBATB is internally pulled to BATT through an external resistor.

DETBATB status bit is valid when BATT is not present.

Input Validation

As shown in Figure 4, the charger input is compared with several voltage thresholds to determine if it is valid. A charger input must meet the following three characteristics to be valid:

CHGIN must be above V_{CHGIN_UVLO} to be valid.

CHGIN must be below its overvoltage lockout threshold (V_{OVLO}).

CHGIN must be above the system voltage by $V_{CHGIN2SYS}$.

CHGIN input generates a CHGIN_I interrupt when its status changes. The input status can be read with CHGIN_OK and CHGIN_DTLS. Interrupts can be masked with CHGIN_M.

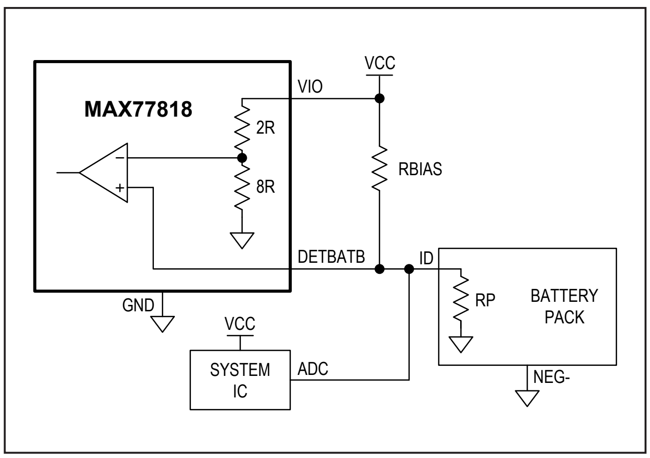


Figure 3. DETBATB Internal Circuitry and System Diagram

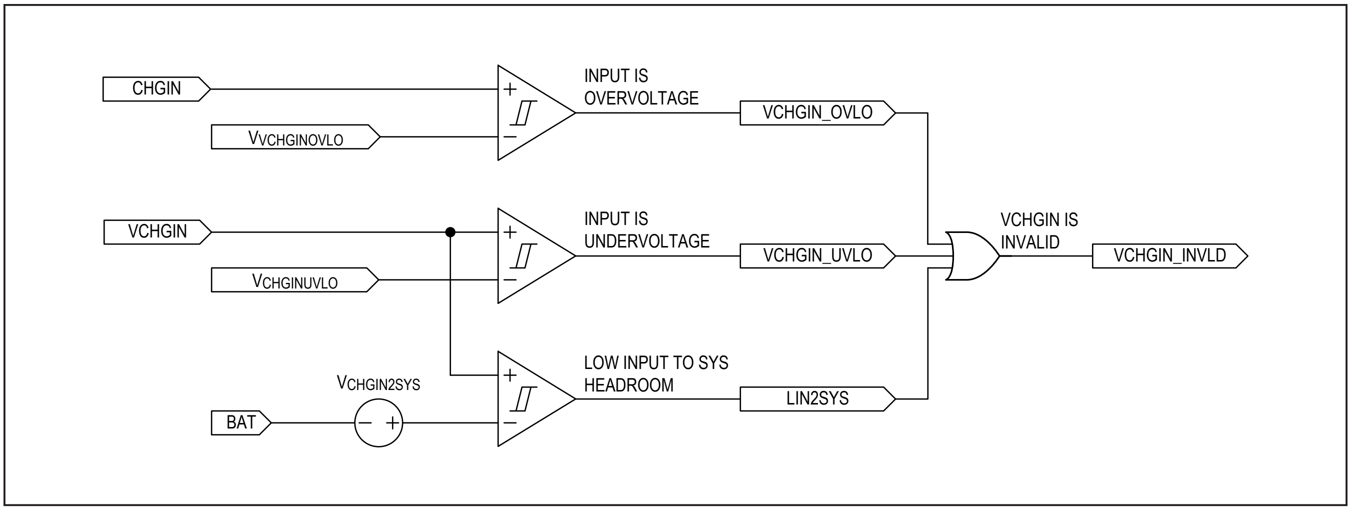


Figure 4. Charger Input Validation

Input Current Limit

The default settings of the CHGIN_ILIM and MODE control bits are such that when a charge source is applied to CHGIN, the MAX77818 turns its DC-DC converter on in BUCK mode, limit V_{SYS} to V_{BATREG}, and limit the charge source current to 500mA. All control bits are reset on global shutdown.

Input Voltage Regulation Loop

An input voltage regulation loop allows the charger to be well behaved when it is attached to a poor quality power source (CHGIN pin) or wireless charger (WCIN pin). The loop improves performance with relatively high-resistance charge sources that exist when long cables are used or devices are charged with noncompliant USB hub configurations. Additionally, this input voltage regulation loop improves performance with current limited adapters. If the MAX77818's input current limit is programmed above the current limit threshold of given adapter, the input voltage loop allows the MAX77818 to regulate at the current limit of the adapter. Finally, the input voltage regulation loop allows the MAX77818 to perform well with adapters that have poor transient load response times.

The input voltage regulation loop automatically reducing the input current limit in order to keep the input voltage at V_{CHGIN_REG}, V_{WCIN_REG}. If the input current limit is reduced to $I_{CHGIN\_REG\_OFF}$ (50mA typ) and the input voltage is below V_{CHGIN_REG}, then the charger input is turned off. V_{CHGIN_REG}, V_{WCIN_REG} is programmable with V_{CHGIN_REG} and V_{WCIN_REG}.

After operating with the input voltage regulation active, a BYP_I interrupt is generated, BYP_OK is cleared and BYP_DTLS = 0b1xxx. To optimize input power when working with a current limited charge source, monitor the BYP_DTLS while decreasing the input current limit. When the input current limit is set below the limit of the adapter, the input voltage rises. Although the input current limit is lowered, more power can be extracted from the input source when the input voltage is allowed to rise.

Example 1: Optimum use of the input voltage regulation loop along with a current limited adapter.

Sequence of Events

V_{BATT} = 3.2V, the system is operating normally

A 5.0V 1.2A current limited dedicated USB charger is applied to CHGIN.

The DC-DC buck regulator turns on, V_{SYS} is regulated to V_{BATREG} (4.2V) and the input is allowed to provide 100mA to the system.

The system detects that the charge source is a dedicated USB charger and enables the battery charger (MODE = 0x05) and programs an input current limit to 1.8A (CHGIN_ILIM = 0x36 = 1.8A).

The input current limit starts to ramp up from 100mA to 1.8A, but at the input current limit of the adapter (1.2A), the adapter voltage collapses. The MAX77818's input-voltage regulation loop prevents the adapter voltage from falling below 4.3V (V_{CHGIN_REG} = 4.3V). A BYP_I interrupt is generated and BYP_DTLS3 is set.

With the input voltage regulation loop active, the adapter provides 1.2A at 4.3V, which is a total of 5.04W being delivered to the system.

The system software detects that the input voltage regulation loop is active and it begins to ramp down the programmed input current limit. When the current limit ramps down to 1.167A (CHGIN_ILIM), the adapter is no longer in current limit and the adapter voltage increases from 4.3V to 5.0V.

With the adapter operating just below its current limit, it provides 1.167A at 5.0V which is a total of 5.84W to the system. This is 800mW more than when the adapter was in current limit.

Input Self-Discharge for Reliable Charger Input Interrupt

To ensure that a rapid removal and reinsertion of a charge source always results in a charger input interrupt, the charger input presents loading to the input capacitor to ensure that when the charge source is removed the input voltage decays below the UVLO threshold in a reasonable time. A 10μF input capacitance charged up to the maximum OVLO threshold (6.0V - V_{OVLO}) decays down to the minimum UVLO threshold (4.3V - $V_{CHGINx\_UVLO\_MIN}$) within 300ms (t_{INSD}). The input self-discharge is implemented by with a 30kΩ resistor (R_{INSD}) from CHGIN input to ground.

System Self-Discharge with No Power

To ensure a timely, complete, repeatable, and reliable reset behavior when the system has no power, the MAX77818 actively discharges the BATT and SYS nodes when the main battery is removed and V_{SYS} is less than $V_{SYSUVLO}$. As shown in Figure 5, the BATT and SYS discharge resistors are both 600Ω.

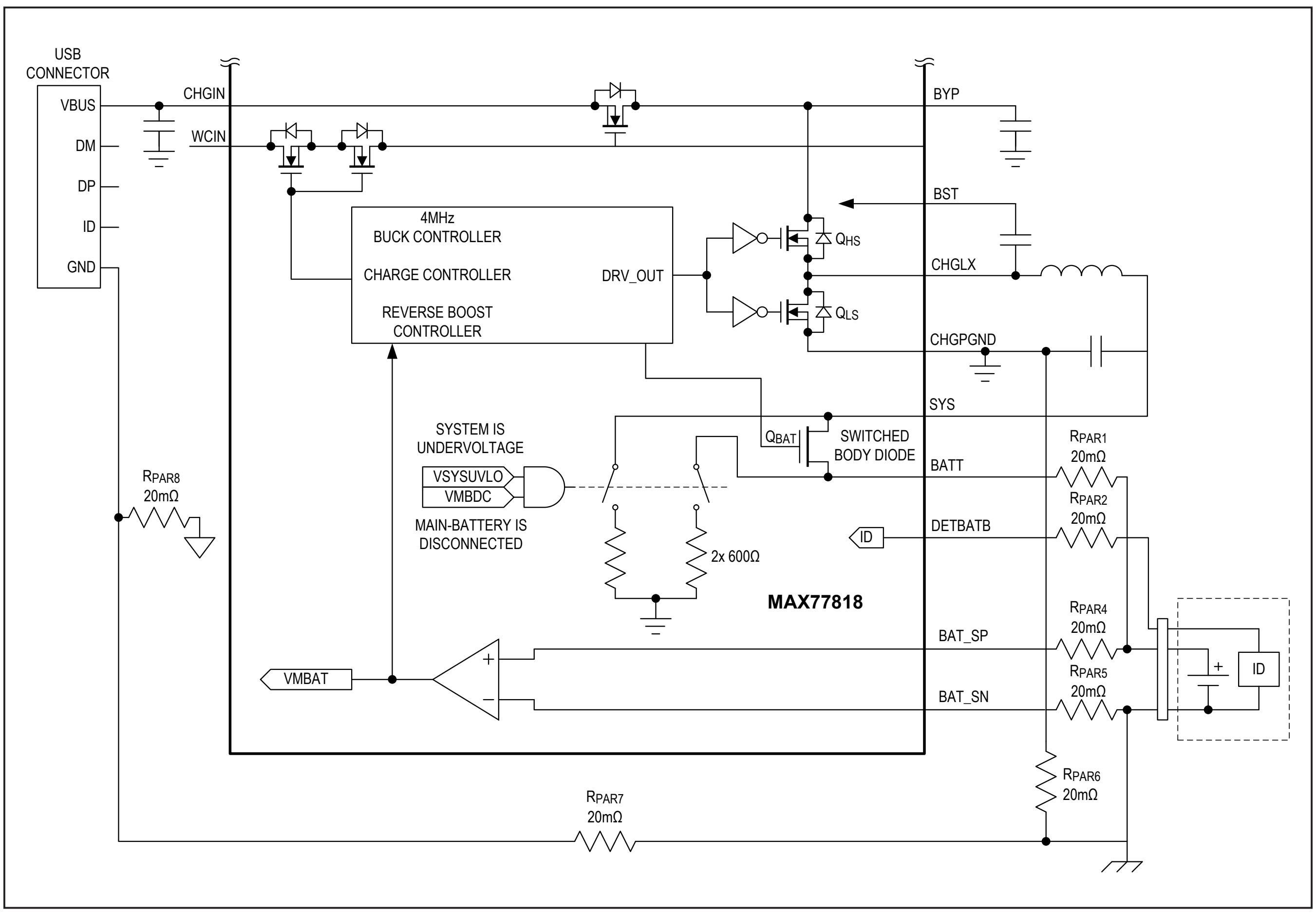
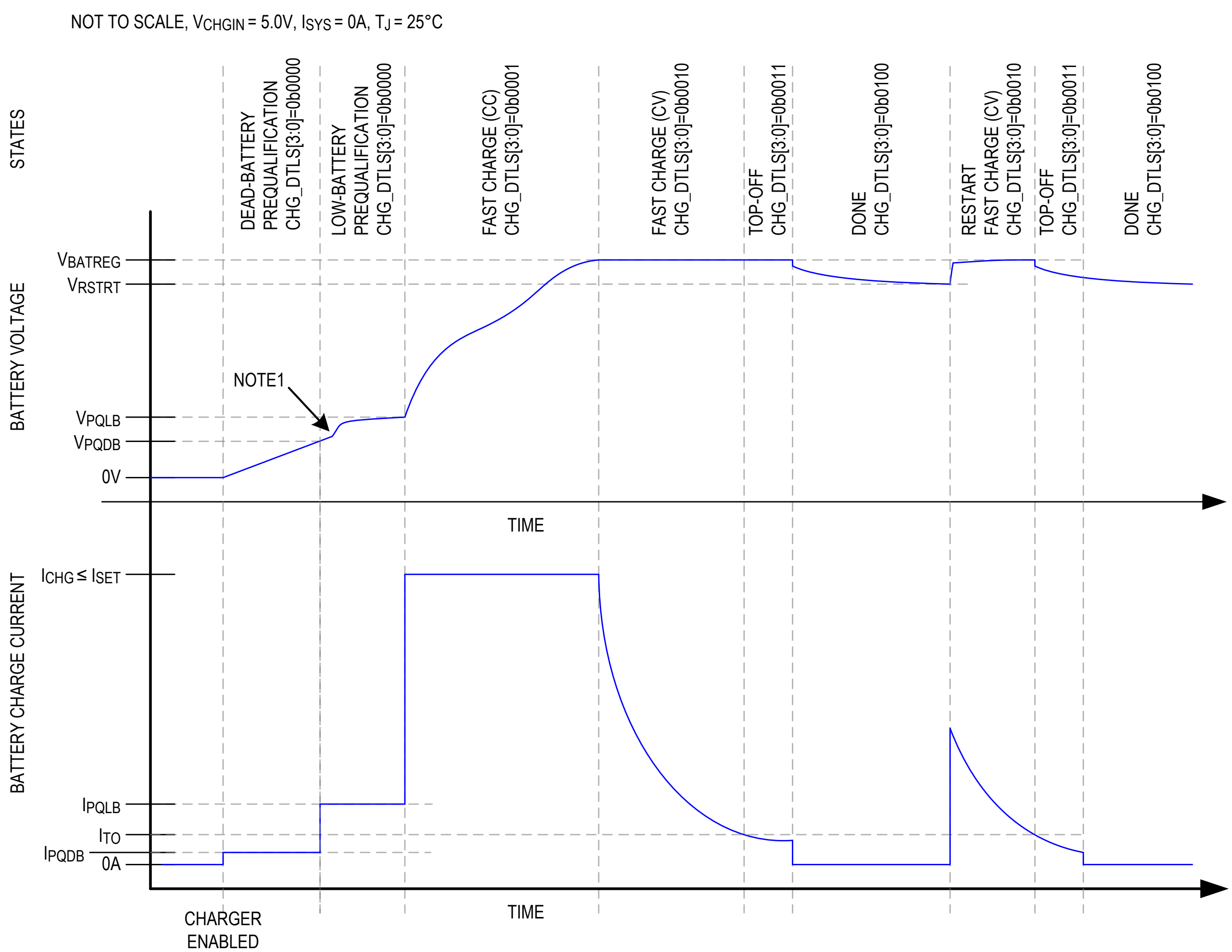


Figure 5. Main Battery Charger High-Current Paths with Typical Parasitic Resistances and Self-Discharging Resistors

Charge States

The MAX77818 utilizes several charging states to safely and quickly charge batteries as shown in Figure 6 and Figure 7. Figure 6 shows an exaggerated view of a Li+/Li-Poly battery progressing through the following charge states when there is not system load and the die and battery are close to room temperature: prequalification ➔ fast-charge ➔ top-off ➔ done.



NOTE 1: A TYPICAL LI+/LI-POLY HAS AN INTERNAL BATTERY PACK PROTECTION CIRCUIT THAT WILL OPEN THE BATTERY CONNECTION WHEN THE BATTERY'S CELL VOLTAGE IS LOWER THAN A DEAD BATTERY THRESHOLD ($V_{DB.FALLING}$~2.5V). TO GET THE PACK PROTECTION TO CLOSE AGAIN, THE CHARGER CHARGES THE BATTERY CAPACITOR WITH I_{PQDB} UNTIL THE VOLTAGE EXCEEDS V_{PQDB}. THEN THE CHARGER CHARGES THE BATTERY CAPACITOR WITH I_{PQLB}. WHEN THE BATTERY CAPACITOR'S VOLTAGE EXCEEDS $V_{DB.RISING}$~2.6V, THEN THE BATTERY PACK PROTECTION CIRCUIT CLOSES WHICH CONNECTS THE CELL TO THE CHARGER. $V_{DB.FALLING}$ AND $V_{DB.RISING}$ ARE NOT DETERMINED BY THE CHARGER – THEY ARE PROPERTIES OF THE BATTERY.

Figure 6. Li+/Li-Poly Charge Profile

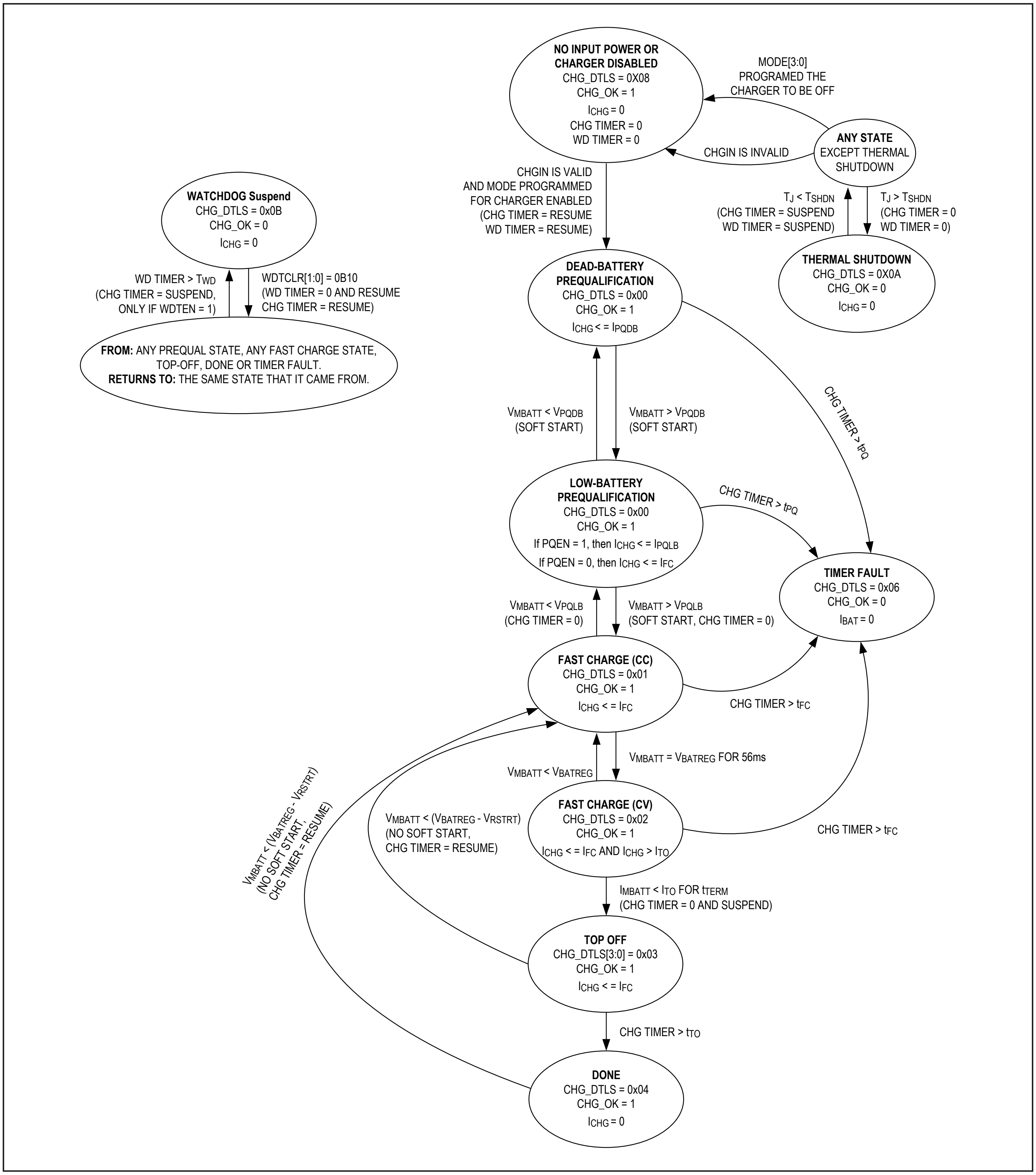


Figure 7. Charger State Diagram

No Input Power or Charger Disabled State

From any state shown in Figure 7 except thermal shutdown, the no input power or charger disabled state is entered whenever the charger is programmed to be off or the charger input CHGIN is invalid. After being in this state for t_{SCIDG}, a CHG_I interrupt is generated, CHG_OK is set and CHG_DTLS is set to 0x08

While in the no input power or charger disabled state, the charger current is 0mA, the watchdog and charge timers are forced to 0, and the power to the system is provided by either the battery or the adapter. When both battery and adapter power is available, the adapter provides primary power to the system and the battery contributes supplemental energy to the system if necessary.

To exit the no input power or charger disabled state, the charger input must be valid and the charger must be enabled.

Dead Battery Prequalificiation State

As shown in Figure 7, the dead battery prequalification state occurs when the main battery voltage is less than V_{PQDB}. After being in this state for t_{SCIDG}, a CHG_I interrupt is generated, CHG_OK is set and CHG_DTLS is set to 0x00. In the dead battery prequalification state charge current into the battery is I_{PQDB}.

Following events causes the state machine to exit this state:

The main battery voltage rises above V_{PQDB} and the charger enters the next state in the charging cycle: low battery prequalification.

If the battery charger remains in this state for longer than t_{PQ}, the charger state machine transitions to the timer fault state.

If the watchdog timer is not serviced, the charger state machine transitions to the watchdog suspend state.

Note that the dead battery prequalification state works with battery voltages down to 0V. The low 0V operation typically allows this battery charger to recover batteries that have an open internal pack protector. Typically a packs internal protection circuit opens if the battery has seen an over current, undervoltage, or overvoltage. When a battery with an open internal pack protector is used with this charger, the low battery prequalification mode current flows into the 0V battery. This current raises the pack's terminal voltage to the pointer where the internal pack protection switch closes.

Note that a normal battery typically stays in the low battery prequalification state for several minutes or less. Therefore, a battery that stays in low battery prequalification for longer than t_{PQ} may be experiencing a problem.

Fast-Charge Constant Current State

As shown in Figure 7, the fast-charge constant current (CC) state occurs when the main battery voltage is greater than the low battery prequalification threshold and less than the battery regulation threshold ($V_{PQLB} < V_{BATT} < V_{BATREG}$). After being in the fast-charge CC state for t_{SCIDG}, a CHG_I interrupt is generated, CHG_OK is set and CHG_DTLS = 0x01.

In the fast-charge CC state, the current into the battery is less than or equal to I_{FC}. Charge current can be less than I_{FC} for any of the following reasons:

The charger input is in input current limit.

The charger input voltage is low.

The charger is in thermal foldback.

The system load is consuming adapter current. Note that the system load always gets priority over the battery charge current.

Following events causes the state machine to exit this state:

When the main battery voltage rises above V_{BATREG}, the charger enters the next state in the charging cycle: fast charge (CV).

If the battery charger remains in this state for longer than t_{FC}, the charger state machine transitions to the timer fault state.

If the watchdog timer is not serviced, the charger state machine transitions to the watchdog suspend state.

The battery charger dissipates the most power in the fast-charge constant current state. This power dissipation causes the internal die temperature to rise. If the die temperature exceeds T_{REG}, I_{FC} is reduced.

Fast-Charge Constant Voltage State

As shown in Figure 7, the fast-charge constant voltage (CV) state occurs when the battery voltage rises to V_{BATREG} from the fast-charge CC state. After being in the fast-charge CV state for t_{SCIDG}, a CHG_I interrupt is generated, CHG_OK is set and CHG_DTLS = 0x02.

In the fast-charge CV state the battery charger maintains V_{BATREG} across the battery and the charge current is less than or equal to I_{FC}. As shown in Figure 6, charger current decreases exponentially in this state as the battery becomes fully charged.

The smart power selector control circuitry may reduce the charge current lower than the battery may otherwise consume for any of the following reasons:

The charger input is in input current limit.

The charger input voltage is low.

The charger is in thermal foldback.

The system load is consuming adapter current. Note that the system load always gets priority over the battery charge current.

Following events causes the state machine to exit this state:

When the charger current is below I_{TO} for t_{term}, the charger enters the next state in the charging cycle: TOP OFF.

If the battery charger remains in this state for longer than t_{FC}, the charger state machine transitions to the timer fault state.

If the watchdog timer is not serviced, the charger state machine transitions to the watchdog suspend state.

Top-Off State

As shown in Figure 7, the top-off state can only be entered from the fast-charge CV state when the charger current decreases below I_{TO} for t_{TERM}. After being in the top-off state for t_{SCIDG}, a CHG_I interrupt is generated, CHG_OK is set and CHG_DTLS = 0x03. In the top-off state the battery charger tries to maintain V_{BATREG} across the battery and typically the charge current is less than or equal to I_{TO}.

The smart power selector control circuitry can reduce the charge current lower than the battery is able to. Otherwise, consume for any of the following reasons:

The charger input is in input current limit.

The charger input voltage is low.

The charger is in thermal foldback.

The system load is consuming adapter current. Note that the system load always gets priority over the battery charge current.

Following events causes the state machine to exit this state:

After being in this state for the top-off time (t_{TO}), the charger enters the next state in the charging cycle: DONE.

If $V_{BATT} < V_{BATREG} - V_{RSTRT}$, the charger goes back to the FAST CHARGE (CC) state.

If the watchdog timer is not serviced, the charger state machine transitions to the watchdog suspend state.

Done State

As shown in Figure 7, the battery charger enters its done state after the charger has been in the top-off state for t_{TO}. After being in this state for t_{SCIDG}, a CHG_I interrupt is generated, CHG_OK is cleared and CHG_DTLS = 0x04.

Following events causes the state machine to exit this state:

If $V_{BATT} < V_{BATREG} – V_{RSTRT}$, the charger goes back to the fast charge (CC) state.

If the watchdog timer is not serviced, the charger state machine transitions to the watchdog suspend state.

In the done state, the charge current into the battery (I_{CHG}) is 0A. In the done state, the charger presents a very low load (I_{MBDN}) to the battery. If the system load presented to the battery is low (<< 100µA), then a typical system can remain in the done state for many days. If left in the done state long enough, the battery voltage decays below the restart threshold (V_{RSTRT}) and the charger state machine transitions back into the fast-charge CV state. There is no soft-start (di/dt limiting) during the done to fast-charge state transition.

Timer Fault State

The battery charger provides both a charge timer and a watchdog timer to ensure safe charging. As shown in Figure 7, the charge timer prevents the battery from charging indefinitely. The time that the charger is allowed to remain in its each of its prequalification states is t_{PQ}. The time that the charger is allowed to remain in the fast-charge CC and CV states is t_{FC} which is programmable with FCHGTIME. Finally, the time that the charger is in the top-off state is t_{TO}, which is programmable with TO_TIME. Upon entering the timer fault state a CHG_I interrupt is generated without a delay, CHG_OK is cleared and CHG_DTLS = 0x06.

In the timer fault state the charger is off. The charger can exit the timer fault state by programming the charger to be off and then programming it to be on again through the MODE bits. Alternatively, the charger input can be removed and reinserted to exit the timer fault state. See the any state bubble in the upper right of Figure 7.

Watchdog Timer

The battery charger provides both a charge timer and a watchdog timer to ensure safe charging. As shown in Figure 7, the watchdog timer protects the battery from charging indefinitely in the event that the host hangs or otherwise cannot communicate correctly. The watchdog timer is disabled by default with WDTEN = 0. To use the watchdog timer feature enable the feature by setting WDTEN. While enabled, the system controller must reset the watchdog timer within the timer period (t_{WD}) for the charger to operate normally. Reset the watchdog timer by programming WDTCLR = 0x01.

If the watchdog timer expires while the charger is in dead battery prequalification, low battery prequalification, fast charge CC or CV, top-off, done, or timer fault, the charging stops, a CHG_I interrupt is generated without a delay, CHG_OK is cleared, and CHG_DTLS indicates that the charger is off because the watchdog timer expired. Once the watchdog timer has expired, the charger can be restarted by programming WDTCLR = 0x01. The SYS node can be supported by the battery and/or the adapter through the DC-DC buck while the watchdog timer is expired.

Thermal Shutdown State

As shown in Figure 7, the thermal shutdown state occurs when the battery charger is in any state and the junction temperature (T_J) exceeds the device's thermal shutdown threshold (T_{SHDN}). When T_J is close to T_{SHDN}, the charger has folded back the input current limit to 0A so the charger and inputs are effectively off. Upon entering this state, CHG_I interrupt is generated without a delay, CHG_OK is cleared, and CHG_DTLS = 0x0A.

In the thermal shutdown state the charger is off and timers are suspended. The charger exits the temperature suspend state and returns to the state it came from once the die temperature has cooled. The timers resume once the charger exits this state.

Main Battery Differential Voltage Sense

As shown in Figure 2, BAT_SP and BAT_SN are differential remote sense lines for the main battery. To improve accuracy and decrease charging times, the battery charger voltage sense is based on the differential voltage between BAT_SP and BAT_SN.

Figure 5 shows the high-current paths of the battery charger along with some example parasitic resistances. A Maxim battery charger without the remote-sensing function would typically measure the battery voltage between BATT and GND. In the case Figure 5 with a charge current of 1A measuring from BATT to GND leads to a V_{BATT} that is 40mV higher than the real voltage because of R_{PAR1} and R_{PAR7} (I_{CHG} x (R_{PAR1} + R_{PQR7}) = 1A x 40mΩ = 40mV). Since the charger thinks the battery voltage is higher than it actually is, it will enter its fast-charge CV state sooner and the effective charge time may be extended by 10 minutes (based on real lab measurements). This charger with differential remote sensing does not experience this type of problem because BAT_SP and BAT_SN sense the battery voltage directly. To get the maximum benefit from these sense lines connect them as close as possible to the main battery connector.

OTG Mode

The DC-DC converter topology of the MAX77818 allows it to operate as a forward buck converter or as a reverse boost converter. The modes of the DC-DC converter are controlled with MODE. When MODE = 0x09 or 0x0A the DC-DC converter operates in reverse boost mode allowing it to source current to CHGIN. These two modes allow current to be sourced from CHGIN are commonly referred to as OTG modes (the term OTG is based off of the Universal Serial Bus's On the Go concept).

When MODE = 0x09 or 0x0A the DC-DC converter operates in reverse boost mode and regulates V_{BYP} to $V_{BYP.OTG}$ (5.1V typ) and the switch from BYP to CHGIN is closed. The current through the BYP to CHGIN switch is limited to the value programmed by OTG_ILIM. The two OTG_ILIM options allow for supplying 100mA or 500mA to an external load.. When the OTG mode is selected, the unipolar CHGIN transfer function measures current going out of CHGIN. When OTG mode is not selected, the unipolar CHGIN transfer function measures current going into CHGIN.

If the external OTG load at CHGIN exceeds $I_{CHGIN.OTG.ILIM}$, then a BYP_I interrupt is generated, BYP_OK = 0, and BYP_DTLS = 0bxxx1. In response to an overload at CHGIN during OTG mode operation, the BYP to CHGIN switch is latched off. The BYP to CHGIN switch will automatically try to retry in ~300ms. If the overload at CHGIN persists, then the switch will toggle on and off with ~30ms on and ~300ms off.

Main Battery Overcurrent Protection During System Power-Up

The main battery overcurrent protection during system power-up feature limits the main battery to system current to I_{SYSPU} as long as V_{SYS} is less than V_{SYSPU}. This feature limits the surge current that typically flows from the main battery to the device's low-impedance system bypass capacitors during a system power-up. System power-up is anytime that energy from the battery is supplied to SYS when $V_{SYS} < V_{SYSPU}$. This system power-up condition typically occurs when a battery is hot-inserted into an otherwise unpowered device. Similarly, the system power-up condition could occur when the DISIBS bit is driven low.

When system power-up occurs due to hot insertion into an otherwise unpowered device, a small delay of (t_{SYS-PU}) is required in order for this feature's control circuits to activate. A current spike over I_{SYSPU} can occur during this time.

Main Battery Overcurrent Protection Due to Fault

The MAX77818 protects itself, the battery, and the system from potential damage due to excessive battery discharge current. Excessive battery discharge current may occur in a smartphone for several reasons such as exposure to moisture, a software problem, an IC failure, a component failure, or a mechanical failure that causes a short circuit. The main battery overcurrent protection feature is enabled with B2SOVRC; disabling this feature reduces the main battery current consumption by I_{MBOVRC}.

When the main battery (BATT) to system (SYS) discharge current (I_{BATT}) exceeds the programmed overcurrent threshold for at least t_{MBOVRC}, a BAT_I interrupt is generated, BAT_OK is cleared, and BAT_DTLS reports and overcurrent condition. Typically when the system's processor detects this overcurrent interrupt it executes a housekeeping routine that tries to mitigate the overcurrent situation. If the processor cannot correct the overcurrent, then it can disable the BATT to SYS discharge path (B2S switch) by driving DISIBS bit to a logic high.

There are different scenarios of how the MAX77818 responds to setting the DISIBS bit high depending on the available power source and the state of the charger.

The MAX77818 is only powered from BATT and DISIBS bit is set.

SYS collapses and is allowed to go to 0V.

DISIBS holds state.

To exit from this state, plug in a valid input charger, then SYS is powered up, and the system wakes up.

The MAX77818 is powered from BATT and CHGIN, and the charger buck is not switching and DISIBS bit is set.

To exit from this state, plug in a valid input charger, then SYS is powered up and the system wakes up.

The MAX77818 is powered from BATT and CHGIN and the charger buck is switching and DISIBS bit is set.

The DISIBIS bit is ignored.

Thermal Management

The MAX77818 charger uses several thermal management techniques to prevent excessive battery and die temperatures.

Thermal Monitor

The user can monitor thermistor temperature using the fuel gauge and adjust the charger voltage/current as needed.

Thermal Foldback

Thermal foldback maximizes the battery charge current while regulating the MAX77818 junction temperature. As shown in Figure 8, when the die temperature exceeds the value programmed by REGTEMP (T_{JREG}), a thermal limiting circuit reduces the battery charger's target current by 105mA/°C (A_{TJREG}). The target charge current reduction is achieved with an analog control loop (i.e., not a digital reduction in the input current). When the thermal foldback loop changes state a CHG_I interrupt is generated and the system's microprocessor may want to read the status of the thermal regulation loop through the TREG status bit. Note that the thermal foldback loop being active is not considered to be abnormal operation and the thermal foldback loop status does not affect the CHG_OK bit (only information contained within CHG_DTLS affects CHG_OK).

Analog Low-Noise Power Input (AVL) and PVL

As shown in Figure 2, AVL is a regulated output from BYPC node. AVL is the power input for the MAX77818 charger's analog circuitry. PVL has a 12.5Ω resistor internal to the MAX77818 and a 10μF ceramic capacitor external bypass capacitor to isolate noises from AVL.

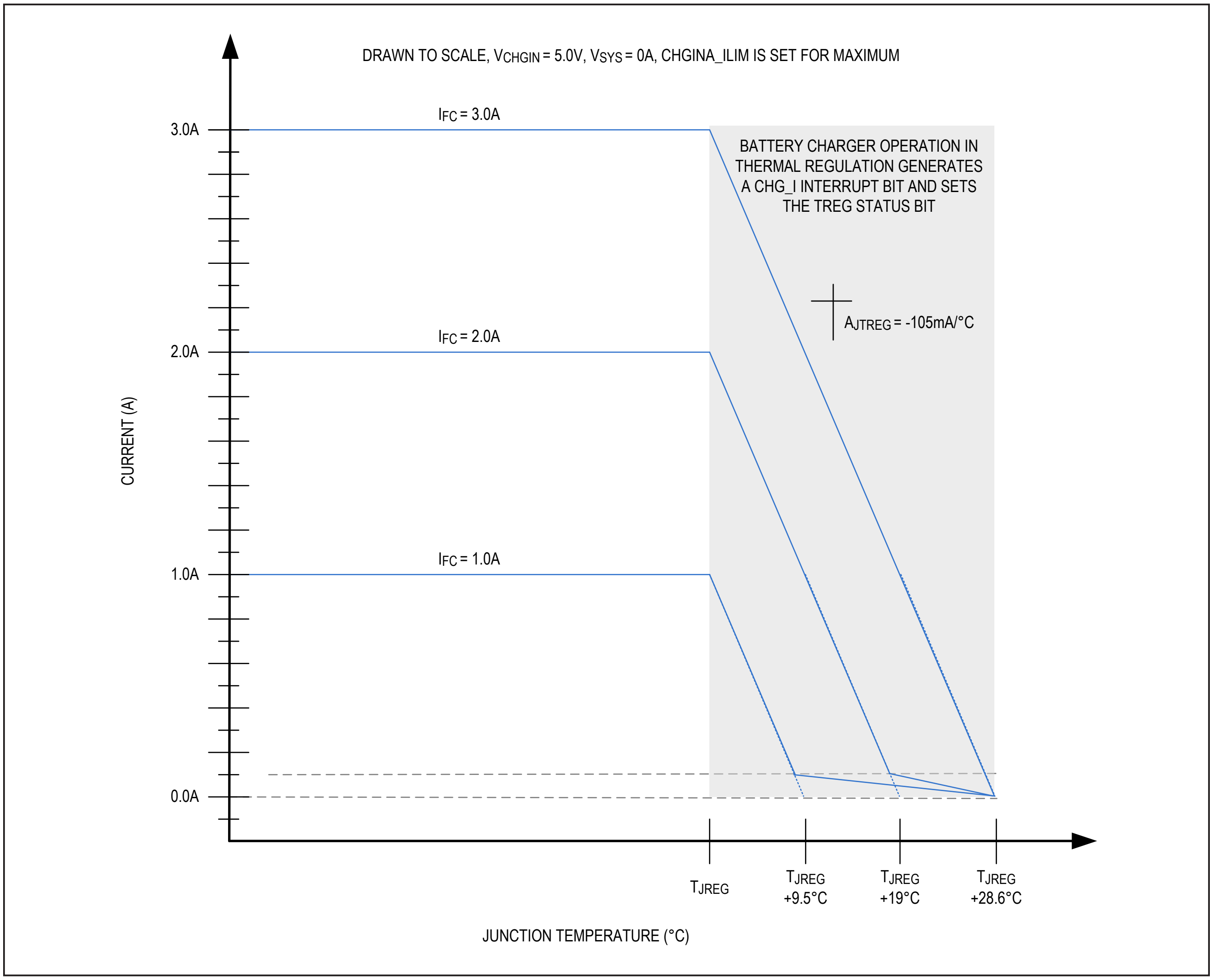


Figure 8. Charge Currents vs. Junction Temperature

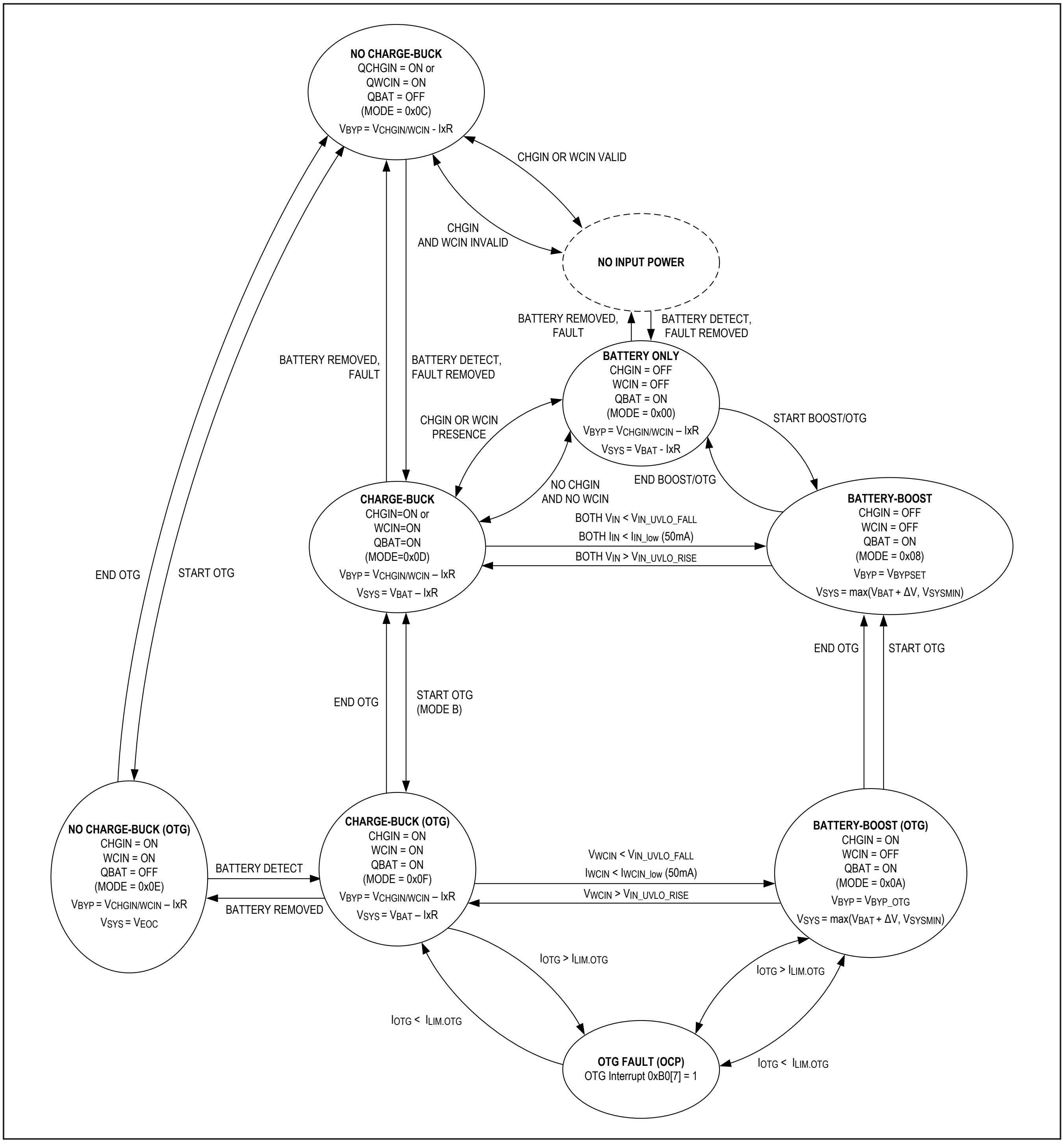


Figure 9: Power State Diagram

Power States

The MAX77818 transitions between power states as input/battery and load conditions dictate; see Figure 9.

The MAX77818 provides seven (7) power states and one (1) no power state (see the **TBD** section, register description CHG_CNFG_00 [3:0]). Under power-limited conditions, the power path feature maintains SYS and USB-OTG loads at the expense of battery charge current. In addition, the battery supplements the input power when required. As shown, transitions between power states are initiated by detection/removal of valid power sources, OTG events, and under-voltage conditions. Details of the BYP and SYS voltages are provided for each state.

No Input Power, MODE = undefined: No input adapter or battery is detected. The charger and system is off. Battery is disconnected and charger is off.

Battery Only, MODE = 0x00: Adapter and wireless charger are invalid, outside the input voltage operating range (QCHGIN = off, QWCIN = off). Battery is connected to power the SYS load (QBAT = on), and boost is ready to power OTG (Boost=standby), see Figure 10. **Battery Only.**

Battery Boost, MODE = 0x08: Adapter and Wireless inputs are invalid, outside the input voltage operating range (QCHGIN = off, QWCIN = off). Battery is connected to power the SYS load (QBAT = on), and charger is operating in Boost mode (Boost = on). See Figure 11.

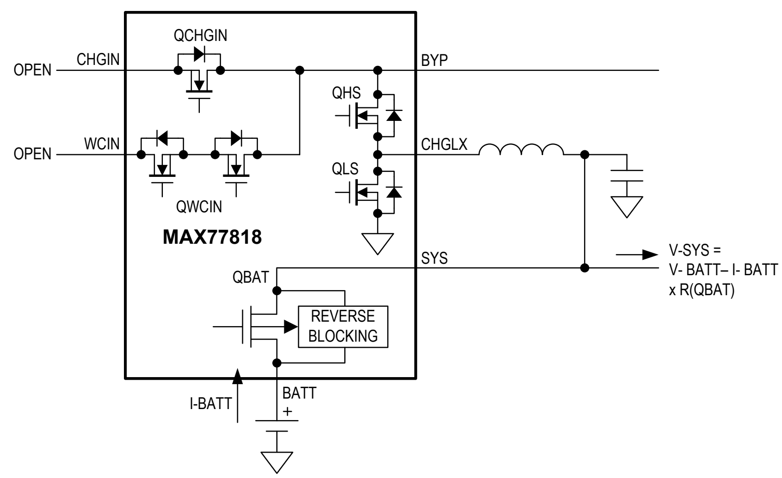


Figure 10. Battery-Only

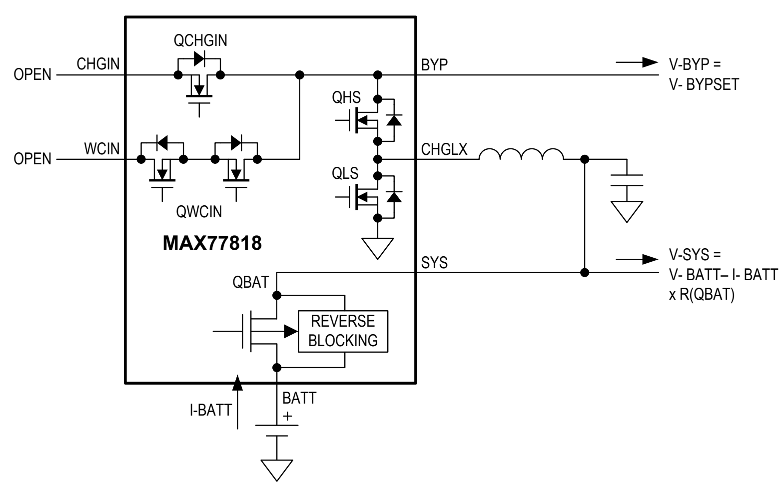


Figure 11. Battery-Boost

Battery Boost

Battery Boost (OTG), MODE = 0x0A: Wireless input is turned off (QWCIN = off) and OTG is active (QCHGIN = on). Battery is connected to support SYS and OTG loads (QBAT = on), and charger is operating in boost mode (boost = on). See Figure 12.

No Charge Buck, MODE = 0x0C: Adapter or wireless charger are detected, within the input voltage operating range (QCHGIN = on or QWCIN = on). Battery is disconnected (QBAT = off), and charger is operating in buck mode powering the SYS node. See Figure 13.

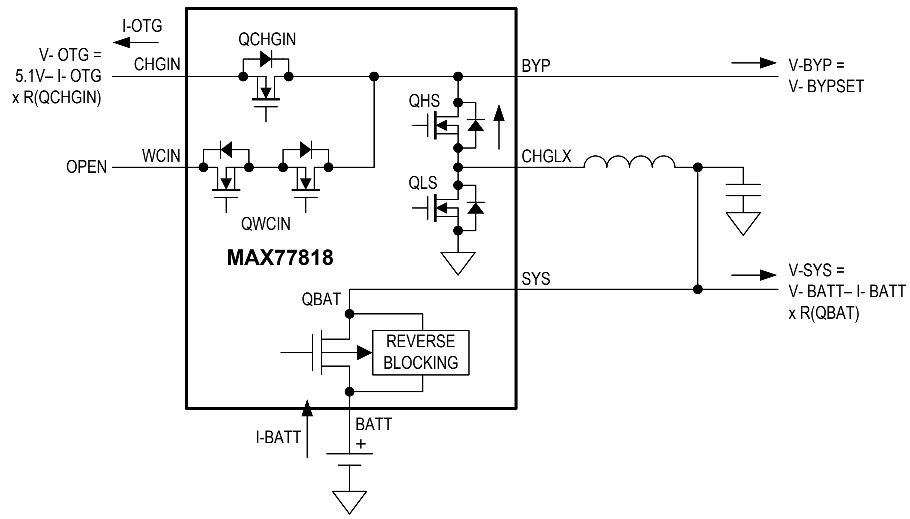


Figure 12. Battery Boost (OTG)

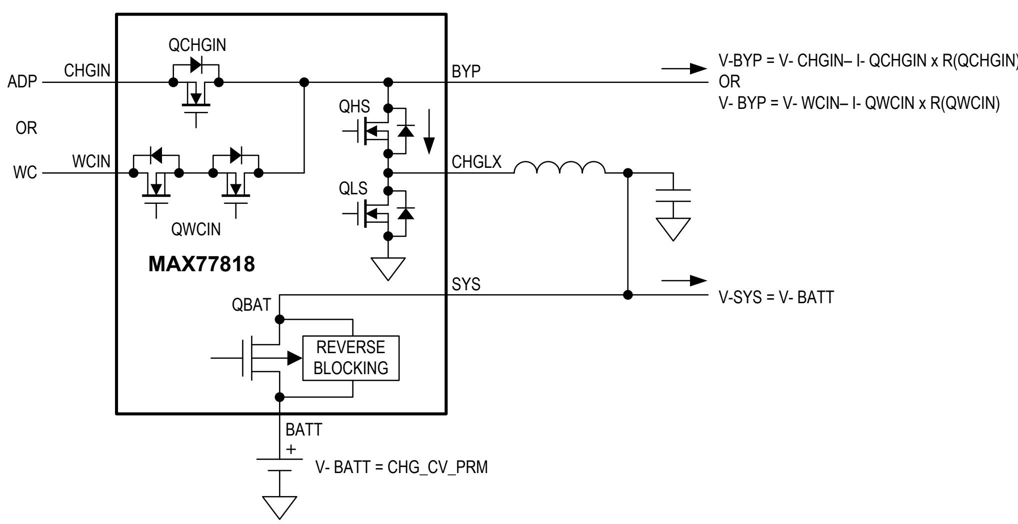


Figure 13. No Charge Buck

Charge Buck, MODE = 0x0D: Adapter or wireless charger are detected, within the input voltage operating range (QCHGIN = on or QWCIN = on). Battery is connected in charge mode (QBAT = on), and charger is operating in buck mode. See Figure 14.

No Change Buck (OTG), MODE = 0x0E: Wireless charger is detected within the input voltage operating range (QWCIN = on) and OTG is active (QCHGIN = of). Battery is connected in charge mode (QBAT = on), and charger is operating in buck mode. See Figure 15.

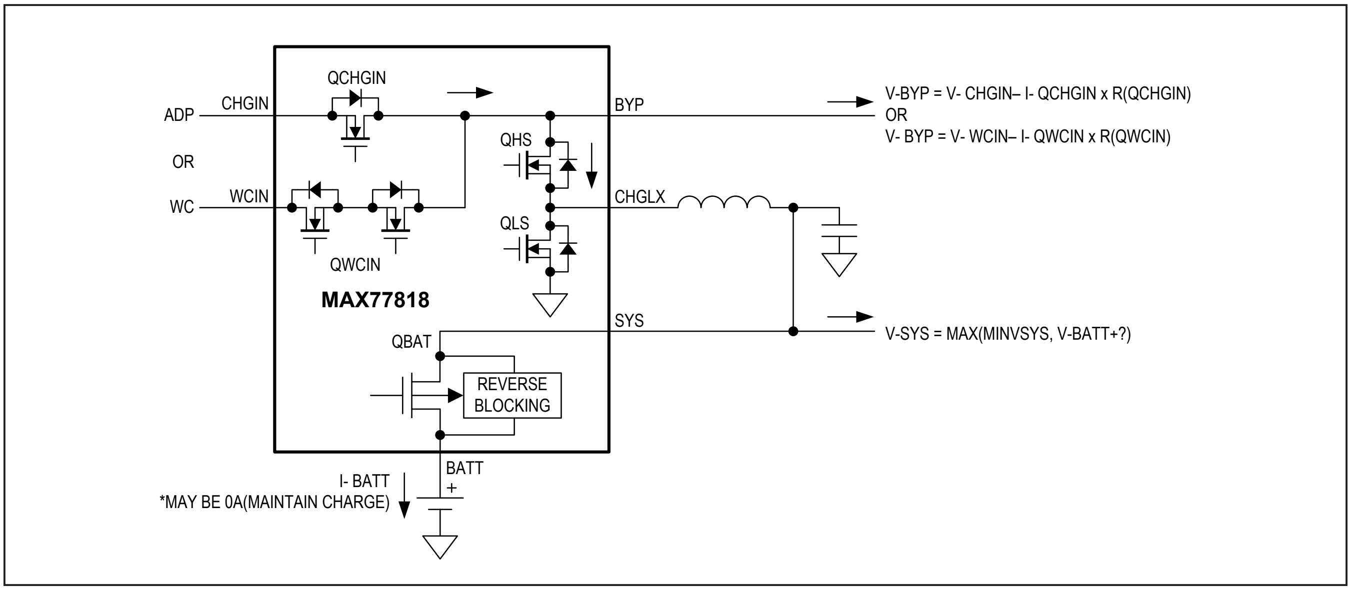


Figure 14. Charge Buck

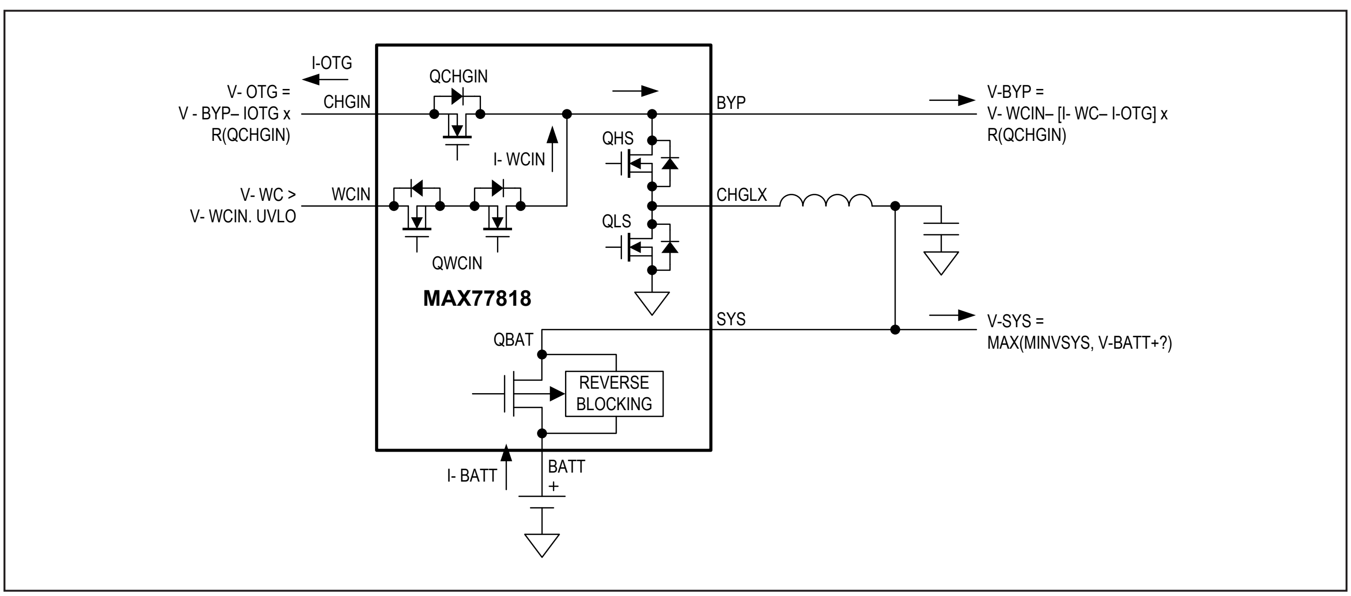


Figure 15. No Charge Buck (OTG)

Charge Buck (OTG), MODE = 0x0F: Wireless charger is detected within the input voltage operating range (QWCIN = on) and OTG is active (QCHGIN = on). Battery is connected in charge mode (QBAT = on), and charger is operating in buck mode powering the SYS node. See Figure 16.

Safeout LDOs

Safeout with Input Overvoltage Protection

The safeout LDOs are linear regulators that provides an output voltage of 3.3V, 4.85V, 4.9V, or 4.95V and can be used to supply low voltage rated USB systems. The SAFEOUT1 linear regulator turns on when CHGIN ≥ CHGIN_UVLO and ENSAFEOUT_ = logic-high regardless of charger enable or DETBATB. SAFEOUT_ is disabled when CHGIN is greater than the overvoltage threshold (13.7V typ). The safeout LDOs integrate high-voltage MOSFETs to provide 14V protection at their inputs, which are internally connected to the BYP.

SAFEOUT1 is default ON at 4.9V. SAFEOUT2 is default off.

Fuel Gauge

The MAX77818 incorporates the ModelGauge m5 algorithm that combines the excellent short-term accuracy and linearity of a coulomb counter with the excellent long-term stability of a voltage-based fuel gauge, along with temperature compensation to provide industry-leading fuel-gauge accuracy. ModelGauge m5 cancels offset accumulation error in the coulomb counter, while providing better short-term accuracy than any purely voltage-based fuel gauge. Additionally, the ModelGauge m5 algorithm does not suffer from abrupt corrections that normally occur in coulomb-counter algorithms, since tiny continual corrections are distributed over time.

The device automatically compensates for aging, temperature, and discharge rate and provides accurate state of charge (SOC) in mAh or %, as well as time-to-empty over a wide range of operating conditions. The device provides two methods for reporting the age of the battery: reduction in capacity and cycle odometer.

The device provides precision measurements of current, voltage, and temperature. Temperature of the battery pack is measured using an external thermistor supported by ratiometric measurements on an auxiliary input. A 2-wire (I^2C) interface provides access to data and control registers.

Features

- Accurate battery capacity and time-to-empty readings
- Estimation
  - Temperature, age, and rate Compensated
  - Does not require empty, full, or idle states to
- Maintain accuracy
- Precision measurement system
  - No calibration required

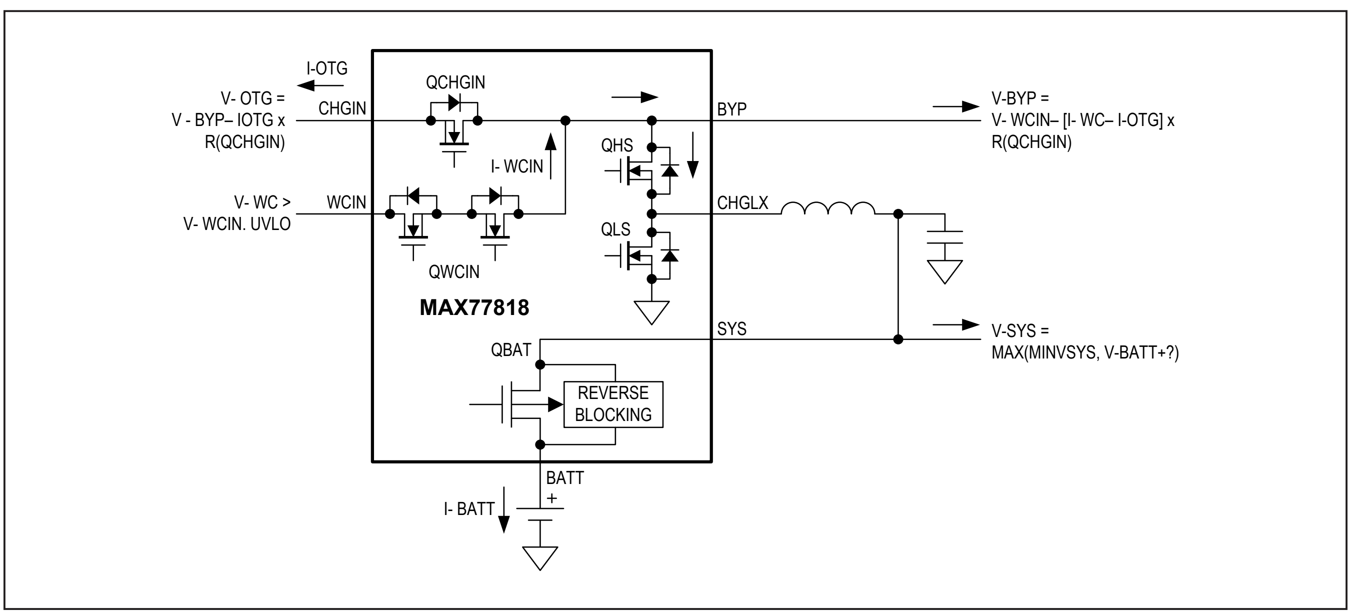


Figure 16. Charge-Buck (OTG)

- ModelGauge m5 algorithm
  - Long-term influence by voltage fuel gauge
- Cancels coulomb-counter drift
  - Short-term influence by coulomb counter
- Provides excellent linearity
  - Adapts to cell characteristics
- External temperature-measurement network
  - Actively switched thermistor resistive divider
  - Reduces current consumption
- Low quiescent current
  - 25µA active, < 0.5µA shutdown
- Alert Indicator for SOC, voltage, temperature, and battery removal/insertion events
- At rate estimation of remaining capacity

I2C Interface

The MAX77818 acts as a slave transmitter/receiver. The MAX77818 has the following slave address.

Slave Addresses

Charger : 0xD2/D3h

Clogic, GTEST and Safeout LDOs: 0xCCh/0xCDh

Fuel Gauge: 0x6C/0x6D. See the Fuel Gauge I2C Protocol for details in *Fuel Gauge* section.

I2C Bit Transfer

One data bit is transferred for each clock pulse. The data on SDA must remain stable during the high portion of the clock pulse as changes in data during this time are interpreted as a control signal.

I2C Start and Stop Conditions

Both SDA and SCL remain High when the bus is not busy. A high-to-low transition of SDA, while SCL is high is defined as the start (S) condition. A low-to-high transition of SDA while SCL is high is defined as the stop (P) condition.

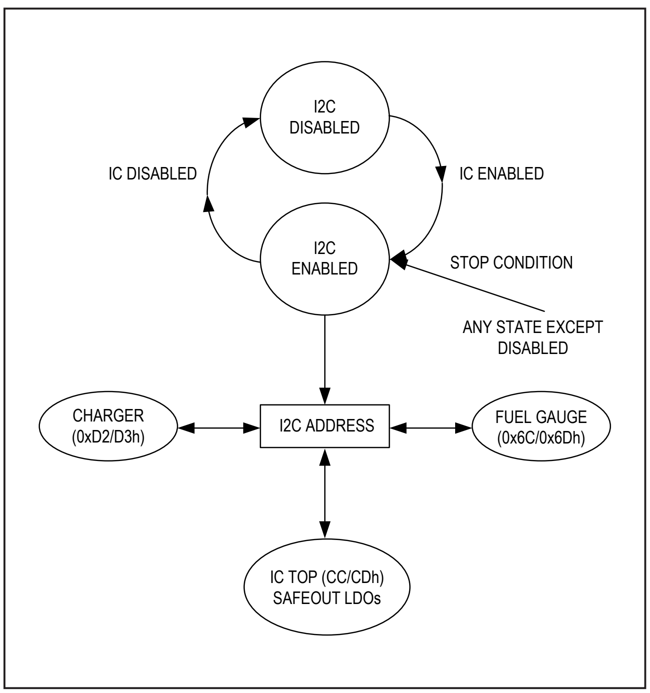


Figure 17. I2C Slave Address Structure

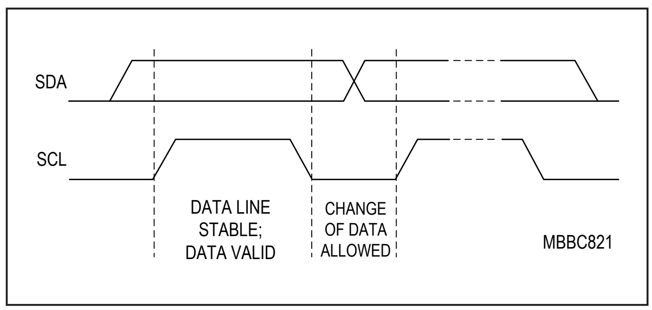


Figure 18. I2C Bit Transfer

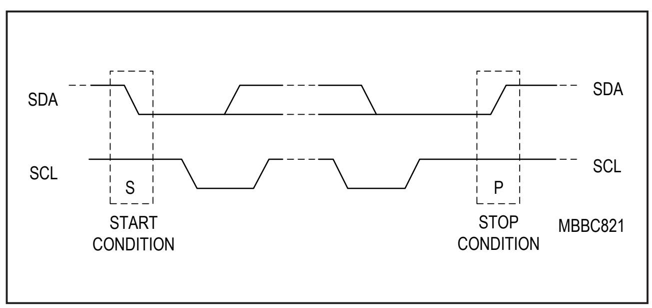


Figure 19. I2C Start and Stop

I2C System Configuration

A device on the I2C bus that generates a message is called a transmitter and a device that receives the message is a receiver. The device that controls the message is the master. The devices that are controlled by the master are called slaves.

I2C Acknowledge

The number of data bytes between the start and stop conditions for the transmitter and receiver are unlimited.

Each 8-bit byte is followed by an acknowledge bit. The acknowledge bit is a high-level signal put on SDA by the transmitter during the time the master generates an extra acknowledge-related clock pulse. A slave receiver that is addressed must generate an acknowledge after each byte it receives. Also, a master receiver must generate an acknowledge after each byte it receives that has been clocked out of the slave transmitter.

The device that acknowledges must pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable low during the high period of the acknowledge clock pulse (set-up and hold times must also be met). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this case, the transmitter must leave SDA high to enable the master to generate a stop condition.

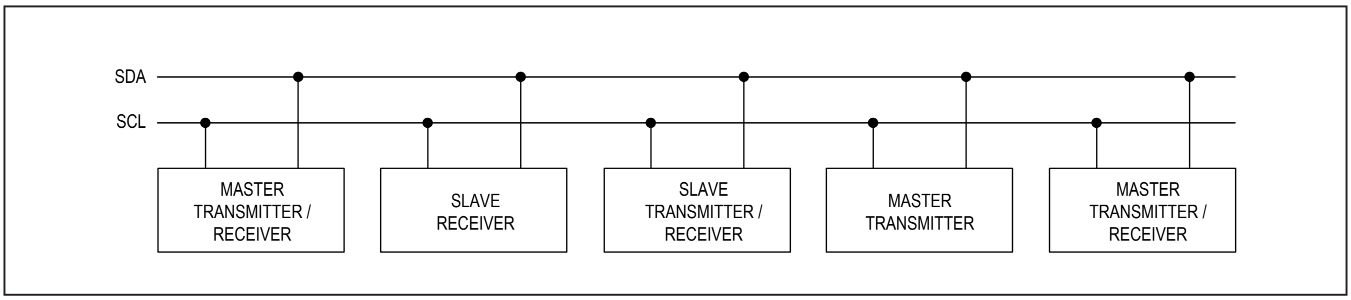


Figure 20. I2C System Configuration

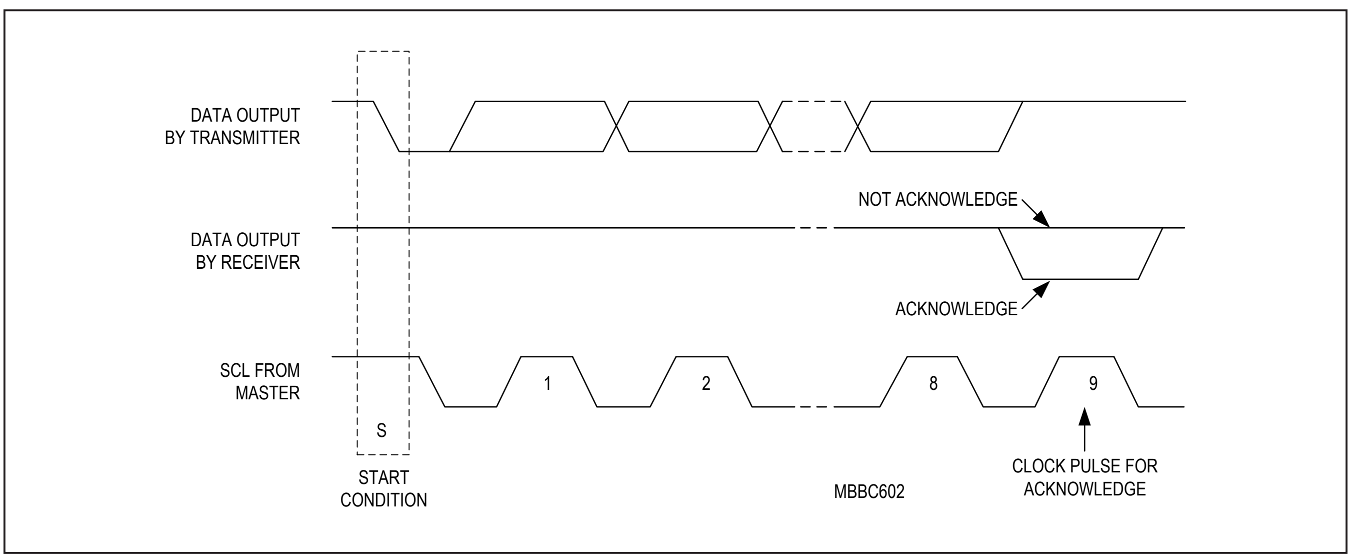
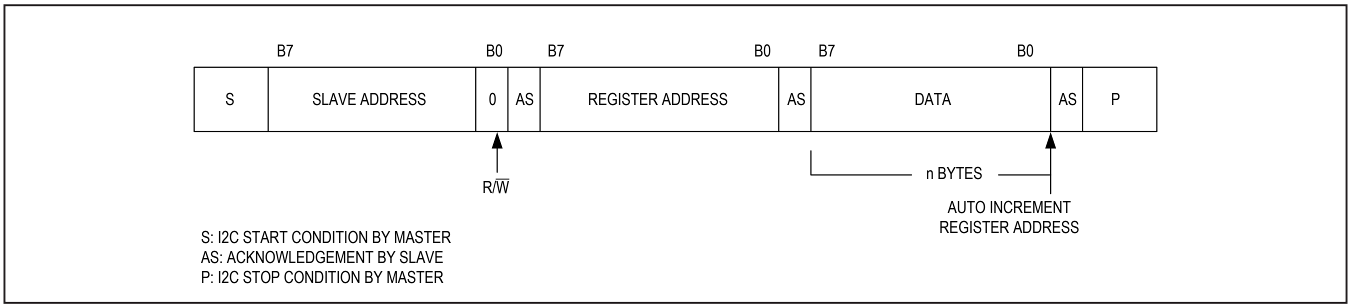


Figure 21. I2C Knowledge

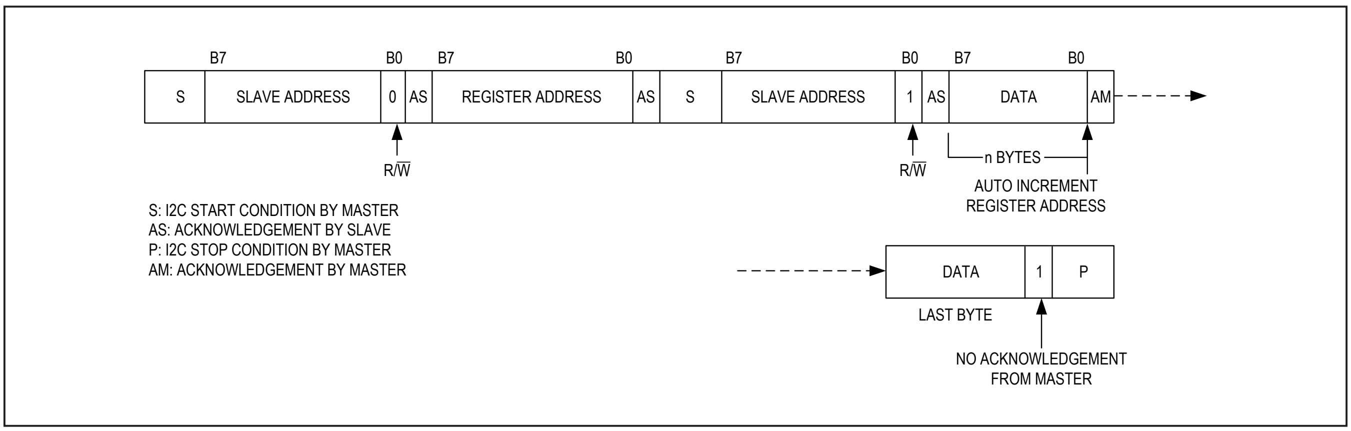
Master Transmits (Write Mode)

When master writes to slave, use the following format:



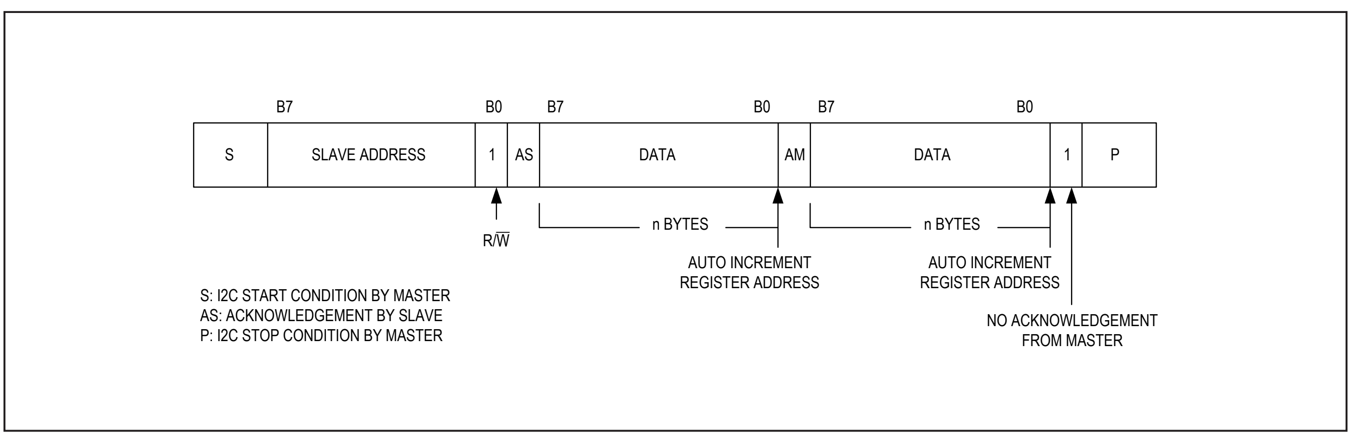
Master Reads After Setting Register Address (Write Register Address and Read Data)

When reading a specific register, use the following format:



Master Reads Register Data Without Setting Register Address (Read Mode)

When reading registers from the first address, use the following format:



I²C Register Map and Detail Descriptions

Register Reset Conditions in R column

Type S: Registers are reset each time when SYS < SYS POR (~1.55V)

Type O: Registers are reset each time when SYS < SYS UVLO (2.55V max) or SYS > SYS OVLO or Die temp > 165° (or MAX77818 transitions from on to off state)

Top Level I²C Registers

The MAX77818 acts as a slave transmitter/receiver. The slave address of the MAX77818 top is 0xCCh/0xCDh (OTP option for 0xDC/0xDDh). The least significant bit is the read/write indicator.

The MAX77818's tope level has the following registers:

0x20: PMIC ID Register

NAME	FUNCTION	ADDR	TYPE	RESET
PMICID	PMIC ID	0x20	O	0x23

BIT	MODE	NAME	RESET	DESCRIPTION
3:0	R	ID	0011	ID of MAX77818
7:4	R	ID	0010	

0x21: PMIC Version/Rev Register

NAME	FUNCTION	ADDR	TYPE	RESET
PMICREV	PMIC revision	0x21	O	0x80

BIT	MODE	NAME	RESET	DESCRIPTION
2:0	R	REV	—	Pass 0b000 = pass 1 0b001 = pass 2 0b010 = pass 3
7:3	R	VERSION	—	Version 0b00000 = zmo 0b00001 = ymo … Null Trim Version 0b10000 = tmo 0b10001 = umo

0x22: Interrupt Source

NAME	FUNCTION	ADDR	TYPE	RESET
INTSRC	Interrupt source	0x22	S	0x00

BIT	MODE	NAME	RESET	DESCRIPTION
0	R	CHGR_INT	0	0: No charger interrupt. 1: Charger interrupt is detected.
1	R	FG_INT	0	0 = No interrupt pending from FG block. 1 = interrupt from FG block is detected .
2	R	SYS_INT	0	0: No SYS INT 1: SYS interrupt is detected.
3	R	RSVD	0	Reserved
4	R	RSVD	0	Reserved
5	R	RSVD	0	Reserved
6	R	RSVD	0	Reserved
7	R	RSVD	0	Reserved

0x23: Interrupt Source Mask

NAME	FUNCTION	ADDR	TYPE	RESET
INTSRCMASK	Interrupt source mask	0x23	S	0xFF

BIT	MODE	NAME	RESET	DESCRIPTION
0	R/W	CHGR_INT_MASK	1	1: Charger interrupt is masked.
1	R/W	FG_INT_MASK	1	1: FG interrupt is masked.
2	R/W	SYS_INT_MASK	1	1: SYS interrupt is masked.
3	R/W	RSVD	1	Reserved
4	R/W	RSVD	1	Reserved
5	R/W	RSVD	1	Reserved
6	R/W	RSVD	1	Reserved
7	R/W	RSVD	1	Reserved

0x24: SYSTEM Interrupt

NAME	FUNCTION	ADDR	TYPE	RESET
SYSINTSRC	SYS interrupt source	0x24	S	0x00

BIT	MODE	NAME	RESET	DESCRIPTION
0	R	SYSUVLO_INT	0	0: No SYSUVLO INT. 1: SYSUVLO interrupt is detected (falling).
1	R	SYSOVLO_INT	0	0: No SYSOVLO interrupt. 1: SYSOVLO interrupt is detected (rising and falling).
2	R	TSHDN_INT		0: No TSHDN interrupt. 1: TSHDN interrupt is detected.
3	R	RSVD	0	Reserved
4	R	RSVD	0	Reserved
5	R	RSVD	0	Reserved
6	R	RSVD	0	Reserved
7	R	TM_INT	0	0: Test mode interrupt is not set. 1: Test mode interrupt is set.

0x26: SYSTEM Interrupt Source Mask

NAME	FUNCTION	ADDR	TYPE	RESET
SYSINTMASK	System interrupt mask	0x26	S	0xFF

BIT	MODE	NAME	RESET	DESCRIPTION
0	R/W	SYSUVLO_INT_MASK	1	1: SYSUVLO interrupt is masked.
1	R/W	SYSOVLO_INT_MASK	1	1: SYSUVLO interrupt is masked.
2	R/W	TSHDN_INT_MASK	1	1: Thermal shutdown interrupt is masked.
3	R/W	RSVD	1	Reserved
4	R/W	RSVD	1	Reserved
5	R/W	RSVD	1	Reserved
6	R/W	RSVD	1	Reserved
7	R/W	TM_INT_MASK	0	1: INT test mode interrupt is masked.

0xC6: SAFEOUT LDO Control

NAME	FUNCTION	ADDR	TYPE	RESET
SAFEOUTCTRL	SAFEOUT linear regulator control	0xC6	O	0x75

BIT	MODE	NAME	RESET	DESCRIPTION
1:0	R/W	SAFEOUT1[1:0]	01	SAFEOUT1 output voltage 00: 4.85V 01: 4.90V (default) 10: 4.95V 11: 3.3V.
3:2	R/W	SAFEOUT2[3:2]	01	SAFEOUT2 output voltage 00: 4.85V 01: 4.90V (default) 10: 4.95V 11: 3.3V
4	R/W	ACTDISSAFEO1	1	0: No active discharge 1: Active discharge
5	R/W	ACTDISSAFEO2	1	0: No active discharge 1: Active discharge
6	R/W	ENSAFEOUT1	1	SAFEOUTLDO1 enable bit 0: Disable SAFEOUT1. 1: Enable SAFEOUT1.
7	R/W	ENSAFEOUT2	0	SAFEOUTLDO2 enable bit 0: Disable SAFEOUT2. 1: Enable SAFEOUT2.

Charger I^{2}C Registers

The MAX77818's charger has convenient default register settings and a complete charger state machine that allow it to be used with minimal software interaction. Software interaction with the register map enhances the charger by allowing a high degree of configurability. An easy-to-navigate interrupt structure and in-depth status reporting allows software to quickly track the changes in the charger's status.

Register Protection

The CHG_CNFG_01, CHG_CNFG_02, CHG_CNFG_03, CHG_CNFG_04, CHG_CNFG_05, and CHG_CNFG07 registers contain settings for static parameters that are associated with a particular system and battery. These static settings are typically set once each time the system's microprocessor runs its boot-up initialization code; then they are not changed again until the microprocessor re-boots. CHGPROT allows for blocking the "write" access to these static settings to protect them from being changed unintentionally. This protection is particularly useful for critical parameters such as the battery charge current CHG_CC and the battery charge voltage CHG_CV_PRM

Determine the following registers bit settings by considering the characteristics of the battery. Maxim recommends that CHG_CC be set to the maximum acceptable charge rate for your battery – there is typically no need to actively adjust the CHG_CC setting based on the capabilities of the source at CHGIN, system load, or thermal limitations of the PCB; the smart power selector intelligently manages all these parameters to optimize the power distribution.

Charger Restart Threshold ➔ CHG_RSTRT

Fast-Charge Timer (t_{FC}) ➔ FCHGTIME

Fast-Charge Current ➔ CHG_CC

Top-Off Time ➔ TO_TIME

Top-Off Current ➔ TO_ITH

Battery Regulation Voltage ➔ CHG_CV_PRM

Determine the following register bit settings by considering the characteristics of the system:

Low Battery Prequalification Enable ➔ PQEN

Minimum System Regulation Voltage ➔ MINVSYS

Junction Temperature Thermal Regulation
Loop Setpoint ➔ REGTEMP

Interrupt, Mask, OK, and Detail Registers

The battery charger section of the MAX77818 provides detailed interrupt generation and status for the following subblocks:

Charger Input

Charger State Machine

Battery

Bypass Node

State changes on any subblock report interrupts through the CHG_INT register. Interrupt sources are masked from affecting the hardware interrupt pin when bits in the CHG_INT_MASK register are set. The CHG_INT_OK register provides a single-bit status indication of whether the interrupt generating sub-block is okay or not. The full status of interrupt generating subblock is provided in the CHG_DETAILS_00, CHG_DETAILS_01, CHG_DETAILS_02, and CHG_DETAILS_03 registers.

Note that CHG_INT, CHG_INT_MASK and CHG_INT_OK use the same bit position for each interrupt generating block to simplify software development.

Interrupt bits are automatically cleared upon reading a given interrupt register. When all pending CHG_INT interrupts are cleared, the top level interrupt bit deasserts.

CHG_INT Register Bit Description (0xB0)

NAME	FUNCTION	ADDR	TYPE	RESET
CHG_INT	Charger interrupt	0xB0	O	0x00

BIT	MODE	NAME	RESET	DESCRIPTION
0	R/C	BYP_I	0	Bypass Node Interrupt 0 = The BYP_OK bit has not changed since the last time this bit was read. 1 = The BYP_OK bit has changed since the last time this bit was read.
1	R/C	RSVD	0	Reserved
2	R/C	BATP_I	0	Battery Presence Interrupt. 0 = The BATP_OK bit has not changed since the last time this bit was read. 1 = The BATP_OK bit has changed since the last time this bit was read.s
3	R/C	BAT_I	0	Battery Interrupt 0 = The BAT_OK bit has not changed since the last time this bit was read. 1 = The BAT_OK bit has changed since the last time this bit was read.
4	R/C	CHG_I	0	Charger Interrupt 0 = The CHG_OK bit has not changed since the last time this bit was read. 1 = The CHG_OK bit has changed since the last time this bit was read.
5	R/C	WCIN_I	0	WCIN Interrupt. 0 = The WCIN_OK bit has not changed since the last time this bit was read. 1 = The WCIN_OK bit has changed since the last time this bit was read.
6	R/C	CHGIN_I	0	CHGIN Interrupt. 0 = The CHGIN_OK bit has not changed since the last time this bit was read. 1 = The CHGIN_OK bit has changed since the last time this bit was read.
7	R/C	AICL_I	0	AICL interrupt 0=The AICL_OK bit has not changed since the last time this bit was read. 1=The AICL_OK bit has changed since the last time this bit was read.

CHG_INT_MASK Register Bit Description (0xB1)

NAME	FUNCTION	ADDR	TYPE	RESET
CHG_INT_MASK	Charger interrupt mask	0xB1	O	0xFF

BIT	MODE	NAME	RESET	DESCRIPTION
0	R/W	BYP_M	1	Bypass Interrupt Mask 0 = Unmasked 1 = Masked
1	R/W	RSVD	1	Reserved
2	R/W	BATP_M	1	Battery Presence Interrupt Mask 0 = Unmasked 1 = Masked
3	R/W	BAT_M	1	Battery Interrupt Mask 0 = Unmasked 1 = Masked
4	R/W	CHG_M	1	Charger Interrupt Mask 0 = Unmasked 1 = Masked
5	R/W	WCIN_M	1	WCIN Interrupt Mask 0 = Unmasked 1 = Masked
6	R/W	CHGIN_M	1	CHGIN Interrupt Mask 0 = Unmasked 1 = Masked
7	R/W	AICL_M	1	AICL Interrupt Mask 0 = Unmasked 1 = Masked

CHG_INT_OK Register Bit Description (0xB2)

NAME	FUNCTION	ADDR	TYPE	RESET
CHG_INT_OK	Charger status	0xB2	O	0x00

BIT	MODE	NAME	RESET	DESCRIPTION
0	R	BYP_OK	0	Single-Bit Bypass Status Indicator. See BYP_DTLS for more information. 0 = Something powered by the bypass node has hit current limit. i.e., BYP_DTLS ≠ 0x00. 1 = The bypass node is okay. i.e., BYP_DTLS = 0x00.
1	R	RSVD	0	Reserved
2	R	BATP_OK	0	BAT present status indicator. 0 = Main Battery is not present 1 = Main Battery is present.
3	R	BAT_OK	0	Single-Bit Battery Status Indicator. See BAT_DTLS for more information. 0 = The battery has an issue or the charger has been suspended, i.e., BAT_DTLS ≠ 0x03 or 0x04 1 = The battery is okay. i.e., BAT_DTLS = 0x03 or 0x04
4	R	CHG_OK	0	Single-Bit Charger Status Indicator. See CHG_DTLS for more information. 0 = The charger has suspended charging or TREG = 1 i.e., CHG_DTLS ≠ 0x00 or 0x01 or 0x02 or 0x03 or 0x05 or 0x08 1 = The charger is okay or the charger is off i.e., CHG_DTLS = 0x00 or 0x01 or 0x02 or 0x03 or 0x05 or 0x08
5	R	WCIN_OK	0	Single-Bit WCIN Input Status Indicator. See WCIN_DTLS for more information. 0 = The WCIN input is invalid. i.e., WCIN_DTLS ≠ 0x03. 1 = The WCIN input is valid. i.e., WCIN_DTLS = 0x03.
6	R	CHGIN_OK	0	Single-Bit CHGIN Input Status Indicator. See CHGIN_DTLS for more information. 0 = The CHGIN input is invalid. i.e., CHGIN_DTLS ≠ 0x03. 1 = The CHGIN input is valid. i.e., CHGIN_DTLS = 0x03.
7	R	AICL_OK	0	AICL_OK 0 = AICL mode 1 = Not in AICL mode

CHG_DETAILS_00 Register Bit Description (0xB3)

NAME	FUNCTION	ADDR	TYPE	RESET
CHG_DTLS_00	Charger details 00	0xB3	O	0x00

BIT	MODE	NAME	RESET	DESCRIPTION
0	R	BATP_DTLS	0	Battery Detection 0 = Battery presence 1 = No battery presence
2:1	R	RSVD	00	Reserved
4:3	R	WCIN_DTLS	00	WCIN Details 0x00 = VWCIN is invalid. $V_{WCIN} < V_{WCIN\_UVLO}$ 0x01 = VWCIN is invalid. $V_{WCIN} < V_{MBAT} + V_{WCIN2SYS}$ and $V_{WCIN} > V_{WCIN\_UVLO}$ 0 x 02 = VWCIN is invalid. $V_{WCIN}>V_{WCIN\_OVLO}$ 0 x 03 = VWCIN is valid. $V_{WCIN} > V_{WCIN\_UVLO}$, VWCIN > $V_{MBAT} + V_{WCIN2SYS}$, $V_{WCIN} < V_{WCIN\_OVLO}$
6:5	R	CHGIN_DTLS	00	CHGIN Details 0x00 = VBUS is invalid. $V_{CHGIN} < V_{CHGIN\_UVLO}$ 0x01 = VBUS is invalid. $V_{CHGIN} < V_{MBAT} + V_{CHGIN2SYS}$ and $V_{CHGIN} > V_{CHGIN\_UVLO}$ 0x02 = VBUS is invalid. $V_{CHGIN} > V_{CHGIN\_OVLO}$ 0x03 = VBUS is valid. $V_{CHGIN} > V_{CHGIN\_UVLO}$, $V_{CHGIN} > V_{MBAT} + V_{CHGIN2SYS}$, $V_{CHGIN} < V_{CHGIN\_OVLO}$
7	R	RSVD	0	Reserved

CHG_DETAILS_01 Register Bit Description (0xB4)

NAME	FUNCTION	ADDR	TYPE	RESET
CHG_DTLS_01	Charger details 01	0xB4	O	0x00

BIT	MODE	NAME	RESET	DESCRIPTION
3:0	R	CHG_DTLS	0000	Charger Details 0x00 = charger is in dead-battery prequalification or low-battery prequalification mode, CHG_OK = 1, $V_{MBATT} < V_{PQLB}$, $T_J < T_{JSHDN}$ 0x01 = charger is in fast-charge constant current mode, CHG_OK = 1, $V_{MBATT} < V_{BATREG}$, $T_J < T_{JSHDN}$ 0x02 = charger is in fast-charge constant voltage mode, CHG_OK = 1, V_{MBATT} = VBATREG, $T_J < T_{JSHDN}$ 0x03 = charger is in top-off mode, CHG_OK = 1, $V_{MBATT} \geq V_{BATREG}$, $T_J < T_{JSHDN}$ 0x04 = charger is in done mode, CHG_OK=0, $V_{MBATT} > V_{BATREG} - V_{RSTRT}$, $T_J < T_{JSHDN}$ 0x06 = charger is in timer fault mode, CHG_OK = 0, $V_{MBATT} < V_{BATOV}$, if BAT_DTLS = 0b001 then $V_{MBATT} < V_{BATPQ}$, $T_J < T_{JSHDN}$ 0x07 = charger is in DETBAT = High suspend mode, CHG_OK = 0, $V_{MBATT} < V_{BATOV}$, if BAT_DTLS = 0b001 then $V_{MBATT} < V_{PQLB}$, $T_J < T_{JSHDN}$ 0x08 = Charger is off, charger input invalid and/or charger is disabled, CHG_OK = 1. 0x09 = Reserved 0x0A = Charger is off and the junction temperature is > T_{JSHDN}, CHG_OK = 0. 0x0B = Charger is off because the watchdog timer expired, CHG_OK = 0. 0x0C-0x0F = Reserved
6:4	R	BAT_DTLS	000	Battery Details 0x00 = No battery and the charger is suspended. 0x01 = $V_{MBATT} < V_{PQLB}$. This condition is also reported in the CHG_DTLS as 0x00 0x02 = the battery is taking longer than expected to charge. This could be due to high system currents, an old battery, a damaged battery or something else. Charging has suspended and the charger is in its timer fault mode. This condition is also reported in the CHG_DTLS as 0x06. 0x03 = the battery is okay and its voltage is greater than the minimum system voltage ($V_{SYSMIN} < V_{MBATT}$), QBAT is on and V_{SYS} is approximately equal to V_{MBATT}. 0x04 = the battery is okay but its voltage is low: $V_{PQLB} < V_{MBATT} < V_{SYSMIN}$. Q_{BAT} is operating like an LDO to regulate V_{SYS} to V_{SYSMIN}. 0x05 = the battery voltage is greater than the battery overvoltage flag threshold (V_{BATOVF}) or it has been greater than this threshold within the last 37.5ms. V_{BATOVF} is set to a percentage above the V_{BATREG} target as programmed by CHG_CV_PRM. Note that this flag is only be generated when there is a valid input or when the DC-DC is operating as a boost. 0x06 = the battery is overcurrent or it has been overcurrent for at least 6ms since the last time this register has been read. 0x07 = Reserved In the event that multiple faults occur within the battery details category, overcurrent has priority followed by no battery, then overvoltage, then timer fault, then below prequel.

CHG_DETAILS_01 Register Bit Description (0xB4) (continued)

BIT	MODE	NAME	RESET	DESCRIPTION
7	R	TREG	0	Temperature Regulation Status 0 = The junction temperature is less than the threshold set by REGTEMP and the full charge current limit is available. 1 = The junction temperature is greater than the threshold set by REGTEMP and the charge current limit may be folding back to reduce power dissipation.

CHG_DETAILS_02 Register Bit Description (0xB5)

NAME	FUNCTION	ADDR	TYPE	RESET
CHG_DTLS_02	Charger details 02	0xB5	O	0x00

BIT	MODE	NAME	RESET	DESCRIPTION
3:0	R	BYP_DTLS	0000	Bypass Node Details. All bits in this family are independent from each other. They are grouped together only because they all relate to the health of the BYP node and any change in these bits generates a BYP_I interrupt. BYP_DTLS0 = OTGILIM = **0bxxx1** BYP_DTLS1 = BSTILIM = **0bxx1x** BYP_DTLS2 = BCKNegILIM = **0bx1xx** ******************************** 0x00=The bypass node is okay. 0bxxx1=The BYP to CHGIN switch (OTG switch) current limit was reached within the last 37.5ms. 0bxx1x=The BYP reverse boost converter has hit its current limit -- this condition persists for 37.5ms. 0bx1xx= The BYP buck converter has hit the max negative demand current limit.
7:4	R	RSVD	00	Reserved

CHG_CNFG_00 Register Bit Description (0xB7)

NAME	FUNCTION	ADDR	TYPE	RESET
CHG_CNFG_00	Charger configuration 00	0xB7	O	0x05

BIT	MODE	NAME	RESET	DESCRIPTION
3:0	R/W	MODE	0101	Smart Power Selector Configuration 0x00 = 0b0000 = charger = off, OTG = off, buck = off, boost = off. The QBAT switch is on to allow the battery to support the system. BYP may or may not be biased based on the CHGIN availability. 0x01 = 0b0001 = same as 0b0000 0x02 = 0b0010= same as 0b0000 0x03 = 0b0011= same as 0b0000 0x04 = 0b0100 = charger = off, OTG = off, **buck = on**, boost = off. When there is a valid input, the buck converter regulates the system voltage to be V_{BATREG}. 0x05 = 0b0101 = **charger = on**, OTG = off, **buck = on**, boost = off. When there is a valid input, the battery is charging. V_{SYS} is the larger of V_{SYSMIN} and ~VMBATT + IMBATT x RBAT2SYS. 0x06 = 0b0110 = same as 0b101 0x07 = 0b0111 = same as 0b101 0x08 = 0b1000 = charger = off, OTG = off, buck = off, **boost = on.** The Q_{BAT} switch is on to allow the battery to support the system and the charger's DC-DC operates as a boost converter. The BYP voltage is regulated to VBYPSET. QCHGIN is off. . 0x09 = 0b1001=same as 0b1000 0x0A = 0b1010 = charger = off, **OTG = on**, buck = off, **boost = on**. The Q_{BAT} switch is on to allow the battery to support the system, the charger's DC-DC operates as a boost converter. **Q_{CHGIN} is on** allowing it to source current up to $I_{CHGIN.OTG.MAX}$. The boost target voltage is 5.1V ($V_{BYP.OTG}$) . 0x0B = reserved 0x0C = 0b1100 = charger = off, OTG = off, **buck = on**, **boost = on**. When there is a valid input, the system is supported from that input: V_{SYS} = 4.2V. When input is invalid the boost is on with a target voltage that is VBYPSET 0x0D = 0b1101 = **charger = on**, OTG = off, **buck = on**, **boost = on**. When there is a valid input, the system is supported from that input: V_{SYS} is the larger of V_{SYSMIN} and ~V_{MBATT} + I_{MBATT} x $R_{BAT2SYS}$. When input is invalid the boost is on with a target voltage that is VBYPSET 0x0E = 0b1110=charger=off, **OTG = on**, **buck = on**, **boost = on**. When there is a valid WCIN input, the system is supported from that input: V_{SYS} = 4.2V and **Q_{CHGIN} is on**, allowing it to source current up to $I_{CHGIN.OTG.MAX}$. When WCIN input is invalid the boost is on with a target voltage of 5.1V ($V_{BYP.OTG}$). 0x0F = 0b1111 = **charger = on**, **OTG = on**, **buck = on**, **boost = on**. When there is a valid WCIN input, the system is supported from that input: V_{SYS} is the larger of V_{SYSMIN} and ~V_{MBATT} + I_{MBATT} x $R_{BAT2SYS}$. **Q_{CHGIN} is on** allowing it to source current up to $I_{CHGIN.OTG.MAX}$. When WCIN input is invalid the boost is on with a target voltage of 5.1V ($V_{BYP.OTG}$)

CHG_CNFG_00 Register Bit Description (0xB7) (continued)

BIT	MODE	NAME	RESET	DESCRIPTION
4	R/W	WDTEN	0	Watchdog Timer Enable Bit. While enabled, the system controller must reset the watchdog timer within the timer period (t_{WD}) for the charger to operate normally. Reset the watchdog timer by programming WDTCLR = 0x01. 0 = Watchdog Timer disabled 1 = Watchdog Timer enabled
5	R/W	SPREAD	0	Spread Spectrum Feature Feature is operational both for 9V and 12V CHGIN input voltage. Feature is not guaranteed to be operational for 5V CHGIN/WCIN input voltage. When feature is not operational, it can be kept enabled without side effect. 0: Disabled 1: Enabled
6	R/W	DISIBS	0	MBATT to SYS FET Disable Control 0 = MBATT to SYS FET is controlled by the power path state machine. 1 = MBATT to SYS FET is forced off.
7	R/W	OTG_CTRL	0	OTG FET Control 0 = Forces the CHGIN input switch to be on when in Mode = 0x0E or 0x0F. 1 = The CHGIN turns off anytime power switches between WCIN and BATT.

CHG_CNFG_01 Register Bit Description (0xB8)

NAME	FUNCTION	ADDR	TYPE	RESET
CHG_CNFG_01	Charger details 01	0xB8	O R/W (protected with CHGPROT)	0x10

BIT	MODE	NAME	RESET	DESCRIPTION
2:0	R/W	FCHGTIME	001	Fast-Charge Timer Duration (t_{FC}) 0x00 = disable 0x01 = 4hrs 0x02 = 6hrs 0x03 = 8hrs 0x04 = 10hrs 0x05 = 12hrs 0x06 = 14hrs 0x07 = 16hrs
3	R/W	FSW	0	Switching Frequency Option 0: 4MHz 1: 2MHz
5:4	R/W	CHG_RSTRT	01	Charger Restart Threshold 0x00 = 100mV below the value programmed by CHG_CV_PRM 0x01 = 150mV below the value programmed by CHG_CV_PRM 0x02 = 200mV below the value programmed by CHG_CV_PRM 0x03 = Disabled
6	R/W	LSEL	0	Inductor Selection 0:0.47μH (for 4MHz without restriction) 2MHz/0.47μH option can be used only in the charge mode and is forbidden in following use cases: Boost mode Buck mode 1:1μH (for 2MHz and 4MHz option)
7	R/W	PQEN	0	Low Battery Prequalification Mode Enable 0 = Low battery prequalification mode is disabled. 1 = Low battery prequalification mode is enabled.

CHG_CNFG_02 Register Bit Description (0xB9)

NAME	FUNCTION	ADDR	TYPE	RESET
CHG_CNFG_02	Charger configuration 02	0xB9	O R/W (protected with CHGPROT)	0x09

<table>
<tr><th>BIT</th><th>MODE</th><th>NAME</th><th>RESET</th><th>DESCRIPTION</th></tr>
<tr><td>5:0</td><td>R/W</td><td>CHG_CC</td><td>001001
(450mA)</td><td>Fast-Charge Current Selection. When the charger is enabled, the charge current limit is set by these bits. These bits range from 0.10A (0x00) to 3.0A (0x3C) in 50mA step. Note that the first 3 codes are all 100mA
<table>
<tr><td>Bits</td><td>(mA)</td><td>Bits</td><td>(mA)</td><td>Bits</td><td>(mA)</td><td>Bits</td><td>(mA)</td></tr>
<tr><td>0x00</td><td>100</td><td>0x10</td><td>800</td><td>0x20</td><td>1600</td><td>0x30</td><td>2400</td></tr>
<tr><td>0x01</td><td>100</td><td>0x11</td><td>850</td><td>0x21</td><td>1650</td><td>0x31</td><td>2450</td></tr>
<tr><td>0x02</td><td>100</td><td>0x12</td><td>900</td><td>0x22</td><td>1700</td><td>0x32</td><td>2500</td></tr>
<tr><td>0x03</td><td>150</td><td>0x13</td><td>950</td><td>0x23</td><td>1750</td><td>0x33</td><td>2550</td></tr>
<tr><td>0x04</td><td>200</td><td>0x14</td><td>1000</td><td>0x24</td><td>1800</td><td>0x34</td><td>2600</td></tr>
<tr><td>0x05</td><td>250</td><td>0x15</td><td>1050</td><td>0x25</td><td>1850</td><td>0x35</td><td>2650</td></tr>
<tr><td>0x06</td><td>300</td><td>0x16</td><td>1100</td><td>0x26</td><td>1900</td><td>0x36</td><td>2700</td></tr>
<tr><td>0x07</td><td>350</td><td>0x17</td><td>1150</td><td>0x27</td><td>1950</td><td>0x37</td><td>2750</td></tr>
<tr><td>0x08</td><td>400</td><td>0x18</td><td>1200</td><td>0x28</td><td>2000</td><td>0x38</td><td>2800</td></tr>
<tr><td>0x09</td><td>450</td><td>0x19</td><td>1250</td><td>0x29</td><td>2050</td><td>0x39</td><td>2850</td></tr>
<tr><td>0x0A</td><td>500</td><td>0x1A</td><td>1300</td><td>0x2A</td><td>2100</td><td>0x3A</td><td>2900</td></tr>
<tr><td>0x0B</td><td>550</td><td>0x1B</td><td>1350</td><td>0x2B</td><td>2150</td><td>0x3B</td><td>2950</td></tr>
<tr><td>0x0C</td><td>600</td><td>0x1C</td><td>1400</td><td>0x2C</td><td>2200</td><td>0x3C</td><td>3000</td></tr>
<tr><td>0x0D</td><td>650</td><td>0x1D</td><td>1450</td><td>0x2D</td><td>2250</td><td>0x3D</td><td>3000</td></tr>
<tr><td>0x0E</td><td>700</td><td>0x1E</td><td>1500</td><td>0x2E</td><td>2300</td><td>0x3E</td><td>3000</td></tr>
<tr><td>0x0F</td><td>750</td><td>0x1F</td><td>1550</td><td>0x2F</td><td>2350</td><td>0x3F</td><td>3000</td></tr>
</table>
Note that the thermal foldback loop can reduce the battery charger's target current by A_{TJREG}</td></tr>
<tr><td>7:6</td><td>R/W</td><td>OTG_ILIM</td><td>00</td><td>CHGIN Output Current Limit in OTG Mode ($I_{CHGIN.OTG.LIM}$)
When MODE = 0x09 or 0x0A the CHGIN current limit is set at the following current limit:
00 = 500mA
01 = 900mA
10 =1200mA
11 = 1500mA</td></tr>
</table>

CHG_CNFG_03 Register Bit Description (0xBA):

NAME	FUNCTION	ADDR	TYPE	RESET
CHG_CNFG_03	Charger configuration 03	0xBA	O R/W (protected with CHGPROT)	0xDA

BIT	MODE	NAME	RESET	DESCRIPTION
2:0	R/W	TO_ITH	010 (150mA)	Top-Off Current Threshold. The charger transitions from its fast-charge constant voltage mode to its top-off mode when the charger current decays to the value programmed by this register. This transition generates a CHG_I interrupt and causes the CHG_DTLS register to report top-off mode. This transition also starts the top-off time as programmed by TO_TIME. 0x00 = 0.1A 0x01 = 0.125A 0x02 = 0.15A 0x03 = 0.175A 0x04 = 0.2A 0x05 = 0.25A 0x06 = 0.3A 0x07 = 0.35A
5:3	R/W	TO_TIME	011 (30min)	Top-Off Timer Setting 0x00 = 0min 0x01 = 10min 0x02 = 20min 0x03 = 30min 0x04 = 40min 0x05 = 50min 0x06 = 60min 0x07 = 70min
7:6	R/W	ILIM	11	Program Buck Peak Current Limit 00: support ICHG=3.00A 01: support ICHG=2.75A 10: support ICHG= 2.50A 11: support ICHG=2.25A

CHG_CNFG_04 Register Bit Description (0xBB):

NAME	FUNCTION	ADDR	TYPE	RESET
CHG_CNFG_04	Charger configuration 04	0xBB	O R/W (protected with CHGPROT)	0x96

<table>
<tr><th>BIT</th><th>MODE</th><th>NAME</th><th>RESET</th><th colspan="6">DESCRIPTION</th></tr>
<tr><td rowspan="18">5:0</td><td rowspan="18">R/W</td><td rowspan="18">CHG_CV_PRM</td><td rowspan="18">010110
(4.2V)</td><td colspan="6">Primary Charge Termination Voltage Setting
When the charger is enabled and the main-battery temperature is < T3 if JEITA = 1 or < T4 if JEITA = 0, then, the charger's battery regulation voltage (V_{BATREG}) is set by CHG_CV_PRM.</td></tr>
<tr><th>BITS</th><th>V</th><th>BITS</th><th>V</th><th>BITS</th><th>V</th></tr>
<tr><td>0x00</td><td>3.650</td><td>0x10</td><td>4.050</td><td>0x20</td><td>4.425</td></tr>
<tr><td>0x01</td><td>3.675</td><td>0x11</td><td>4.075</td><td>0x21</td><td>4.450</td></tr>
<tr><td>0x02</td><td>3.700</td><td>0x12</td><td>4.100</td><td>0x22</td><td>4.475</td></tr>
<tr><td>0x03</td><td>3.725</td><td>0x13</td><td>4.125</td><td>0x23</td><td>4.500</td></tr>
<tr><td>0x04</td><td>3.750</td><td>0x14</td><td>4.150</td><td>0x24</td><td>4.525</td></tr>
<tr><td>0x05</td><td>3.775</td><td>0x15</td><td>4.175</td><td>0x25</td><td>4.550</td></tr>
<tr><td>0x06</td><td>3.800</td><td>0x16</td><td>4.200</td><td>0x26</td><td>4.575</td></tr>
<tr><td>0x07</td><td>3.825</td><td>0x17</td><td>4.225</td><td>0x27</td><td>4.600</td></tr>
<tr><td>0x08</td><td>3.850</td><td>0x18</td><td>4.250</td><td>0x28</td><td>4.625</td></tr>
<tr><td>0x09</td><td>3.875</td><td>0x19</td><td>4.275</td><td>0x29</td><td>4.650</td></tr>
<tr><td>0x0A</td><td>3.900</td><td>0x1A</td><td>4.300</td><td>0x2A</td><td>4.675</td></tr>
<tr><td>0x0B</td><td>3.925</td><td>0x1B</td><td>4.325</td><td>0x2B</td><td>4.700</td></tr>
<tr><td>0x0C</td><td>3.950</td><td>0x1C</td><td>4.340</td><td></td><td></td></tr>
<tr><td>0x0D</td><td>3.975</td><td>0x1D</td><td>4.350</td><td></td><td></td></tr>
<tr><td>0x0E</td><td>4.000</td><td>0x1E</td><td>4.375</td><td></td><td></td></tr>
<tr><td>0x0F</td><td>4.025</td><td>0x1F</td><td>4.400</td><td></td><td></td></tr>
<tr><td>7:6</td><td>R/W</td><td>MINVSYS</td><td>10
(3.6V)</td><td colspan="6">Minimum System Regulation Voltage (V_{SYSMIN})
0x00 = 3.4V
0x01 = 3.5V
0x02 = 3.6V
0x03 = 3.7V</td></tr>
</table>

CHG_CNFG_06 Register Bit Description (0xBD):

NAME	FUNCTION	ADDR	TYPE	RESET
CHG_CNFG_06	Charger configuration 06	0xBD	O	0x00

BIT	MODE	NAME	RESET	DESCRIPTION
1:0	R/W	WDTCLR	00	Watchdog Timer Clear Bits Writing 01 to these bits clears the watchdog timer when the watchdog timer is enabled. 0x00 = the watchdog timer is not cleared 0x01 = the watchdog timer is cleared 0x02 = the watchdog timer is not cleared 0x03 = the watchdog timer is not cleared
3:2	R/W	CHGPROT	00	Charger Settings Protection Bits Writing 11 to these bits unlocks the write capability for the registers who are protected with CHGPROT writing any value besides 11 locks these registers. 0x00 = write capability is locked 0x01 = write capability is locked 0x02 = write capability is locked 0x03 = write capability is unlocked
7:4	R/W	RSVD	0000	Reserved

CHG_CNFG_07 Register Bit Description (0xBE):

NAME	FUNCTION	ADDR	TYPE	RESET
CHG_CNFG_07	Charger configuration 07	0xBE	O R/W (protected with CHGPROT)	0x40

BIT	MODE	NAME	RESET	DESCRIPTION
4:0	R/W	RSVD	00000	Reserved
6:5	R/W	REGTEMP	10	Junction Temperature Thermal Regulation Loop Set point. The charger's target current limit starts to foldback and the TREG bit is set if the junction temperature is greater than the REGTEMP setpoint. 0x00 = 85°C 0x01 = 100°C 0x02 = 115°C 0x03 = 130°C
7	R/W	RSVD	0	Reserved

CHG_CNFG_09 Register Bit Description (0xC0):

NAME	FUNCTION	ADDR	TYPE	RESET
CHG_CNFG_09	Charger configuration 09	0xC0	O	0x0F

BIT	MODE	NAME	RESET	DESCRIPTION
6:0	R/W	CHGIN_ILIM	0x0F (0.50A)	Maximum Input Current Limit Selection 7-bit adjustment from 100mA to 4.0A in 33mA steps. Note that the first 4 codes are all 100mA:
7	R/W	RSVD	0	Reserved

Bits	Unit (mA)	Bits	Unit (mA)	Bits	Unit (mA)	Bits	Unit (mA)
0x00	100	0x20	1067	0x40	2133	0x60	3200
0x01	100	0x21	1100	0x41	2167	0x61	3233
0x02	100	0x22	1133	0x42	2200	0x62	3267
0x03	100	0x23	1167	0x43	2233	0x63	3300
0x04	133	0x24	1200	0x44	2267	0x64	3333
0x05	167	0x25	1233	0x45	2300	0x65	3367
0x06	200	0x26	1267	0x46	2333	0x66	3400
0x07	233	0x27	1300	0x47	2367	0x67	3433
0x08	267	0x28	1333	0x48	2400	0x68	3467
0x09	300	0x29	1367	0x49	2433	0x69	3500
0x0A	333	0x2A	1400	0x4A	2467	0x6A	3533
0x0B	367	0x2B	1433	0x4B	2500	0x6B	3567
0x0C	400	0x2C	1467	0x4C	2533	0x6C	3600
0x0D	433	0x2D	1500	0x4D	2567	0x6D	3633
0x0E	467	0x2E	1533	0x4E	2600	0x6E	3667
0x0F	**500**	0x2F	1567	0x4F	2633	0x6F	3700
0x10	533	0x30	1600	0x50	2667	0x70	3733
0x11	567	0x31	1633	0x51	2700	0x71	3767
0x12	600	0x32	1667	0x52	2733	0x72	3800
0x13	633	0x33	1700	0x53	2767	0x73	3833
0x14	667	0x34	1733	0x54	2800	0x74	3867
0x15	700	0x35	1767	0x55	2833	0x75	3900
0x16	733	0x36	1800	0x56	2867	0x76	3933
0x17	767	0x37	1833	0x57	2900	0x77	3967
0x18	800	0x38	1867	0x58	2933	0x78	4000
0x19	833	0x39	1900	0x59	2967	0x79	4000
0x1A	867	0x3A	1933	0x5A	3000	0x7A	4000
0x1B	900	0x3B	1967	0x5B	3033	0x7B	4000
0x1C	933	0x3C	2000	0x5C	3067	0x7C	4000
0x1D	967	0x3D	2033	0x5D	3100	0x7D	4000
0x1E	1000	0x3E	2067	0x5E	3133	0x7E	4000
0x1F	1033	0x3F	2100	0x5F	3167	0x7F	4000

CHG_CNFG_10 Register Bit Description (0xC1):

NAME	FUNCTION	ADDR	TYPE	RESET
CHG_CNFG_10	Charger configuration 09	0xC1	O	0x19

<table>
<tr><th>BIT</th><th>MODE</th><th>NAME</th><th>RESET</th><th>DESCRIPTION</th></tr>
<tr><td>5:0</td><td>R/W</td><td>WCIN_ILIM</td><td>0x19
(0.50A)</td><td>Maximum Input Current Limit Selection
6bit adjustment from 60mA to 1.260A in 20mA steps. Note that the first 4 codes are all 60mA:
<table>
<tr><th>Bits</th><th>(mA)</th><th>Bits</th><th>(mA)</th></tr>
<tr><td>0x00</td><td>60</td><td>0x20</td><td>640</td></tr>
<tr><td>0x01</td><td>60</td><td>0x21</td><td>660</td></tr>
<tr><td>0x02</td><td>60</td><td>0x22</td><td>680</td></tr>
<tr><td>0x03</td><td>60</td><td>0x23</td><td>700</td></tr>
<tr><td>0x04</td><td>80</td><td>0x24</td><td>720</td></tr>
<tr><td>0x05</td><td>100</td><td>0x25</td><td>740</td></tr>
<tr><td>0x06</td><td>120</td><td>0x26</td><td>760</td></tr>
<tr><td>0x07</td><td>140</td><td>0x27</td><td>780</td></tr>
<tr><td>0x08</td><td>160</td><td>0x28</td><td>800</td></tr>
<tr><td>0x09</td><td>180</td><td>0x29</td><td>820</td></tr>
<tr><td>0x0A</td><td>200</td><td>0x2A</td><td>840</td></tr>
<tr><td>0x0B</td><td>220</td><td>0x2B</td><td>860</td></tr>
<tr><td>0x0C</td><td>240</td><td>0x2C</td><td>880</td></tr>
<tr><td>0x0D</td><td>260</td><td>0x2D</td><td>900</td></tr>
<tr><td>0x0E</td><td>280</td><td>0x2E</td><td>920</td></tr>
<tr><td>0x0F</td><td>300</td><td>0x2F</td><td>940</td></tr>
<tr><td>0x10</td><td>320</td><td>0x30</td><td>960</td></tr>
<tr><td>0x11</td><td>340</td><td>0x31</td><td>980</td></tr>
<tr><td>0x12</td><td>360</td><td>0x32</td><td>1000</td></tr>
<tr><td>0x13</td><td>380</td><td>0x33</td><td>1020</td></tr>
<tr><td>0x14</td><td>400</td><td>0x34</td><td>1040</td></tr>
<tr><td>0x15</td><td>420</td><td>0x35</td><td>1060</td></tr>
<tr><td>0x16</td><td>440</td><td>0x36</td><td>1080</td></tr>
<tr><td>0x17</td><td>460</td><td>0x37</td><td>1100</td></tr>
<tr><td>0x18</td><td>480</td><td>0x38</td><td>1120</td></tr>
<tr><td>0x19</td><td>500</td><td>0x39</td><td>1140</td></tr>
<tr><td>0x1A</td><td>520</td><td>0x3A</td><td>1160</td></tr>
<tr><td>0x1B</td><td>540</td><td>0x3B</td><td>1180</td></tr>
<tr><td>0x1C</td><td>560</td><td>0x3C</td><td>1200</td></tr>
<tr><td>0x1D</td><td>580</td><td>0x3D</td><td>1220</td></tr>
<tr><td>0x1E</td><td>600</td><td>0x3E</td><td>1240</td></tr>
<tr><td>0x1F</td><td>620</td><td>0x3F</td><td>1260</td></tr>
</table></td></tr>
<tr><td>7:6</td><td>R/W</td><td>RSVD</td><td>00</td><td>Reserved</td></tr>
</table>

CHG_CNFG_11 Register Bit Description (0xC2):

NAME	FUNCTION	ADDR	TYPE	RESET
CHG_CNFG_11	Charger configuration 11	0xC2	O	0x00

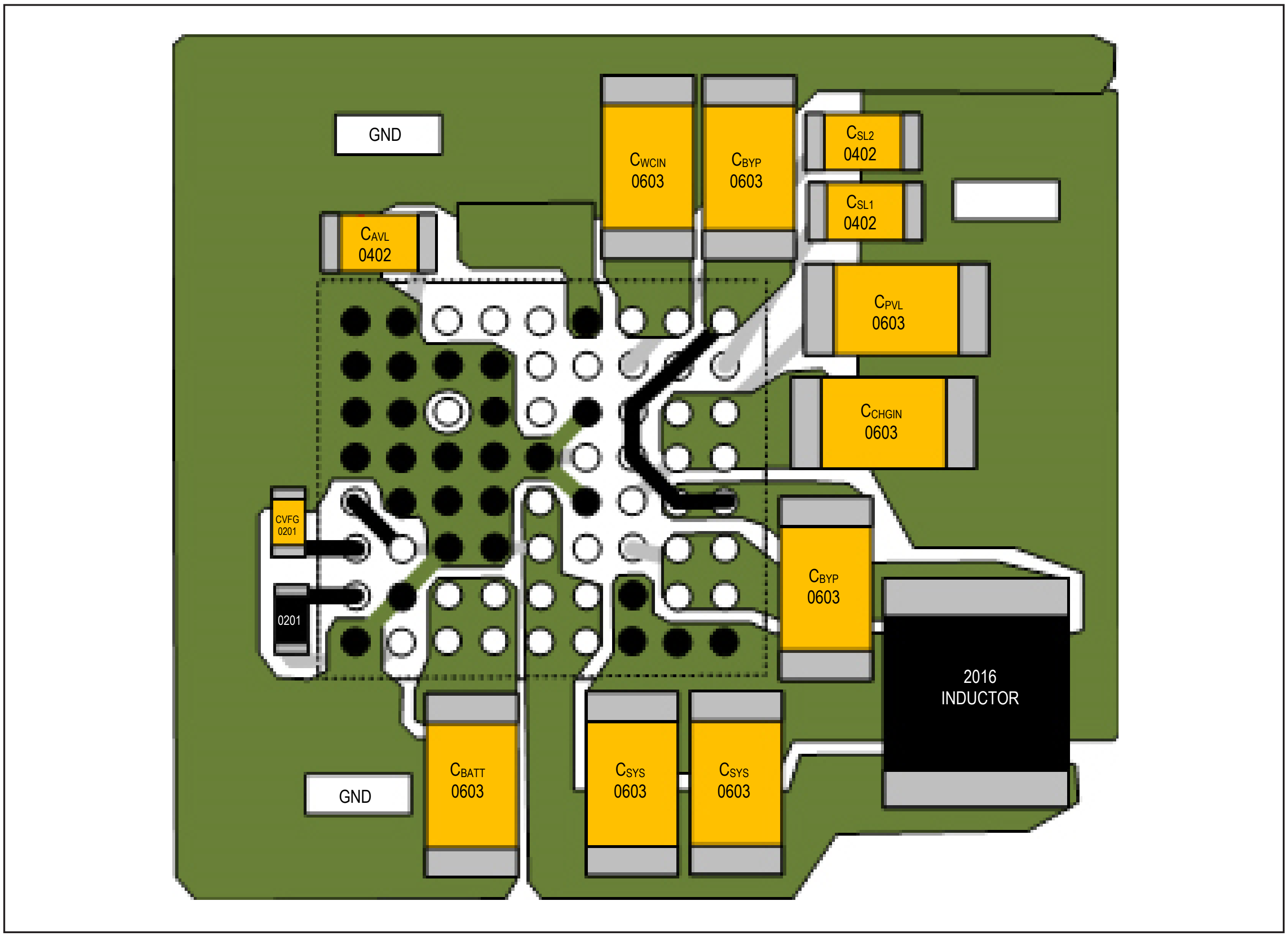
<table>
<tr><th>BIT</th><th>MODE</th><th>NAME</th><th>RESET</th><th colspan="8">DESCRIPTION</th></tr>
<tr><td rowspan="34">6:0</td><td rowspan="34">R/W</td><td rowspan="34">VBYPSET</td><td rowspan="34">0x00
(3V)</td><td colspan="8">Bypass Target Output Voltage in Boost Mode
3V (0x00) to 5.8V (0x70) in 0.025V steps. This setting is valid for the “boost only” mode (MODE = 0x08).</td></tr>
<tr><th>Bits</th><th>Unit (mA)</th><th>Bits</th><th>Unit (mA)</th><th>Bits</th><th>Unit (mA)</th><th>Bits</th><th>Unit (mA)</th></tr>
<tr><td>0x00</td><td>3.000</td><td>0x20</td><td>3.800</td><td>0x40</td><td>4.600</td><td>0x60</td><td>5.400</td></tr>
<tr><td>0x01</td><td>3.025</td><td>0x21</td><td>3.825</td><td>0x41</td><td>4.625</td><td>0x61</td><td>5.425</td></tr>
<tr><td>0x02</td><td>3.050</td><td>0x22</td><td>3.850</td><td>0x42</td><td>4.650</td><td>0x62</td><td>5.450</td></tr>
<tr><td>0x03</td><td>3.075</td><td>0x23</td><td>3.875</td><td>0x43</td><td>4.675</td><td>0x63</td><td>5.475</td></tr>
<tr><td>0x04</td><td>3.100</td><td>0x24</td><td>3.900</td><td>0x44</td><td>4.700</td><td>0x64</td><td>5.500</td></tr>
<tr><td>0x05</td><td>3.125</td><td>0x25</td><td>3.925</td><td>0x45</td><td>4.725</td><td>0x65</td><td>5.525</td></tr>
<tr><td>0x06</td><td>3.150</td><td>0x26</td><td>3.950</td><td>0x46</td><td>4.750</td><td>0x66</td><td>5.550</td></tr>
<tr><td>0x07</td><td>3.175</td><td>0x27</td><td>3.975</td><td>0x47</td><td>4.775</td><td>0x67</td><td>5.575</td></tr>
<tr><td>0x08</td><td>3.200</td><td>0x28</td><td>4.000</td><td>0x48</td><td>4.800</td><td>0x68</td><td>5.600</td></tr>
<tr><td>0x09</td><td>3.225</td><td>0x29</td><td>4.025</td><td>0x49</td><td>4.825</td><td>0x69</td><td>5.625</td></tr>
<tr><td>0x0A</td><td>3.250</td><td>0x2A</td><td>4.050</td><td>0x4A</td><td>4.850</td><td>0x6A</td><td>5.650</td></tr>
<tr><td>0x0B</td><td>3.275</td><td>0x2B</td><td>4.075</td><td>0x4B</td><td>4.875</td><td>0x6B</td><td>5.675</td></tr>
<tr><td>0x0C</td><td>3.300</td><td>0x2C</td><td>4.100</td><td>0x4C</td><td>4.900</td><td>0x6C</td><td>5.700</td></tr>
<tr><td>0x0D</td><td>3.325</td><td>0x2D</td><td>4.125</td><td>0x4D</td><td>4.925</td><td>0x6D</td><td>5.725</td></tr>
<tr><td>0x0E</td><td>3.350</td><td>0x2E</td><td>4.150</td><td>0x4E</td><td>4.950</td><td>0x6E</td><td>5.750</td></tr>
<tr><td>0x0F</td><td>3.375</td><td>0x2F</td><td>4.175</td><td>0x4F</td><td>4.975</td><td></td><td></td></tr>
<tr><td>0x10</td><td>3.400</td><td>0x30</td><td>4.200</td><td>0x50</td><td>5.000</td><td></td><td></td></tr>
<tr><td>0x11</td><td>3.425</td><td>0x31</td><td>4.225</td><td>0x51</td><td>5.025</td><td></td><td></td></tr>
<tr><td>0x12</td><td>3.450</td><td>0x32</td><td>4.250</td><td>0x52</td><td>5.050</td><td></td><td></td></tr>
<tr><td>0x13</td><td>3.475</td><td>0x33</td><td>4.275</td><td>0x53</td><td>5.075</td><td></td><td></td></tr>
<tr><td>0x14</td><td>3.500</td><td>0x34</td><td>4.300</td><td>0x54</td><td>5.100</td><td></td><td></td></tr>
<tr><td>0x15</td><td>3.525</td><td>0x35</td><td>4.325</td><td>0x55</td><td>5.125</td><td></td><td></td></tr>
<tr><td>0x16</td><td>3.550</td><td>0x36</td><td>4.350</td><td>0x56</td><td>5.150</td><td></td><td></td></tr>
<tr><td>0x17</td><td>3.575</td><td>0x37</td><td>4.375</td><td>0x57</td><td>5.175</td><td></td><td></td></tr>
<tr><td>0x18</td><td>3.600</td><td>0x38</td><td>4.400</td><td>0x58</td><td>5.200</td><td></td><td></td></tr>
<tr><td>0x19</td><td>3.625</td><td>0x39</td><td>4.425</td><td>0x59</td><td>5.225</td><td></td><td></td></tr>
<tr><td>0x1A</td><td>3.650</td><td>0x3A</td><td>4.450</td><td>0x5A</td><td>5.250</td><td></td><td></td></tr>
<tr><td>0x1B</td><td>3.675</td><td>0x3B</td><td>4.475</td><td>0x5B</td><td>5.275</td><td></td><td></td></tr>
<tr><td>0x1C</td><td>3.700</td><td>0x3C</td><td>4.500</td><td>0x5C</td><td>5.300</td><td></td><td></td></tr>
<tr><td>0x1D</td><td>3.725</td><td>0x3D</td><td>4.525</td><td>0x5D</td><td>5.325</td><td></td><td></td></tr>
<tr><td>0x1E</td><td>3.750</td><td>0x3E</td><td>4.550</td><td>0x5E</td><td>5.350</td><td></td><td></td></tr>
<tr><td>0x1F</td><td>3.775</td><td>0x3F</td><td>4.575</td><td>0x5F</td><td>5.375</td><td></td><td></td></tr>
<tr><td>7</td><td>R/W</td><td>RSVD</td><td>0</td><td colspan="8">Reserved</td></tr>
</table>

CHG_CNFG_12 Register Bit Description (0xC3):

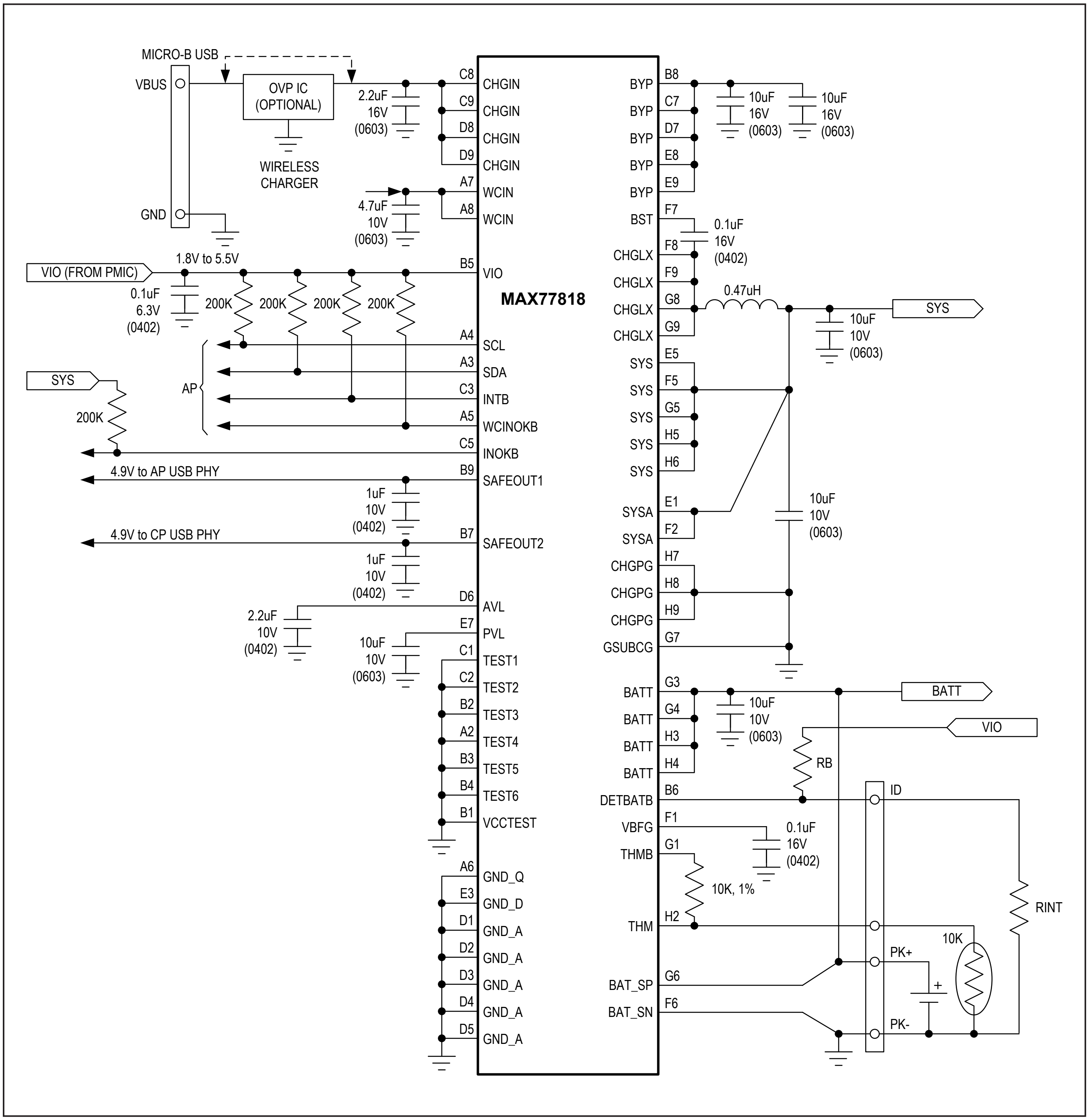
NAME	FUNCTION	ADDR	TYPE	RESET
CHG_CNFG_12	Charger configuration 12	0xC3	O	0x67

BIT	MODE	NAME	RESET	DESCRIPTION
2:0	R/W	B2SOVRC	111	BAT to SYS Overcurrent Threshold 0x00 = Disabled 0x01 = 3.00A 0x02 = 3.25A 0x03 = 3.50A 0x04 = 3.75A 0x05 = 4.00A 0x06 = 4.25A 0x07 = 4.50A
4:3	R/W	VCHGIN_REG	00	CHGIN Voltage Regulation Threshold (V_{CHGIN_REG}) Adjustment The CHGIN to GND Minimum Turn-On Threshold (V_{CHGIN_UVLO}) also scales with this adjustment. 0x00 = V_{CHGIN_REG} = 4.3V and V_{CHGIN_UVLO} = 4.5V 0x01 = V_{CHGIN_REG} = 4.7V and V_{CHGIN_UVLO} = 4.9V 0x02 = V_{CHGIN_REG} = 4.8V and V_{CHGIN_UVLO} = 5.0V 0x03 = V_{CHGIN_REG} = 4.9V and V_{CHGIN_UVLO} = 5.1V
5	R/W	CHGINSEL	1	CHGIN/USB Input Channel Select 0 = Disabled 1 = Enabled
6	R/W	WCINSEL	1	WCIN Input Channel Select 0 = Disabled 1 = Enabled
7	R/W	Reserved	0	Reserved

PCB Layout Guide



Typical Application Circuit



Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX77818EWZ+	-40°C to +85°C	72-pin WLP 0.4mm pitch, 3.867mm x 3.608mm (±0.015mm X and Y)

+Denotes lead(Pb)-free/RoHS-compliant package.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
72 WLP	W723B3+1	21-0477	Refer to Application Note 1891

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/15	Initial release	—

EPlast1.ru

Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits,General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.

Как с нами связаться

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