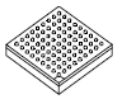
Freescale Semiconductor
Data Sheet: Advanced Information

Document Number: LS1024A
Rev. 0, **09/2014**

QorIQ LS1024A Data Sheet



LS1024A

The LS1024A product family addresses a wide variety of applications ranging from high-end VoIP and Video enabled home gateways, Small-to-Midsized Business (SMB) high performance security appliances to Ethernet powered 802.11ac enterprise access points and consumer networked storage products.

Building upon the field-hardened LS102MA, the LS1024A series of processors delivers vastly increased processing power and VoIP density, wire speed handling of small packets, DRM compliant security and enterprise grade VPN and SSL throughput. The new chip allows considerable system cost savings by integrating the new features that are now emerging in the CPE market.

LS1024A leverages the energy efficient core technology of ARM® and Freescale's low-power design process to achieve the lowest power consumption in its class. Additionally, the companion software development kit provides a rich set of power management features to address the energy saving goals of service providers and product manufacturers worldwide.

In addition to providing high throughput IPSec and SSL CPU offload, the LS1024A's onboard security engine includes a powerful Deep Packet Inspection Engine with GZIP decompression capability. The device's three Ethernet interfaces allow for DMZ configuration providing further security for SOHO/SMB routers and gateways.

LS1024A I/O interfaces in conjunction with Freescale's innovative multi-layer bus architecture allows non-blocking concurrent transactions across all data interfaces, thus minimizing on-chip packet processing latency. The LS1024A's SATA-2 interfaces, along with the powerful LRO/TSO and XOR Engine, provide an ideal solution for Network Attached Storage applications.

In order to provide performance scalability and maximum flexibility the LS1024A family of processors includes single and dual ARM® Cortex®-A9 core devices from 650 MHz to 1.2 GHz delivering up to 6000 DMIPS.

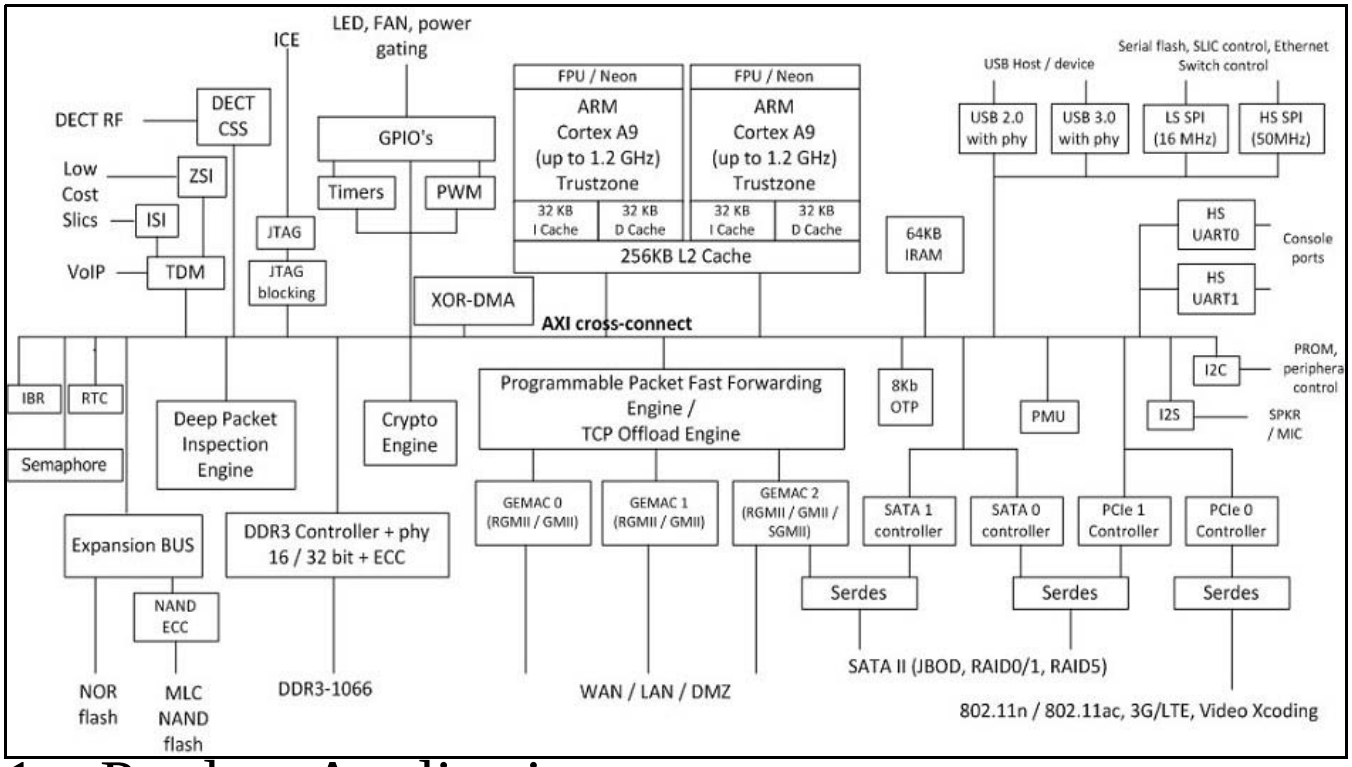
The LS1024A OpenWRT Linux-based SDK is optimized for both single- and dual-core operation. The software deliverable for the LS1024A dual core devices are backward compatible with the LS102MA and 100 line of products.

Additionally, Freescale's rich ecosystem delivers turnkey solutions that reduce time-to-market and lower development costs for VPN/SSL SMB routers, home gateway, Consumer NAS, and Enterprise Access Point manufacturers.

Figure 1-1 shows the block diagram of LS1024A device.

Table of Contents

Figure 1-1 LS1024A Block Diagram



1 Product Applications

The LS1024A product family addresses a wide variety of applications ranging from high-end VoIP and Video enabled home gateways, Small-to-Midsized business (SMB) high performance security appliances to Ethernet powered 802.11ac Enterprise Access Points and Consumer Networked Storage products.

The LS1024A product family provides ideal solution for:

- SMB IP-PBX / VoIP Gateways
- SOHO and SMB VPN Routers
- VoIP Residential Gateways
- Video Distribution Gateways
- Enterprise WiFi Access Points
- Network Attached Storage
- SMB VoIP Routers
- Secure Payment Terminals
- Mobile Broadband Routers

1.1 Features by Device Summary

The LS1024A devices differ in the number of complex voice channels they support in Data and Voice mode.

CAUTION: The device is screened for the specified frequency. Freescale cannot guarantee the operation if any changes are made in software. Any changes without prior approval from Freescale may cause unexpected results and void the warranty.

Table 1.1 Features by Device Summary

Cortex-A9 Frequency	Number of Cortex-A9 Cores	Device Number	VoIP Channels	DPI	DECT
1.2GHz	2	LS1024ASN7MLA	16	No	No
		LS1024ASE7MLA	16	Yes	Yes
900MHz	2	LS1024ASN7JLA	16	No	No
		LS1024ASE7JLA	16	Yes	Yes
650MHz	2	LS1024ASN7ELA	8	No	No
		LS1024ASE7ELA	8	No	Yes

2 Technical Overview

This section gives an overview of LS1024A device hardware interfaces, functional blocks, and software interfaces.

CAUTION: Freescale provides schematic and layout review. However, Freescale highly recommends customers to submit their designs to Freescale for a complete confidential review.

2.1 External Interfaces and Functional Blocks

2.1.1 External Interfaces

The LS1024A device provides the following external interfaces:

- DDR3 Controller — 16/32-bit DDR3 memory interface up to 533MHz (DDR3-1066) with optional ECC support. For more details, refer to Section 5 “DDR3 Controller” on page 61.
- Peripheral Component Interconnect Express (PCIe) Controller — The LS1024A device includes two single-lane PCIe interfaces conforming to the PCI Express Base Specification, Revision 2.1 and support Gen1 (2.5Gbps) and Gen2 (5Gbps) link rates. For more details, refer to Section 12 “PCI Express Interface” on page 99.
- Universal Serial Bus (USB) 2.0 Interface — USB high speed (480Mbps) controller and PHY with backward compatibility to USB 1.1. For more details. refer to Section 26 “USB 2.0 Interface” on page 159.
- Universal Serial Bus (USB) 3.0 Interface — USB super speed controller and PHY with dual-bus architecture to support concurrent USB2.0 (high speed, low speed and full speed) and USB3.0 (SuperSpeed) operations. For more details, refer to Section 27 “USB 3.0 Interface” on page 163.
- Serial Advanced Technology Attachment (SATA Controller) — Two (2) 3-Gbps SATA-2 interfaces. For more details, refer to Section 23 “SATA Interface” on page 149.
- Time-Division Multiplexing (TDM) Bus — Full duplex serial TDM bus supporting up to 128 time slots at 8.192MHz. For more details, refer to Section 20 “TDM Bus Interface” on page 137.
- Expansion Bus — Provides address, data, and control lines for connection to system peripheral devices. The Expansion Bus provides chip selects for system peripheral devices such as Flash memory, Boot ROM, and so on. The expansion bus supports 5 chip-selects: one for NAND and four for general purpose. For more details, refer to Section 4 “Expansion Bus Interface” on page 45.
- Inter-IC (I^2C) Bus — Supporting master, slave or multi-master modes. The I^2C bus can be used for booting. For more details. refer to Section 25 “Inter-IC Interface” on page 155.
- High-Speed Serial Peripheral Interface (HS-SPI) — Up to 50MHz, with 2 slave select. For more details, refer to Section 15 “DUSI Subsystem” on page 113.
- Low Speed Serial Peripheral Interface (LS-SPI) — Up to 16MHz, with 3 slave select. The LS-SPI interface can be used for booting. For more details, refer to Section 9 “Low Speed SPI” on page 85.
- General Purpose Input Output (GPIO) Interface — Up to 64 GPIOs. Eight (8) of the GPIOS can be configured to receive interrupts. Six (6) of the GPIOs can be pulse-width modulated. For more details, refer to Section 6 “General Purpose Input Output” on page 67.
- SerDes — Three programmable SerDes interfaces up to 5 Gbps.
  - SerDes #0 — PCIe0
  - SerDes #1 — PCIe1 or SATA0 - selection through bootstrap

  - SerDes #2 — SATA1 or SGMII - selection through bootstrap
- Silicon Labs Integrated Serial Interface (ISI)— 3-pin interface for reduced cost designs using Silabs SLICs. For more details, refer to Section 22 “SiLabs Integrated Serial Interface” on page 147.
- Microsemi ZSI Interface — 4-pin interface for reduced cost designs using Microsemi SLICs. For more details, refer to Section 21 “Microsemi ZSI Interface” on page 145.
- Dual Universal Asynchronous Receiver/Transmitter (UART) — With support for RS-232 and flow control. UART0 is Bluetooth capable with frequency up to 3Mbps. For more details, refer to Section 15 “DUSI Subsystem” on page 113.
- Inter-IC Sound (I2S) Interface — Master or slave, with sampling frequency up to 96kHz and 8/16 or 24 bits per channel. For more details, refer to Section 15 “DUSI Subsystem” on page 113.
- Joint Test Action Group (JTAG) Interface — The JTAG interface provides access to both Cortex®-A9 cores. It supports IEEE 1149.1 and boundary scan for manufacturing and test. For more details, refer to Section 24 “Joint Test Action Group (JTAG)” on page 153.
- Reference Clock — Using a single oscillator/crystal at 48MHz or 24MHz. For more details, refer to Section 7 “Clock and Reset” on page 69.

2.1.2 Functional Blocks

The LS1024A device provides the following functional blocks:

- Dual Core SMP ARM® Cortex®-A9 — Up to 1.2GHz, with two Neon® floating point DSPs, ARM Trustzone®, Coresight®, 32kB of I-Cache, 32kB of D-Cache and 256kB of L2 cache. Section 13, Dual Core SMP ARM® Cortex®-A9
- Hardware Packet Forwarding Engine also knows as Programmable Packet Forwarding Engine (PPFE) — Fully programmable engine for protocol handling, QoS, classification, ingress and egress control, and TCP offload. For more details, refer to Section 17 “PPFE (Ethernet Interface)” on page 123.
- Deep Packet Inspection (DPI) — High performance DPI engine to allow options such as antivirus, content blocking, copyright and policy enforcement and application aware QoS. For more details, refer to Section 16 “Deep Packet Inspection” on page 121.
- Security Engines — NIST- Certified, integrated hardware crypto engine for IPSEC and SSL/TLS offloads.
- Communication Sub-System (CSS) — DECT digital processor supporting CATiq 2.0, 2.1 and 3.0 and DECT-ULE for home automation. For more details, refer to Section 18 “DECT Communication Sub-System” on page 131.
- Power Management Unit (PMU) — Always-on, low power, programmable controller interruptible by PCIe, GMAC, PPFE, USB, SATA, UART, GPIO, timer and SLIC. Manages power states, clock domains and DVFS regulation based on processor load and traffic.Section 30 “Power Management” on page 175.
- XOR-DMA Controller — Multi-purpose DMA controller. Processes blocks up to 15 blocks of 4kB. For more details, refer to Section 28 “XOR-DMA Controller” on page 167.
- AXI / AHB Cross Connect Fabric — Multi-layer, 64-bit bus with support for ARM Trustzone® and multi-master mode. Section 14, AXI / AHB Cross Connect Fabric.
- Timer Block — Includes six general purpose interrupt capable timers. Two of the timers connect to I/O pins to drive an external output or allow an external signal to increment the timer. For more details, refer to Section 10 “Timer” on page 91.
- Internal Boot ROM (IBR) — 32kB of internal boot ROM with secondary boot from NOR flash, serial flash (SPI), EEPROM (I2C) or SATA. Section 31.1 “Internal Boot ROM” on page 181
- One Time Programmable Memory (OTPM) — High reliability, permanent, 8KBits memory for secure key or certificate storage. Section 11 “One Time Programmable Memory” on page 95.

- Internal SRAM (IRAM) — 64kBytes.
- Real Time Clock (RTC) — Battery operated, running from a 32.768 kHz crystal. Section 8, Real Time Clock
- Hardware Semaphore

3 Pinout and Signal Summary

This chapter gives a list of pinouts and a summary of device signal tables and its description.

3.1 Ball Map

Figure 3-1 illustrates the ball map (looking through the top of the package). Table 3-1 shows the ball name and location of the pins.

Figure 3-1 LS1024A Ball Map

Table 3-1 LS1024A Pinout List

Location	Signal Symbol	Direction	Type	Tolerant	PU/PD	Strength
A1	VSS_RING					
A2	VSS_RING					
A3	S0_CK_100P	O		1.1 V		
A4	S0_CK_100M	O		1.1 V		
A5	PS_XI	I	OSCL	3.3 V		
A6	SPI_2_SS0_N	O	LVCMOS	3.3 V		11 mA
A7	VSS_RING					
A8	USB0_DVSS					
A9	USB0_DP	I/O	ANLG			
A10	USB0_VSSA					
A11	USB1_RX_P	I				
A12	VSS_RING					
A13	USB1_TX_P	O				
A14	USB1_DP	I/O	ANLG			
A15	DDR_ECC_DATA_7	I/O	SSTL			
A16	DDR_ECC_DATA_4	I/O	SSTL			
A17	DDR_ECC_DATA_3	I/O	SSTL			
A18	DDR_DATA_31	I/O	SSTL			
A19	DDR_DATA_28	I/O	SSTL			
A20	DDR_DATA_27	I/O	SSTL			
A21	DDR_DM_2	O	SSTL			
A22	DDR_DATA_16	I/O	SSTL			
A23	DDR_DATA_21	I/O	SSTL			
A24	VSS_RING					
A25	VSS_RING					
B1	VSS_RING					
B2	VSS_RING					

Table 3-1 LS1024A Pinout List (continued)

Location	Signal Symbol	Direction	Type	Tolerant	PU/PD	Strength
B3	S1_CK_100P	O		1.1 V		
B4	S1_CK_100M	O		1.1 V		
B5	PS_XO	O	OSCL	3.3 V		
B6	SPI_2_SS1_N	O	LVCMOS	3.3 V		11 mA
B7	VSS_RING					
B8	TM_TESTMODE_N_1	I	LVCMOS	3.3 V	PU	
B9	USB0_DM	I/O	ANLG			
B10	USB0_VSSAC					
B11	USB1_RX_M	I				
B12	VSS_RING					
B13	USB1_TX_M	O				
B14	USB1_DM	I/O	ANLG			
B15	DDR_ZQ	O	SSTL			
B16	DDR_ECC_DATA_6	I/O	SSTL			
B17	DDR_ECC_DATA_2	I/O	SSTL			
B18	DDR_VDDQ					
B19	DDR_DATA_30	I/O	SSTL			
B20	DDR_DATA_26	I/O	SSTL			
B21	DDR_VDDQ					
B22	DDR_DATA_18	I/O	SSTL			
B23	DDR_DATA_22	I/O	SSTL			
B24	DDR_BA_0	O	SSTL			
B25	VSS_RING					
C1	S0_RXP	I	ANLG			
C2	S0_RXM	I	ANLG			
C3	VSS_RING					
C4	TM_TESTMODE_N_2	I	LVCMOS	3.3 V	PU	
C5	GPIO00	I/O	LVCMOS	5 V	PU	10 mA
C6	SPI_2_TXD	O	LVCMOS	3.3 V		11 mA
C7	VSS_RING					
C8	VSS_RING					
C9	USB0_VDD33					
C10	UP_XI	I	OSCL	3.3 V		
C11	USB0_REXT	I/O	ANLG			
C12	USB1_RESREF	I/O	ANLG			
C13	VSS_RING					

Table 3-1 LS1024A Pinout List (continued)

Location	Signal Symbol	Direction	Type	Tolerant	PU/PD	Strength
C14	VSS_RING					
C15	DDR_VDDQZQ					
C16	DDR_ECC_DATA_5	I/O	SSTL			
C17	DDR_ECC_DM	O	SSTL			
C18	VSS_RING					
C19	DDR_DATA_29	I/O	SSTL			
C20	DDR_DM_3	O	SSTL			
C21	VSS_RING					
C22	DDR_DATA_19	I/O	SSTL			
C23	DDR_DATA_20	I/O	SSTL			
C24	DDR_BA_2	O	SSTL			
C25	DDR_BA_1	O	SSTL			
D1	S0_TXM	O	ANLG			
D2	S0_TXP	O	ANLG			
D3	VSS_RING					
D4	GPIO07	I/O	LVCMOS	5 V	PU	10 mA
D5	SPI_2_RXD	I	LVCMOS	3.3 V	PD	
D6	SPI_2_SCLK	O	LVCMOS	3.3 V		11 mA
D7	TM_TESTMODE_N_0	I	LVCMOS	3.3 V	PU	
D8	PLL3_FILTER	I	ANLG	3.3 V		
D9	USB0_VBUS	I	ANLG	5 V		
D10	UP_XO	O	OSCL	3.3 V		
D11	VSS_RING					
D12	USB1_REF_CLK_M	I	ANLG			
D13	USB1_REF_CLK_P	I	ANLG			
D14	USB1_VBUS	I/O	ANLG	5 V		
D15	DDR_VSSQZQ					
D16	DDR_ECC_DATA_1	I/O	SSTL			
D17	DDR_ECC_DATA_0	I/O	SSTL			
D18	DDR_VDDQ					
D19	DDR_DATA_25	I/O	SSTL			
D20	DDR_DATA_24	I/O	SSTL			
D21	DDR_VDDQ					
D22	DDR_DATA_17	I/O	SSTL			
D23	DDR_DATA_23	I/O	SSTL			
D24	DDR_A_11	O	SSTL			

Table 3-1 LS1024A Pinout List (continued)

Location	Signal Symbol	Direction	Type	Tolerant	PU/PD	Strength
D25	DDR_A_14	O	SSTL			
E1	S0_REFCLKP	I	ANLG			
E2	S0_REFCLKM	I	ANLG			
E3	VSS_RING					
E4	GPIO06	I/O	LVCMOS	5 V	PU	10 mA
E5	TM_LEGACY_MODE_N	I	LVCMOS	3.3 V	PU	
E6	IO_VDD_RING					
E7	VSS_RING					
E8	VSS_RING					
E9	VSS_RING					
E10	USB0_VDD33					
E11	USB0_ATEST	I/O	ANLG			
E12	UPOSC_DVDD					
E13	VSS_RING					
E14	VSS_RING					
E15	VSS_RING					
E16	DDR_ECC_DQS_N	I/O	SSTL			
E17	DDR_ECC_DQS	I/O	SSTL			
E18	VSS_RING					
E19	DDR_DQS_N_3	I/O	SSTL			
E20	DDR_DQS_3	I/O	SSTL			
E21	VSS_RING					
E22	DDR_DQS_N_2	I/O	SSTL			
E23	DDR_DQS_2	I/O	SSTL			
E24	VSS_RING					
E25	DDR_A_12	O	SSTL			
F1	VSS_RING					
F2	VSS_RING					
F3	VSS_RING					
F4	GPIO14	I/O	LVCMOS	5 V	PU	10 mA
F5	IO_VDD_RING					
F6	PCIE1_CLKO	O	LVCMOS	3.3 V		8 mA
F7	PLL0_AVDD					
F8	PLL3_AVSS					
F9	PLL3_AVDD					
F10	USB0_DVDD					

Table 3-1 LS1024A Pinout List (continued)

Location	Signal Symbol	Direction	Type	Tolerant	PU/PD	Strength
F11	CORE_VDD_RING					
F12	USB1_ID	I/O	ANLG			
F13	CORE_VDD_RING					
F14	VSS_RING					
F15	E_DVDD					
F16	DDR_VDDQ					
F17	VSS_RING					
F18	DDR_VDDQ					
F19	DDR_VDDQ					
F20	VSS_RING					
F21	DDR_VDDQ					
F22	DDR_VDDQ					
F23	DDR_CKE	O	SSTL		PD	
F24	DDR_ODT_1	O	SSTL			
F25	DDR_A_13	O	SSTL			
G1	S1_RXP	I	ANLG			
G2	S1_RXM	I	ANLG			
G3	VSS_RING					
G4	PSOSC_DVDD					
G5	VSS_RING					
G6	PCIE0_CLKO	O	LVCMOS	3.3 V		8 mA
G7	PLL0_AVSS					
G8	FSOURCE_ECID	I/O	PWR			
G9	CORE_VDD_RING					
G10	CORE_VDD_RING					
G11	CORE_VDD_RING					
G12	VSS_RING					
G13	CORE_VDD_RING					
G14	VSS_RING					
G15	DDR_VDDQ					
G16	VSS_RING					
G17	DDR_VDDQ					
G18	VSS_RING					
G19	DDR_VREF_RING					
G20	DDR_VDDQ					
G21	VSS_RING					

Table 3-1 LS1024A Pinout List (continued)

Location	Signal Symbol	Direction	Type	Tolerant	PU/PD	Strength
G22	DDR_A_2	O	SSTL			
G23	DDR_A_9	O	SSTL			
G24	DDR_A_8	O	SSTL			
G25	DDR_ODT_0	O	SSTL			
H1	S1_TXM	O	ANLG			
H2	S1_TXP	O	ANLG			
H3	VSS_RING					
H4	GPIO15	I/O	LVCMOS	5 V	PU	10 mA
H5	VSS_RING					
H6	S0_ATEST	O	ANLG			
H7	PLL1_AVSS					
H8	PLL1_AVDD					
H9	CORE_VDD_RING					
H10	CORE_VDD_RING					
H11	CORE_VDD_RING					
H12	USB3_VDD_RING					
H13	CORE_VDD_RING					
H14	VSS_RING					
H15	DDR_VDDQ					
H16	VSS_RING					
H17	DDR_VDDQ					
H18	CORE_VDD_RING					
H19	CORE_VDD_RING					
H20	VSS_RING					
H21	DDR_VDDQ					
H22	DDR_A_4	O	SSTL			
H23	DDR_A_5	O	SSTL			
H24	DDR_A_6	O	SSTL			
H25	DDR_A_7	O	SSTL			
J1	S1_REFCLKP	I	ANLG			
J2	S1_REFCLKM	I	ANLG			
J3	VSS_RING					
J4	S0_RESREF	I/O	ANLG			
J5	VSS_RING					
J6	S1_ATEST	O	ANLG			
J7	PLL2_AVSS					

Table 3-1 LS1024A Pinout List (continued)

Location	Signal Symbol	Direction	Type	Tolerant	PU/PD	Strength
J8	PLL2_AVDD					
J9	IO_VDD_RING					
J10	CORE_VDD_RING					
J11	VP					
J12	USB3_VDD_RING					
J13	CORE_VDD_RING					
J14	VSS_RING					
J15	DDR_VDDQ					
J16	VSS_RING					
J17	DDR_VDDQ					
J18	CORESIGHT_D15	0	LVCMOS	3.3 V		28 mA
J19	CORESIGHT_D14	0	LVCMOS	3.3 V		28 mA
J20	DDR_VDDQ					
J21	VSS_RING					
J22	DDR_CS_N_0	O	SSTL			
J23	DDR_A_0	O	SSTL			
J24	DDR_A_1	O	SSTL			
J25	DDR_A_3	O	SSTL			
K1	S2_TXM	O	ANLG			
K2	S2_TXP	O	ANLG			
K3	S2_REFCLKM	I	ANLG			
K4	S1_RESREF	I/O	ANLG			
K5	VSS_RING					
K6	S2_ATEST	O	ANLG			
K7	S0_VDDT_0					
K8	S0_VDDA					
K9	S0_VDDHA					
K10	CORE_VDD_RING					
K11	VPTX0					
K12	DVDD					
K13	CORE_VDD_RING					
K14	VSS_RING					
K15	DDR_VDDQ					
K16	VSS_RING					
K17	DDR_VDDQ					
K18	CORESIGHT_D13	0	LVCMOS	3.3 V		28 mA

Table 3-1 LS1024A Pinout List (continued)

Location	Signal Symbol	Direction	Type	Tolerant	PU/PD	Strength
K19	CORESIGHT_D12	0	LVCMOS	3.3 V		28 mA
K20	VSS_RING					
K21	DDR_VDDQ					
K22	DDR_GATE_I	I	SSTL			
K23	DDR_GATE_O	O	SSTL			
K24	DDR_CLK_1	O	SSTL			
K25	DDR_CLK_N_1	O	SSTL			
L1	S2_RXP	I	ANLG			
L2	S2_RXM	I	ANLG			
L3	S2_REFCLKP	I	ANLG			
L4	S2_RESREF	I/O	ANLG			
L5	VSS_RING					
L6	VSS_RING					
L7	S1_VDDT_0					
L8	S1_VDDA					
L9	S1_VDDHA					
L10	VSS_RING					
L11	CORE_VDD_RING					
L12	CORE_VDD_RING					
L13	CORE_VDD_RING					
L14	VSS_RING					
L15	DDR_VDDQ					
L16	DDR_VDDQ					
L17	DDR_VDDQ					
L18	CORE_VDD_RING					
L19	CORE_VDD_RING					
L20	DDR_VDDQ					
L21	VSS_RING					
L22	DDR_CS_N_1	O	SSTL			
L23	DDR_WE_N	O	SSTL			
L24	DDR_CLK_0	O	SSTL			
L25	DDR_CLK_N_0	O	SSTL			
M1	VSS_RING					
M2	VSS_RING					
M3	VSS_RING					
M4	GEM0_REFCLK	O	LVCMOS	3.3 V		8 mA

Table 3-1 LS1024A Pinout List (continued)

Location	Signal Symbol	Direction	Type	Tolerant	PU/PD	Strength
M5	VSS_RING					
M6	VSS_RING					
M7	S2_VDDT_0					
M8	S2_VDDA					
M9	S2_VDDHA					
M10	VSS_RING					
M11	CORE_VDD_RING					
M12	CORE_VDD_RING					
M13	CORE_VDD_RING					
M14	CORE_VDD_RING					
M15	DDR_VDDQ					
M16	DDR_VDDQ					
M17	DDR_VDDQ					
M18	CORESIGHT_D10	0	LVCMOS	3.3 V		28 mA
M19	CORESIGHT_D11	0	LVCMOS	3.3 V		28 mA
M20	VSS_RING					
M21	DDR_VDDQ					
M22	DDR_RESET_N	O				
M23	DDR_CAS_N	O	SSTL			
M24	DDR_A_10	O	SSTL			
M25	DDR_RAS_N	O	SSTL			
N1	GEM0_RXC	I		3.3 V		17 mA
N2	GEM0_RX_CTL	I		3.3 V		17 mA
N3	GEM0_RXD_3	I		3.3 V		17 mA
N4	GEM0_RXD_2	I		3.3 V		17 mA
N5	GEM0_RXD_1	I		3.3 V		17 mA
N6	VSS_RING					
N7	GEM0_DVDD					
N8	GEM0_DVDD					
N9	GEM0_DVDD					
N10	VDD_HFE					
N11	VDD_HFE					
N12	VDD_HFE					
N13	VDD_A9					
N14	VSS_RING					
N15	DDR_VDDQ					

Table 3-1 LS1024A Pinout List (continued)

Location	Signal Symbol	Direction	Type	Tolerant	PU/PD	Strength
N16	VSS_RING					
N17	DDR_VDDQ					
N18	CORESIGHT_D8	0	LVCMOS	3.3 V		28 mA
N19	CORESIGHT_D9	0	LVCMOS	3.3 V		28 mA
N20	DDR_VDDQ					
N21	VSS_RING					
N22	DDR_VDDQ					
N23	VSS_RING					
N24	DDR_VDDQ					
N25	DDR_DATA_8	I/O	SSTL			
P1	GEM0_RXD_0	I		3.3 V		17 mA
P2	GEM0_TXC	O		3.3 V		17 mA
P3	GEM0_TX_CTL	O		3.3 V		17 mA
P4	GEM0_TXD_3	O		3.3 V		17 mA
P5	GEM0_TXD_2	O		3.3 V		17 mA
P6	VSS_RING					
P7	GEM1_DVDD					
P8	GEM0_DVDD					
P9	GEM0_DVDD					
P10	VDD_HFE					
P11	VDD_HFE					
P12	VDD_HFE					
P13	VDD_A9					
P14	VSS_RING					
P15	VDD_A9					
P16	VSS_RING					
P17	DDR_VDDQ					
P18	VSS_RING					
P19	VSS_RING					
P20	VSS_RING					
P21	DDR_DQS_1	I/O	SSTL			
P22	DDR_DATA_9	I/O	SSTL			
P23	DDR_DATA_11	I/O	SSTL			
P24	DDR_DATA_10	I/O	SSTL			
P25	DDR_DM_1	O	SSTL			
R1	GEM0_TXD_1	O		3.3 V		17 mA

Table 3-1 LS1024A Pinout List (continued)

Location	Signal Symbol	Direction	Type	Tolerant	PU/PD	Strength
R2	GEM0_TXD_0	O		3.3 V		17 mA
R3	VSS_RING					
R4	VSS_RING					
R5	VSS_RING					
R6	VSS_RING					
R7	GEM1_DVDD					
R8	GEM1_DVDD					
R9	GEM1_DVDD					
R10	VDD_HFE					
R11	VDD_A9					
R12	VDD_HFE					
R13	VDD_A9					
R14	VSS_RING					
R15	VDD_A9					
R16	VSS_RING					
R17	DDR_VDDQ					
R18	CORESIGHT_D6	0	LVCMOS	3.3 V		28 mA
R19	CORESIGHT_D7	0	LVCMOS	3.3 V		28 mA
R20	DDR_VDDQ					
R21	DDR_DQS_N_1	I/O	SSTL			
R22	DDR_DATA_15	I/O	SSTL			
R23	DDR_DATA_12	I/O	SSTL			
R24	DDR_DATA_14	I/O	SSTL			
R25	DDR_DATA_13	I/O	SSTL			
T1	GEM1_RXC	I		3.3 V		17 mA
T2	GEM1_RX_CTL	I		3.3 V		17 mA
T3	GEM1_RXD_3	I		3.3 V		17 mA
T4	GEM1_RXD_2	I		3.3 V		17 mA
T5	GEM1_REFCLK	O	LVCMOS	3.3 V		8 mA
T6	VSS_RING					
T7	GEM2_DVDD					
T8	GEM2_DVDD					
T9	GEM2_DVDD					
T10	VDD_HFE					
T11	VDD_A9					
T12	VDD_HFE					

Table 3-1 LS1024A Pinout List (continued)

Location	Signal Symbol	Direction	Type	Tolerant	PU/PD	Strength
T13	VDD_A9					
T14	VSS_RING					
T15	VDD_A9					
T16	VSS_RING					
T17	DDR_VDDQ					
T18	CORESIGHT_D4	0	LVCMOS	3.3 V		28 mA
T19	CORESIGHT_D5	0	LVCMOS	3.3 V		28 mA
T20	DDR_VREF_RING	I				
T21	VSS_RING					
T22	DDR_VDDQ					
T23	VSS_RING					
T24	DDR_VDDQ					
T25	DDR_DATA_7	I/O	SSTL			
U1	GEM1_RXD_1	I		3.3 V		17 mA
U2	GEM1_RXD_0	I		3.3 V		17 mA
U3	GEM1_TXC	O		3.3 V		17 mA
U4	GEM1_TX_CTL	O		3.3 V		17 mA
U5	GEM1_TXD_3	O		3.3 V		17 mA
U6	VSS_RING					
U7	VSS_RING					
U8	GEM2_DVDD					
U9	VSS_RING					
U10	VSS_RING					
U11	VSS_RING					
U12	CORE_VDD_RING					
U13	VDD_A9					
U14	VSS_RING					
U15	VDD_A9					
U16	VSS_RING					
U17	DDR_VDDQ					
U18	CORE_VDD_RING					
U19	CORE_VDD_RING					
U20	DDR_VDDQ					
U21	DDR_DQS_N_0	I/O	SSTL			
U22	DDR_DATA_1	I/O	SSTL			
U23	DDR_DATA_5	I/O	SSTL			

Table 3-1 LS1024A Pinout List (continued)

Location	Signal Symbol	Direction	Type	Tolerant	PU/PD	Strength
U24	DDR_DATA_6	I/O	SSTL			
U25	DDR_DATA_4	I/O	SSTL			
V1	GEM1_TXD_2	O		3.3 V		17 mA
V2	GEM1_TXD_1	O		3.3 V		17 mA
V3	VSS_RING					
V4	VSS_RING					
V5	VSS_RING					
V6	VSS_RING					
V7	VSS_RING					
V8	VSS_RING					
V9	IO_VDD_RING					
V10	VSS_RING					
V11	IO_VDD_RING					
V12	VSS_RING					
V13	VDD_A9					
V14	VSS_RING					
V15	VDD_A9					
V16	VSS_RING					
V17	VSS_RING					
V18	CORESIGHT_D3	0	LVCMOS	3.3 V		28 mA
V19	CORESIGHT_D2	0	LVCMOS	3.3 V		28 mA
V20	VSS_RING					
V21	DDR_DQS_0	I/O	SSTL			
V22	DDR_DATA_0	I/O	SSTL			
V23	DDR_DM_0	O	SSTL			
V24	DDR_DATA_2	I/O	SSTL			
V25	DDR_DATA_3	I/O	SSTL			
W1	GEM1_TXD_0	O		3.3 V		17 mA
W2	GEM2_RXC	I/O		3.3 V		17 mA
W3	GEM2_RX_CTL	I/O		3.3 V		17 mA
W4	GEM2_RXD_3	I/O		3.3 V		17 mA
W5	GEM2_RXD_2	I/O		3.3 V		17 mA
W6	VSS_RING					
W7	IO_VDD_RING					
W8	VSS_RING					
W9	IO_VDD_RING					

Table 3-1 LS1024A Pinout List (continued)

Location	Signal Symbol	Direction	Type	Tolerant	PU/PD	Strength
W10	VSS_RING					
W11	IO_VDD_RING					
W12	VSS_RING					
W13	VDD_A9					
W14	VSS_RING					
W15	VDD_A9					
W16	VSS_RING					
W17	VSS_RING					
W18	CORESIGHT_D1	0	LVCMOS	3.3 V		28 mA
W19	CORESIGHT_D0	0	LVCMOS	3.3 V		28 mA
W20	CORESIGHT_CLK	O	LVCMOS	3.3 V		28 mA
W21	VSS_RING					
W22	RTC_VDD					
W23	OTP_VDDIO					
W24	RTC_XI	I	OSCL	3.3 V		
W25	RTC_XO	O	OSCL	3.3 V		
Y1	GEM2_RXD_1	I/O		3.3 V		17 mA
Y2	GEM2_RXD_0	I/O		3.3 V		17 mA
Y3	GEM2_TXC	I/O		3.3 V		17 mA
Y4	GEM2_TX_CTL	I/O		3.3 V		17 mA
Y5	GEM2_TXD_3	I/O		3.3 V		17 mA
Y6	VSS_RING					
Y7	IO_VDD_RING					
Y8	VSS_RING					
Y9	IO_VDD_RING					
Y10	VSS_RING					
Y11	IO_VDD_RING					
Y12	VSS_RING					
Y13	IO_VDD_RING					
Y14	VSS_RING					
Y15	IO_VDD_RING					
Y16	VSS_RING					
Y17	IO_VDD_RING					
Y18	VSS_RING					
Y19	IO_VDD_RING					
Y20	VSS_RING					

Table 3-1 LS1024A Pinout List (continued)

Location	Signal Symbol	Direction	Type	Tolerant	PU/PD	Strength
Y21	IO_VDD_RING					
Y22	OTP_VDD					
Y23	TM_EXT_RESET	O	LVCMOS	5 V	PD	8 mA
Y24	GPIO04	I/O	LVCMOS	5 V	PU	10 mA
Y25	GPIO05	I/O	LVCMOS	5 V	PU	10 mA
AA1	GEM2_TXD_2	O		3.3 V		17 mA
AA2	GEM2_TXD_1	O		3.3 V		17 mA
AA3	VSS_RING					
AA4	VSS_RING					
AA5	VSS_RING					
AA6	VSS_RING					
AA7	IO_VDD_RING					
AA8	VSS_RING					
AA9	IO_VDD_RING					
AA10	VSS_RING					
AA11	IO_VDD_RING					
AA12	VSS_RING					
AA13	IO_VDD_RING					
AA14	VSS_RING					
AA15	IO_VDD_RING					
AA16	VSS_RING					
AA17	IO_VDD_RING					
AA18	VSS_RING					
AA19	IO_VDD_RING					
AA20	VSS_RING					
AA21	IO_VDD_RING					
AA22	SPI_SS3_N	O	LVCMOS	3.3 V		8 mA
AA23	JTAG_TMS	I	LVCMOS	5 V	PU	
AA24	RESET_N	I	LVCMOS	3.3 V		
AA25	JTAG_TRST_N	I	LVCMOS	5 V	PU	
AB1	GEM2_TXD_0	O		3.3 V		17 mA
AB2	GEM2_REFCLK	O	LVCMOS	3.3 V		8 mA
AB3	GEM_MDC	O	LVCMOS	3.3 V		8 mA
AB4	VSS_RING					
AB5	EXP_NAND_RDY	I	LVCMOS	5 V	PU	
AB6	DOSC_DVDD					

Table 3-1 LS1024A Pinout List (continued)

Location	Signal Symbol	Direction	Type	Tolerant	PU/PD	Strength
AB7	EXP_DQ_3	I/O	LVCMOS	5 V		8 mA
AB8	EXP_DQ_7	I/O	LVCMOS	5 V		8 mA
AB9	EXP_DQ_11	I/O	LVCMOS	5 V		8 mA
AB10	EXP_CLK	O	LVCMOS	5 V		8 mA
AB11	EXP_RE_N	O	LVCMOS	5 V		8 mA
AB12	EXP_DM_0	O	LVCMOS	5 V		8 mA
AB13	EXP_A_0	O	LVCMOS	5 V		8 mA
AB14	EXP_A_4	O	LVCMOS	5 V		8 mA
AB15	EXP_A_8	O	LVCMOS	5 V		8 mA
AB16	EXP_A_15	O	LVCMOS	5 V		8 mA
AB17	EXP_A_19	O	LVCMOS	5 V		8 mA
AB18	EXP_A_23	O	LVCMOS	5 V		8 mA
AB19	GPIO09	I/O	LVCMOS	5 V	PU	10 mA
AB20	GPIO13	I/O	LVCMOS	5 V	PU	10 mA
AB21	I2C_SDA	I/O	LVCMOS	5 V	PU	8 mA
AB22	SPI_SS0_N	O	LVCMOS	3.3 V		8 mA
AB23	JTAG_TDO	O	LVCMOS	5 V		12 mA
AB24	JTAG_TCK	I	LVCMOS	5 V	PU	
AB25	JTAG_TDI	I	LVCMOS	5 V	PU	
AC1	GEM_MDIO	I/O	LVCMOS	3.3 V	PD	8 mA
AC2	DECT_RSTN	O	LVCMOS	3.3 V	PD	8 mA
AC3	GPIO03	I/O	LVCMOS	5 V	PU	10 mA
AC4	GPIO01	I/O	LVCMOS	5 V	PU	10 mA
AC5	EXP_NAND_CS	O	LVCMOS	5 V		8 mA
AC6	EXP_NAND_WE_N	O	LVCMOS	5 V		8 mA
AC7	EXP_DQ_4	I/O	LVCMOS	5 V		8 mA
AC8	EXP_DQ_8	I/O	LVCMOS	5 V		8 mA
AC9	EXP_DQ_12	I/O	LVCMOS	5 V		8 mA
AC10	EXP_DQ_15	I/O	LVCMOS	5 V		8 mA
AC11	EXP_WE_N	O	LVCMOS	5 V		8 mA
AC12	EXP_DM_1	O	LVCMOS	5 V		8 mA
AC13	EXP_A_1	O	LVCMOS	5 V		8 mA
AC14	EXP_A_5	O	LVCMOS	5 V		8 mA
AC15	EXP_A_9	O	LVCMOS	5 V		8 mA
AC16	EXP_A_14	O	LVCMOS	5 V		8 mA
AC17	EXP_A_18	O	LVCMOS	5 V		8 mA

Table 3-1 LS1024A Pinout List (continued)

Location	Signal Symbol	Direction	Type	Tolerant	PU/PD	Strength
AC18	EXP_A_22	O	LVCMOS	5 V		8 mA
AC19	GPIO08	I/O	LVCMOS	5 V	PU	10 mA
AC20	GPIO12	I/O	LVCMOS	5 V	PU	10 mA
AC21	I2C_SCL	O	LVCMOS	5 V	PU	8 mA
AC22	SPI_SCLK	O	LVCMOS	3.3 V		8 mA
AC23	TDM_CK	I/O	LVCMOS	3.3 V		12 mA
AC24	TDM_DX	O	LVCMOS	3.3 V		8 mA
AC25	TDM_DR	I	LVCMOS	3.3 V	PU	
AD1	VSS_RING					
AD2	DECT_BCLK	O	LVCMOS	3.3 V		8 mA
AD3	GPIO02	I/O	LVCMOS	5 V	PU	10 mA
AD4	DECT_XO	O	OSCL	3.3 V		
AD5	EXP_NAND_RE_N	O	LVCMOS	5 V		8 mA
AD6	EXP_DQ_1	I/O	LVCMOS	5 V		8 mA
AD7	EXP_DQ_5	I/O	LVCMOS	5 V		8 mA
AD8	EXP_DQ_9	I/O	LVCMOS	5 V		8 mA
AD9	EXP_DQ_13	I/O	LVCMOS	5 V		8 mA
AD10	EXP_CS1_N	O	LVCMOS	5 V		8 mA
AD11	EXP_CS2_N	O	LVCMOS	5 V		8 mA
AD12	EXP_RDY	I	LVCMOS	5 V	PU	
AD13	EXP_A_2	O	LVCMOS	5 V		8 mA
AD14	EXP_A_6	O	LVCMOS	5 V		8 mA
AD15	EXP_A_10	O	LVCMOS	5 V		8 mA
AD16	EXP_A_13	O	LVCMOS	5 V		8 mA
AD17	EXP_A_17	O	LVCMOS	5 V		8 mA
AD18	EXP_A_21	O	LVCMOS	5 V		8 mA
AD19	EXP_A_25	O	LVCMOS	5 V		8 mA
AD20	GPIO11	I/O	LVCMOS	5 V	PU	10 mA
AD21	UART1_TX	O	LVCMOS	5 V		8 mA
AD22	SPI_RXD	I	LVCMOS	3.3 V	PD	8 mA
AD23	SPI_SS2_N	O	LVCMOS	3.3 V		8 mA
AD24	TDM_FS	I/O	LVCMOS	3.3 V		8 mA
AD25	VSS_RING					
AE1	VSS_RING					
AE2	VSS_RING					
AE3	DECT_SCLK	O	LVCMOS	3.3 V		8 mA

Table 3-1 LS1024A Pinout List (continued)

Location	Signal Symbol	Direction	Type	Tolerant	PU/PD	Strength
AE4	DECT_XI	I	OSCL	3.3 V		
AE5	EXP_DQ_0	I/O	LVCMOS	5 V		8 mA
AE6	EXP_DQ_2	I/O	LVCMOS	5 V		8 mA
AE7	EXP_DQ_6	I/O	LVCMOS	5 V		8 mA
AE8	EXP_DQ_10	I/O	LVCMOS	5 V		8 mA
AE9	EXP_DQ_14	I/O	LVCMOS	5 V		8 mA
AE10	EXP_CS0_N	O	LVCMOS	5 V		8 mA
AE11	EXP_CS3_N	O	LVCMOS	5 V		8 mA
AE12	EXP_ALE	O	LVCMOS	5 V		8 mA
AE13	EXP_A_3	O	LVCMOS	5 V		8 mA
AE14	EXP_A_7	O	LVCMOS	5 V		8 mA
AE15	EXP_A_11	O	LVCMOS	5 V		8 mA
AE16	EXP_A_12	O	LVCMOS	5 V		8 mA
AE17	EXP_A_16	O	LVCMOS	5 V		8 mA
AE18	EXP_A_20	O	LVCMOS	5 V		8 mA
AE19	EXP_A_24	O	LVCMOS	5 V		8 mA
AE20	GPIO10	I/O	LVCMOS	5 V	PU	10 mA
AE21	UART1_RX	I	LVCMOS	5 V	PU	
AE22	SPI_TXD	O	LVCMOS	3.3 V		8 mA
AE23	SPI_SS1_N	O	LVCMOS	3.3 V		8 mA
AE24	VSS_RING					
AE25	VSS_RING					

Table 3-2 lists the LS1024A muxing options.

Table 3-2 Muxing Table

Signal Symbol	Muxing Options			
	Option 1	Option 2	Option 3	Option 4
gem0_rxd0	RGMII0_RXD0	RMII0_RXD0		
gem0_rxd1	RGMII0_RXD1	RMII0_RXD1		
gem0_rxd2	RGMII0_RXD2	RMII0_ RX_ER		
gem0_rxd3	RGMII0_RXD3			
gem0_rx_ctl	RGMII0_ RX_CTL	RMII0_CRS_DV		
gem0_rxc	RGMII0_RXC	RMII0_CLK		
gem0_txd0	RGMII0_TXD0	RMII0_TXD0		
gem0_txd1	RGMII0_TXD1	RMII0_TXD1		

Table 3-2 Muxing Table (continued)

Signal Symbol	Muxing Options			
	Option 1	Option 2	Option 3	Option 4
gem0_txd2	RGMII0_TXD2			
gem0_txd3	RGMII0_TXD3			
gem0_tx_ctl	RGMII0_ TX_CTL	RMII0_TX_EN		
gem0_txc	RGMII0_TXC			
gem1_rxd0	RGMII1_RXD0	RMII1_RXD0		
gem1_rxd1	RGMII1_RXD1	RMII1_RXD1		
gem1_rxd2	RGMII1_RXD2	RMII1_ RX_ER		
gem1_rxd3	RGMII1_RXD3			
gem1_rx_ctl	RGMII1_ RX_CTL	RMII1_CRS_DV		
gem1_rxc	RGMII1_RXC	RMII1_CLK		
gem1_txd0	RGMII1_TXD0	RMII1_TXD0		
gem1_txd1	RGMII1_TXD1	RMII1_TXD1		
gem1_txd2	RGMII1_TXD2			
gem1_txd3	RGMII1_TXD3			
gem1_tx_ctl	RGMII1_ TX_CTL	RMII1_TX_EN		
gem1_txc	RGMII1_TXC			
gem2_rxd0	RGMII2_RXD0	RMII2_RXD0	dect_sdata_in	
gem2_rxd1	RGMII2_RXD1	RMII2_RXD1	dect_sync_match	
gem2_rxd2	RGMII2_RXD2	RMII2_ RX_ER*	dect_sen	
gem2_rxd3	RGMII2_RXD3		dect_sdata_out	
gem2_rx_ctl	RGMII2_ RX_CTL	RMII2_CRS_DV	i2s_bclk	
gem2_rxc	RGMII2_RXC	RMII2_CLK	i2s_sdo	
gem2_txd0	RGMII2_TXD0	RMII2_TXD0	dect_slot_ctrl	
gem2_txd1	RGMII2_TXD1	RMII2_TXD1	dect_radio_en	
gem2_txd2	RGMII2_TXD2		i2s_codclko	
gem2_txd3	RGMII2_TXD3		i2s_codclki	
gem2_tx_ctl	RGMII2_ TX_CTL	RMII2_TX_EN	i2s_lrclk	
gem2_txc	RGMII2_TXC		i2s_sdi	
gem2_refclk	GEM2_REFCLK	GEM2_REFCLK	dect_tr_data	
gpio00	gpio00			
gpio01	gpio01			
gpio02	gpio02			
gpio03	gpio03			
gpio04	gpio04	tim_pwm0		
gpio05	gpio05	tim_pwm1		

Table 3-2 Muxing Table (continued)

Signal Symbol	Muxing Options			
	Option 1	Option 2	Option 3	Option 4
gpio06	gpio06	tim_pwm2	sata0_act_led	
gpio07	gpio07	tim_pwm3	sata0_cp_pod	
gpio08	gpio08		uart0_rx	
gpio09	gpio09		uart0_tx	
gpio10	gpio10		uart0_rts_n	
gpio11	gpio11		uart0_cts_n	
gpio12	gpio12	tim_pwm4		
gpio13	gpio13	tim_pwm5		
gpio14	gpio14	sata1_act_led	tim_evnt0	
gpio15	gpio15	sata1_cp_pod	tim_evnt1	
i2c_scl	i2c_scl	gpio16		
i2c_sda	i2c_sda	gpio17		
spi_ss0_n	spi_ss0_n	gpio18		
spi_ss1_n	spi_ss1_n	gpio19		
spi_2_ss1_n	spi_2_ss1_n	gpio20		
spi_ss2_n	spi_ss2_n	gpio21		
spi_ss3_n	spi_ss3_n	gpio22		
exp_cs2_n	exp_cs2_n	gpio23		
exp_cs3_n	exp_cs3_n	gpio24		
exp_ale	exp_ale	gpio25		
exp_rdy	exp_rdy	gpio26		
tm_ext_reset	tm_ext_reset	gpio27		
exp_nand_cs	exp_nand_cs	gpio28		
exp_nand_rdy	exp_nand_rdy	gpio29		
spi_txd	spi_txd	gpio30		
spi_sclk	spi_sclk	gpio31		
spi_rxd	spi_rxd	gpio32		
spi_2_rxd	spi_2_rxd	gpio33		
spi_2_ss0_n	spi_2_ss0_n	gpio34		
exp_dq[8]	exp_dq[8]	gpio35		
exp_dq[9]	exp_dq[9]	gpio36		
exp_dq[10]	exp_dq[10]	gpio37		
exp_dq[11]	exp_dq[11]	gpio38		
exp_dq[12]	exp_dq[12]	gpio39		
exp_dq[13]	exp_dq[13]	gpio40		

Table 3-2 Muxing Table (continued)

Signal Symbol	Muxing Options			
	Option 1	Option 2	Option 3	Option 4
exp_dq[14]	exp_dq[14]	gpio41		
exp_dq[15]	exp_dq[15]	gpio42		
exp_dm[1]	exp_dm[1]	gpio43		
coresight_d0	coresight_d0	gpio44		
coresight_d1	coresight_d1	gpio45		
coresight_d2	coresight_d2	gpio46		
coresight_d3	coresight_d3	gpio47		
coresight_d4	coresight_d4	gpio48		
coresight_d5	coresight_d5	gpio49		
coresight_d6	coresight_d6	gpio50		
coresight_d7	coresight_d7	gpio51		
coresight_d8	coresight_d8	gpio52		
coresight_d9	coresight_d9	gpio53		
coresight_d10	coresight_d10	gpio54		
coresight_d11	coresight_d11	gpio55		
coresight_d12	coresight_d12	gpio56		
coresight_d13	coresight_d13	gpio57		
coresight_d14	coresight_d14	gpio58		
coresight_d15	coresight_d15	gpio59		
uart1_rx	uart1_rx	uart_s2_rx		
uart1_tx	uart1_tx	uart_s2_tx		
tdm_ck	tdm_ck	zsi_zclk	gpio63	isi_psclk
tdm_fs	tdm_fs	zsi_fsync	gpio62	gpio62
tdm_dr	tdm_dr	zsi_zmiso	gpio61	isi_data_i
tdm_dx	tdm_dx	zsi_zmosi	gpio60	isi_data_o

3.2 Signal Summary

The LS1024A provides the following categories of signals:

- SerDes Signals
- Low Speed SPI Signals
- Timer Signals
- Expansion Bus Signals
  - Normal Mode Signals
  - ALE Mode Signals

3.2.1 SerDes Signals

SerDes supports a multitude of serial standards up to 5Gbps, including PCI-Express (PCIe) and Serial ATA (SATA) specifications, as well as SGMII. Three independent SerDes are used.

- SerDes #0: PCIe0
- SerDes #1: PCIe1 or SATA0 - selection through bootstrap
- SerDes #2: SATA1 or SGMII - selection through bootstrap

Table 3-3 lists the SerDes signals and their descriptions.

Table 3-3 SerDes Signals

Signal Name	Direction	Size	Description
S#_RXP, S#_RXM	I	2	High-Speed Differential Receive Pair
S#_TXP, S#_TXM	O	2	High-Speed Differential Transmit Pair
S#_RESREF	I/O	1	Reference Resistor Connection. Attach a 3K Ohm 1% accurate resistor-to-ground on the board.
S#_REFCLKP S#_REFCLKM	I	2	External SerDes reference clock input. A differential external clock may be provided by utilizing both pins. Note: Optional clock source For more details, refer to Section 7.3.2 “Reference Clocks” on page 74.

Table 3-3 SerDes Signals (continued)

Signal Name	Direction	Size	Description
S#_ATEST	O	1	Analog DC test pad. Leave unconnected.
S#_CK_100P S#_CK_100M	O	2	100 MHz reference clock. The reference clock outputs may be used as a differential pair clock signals. Note: Only valid for SERDES 0 and 1.
Note: The value of "#" for PCIe = "0" or "1" and the value of "#" for SATA = "1" or "2".			

3.2.2 Low Speed SPI Signals

Table 3-4 lists the LS-SPI signals and their descriptions.

Table 3-4 LS-SPI Signals

Signal Name	Direction	Size	Description
SPI_SCLK	O	1	Serial bit-rate Clock. Generated by SPI block from Fabric clock.
SPI_TXD	O	1	Transmit Data Signal. Output data from the serial master or serial slave is transmitted on this line.
SPI_RXD	I	1	Receive Data Signal. Input data from a serial master or serial slave device is received on this line.
SPI_SS#_N	O	4	Slave Select Output. Active Low. Hardware slave select signal. Four slave select output signals are provided. SS0 is used for boot device, when configured for LS SPI boot.

3.2.3 Timer Signals

Table 3-5 lists the Timer signals and their descriptions.

Table 3-5 Timer Signals

Signal Name	Direction	Size	Description
TIM_EVNT	I/O	2	External Timer event (muxed with GPIO14 and GPIO15.) These pins can be independently configured as output, to generate an external clock by the timer, or as input, to count external events (edges).
TIM_PWM	O	6	Pulse Width Modulation signals (muxed with GPIO12 and GPIO13.)

3.2.4 Expansion Bus Signals

Table 3-6 lists the expansion bus signals and their descriptions.

Table 3-6 Expansion Bus Signals

Signal Name	Direction	Size	Description
EXP_CLK	O	1	Expansion Clock to the peripheral devices — This clock is generated in the Expansion block by dividing down the AXI clock by any integer from 3 to 15.
EXP_CS[0:3]	O	4	Programmable active level signals used to enable or disable peripheral devices. Exp_CS0 is specifically used to select NOR Flash boot memory.
EXP_WE_N / EXP_RW_N	O	1	Write Enable Normal Mode: When asserted, indicates a write operation to peripheral. Strobe Mode: Read/Write Enable signal. Assertion level of this signal is configurable.
EXP_RE_N / EXP_STRB_N	O	1	Read Enable Normal Mode: When asserted, indicates a read operation from peripheral. Strobe Mode: Command Strobe signal. Assertion level of this signal is configurable.
EXP_NAND_RE_N	O	1	Read Enable dedicated for NAND flash When asserted low, indicates a read operation from flash device. Assertion level of this signal is configurable.
EXP_NAND_WE_N / EXP_CS4	O	1	Write Enable dedicated for NAND flash When asserted low, indicates a write operation to the flash device. When NAND flash is not used, this pin can be used as a chip-select and can be configured to support generic peripheral device. Assertion level of this signal is configurable.
EXP_DM	O	4	Data Byte Mask Input data byte to the peripheral device is masked when DM is sampled high during a write access. One DM pin per data byte.
EXP_RDY	I	1	Peripheral device ready/busy status When set low indicates that the current transaction is in progress. Set high when the device is ready for a new transaction. Detection edge of this signal is configurable (high->low) or (low->high). When detected, causes deassertion of the CS and RE/WE for the current transaction.
EXP_A	O	26	Expansion Address Bus Specifies one Memory location along with the DM[1:0] (Byte-Enable) when supported.
EXP_ALE	O	1	Address Latch Enable The ALE, active high output, controls address latching to the peripheral device when multiplexed address/data bus mode is used.
EXP_DQ	I/O	8/16	Data bus Is configured to support 8 or 16 active bits. LSBits bits are always active.
EXP_NAND_CS_N	O	1	NAND Chip Select Active low CS# enables and disables selection of the targeted NAND flash devices.
EXP_NAND_RDY	I	1	Ready/Busy NAND device status When high indicates that the device is ready for access. When low indicates no access is granted.

3.2.4.1 Normal Mode Signals

Table 3-7 shows the list of external pins that are valid when the Normal mode is set.

Table 3-7 Normal Mode Signals

Signal Name	Direction	Size	Description
EXP_CLK	O	1	Expansion clock to the peripheral devices This clock is generated in the Expansion block by dividing down the AXI clock by any integer from 3 to 15.
EXP_CSx	O	4	Chip Selects #0-3 are supported by default enables and disables selection of the targeted peripheral devices. Active level is configurable by software.
EXP_CS4 / EXP_NAND_WE_N	O	1	By default this signal provides a NAND Flash write enable function. Under software control, this signal is to be optionally configured to provide a fifth expansion bus chip select.
EXP_RE	O	1	Read Enable When asserted indicates a read operation from peripheral. Active level is configurable by software.
EXP_WE	O	1	Write Enable. When asserted, indicates a write operation to peripheral. Active level is configurable by software.
EXP_DM	O	2	Data Byte Mask Input data byte to the peripheral device is masked when EXP_DM is sampled high during a write access. One EXP_DM pin per data byte. The timing of these signal is configurable to mimic the timing of EXP_CS or EXP_WE. The EXP_DM signals may also be configured inactive.
EXP_RDY	I	1	Peripheral device ready/busy status When set low indicates that the current transaction is in progress. Set high when the device is ready for a new transaction. Detection edge of this signal is configurable (high->low) or (low->high). When Detected causes deassertion of the CS and RE/WE for the current transaction.
EXP_ADDR	O	26	Expansion Address Bus Specifies one Memory location along with the DM[1:0] when supported.
EXP_DATA	B	16	Data bus The data bus may be configured to access 8 and 16 bit peripherals.

3.2.4.2 ALE Mode Signals

Table 3-8 shows the list of signals that are valid when the synchronous mode is set.

Table 3-8 ALE Mode Signals

Signal Name	Direction	Size	Description
EXP_CLK	O	1	Expansion clock to the peripheral devices This clock is generated in the Expansion block by dividing down the AXI clock by any integer from 3 to 15.
EXP_CSx	O	4	Chip Selects #0-3 are supported by default. Enables and disables selection of the targeted peripheral devices. Active level is configurable by software.
EXP_CS4 / EXP_NAND_WE_N	O	1	By default this signal provides a NAND Flash write enable function. Under software control, this signal is to be optionally configured to provide a fifth expansion bus chip select.
EXP_RE	O	1	Read Enable When asserted indicates a read operation from peripheral. Active level is configurable by software.
EXP_WE	O	1	Write Enable When asserted, indicates a write operation to peripheral. Active level is configurable by software.
EXP_DM	O	2	Data Byte Mask Input data byte to the peripheral device is masked when EXP_DM is sampled high during a write access. One EXP_DM pin per data byte. The timing of these signal is configurable to mimic the timing of EXP_CS or EXP_WE. The EXP_DM signals may also be configured inactive.
EXP_RDY	I	1	Peripheral device ready/busy status When set low indicates that the current transaction is in progress. Set high when the device is ready for a new transaction. Detection edge of this signal is configurable (high->low) or (low->high). When detected causes deassertion of the CS and RE/WE for the current transaction.
EXP_DATA	B	16	Expansion multiplexed Address/Data Bus During the address phase, EXP_ALE pulse is used by the peripheral to latch the address. After address hold-time the data is valid on the bus. The data bus may be configured to access 8 and 16 bit peripherals.
EXP_ALE	O	1	Address latch enable pulse, used by the peripheral device to latch the valid address.
EXP_ADDR	O	26	Expansion Address Bus.

3.2.4.3 Strobe Mode Signals

Table 3-9 shows the list of signals that are valid when the Command Strobe mode is set.

Table 3-9 Command Strobe Mode Signals

Signal Name	Direction	Bus width	Description
EXP_CLK	O	1	Expansion clock to the peripheral devices This clock is generated in the Expansion block by dividing down the AXI clock by any integer from 3 to 15.
EXP_CSx	O	4	Chip Selects #0-3 are supported by default. Enables and disables selection of the targeted peripheral devices. Active level is configurable by software.
EXP_CS4 / EXP_NAND_WE_N	O	1	By default this signal provides a NAND Flash write enable function. Under software control, this signal is to be optionally configured to provide a fifth expansion bus chip select.
EXP_RE / EXP_STRB	O	1	Command Strobe By default, when set low, This signal is used by the peripheral for command strobing. Active level is configurable by software.
EXP_WE / EXP_RW	O	1	Read/Write Enable By default, when set high, indicates a read operation from peripheral. When asserted low, indicates a write transaction to the peripheral. Active level is configurable by software.
EXP_DM	O	2	Data Byte Mask Input data byte to the peripheral device is masked when EXP_DM is sampled high during a write access. One EXP_DM pin per data byte. The timing of these signal is configurable to mimic the timing of EXP_CS or EXP_WE. The EXP_DM signals may also be configured inactive.
EXP_RDY	I	1	Peripheral device ready/busy status When set low indicates that the current transaction is in progress. Set high when the device is ready for a new transaction. Detection edge of this signal is configurable (high->low) or (low->high). When Detected causes deassertion of the CS and RE/WE for the current transaction.
EXP_ADDR	O	26	Expansion Address Bus. Specifies one Memory location along with the DM[1:0] when supported.
EXP_DATA	B	16	Data bus The data bus may be configured to access 8 and 16 bit peripherals.

3.2.4.4 NAND Mode Signals

Table 3-10 the list of signals that are valid when the NAND mode is set.

Table 3-10 Nand Mode Signals

Signal Name	Direction	Size	Description
NAND_CS_N (GPIO28)	O	1	Chip Selects Enables and disables selection of the targeted NAND peripheral device. Driven by software.
NAND_RE_N	O	1	Read Enable dedicated for NAND flash, when asserted low, indicates a read operation from flash device. Assertion level of this signal is configurable.
NAND_WE_N	O	1	Write Enable dedicated for NAND flash, when asserted low, indicates a write operation to the flash device. When NAND is not used, this pin can be configured as a peripheral chip-select. Assertion level of this signal is configurable.

Table 3-10 Nand Mode Signals (continued)

Signal Name	Direction	Size	Description
NAND_RDY (GPIO29)	I	1	NAND operating condition Ready/Busy# When high indicates that the device is ready for access. When set low indicates no access is granted.
NAND_ALE	O	1	NAND Address Latch Enable The NAND_ALE output controls writing to the address register. When ALE is high, the address is loaded on the rising edge of WE#. NAND_ALE must remain high during the entire address sequence. EXP_A[9] is used as ALE.
NAND_CLE	O	1	NAND Command Latch Enable The CLE output controls writing to the command register. When CLE is high, the command is loaded on the rising edge of WE#. EXP_A[10] is used as CLE.
EXP_DATA	B	16	Expansion multiplexed Address/Data Bus During the address phase, NAND_ALE pulse is used by the peripheral to latch the address. After address hold-time, the data is valid on the bus. The data bus may be configured to access 8 and 16 bit NAND memory devices.

3.2.5 DDR3 Signals

Table 3-11 lists the DDR3 signals and their descriptions.

Table 3-11 DDR3 Signals

Signal Name	Direction	Size	Description
DDR_CLK, DDR_CLK_N	O	2x2	Differential clock outputs All address and control signals are sampled by the DDR on the crossing of the positive edge of CK and negative edge of CK#. Input data (DQ and DQS) is referenced to the crossings of CK and CK_N. There are two pairs of differential clocks.
DDR_CKE	O	1	Clock Enable active high When set low, memory DDR internal clock, input buffers and output drivers are de-activated. CKE must be maintained HIGH throughout read and write accesses.
DDR_CS_N	O	2	Chip Select Active low CS# enables and disables selection of the targeted memory module. One chip select for each DDR rank.
DDR_RAS_N	O	1	Memory Row address strobe Active low define the raw address for the required data.
DDR_CAS_N	O	1	Memory column address strobe Active low define the column address for the required data.
DDR_WE_N	O	1	Memory Write Enable When set low indicates a write operation to memory, otherwise indicates read.

Table 3-11 DDR3 Signals (continued)

Signal Name	Direction	Size	Description
DDR_DM	O	4	Data Byte Mask Input data byte to the memory is masked when DM is sampled high along with that input data during a write access. The DDR3 samples the DM signal on both edges of DS. One DM pin per data byte. When 16-bit data bus is used, only 2 DM LSbits need to be used.
DDR_DM_ECC	O	1	Data Byte Mask for ECC byte
DDR_BA	O	3	Bank Select Address Selects DDR bank for command access.
DDR_A	O	16	Address Bus Provides row and column addresses for RAS and CAS commands.
DDR_DATA	I/O	32	Data bus Bi-directional data bus with DDR memory. For low-cost low-performance applications, only 16 LSbits may be used.
DDR_ECC_DATA	I/O	8	Data bus for ECC byte
DDR_DQS, DDR_DQS_N	I/O	4x2	Differential Data Strobe Used to latch data read from the DDR memory for reads and used to by the memory to sample data writes. DS is edge-aligned with read data and centered with respect to the write data. One differential DS pair per data byte.
DDR_ECC_DQS, DDR_ECC_DQS_N	I/O	1x2	Differential Data Strobe for ECC byte
DDR_ODT	O	2	On-Die Termination
DDR_RESET_N	O	1	DDR Reset signal (active low)
DDR_GATE_O	O	1	GATE_O and GATE_I signals are used to clean strobe signal, i.e. DQS cleaning. Strobe signal of DDR has high-Z state because it's bi-directional and this high-z state should be cleaned to be used as a clock signal for memory read transaction. The GATE_O pin is connected to GATE_I pin. The length of the GATE_O/GATE_I trace should be 2x the average length of the DDR_CLK/DDR_CLK_N traces to each DDR memory.
DDR_GATE_I	I	1	
DDR_ZQ	O	1	External Resistor for calibration Resistor Value: 240 ohms 1%

3.2.6 GPIO Signals

See for Table 3-2 Muxing information.

3.2.7 I^2C Signals

Table 3-12 lists the I^2C signals and their descriptions.

Table 3-12 I^2C Signals

Signal Name	Direction	Size	Description
I2C_SCL	O	1	I^2C Output Clock Line
I2C_SDA	I/O	1	I^2C Input/Output Data Line

3.2.8 Fast UART Signals

Table 3-13 lists the UART signals and their descriptions.

Table 3-13 UART Signals

Signal Name	Direction	Size	Description
UART#_TX	O	1	Transmit data
UART#_RX	I	1	Receive data
UART#_RTS	O	1	Request To Send - Only used with port 0
UART#_CTS	I	1	Clear To Send - Only used with port 0

3.2.9 High Speed SPI Signals

Table 3-14 lists the HI-SPI signals and their descriptions.

Table 3-14 HI-SPI Signals

Signal Name	Direction	Size	Description
SPI_2_SCLK	O	1	Serial bit-rate Clock Generated by SPI block from Fabric clock.
SPI_2_TXD	O	1	Transmit Data Signal Output data from the serial master or serial slave is transmitted on this line.
SPI_2_RXD	I	1	Receive Data Signal Input data from a serial master or serial slave device is received on this line.
SPI_2_SS#_N	O	2	Slave Select Output Active Low. Hardware slave select signal. The width of the signal is equal to the number of slaves present on the serial bus. SS0 is used for boot device, when configured for HS SPI boot.

3.2.10 I^2S Signals

Table 3-15 lists the I^2S signals and their descriptions.

Table 3-15 I2S Signals

Signal Name	Direction	Size	Description
I2S_CODCLKI	I	1	Input Codec Reference clock
I2S_CODCLKO	O	1	Output Reference clock Divided down from Fabric clock.
I2S_BCLK	I/O	1	Serial Data Bus Bit Clock Master mode: generated out of Fabric or Input Codec reference clock Slave mode: received from external master.
I2S_LRCLK	I/O	1	Left/Right channel select clock Master mode: generated out of Fabric or Input Codec reference clock Slave mode: received from external master.
I2S_SDI	I	1	Serial Input Data
I2S_SDO	O	1	Serial Output Data

3.2.11 TDM Signals

Table 3-16 lists the TDM signals and their descriptions.

Table 3-16 TDM Signals

Signal Name	Direction	Description
TDM_CK	I/O	Data clock input from network, or from device if it is the source of the clock.
TDM_FS	I/O	Frame synchronization input from the network or from device.
TDM_DX	O	Data transmit output from the device.
TDM_DR	I	Data receive input from the network.

3.2.12 RMII Mode

Table 3-17 lists the RMII signals and their descriptions.

Table 3-17 RMII Signals

Signal Name	Direction	Size	Description
RMII_CLK	I	1	Reference Clock Input—Continuous 50 MHz reference clock.
RMII_REFCLK	O	1	Reference Clock Output—Output reference clock for external PHY/Switch.
RMII_TX_EN	O	1	Transmit Enable—When high, indicates that MAC is presenting di-bits. Asserted synchronously with first nibble of the preamble and remains asserted while all di-bits to be transmitted are present. Synchronous to REFCLK.
RMII_TXD[1:0]	O	2	Transmit Data—TXD1 is the most significant. Synchronous to REFCLK.

Table 3-17 RMII Signals (continued)

Signal Name	Direction	Size	Description
RMII_CRS_DV	I	1	Carrier Sense / Receive Data Valid—Asserted by the PHY when the medium is non-idle. Data on RXD is considered valid when CRS_DV is asserted. During a false carrier event, CRS_DV shall remain asserted for the duration of the carrier activity. Not synchronous to REFCLK.
RMII_RX_ER	I	1	Receive Error Detected—High for one or more REFCLK cycles to indicate that an error was detected somewhere in the frame presently being transferred. Synchronous to REFCLK.
RMII_RXD[1:0]	I	2	Receive data—RXD1 is the most significant. Synchronous to REFCLK.

3.2.13 RGMII Mode

Table 3-18 lists the RGMII signals and their descriptions.

3.2.14 GEM Interface

Table 3-18 lists the Management interface signal description.

Table 3-18 Management Interface Signals

Signal Name	Direction	Size	Description
GEM_MDC	O	1	Serial Management Interface Clock—3.3V signal.
GEM_MDIO	I/O	1	Serial Management Interface Data—Transfers data in and out of the device synchronously to MDC. 3.3V signal

3.2.15 CSS Signals

Table 3-19 lists the CSS signals and their descriptions.

Table 3-19 CSS Signals

Signal Name	Direction	Size	Description
DECT_XI, DECT_XO	I O	1	Reference Clock In (13.824MHz XTAL).
DECT_BCLK	O	1	Reference clock for external RF device.
DECT_RSTN	O	1	Reset signal for RF (Resets its SPI registers to their default values).
DECT_SCLK	O	1	Serial Clock. This pin provides the serial data clock function for the 3-line serial data bus. Data is clocked into the RFIC on negative edge transitions. The nominal serial clock rate is 13.824MHz.

Table 3-20 lists the CSS signals muxed with GEM2.

Table 3-20 CSS Muxed Signals

Signal Name	Direction	Size	Description
DECT_SDATA_OUT	O	1	Serial Data Out. It is part of the serial data stream for the 3-line serial data bus.
DECT_SDATA_IN	I	1	Serial Data In. It is part of the serial data stream for the 3-line serial data bus.
DECT_SEN	O	1	Serial Select Enable. This pin provides the Data Latch. Enable function for the 3-line serial data bus. Data is latched into the RFIC on a positive edge transition.
DECT_TR_DATA	I/O	1	It provides data output from the digital demodulator and modem or provides back the FSK modulation input to the modulator.
DECT_SLOT_CTRL	O	1	Slot Timing control LOW = slot disabled, HIGH =slot enabled.
DECT_RADIO_EN	O	1	Radio Enable. Rising edge triggers State Machine transition to Tune Mode. When logic Low is applied, the IC is in Sleep Mode.
DECT_SYNC_MATCH	O	1	Sync Match indication

3.2.16 JTAG Interface Signals

Table 3-21 lists the JTAG interface signals and their descriptions.

Table 3-21 JTAG Interface Signals

Signal Name	Direction	Size	Description
JTAG_TCK	I	1	Clock with internal pull-up
JTAG_TDI	I	1	Input data with internal pull-up
JTAG_TDO	O	1	Output data
JTAG_TMS	I	1	Mode select with internal pull-up
JTAG_TRST_N	I	1	Reset with internal pull-up

3.2.17 Silicon Labs Integrated Serial Interface (ISI) Signals

ISI is muxed with TDM. Table 3-22 lists the ISI signals and their descriptions.

Table 3-22 ISI Signals

Signal Name	Direction	Size	Description
ISI_PSCLK	O	1	18.432/18.528/24.576MHz system clock for ProSLIC ICs.
ISI_DATA_O	O	1	Data output to ProSLIC.
ISI_DATA_I	I	1	Data input from ProSLIC.

3.2.18 Test and Miscellaneous Signals

Table 3-23 lists the test and miscellaneous signals and their descriptions.

Table 3-23 Test and Miscellaneous Signals

Signal Name	Direction	Size	Description
RESET_N	I	1	Device input Reset (active low) RESET_N should remain asserted (low) at least for 10µs after all power supplies are established and the chosen reference clock is running.
TM_EXT_RESET	O	1	External reset pin, to reset other devices on the board. GPIO27 used by LS1024A SDK to reset external devices
PLL3_FILTER	I	1	Connect to a ±5% 1800pf capacitor tied to ground.
PS_XI, PS_XO	I O	1	Reference Clock In (24/48MHz +/- 50 ppm XTAL or CLK) for SerDes, USB PHYs and System PLLs
UP_XI, UP_XO	I O	1	Reserved Tie UP_XI to ground. UP_XO should be left opened
CORESIGHT_CLK	O	1	CA9 Trace Clock
CORESIGHT_D#	O	16	CA9 Trace Data out
TM_TESTMODE_N	I	3	Select JTAG and Test mode for scan, boundary scan, and so on. For testmode and JTAG muxing option see Section 24.3
TM_LEGACY_MODE_N	I	1	Must be pulled high
FSOURCE_ECID	I/O	1	For programming eFuse **on tester.** Tie to ground for normal operation.
Bootstrap	I	26	Muxed with EXP_A. For more details about Bootstrap, refer to "Internal Boot ROM" on page 181.

3.2.19 USB2.0 Interface Signals

Table 3-24 lists the USB2.0 interface signals and their descriptions.

Table 3-24 USB2.0 Interface Signals

Signal Name	Direction	Size	Description
USB0_DP	I/O	1	Positive channel that is connected to the serial USB cable. 3.3V analog signal
USB0_DM	I/O	1	Negative channel that is connected to the serial USB cable. 3.3V analog signal
USB0_VBUS	I	1	Used for monitoring the USB interface VBUS voltage and the detection of over-current conditions. When using voltage monitors within the USB2.0(3.0)PHY, this pin is connected to the +5V Vbus signal. A low on Vbus would indicate an over current condition to the LS1024A. If external over-current monitoring techniques provided by USB hubs or similar devices are used, this pin may be tied to 3.3V.
USB0_REXT	I/O	1	External resistor connection for current reference. Resistor Value: 44.2 ohms 1%
USB0_ATEST	I/O	1	Analog test pin

3.2.20 USB3.0 Interface Signals

Table 3-25 lists the USB3.0 interface signals and their descriptions.

Table 3-25 USB3.0 Interface Signals

Signal Name	Direction	Size	Description
USB1_DP, USB1_DM	I/O	2	Bi-directional differential pin carries USB2.0 data to and from the USB 3.0 PHY. In HS operation, this pin receives/transmits a maximum of 800 mV or 400 mV nominally. In FS or LS operation, this pin receives/transmits 3.3 V nominally.
USB1_RX_P, USB1_RX_M	I	2	High-Speed Differential Receive Pair
USB1_TX_P, USB1_TX_M	O	2	High-Speed Differential Transmit Pair
USB1_RESREF	I/O	1	Reference Resistor Connection Attach a 200 ohm 1% 100-ppm/C precision resistor-to-ground on the board.
USB1_REF_CLK_P, USB1_REF_CLK_M	I	2	Low-Swing Differential Input Clock Pair Note: Optional clock source
USB1_VBUS	I/O	1	Used for monitoring the USB interface VBUS voltage and the detection of over-current conditions. When using voltage monitors within the USB2.0(3.0)PHY, this pin is connected to the +5 V Vbus signal. A low on Vbus would indicate an over current condition to the LS1024A. If external over-current monitoring techniques provided by USB hubs or similar devices are used, this pin may be tied to 3.3 V.
USB1_ID	I/O	1	Reserved. Should be left open.

3.2.21 Microsemi ZSI Interface Signals

ZSI is muxed with TDM. Table 3-26 lists the ZSI signals and their descriptions.

Table 3-26 ZSI Signals

Signal Name	Direction	Size	Description
ZSI_ZCLK	O	1	Output clock to ZSI supported device (such as the Le88536) 1.024 KHz-8.192 MHz
ZSI_ZSYNC	O	1	Output interface synchronization signal to ZSI Device
ZSI_ZMOSI	O	1	Output voice and control data to ZSI Device
ZSI_ZMISO	I	1	Input voice and control data from ZSI Device.

3.3 Unused Interfaces

This section indicates how signals should be terminated in case an interface is not used.

- CRYSTAL/OSC Pads
  - If not used, tie _XI pin to ground and leave _XO open.
  - If input clock is selected, connect clock to _XI and leave _XO open.
- DDR Interface
  - Unused byte(s): Functional signals should be left unconnected.
  - DDR ECC: Unused ECC interface should be left unconnected

  - DDR PHY
    - Unused address/control signals should be left unconnected.
    - If DDR_CLK/DDR_CLK_N[1] is not used they should be left unconnected.
- EXP Interface: Unused signals can be left unconnected
  - EXP_CLK: If not used, it can be left unconnected. There is an option to power EXP_CLK down (software configuration in EXP block) and to tri-state it (software configuration using "Misc Control" register in GPIO block - offset 0x34 bit 13).
- CoreSight, I2C, SPI, UART, GPIO, JTAG: Unused interfaces/signals can be left unconnected.
- TM_EXT_RESET: It can be left unconnected.
- TDM
  - If the TDM interface is not used, all the signals can be left unconnected and the block should not be taken out of reset (software configuration).
- RTC Interface
  - OSC Pad: tie _XI pin to ground and leave _XO open.
  - RTC_VDD: If the Real Time Clock (RTC) interface is not used, tie RTC_VDD to 3.3 V. However, if the RTC interface is used, RTC_VDD should not be left unconnected. The board design should include logic to provide 3.3 V to the RTC_VDD pin in the event an RTC battery is missing or discharged.
- GEM
  - GEM#_REFCLK can be left unconnected. There is an option to tri-state each one of them (software configuration using "Misc Control" register in GPIO block - offset 0x34 bits 16:14).
  - GEM#: If the entire port is not used, all signals can be left open. Since GEMAC block cannot be kept in reset, either tie GEM#_RXC to ground or enable the pull-down in its IO pad (software configuration).
    - GEM0: Set bit 20 "Pad Config 3" register in GPIO (offset 0x10C) to 1.
    - GEM1: Set bit 20 "Pad Config 4" register in GPIO (offset 0x110) to 1.
    - GEM2: Set bit 20 "Pad Config 5" register in GPIO (offset 0x114) to 1.
  - GEM2 signals when operating in I^2S or CSS mode may be left unconnected. If I^2S or CSS is not used, the GEM2 block should be kept in reset (software configuration).
- SerDes
  - External clocks (S#_REFCLKP, S#_REFCLKM) can be floated when the SerDes's internal reference clock option is used.
  - If SerDes# is not being used, power up all supplies to their respective power rails. The SerDes should be kept in reset (software configuration). All unused IO pins can be left unconnected.
- USB2 PHY
  - If USB2.0 PHY is not used, power up all supplies to their respective power rails and set SUSPENDM input to 1'b0 (software configuration). All unused IO pins can be left unconnected.
- USB3 PHY
  - The external reference clock inputs are differential. If the reference clock requirements with a single end-end input clock are met, tie the unused reference to input low or high; do not leave it unconnected.
  - If the internal reference clock is used (by deasserting ref_use_pad), tie both the USB1_REF_CLK_P and USB1_REF_CLK_M clock pins to ground.
  - When the USB3.0 PHY is not used, power up all supplies to their respective power rails and assert the test_powerdown_ssp and test_powerdown_hsp signals to place the PHY in its lowest power state (software configuration). All unused IO pins can be left unconnected.

4 Expansion Bus Interface

This section describes the LS1024A Expansion Bus Interface.

4.1 Introduction

The LS1024A Expansion Bus (EXPBUS) provides address, data, and control lines for connection to system peripheral devices. The Expansion Bus provides chip selects for system peripheral devices such as Flash memory, Boot ROM, and I/O devices. Expansion Bus provides support for up to 5 peripheral devices: NAND flash and 4 general-purpose device interfaces. There are 26 address bits, each chip select allows for 64MB directly addressable 8-bit interface or 128MB directly addressable 16-bit interface. In ALE mode, the chip supports 256 addresses with 8-bit bus or 64K addresses with a 16 bit bus. The Expansion Bus is synchronous and can be driven with the AXI clock using a divide down multiple of 3 to 15.

4.2 Features

The expansion bus provides the following features:

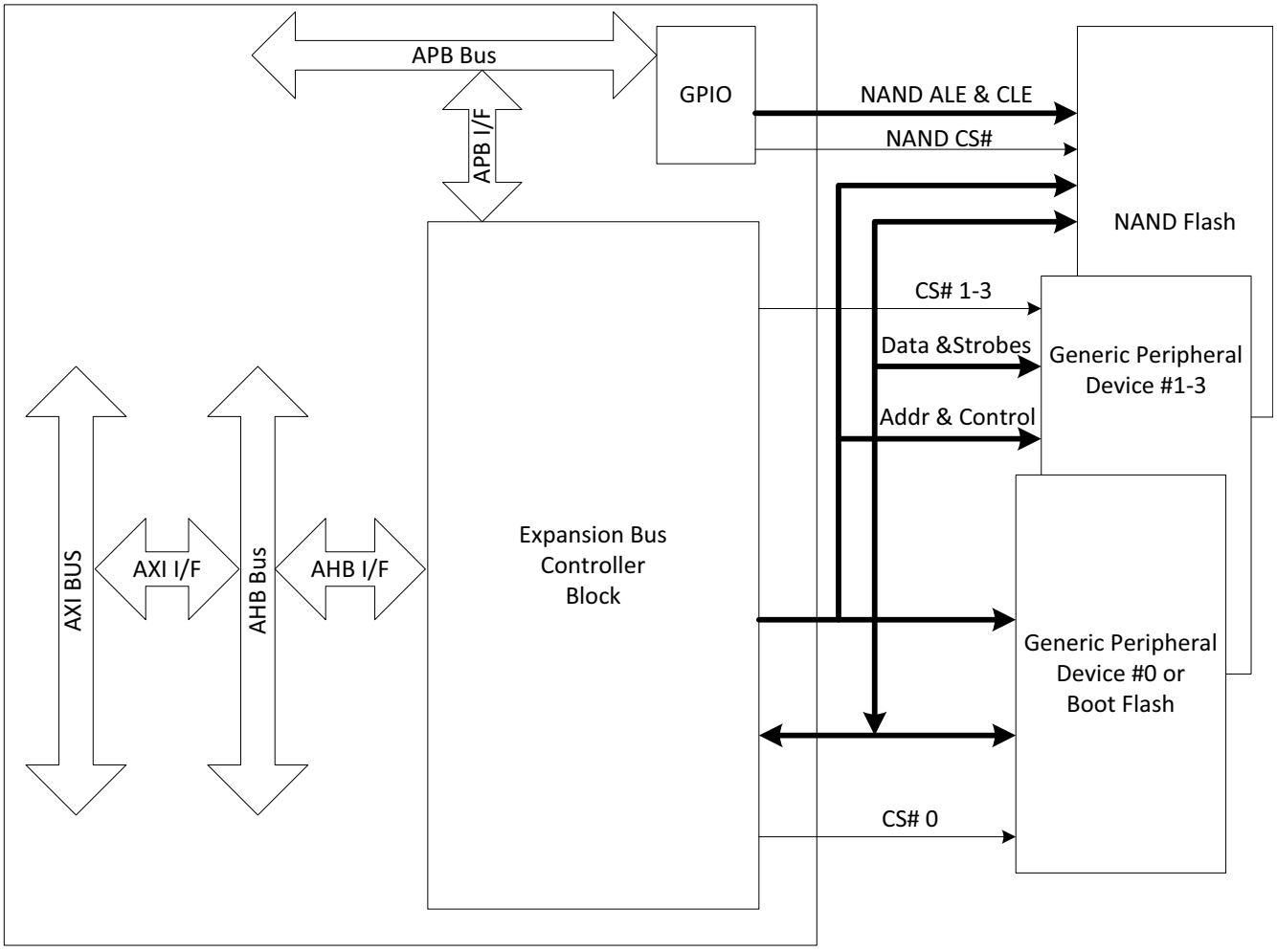
- General
  - Up to 256 MB internal AHB address space
  - 8/16-bit data bus
  - 4 Chip Select (5 if NAND is not used)
  - Each Chip-Select is allocated two configurations registers to define its address space delineation
  - Provides support for Normal (for example, NOR), ALE (multiplexed address-data mode with address latch enable), Strobe and NAND interface timing.
  - Synchronous interface. The AXI clock can be divided by 3 to 15. The divide integer is configurable by software.
  - 26 address bits are available for 64MB directly addressable 8-bit interface or 128MB directly addressable 16-bit interface. ALE mode supports 256 addresses with 8-bit bus or 64K addresses with 16 bit bus.
  - Programmable chip select level, configurable per chip select
  - Support for byte-mask writes, up to 2 bytes on the expansion interface
  - Provides support for Ready/Busy# acknowledge signal for terminating transactions. Detecting the deassertion of Read/Busy# signal overrides the Chip-Select and Write Enable/ Read Enable to conclude current transaction. Detection of Ready signal on rising/falling edge is configurable.
  - External expansion clock is provided and may be powered down or tri-stated by software when not used. All programmable timing parameters are synchronous to the expansion clock.
- NOR
  - 26-bit address bus parallel NOR support
  - Chip-select 0 is dedicated for expansion bus boot
- NAND
  - Supports SLC and MLC NANDs
  - Supports hardware acceleration of multi-bit ECC, as required for MLC NAND
  - Dedicated read/write controls are provided for NAND flash

- ECC main features:
  - BCH IP encodes data into a 16383-bit codeword (214 Galois Field)
  - 2-32 bit error correction
  - 2-1800 data bytes per block
  - Pass through flow (i.e. no data FIFO)
  - Hamming
- Wear leveling and Bad block management supported in standard SDK

4.3 Block Overview

For a view of the Expansion Bus block within the top-level block diagram, see Figure 4-1.

Figure 4-1 Expansion Block Overview



4.4 Block Functional Description

The Expansion Interface controls data flow to/from up to 4 generic devices and 1 dedicated NAND Flash device. When NAND Flash is not used, a fifth generic device may be used. CS0, which is part of the generic interface, can be configured to be used for the external boot flash, occupying address space zero of the expansion memory map; two pins determine the external boot flash bus size.

When the Expansion block is accessed by the system, the expansion controller fetches/stores data from/to peripheral devices until de-selected. Depending on the device type accessed, the required timing parameters are configured to comply with the specific device timing-requirements. The transactions are not initiated until the RDY pulse sampling (when supported) is synchronized with AXI clock (HClk) before casing the deassertion of the CS and the RE or WE control signals. The read data is latched upon deassertion of the CS or RE signal, whichever comes first. A configuration bit per chip-select is provided to enable/disable detection of the RDY signal and should be disabled for devices which don't provide the RDY signals. If the RDY signal, when enabled, is not detected, an error response is generated on the AHB interface.

As for NAND Flash, when accessed (an AHB access to its space), ALE is controlled through EXP address bit 9 and CLE through EXP address bit 10 as well as the device chip-select through pin GPIO28. The expansion controller provides the flash address/data/command and drives the NAND_WE#\NAND_RE# signals. Each NAND flash access phase is considered a full expansion bus access cycle.

Some peripherals may require the support of a single signal to be used for Read/Write indication, along with the command-strobing signal. A special configuration bit, STRB_MODE, is used to select the type of command signals: separate command signals: 1 for read and 1 for write, or 1 signal to be used for read/write indications and a separate signal to be used as the strobe. The active level of these 2 signals is configurable.

Accesses to the expansion block are decoded internally to assert the appropriate chip-select of the targeted device. 32-bit AHB input data is latched in case of write operations. Depending on the peripheral bus size used, the latched data is transferred over a decoded number of expansion cycles. The maximum number of expansion cycles to write 32-bit data over an 8-bit bus peripheral are 4, meanwhile, the AHB bus is halted until all data bytes are transferred. In case of read operations, the input data from the peripheral device is latched and formatted over a 32-bit AHB bus according to the peripheral bus size selected. The read data is duplicated over the 32-bit AHB data bus, that is, if MEM_SIZE is set to 8, the read byte is latched over all bytes of AHB data bus.

4.4.1 AHB Address Decoding

Depending on the memory size and the access size, the expansion address bus is decoded from the internal AHB address bus. The lowest bit of the AHB bus is dropped when a half word access is performed, and the lowest two bits are dropped when a word access is performed. Hence, word accesses are always aligned to word boundaries in memory. Depending on the memory size, the interface completes the Expansion bus address with the Expansion cycle count bits, and decodes the DM signals according to Table 4-1.

Table 4-1 Address Decoding

Expansion Bus Size	AHB Access Size	AHB Address Used Bits	Exp. Cycle Count Bits	Write Data Mask Decoded Bits
Byte	Byte	haddr [25:0]	-	-
	Half	haddr [25:1]	Cycle_cnt [0]	-
	Word	haddr [25:2]	Cycle_cnt [1:0]	-

Table 4-1 Address Decoding (continued)

Expansion Bus Size	AHB Access Size	AHB Address Used Bits	Exp. Cycle Count Bits	Write Data Mask Decoded Bits
Half	Byte	haddr [26:1]	-	haddr [0]
	Half	haddr [26:1]	-	-
	Word	haddr [26:2]	Cycle_cnt [0]	-

Expansion 26-bit generated address to the peripheral = {AHB Address Used Bits, Exp. Cycle Count Bits};
Expansion cycle counter increments on every complete expansion peripheral access cycle.

NOTE: AHB accesses outside the expansion chip-selects allocated memory segments cause an AHB Error response. Each chip select address map is configurable. CS0 boundary address map is defined by the CS0 memory base address register and the CS0 memory segment address register.

4.4.2 Modes of Operation

The expansion bus is highly configurable per chip select to accommodate the most common types of memory/flash in the industry. Four modes of operation can be configured to support the targeted peripheral timings. Note that EXP_CS4 is muxed with EXP_NAND_WE_N. Chip-select 4 address space is used by the NAND chip-select (GPIO pin) when NAND_MODE is enabled (default). Setting NAND_MODE to 0 and CS4_EN to 1 disables NAND support, and CS4 pin is used to access generic peripherals.

These modes support both, synchronous and asynchronous devices. By default, synchronous support is set and the output expansion clock is provided by setting EXP_CLK_EN global bit to 1 (high). When an asynchronous device is accessed, the EXP_CLK_EN global bit should be set to 0 (low) which suppresses expansion clock output.

4.4.2.1 Normal Mode

This mode is supported by all chip selects, and is set by programming the following configuration bits:

- ALE_MODE = 0
- STRB_MODE = 0
- NAND_MODE = 0 (CS4 is used as the 5th chip-select)

Normal Mode is the default mode for all chip selects except for the 5th chip-select which requires NAND_MODE to be set to 0. Figure 4-3 shows the Normal Mode relative signals and their programmable fields. CS and the RE or WE command are asserted, depending on the access type, after a programmed number of expansion clock cycles from the active address. Note that the expansion clock is a divide down frequency from the AXI clock, it is generated from dividing down hclk by one of the configured divide integers (3, 4, 5,...,15).

In the read cycle, the data bus is tri-stated and data is expected to be ready sometime after the assertion of the RE command. The expansion controller latches the data upon deassertion of either the RE command or the CS signal, whichever comes first. The CS is terminated after the expiration of the CS width count or upon detection of the deassertion of the RDY signal provided by the device (when enabled by setting EXP_RDY_EN to 1).

During the Write cycle, CS and WE command are asserted some programmable cycles after the valid address. The external device is expected to latch the data by the deassertion of the WE command. The data is held valid for some programmable cycles after the deassertion of the CS.

Next Read/Write transaction can only be started after the expiration of the Data-hold time count.

When EXP_RDY_EN bit is set high, detected RDY pulse is synchronized with AXI clock (HClk) before causing the deassertion of the CS and the RE or WE control signals. As mentioned above, the read data is latched upon deassertion of the CS or RE signal, whichever comes first. A configuration bit per chip-select is provided to enable/disable detection of the RDY signal and should be disabled for devices that don't provide RDY signals. If RDY is enabled and was not detected by the expansion controller before the deassertion of the CS, an error response is indicated on the AHB interface for this transaction.

NOTE: For more details about Normal mode signals, refer to "Normal Mode Signals" on page 31.

Figure 4-2 Normal Mode Timing Diagram (RDY_EN = 0)

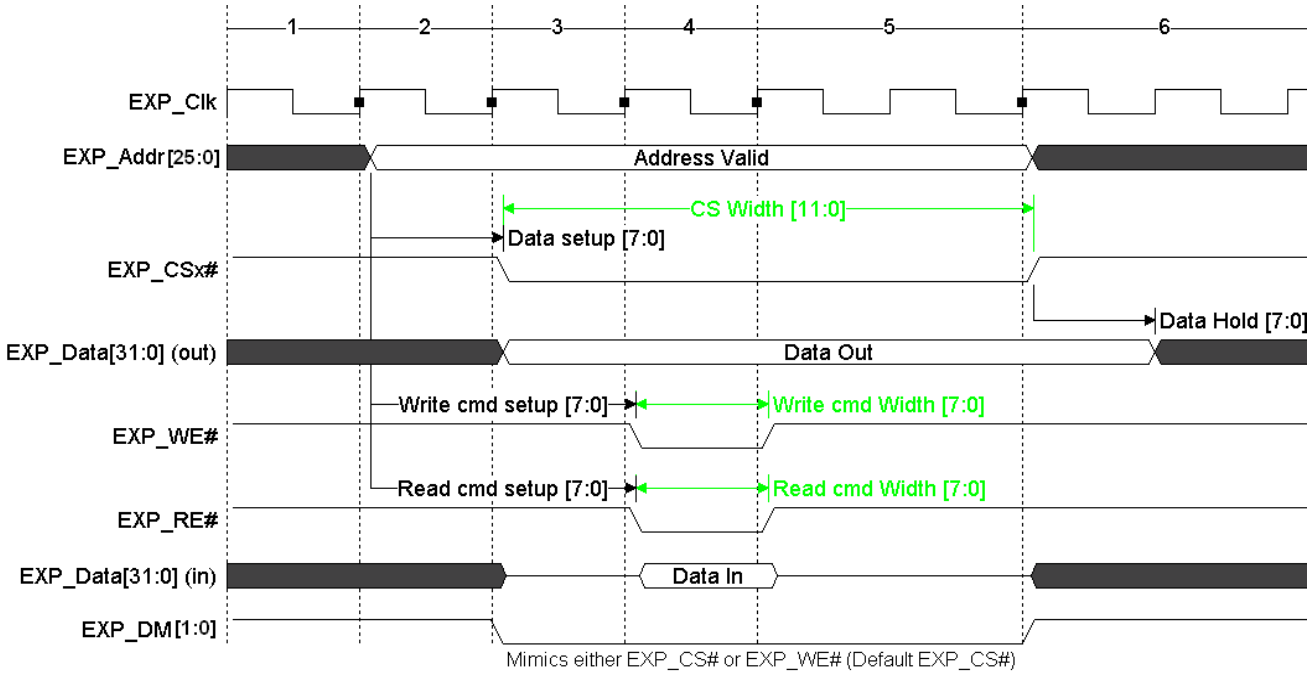
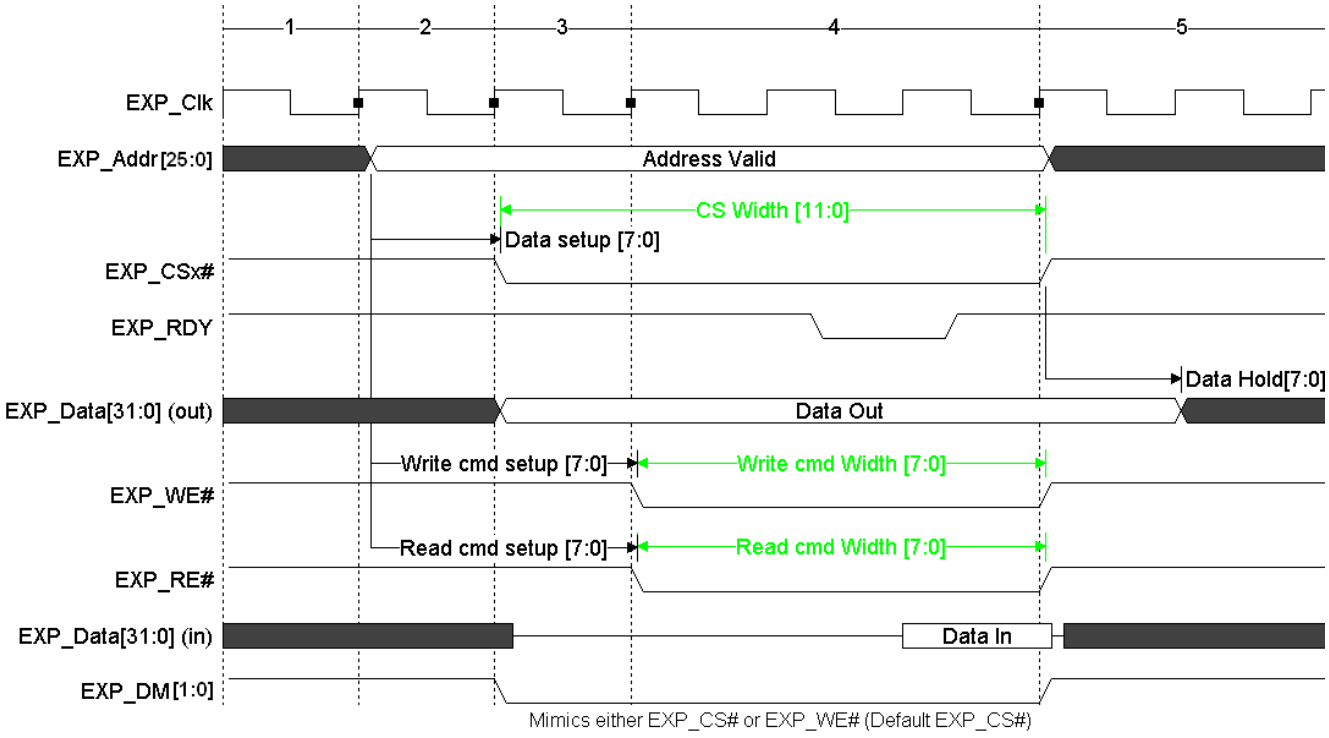


Figure 4-3 Normal Mode Timing Diagram (RDY_EN = 1)



In the above timing diagram, when a read access is performed, only RE signal is toggled and when a write command is performed, only WE command is toggled, not both.

NOTE: Depending on the synchronization timing of the assertion of the EXP_RDY signal, it is possible that the termination of CS/RE/WE occurs at the same cycle in which EXP_RDY was asserted.

4.4.2.2 ALE Mode

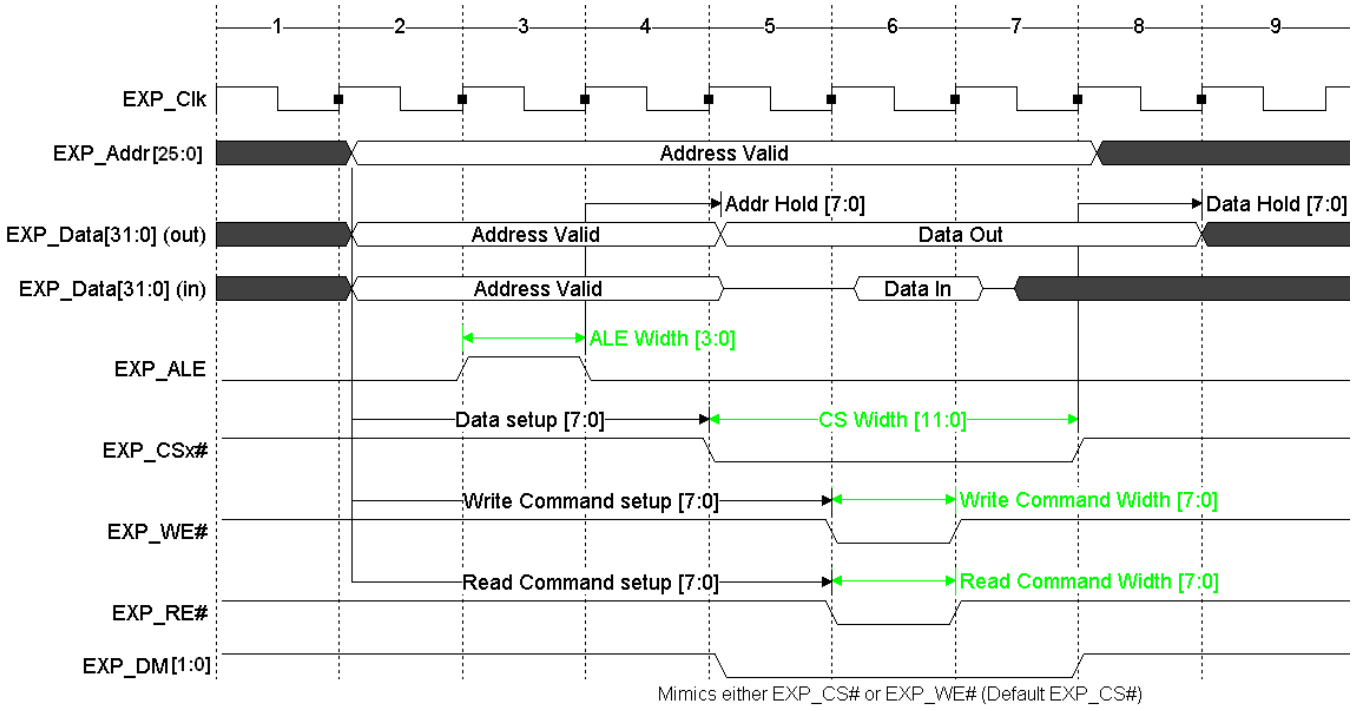
This mode is supported by all chip selects, and is set by programming the following configuration bits:

- ALE_MODE = 1
- STRB_MODE = 0
- NAND_MODE = 0 (CS4 is used)

ALE Mode is supported by chip selects 0-3 by setting ALE_MODE bit to 1. Also, chip select 4 supports this mode when ALE_MODE is set to 1 and NAND_MODE is set to 0. In this mode, the data bus is used to transfer both the valid address and valid data, Active high EXP_ALE is used by the peripheral device to latch the valid address. The valid address should be stable for the configured address hold time before placing valid data on the bus in case of writes. Read data is latched by the Expansion controller upon deassertion of the EXP_RE signal or EXP_CS, whichever comes first. Valid address is also driven on the address bus to provide support for devices that may require it.

NOTE: For more details about ALE mode signals, refer to "ALE Mode Signals" on page 31.

Figure 4-4 ALE Mode Timing Diagram



4.4.2.3 Strobe Mode

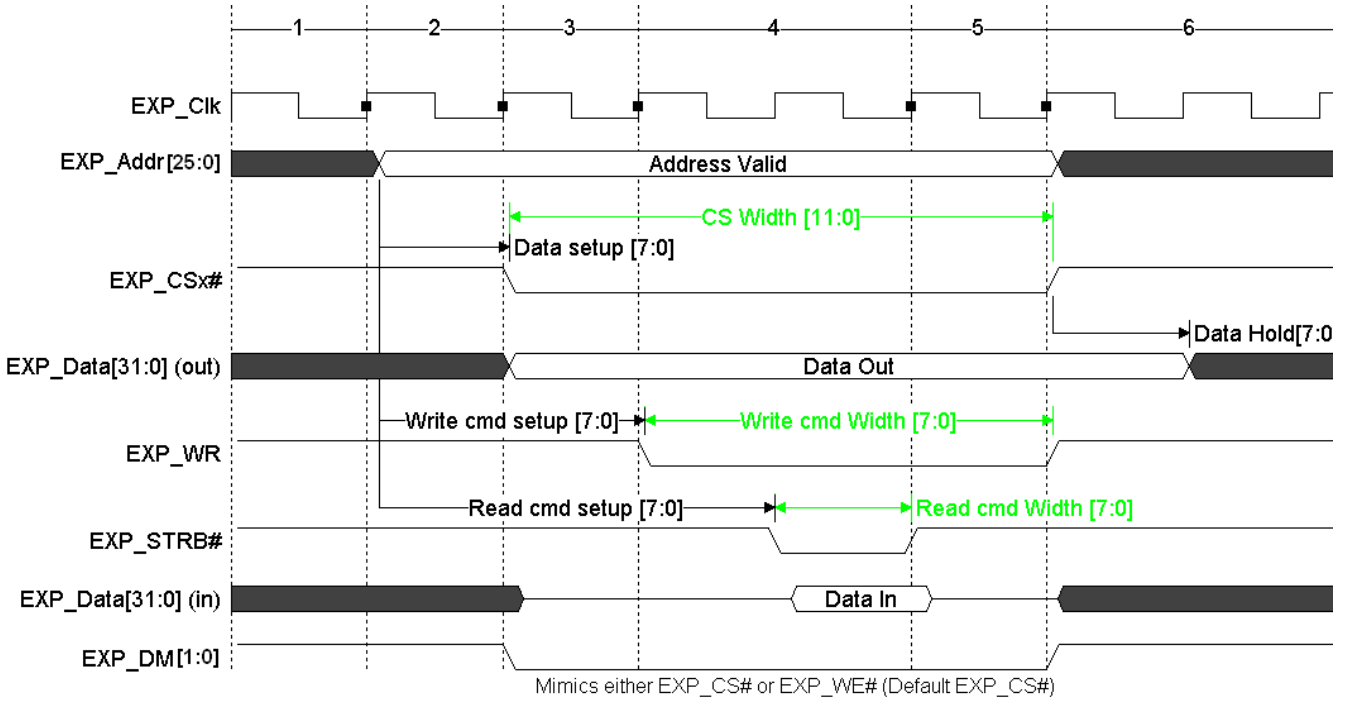
This mode is supported by all chip selects and is set by programming the following configuration bits:

- ALE_MODE = 0
- STRB_MODE = 1
- NAND_MODE = 0 (uses CS4)

This mode is supported by chip selects 0-3 by setting STRB_MODE bit to 1. Also, chip select 4 supports this mode when STRB_MODE is set to 1 and NAND_MODE is set to 0. In this mode, EXP_WE# pin is used by the peripheral device as EXP_RW# command signal. Also, EXP_RE# pin is used by the peripheral as the EXP_STRB command strobe signal. The active level of these 2 signals is configurable, depending on the polarity supported by the peripheral device.

NOTE: For more details about Strobe mode signals, refer to "Strobe Mode Signals" on page 32.

Figure 4-5 Strobe Mode Timing Diagram



NOTE: In this mode, both EXP_RW# and EXP_STRB# signals shall be switching within read and write transactions. The read data is sampled by the expansion block upon deassertion of the EXP_CS or EXP_STRB, whichever comes first.

4.4.2.4 NAND Mode

This mode is relevant for CS4 only, chip select #4 is used as the NAND write enable signal (Exp_nand_we_n).It is not supported by the chip selects #0-3. This mode is set by programming the following configuration bits (set by default):

- ALE_MODE = 0
- STRB_MODE = 0
- NAND_MODE = 1 (disables CS4)

The chip select and latch controls for this mode are provided by a dedicated pin (GPIO28). NAND_RE/NAND_WE commands, address and data are initiated by the expansion block as an expansion cycle. Each NAND transaction should be broken up into several expansion (Normal Mode type) transactions. The software has the ultimate control over NAND transactions.

Figure 4-6 NAND Command Latch Timing Diagram

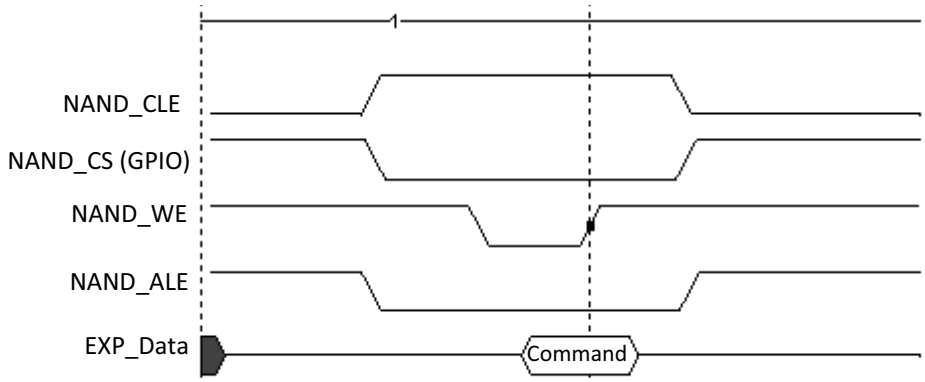


Figure 4-7 NAND Address Latch Timing Diagram

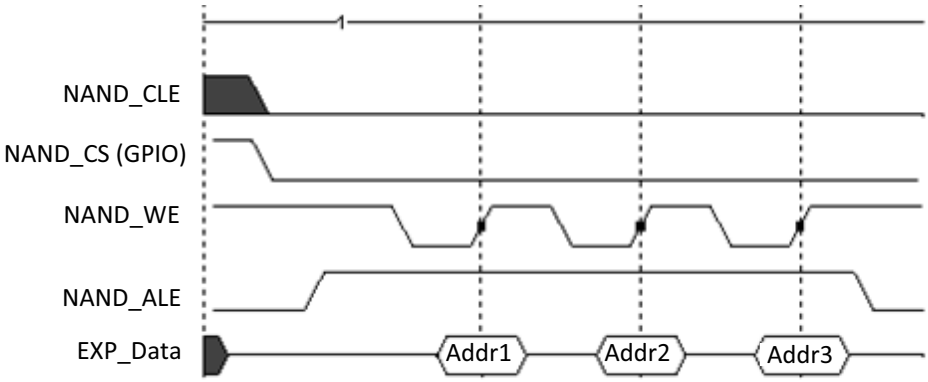
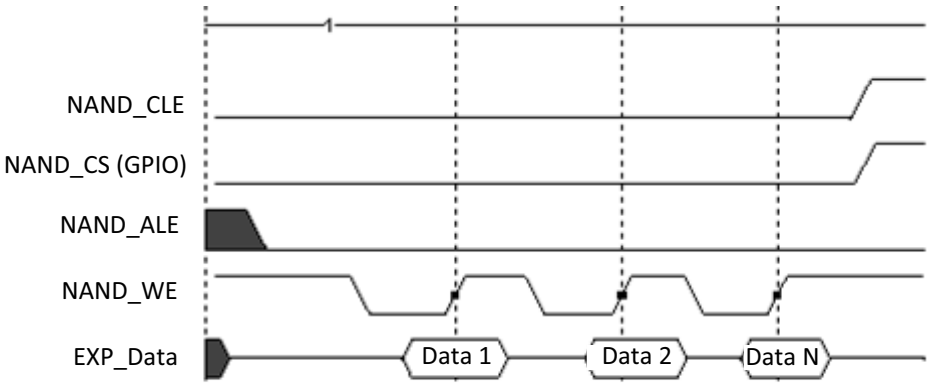


Figure 4-8 NAND Data Latch Timing Diagram



Each toggle of WE or RE to access the NAND flash is executed over a full expansion cycle. From the point of view of the expansion bus, it is an expansion cycle in normal mode. The software initiates a transaction in the NAND allocated address space, which starts an expansion cycle. During the NAND Address cycle or the NAND Command cycle, the software initiates the write transaction to the NAND address space placing the NAND address or command type value on the data bus. The expansion controller issues a write access to the NAND flash, as if it accesses a generic device.

NOTE: NAND_RE and NAND_WE are toggled when there is an access to CS#0-3.

NOTE: For more details about NAND mode signals, refer to "NAND Mode Signals" on page 33.

4.4.3 Booting from Parallel NOR

Chip-select 0 is dedicated for external boot when used. By default, EXP_CS0 is enabled and configured to operate in the Normal Mode. The External flash bus width is determined by the 2 input pins to the expansion block. Mode fields are configured as the following:

- ALE_MODE = 0
- STRB_MODE = 0

4.4.4 ECC Functional Description

4.4.4.1 Write Direction

When writing a data block to NAND flash, parity bytes are generated by the IP. These bytes are then written to the NAND by the software. An enable bit is provided, so SW can do writes which are not included in parity calculations.

When data is written to NAND, the same data is also shifted into the parity module for parity calculation. Once the whole data block is written, the parity module asserts the 'IDLE' indication after the parity calculation is complete. Parity data is then shifted out of the parity module to be written to NAND. The SW performs regular writes to the NAND, but instead of taking the data from the AHB it is taken from the parity module. When writing the parity bytes, SW has the option to either do 8/16-bits transaction (depends on the bus width mode) or to do 32 and 64 bits transaction, when HW translates it to 8/16-bits transactions.

Figure 4-9 shows the write data logic. The following logic is done on 'HWdata' and 'HWdata_new' replaces 'HWdata' in the figure.

Figure 4-9 Write Data Path

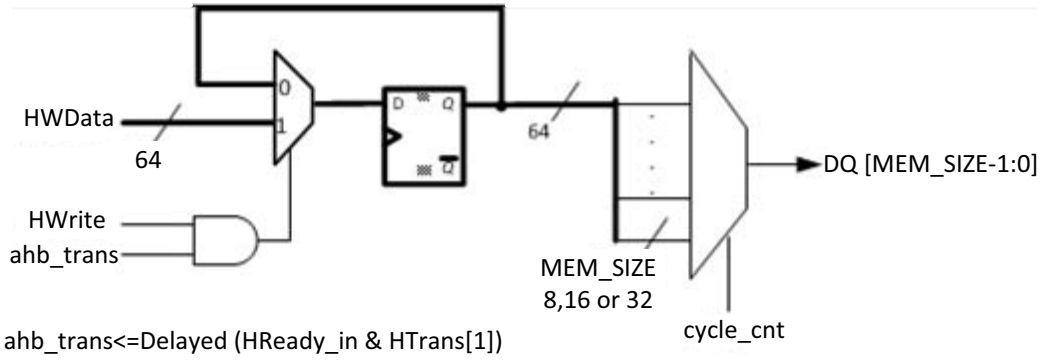
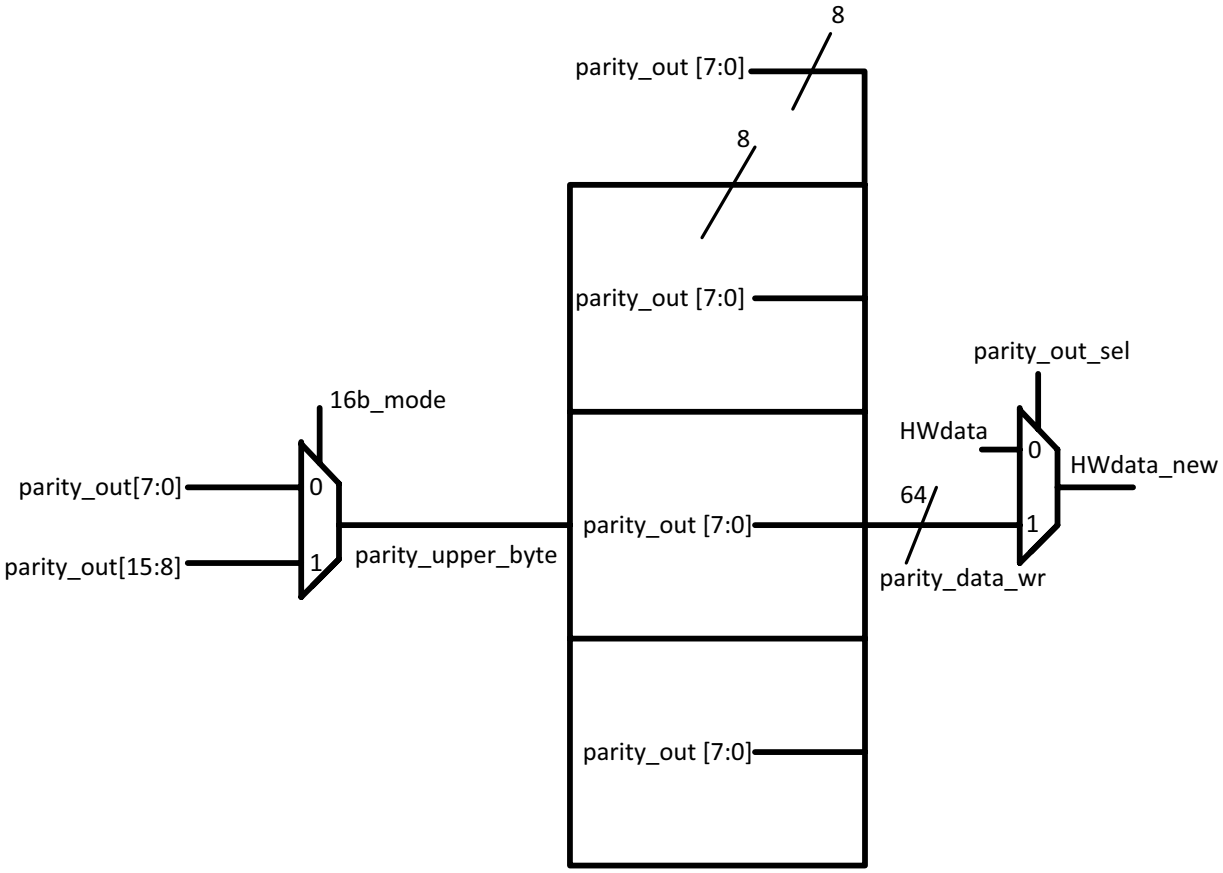


Figure 4-10 shows how the parity output data is integrated into the write data path.

Figure 4-10 Parity Write Data Logic



4.4.4.1.1 BCH Mode

In BCH mode, the number of parity [bytes/half words] generated depends on the ECC level and is defined as: ecc_level*14/[8 or 16].

The equation ecc_level*14 is divided by 16 or 8 depending if the interface is 16 or 8 bits respectively.

The software needs to know how many writes to do according to the configured ECC level and configured interface width. For example, 16 bit interface, ECC8 => 14 bytes of parity, 7 half words. The processor can do one 64-bit write transaction, then one 32 bit write transaction and last, one 16-bit transaction.

4.4.4.1.2 Hamming Mode

In Hamming mode, the number of parity bytes is always 4, therefore, the SW needs to do 32-bit transaction in order to write the parity bytes out to the NAND.

4.4.4.1.3 General Flow

The following steps should be done for every write (registers' name is in capital letters, fields are in regular letters):

1. Set 'prty_mode' field in 'GEN_CFG' register to '1' to set parity module to operate in parity generation mode.
2. Configure 'CS_SEL_CFG' register, 'hamm_mode', 'ecc_lvl', and 'blk_size' fields in 'GEN_CFG' registers to desired values.

3. Configure 'INIT_CFG' register to '1'. The register is a self clear register after cycle 1. This resets the parity module and latch configured values.
4. Configure 'SHIFT_EN' register to '1' to enable shifting of data into the parity module. This should be done only before the data block is written to NAND and not in command or address transactions.
5. Write data block to NAND. Each write triggers a shift into the parity module.
6. Once data writing is done, poll 'IDLE_STAT' register until it's asserted. Indicates that the parity module is done with the parity calculation and parity can be written. At this time the 1st parity is valid on the 'parity_out' lines.
7. If any transaction other than parity writing to NAND is needed, then, configure 'SHIFT_EN' register to '0'. This step can be done in parallel to step 6.
8. Configure 'PRTY_OUT_SEL_CFG' register to '1', to select the 'parity_out' bus from the parity module instead of AHB write data bus. This step can be done in parallel to step 6.
9. Configure 'SHIFT_EN' register to '1' to enable parity shift out at the end of every write to the NAND.
10. Configure 'SHIFT_EN' register to '0'.
11. Repeat steps 2 to 10 as needed.

NOTE: If the software wants to change the ECC level between writes, it needs to keep track on which ECC level was used for each data block, since the same ECC level needs to be configured when reading the data block from the NAND.

4.4.4.2 Read Direction

In the read direction, both parity and ECC modules participate. The parity module generates the syndromes while the ECC indicates the error bits and their location, if there are any errors.

4.4.4.2.1 BCH Mode

When data is read from the NAND, the same data is also shifted into the parity module for syndrome calculation. Once the whole data block is read, the software also reads the parity bytes that were calculated in the write process. These bytes need to be shifted into the parity module also. Once done, the parity module asserts the 'IDLE' indication. At this point the parity module indicates if errors are found using the 'ecc_correction_required' and 'erased_page' outputs. Only in the case when 'ecc_correction_required' is set and 'erased_page' is not set, an error occurs.

In case of an error, the software initiates writing the generated syndromes into the ECC block. The ECC level and block size remains as configured. The software has an option to add a tag number to that ECC block by configuring the 'poly_tag' register. The ECC module pops the syndromes from the parity module and calculates the error locations. Once the ECC is done, it asserts the 'cs_done' signal for 1 cycle. This signal is latched into a status register. Indications of how many errors are found (including parity errors) and if the block can not be corrected (in case more errors were found than the ECC level number), are latched into status register for the software to read.

While the ECC block is working to allocate the errors, the software needs to read the 'Correction Data Status' register in order to get the location information. Since the internal FIFO has place for 16 data and depending on the ECC level, the read needs to be done in parallel to the ECC module operation to clear the internal FIFO.

The first valid data on the correction interface is prefetched into the 'Correction Data Status', each read of the 'Correction Data Status' fetches a new status, if available. The software has a valid indication in the 'Correction Data Status' register to indicate if the register holds valid data or not. The software needs to read the 'Correction Data Status' register until it gets a 0x7FE value in the 'index' field.

4.4.4.2.2 Hamming Mode

The operations in this mode is similar to BCH mode, however, in this mode we have a 'valid' indication at the end of operation instead of the 'idle'. In order to make it simple for SW, the 'valid' is routed to the same register as the 'idle' is, therefore, SW needs to poll the same register and look at the same bit to know that operation is done.

The 'Poly Status' register indicates if errors were found and 'Correction Data Status' register holds the correction information in case the error can be corrected.

4.4.4.2.3 General flow

The following steps should be done for every read (registers' name is in capital letters, fields are in regular letters):

1. Set 'prty_mode' field in 'GEN_CFG' register to '0' to set parity module to operate in syndrome generation mode.
2. Configure 'CS_SEL_CFG' register, 'hamm_mode', 'ecc_lvl', 'blk_size' and 'tag' fields in 'GEN_CFG' register to desired values.
3. Configure 'INIT' register to '1'. The register is a self clear register after 1 cycle. This resets the parity module and latch configured values.
4. Configure 'SHIFT_EN' register to '1' to enable shifting of data into the parity module. This should be done only before the data block is being read from NAND and not in command or address transactions.
5. Read data block from NAND. Each read triggers a shift into the parity module.
6. If any transaction other than parity reading from NAND is needed, then, configure 'SHIFT_EN' register to '0'.
7. If 'SHIFT_EN' register was reset to '0', configure it back to 1 and read parity bytes from NAND. Each read triggers a shift into the parity module.
8. Once data and parity reading are done, poll 'IDLE_STAT' register until it's asserted. Indicates that the parity module is done with the syndrome calculation and status can be checked.
9. Read 'POLY_STAT' register. If the value is 3'b001, a single error occurred, continue to next step. If the value is 3'b100, 2 or more errors occur that cannot be corrected, go to step 14, otherwise, no errors, go to step 14.
10. In Hamming mode, read 'CORR_DATA_STAT' register and go to step 14. In BCH mode, initiate a correction operation by configuring 'POLY_START_CFG' to '1'. This is a self clear register. Continue to step 11.
11. Read 'CORR_DATA_STAT' register to start getting the errors' locations until 'status' flag (0x7FE) is read on the index bits.
12. After 'status' flag was read, one can read (optional) 'CORR_DONE_STAT' register to verify it is asserted, indicating the correction operation is done.
13. Configure 'SHIFT_EN' to '0'.
14. Repeat steps 2 to 13 as needed.

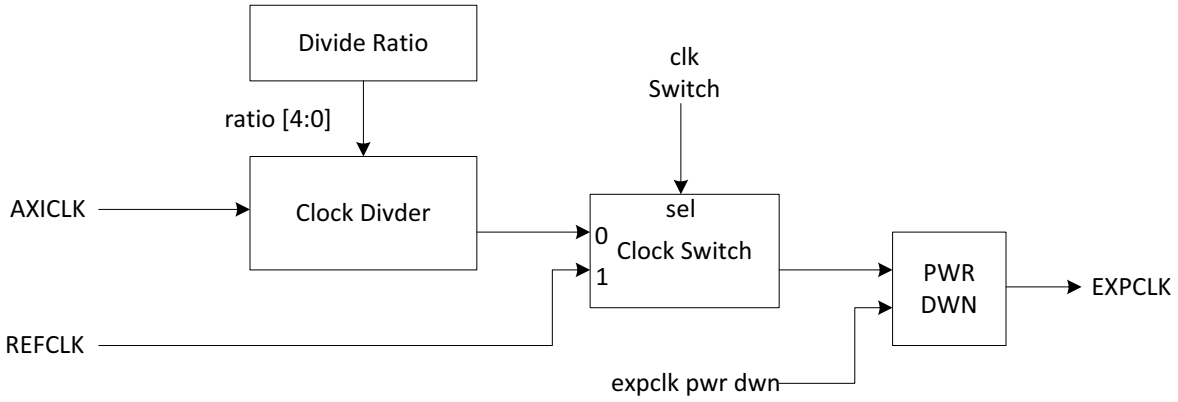
4.4.5 Clocks

One clock is input to the expansion block running at AXI clock rate. The expansion block has a built-in ExpClk Generator, which is responsible for generating a divided synchronous clock to the external peripherals with a maximum of 66.6 MHz. A clock switch selects, glitch-free, between AXI clock and the divider output, and defaults to AXI clock upon reset and switches to the divided AXI clock right after reset ends.

Power down logic defaults to activate the clock. When reset is asserted, output clock might have glitches when switching to reference clock.

This clock generator circuitry can be configured to divide the AXI clock with the following divide values: 3-15. The internal logic of the expansion bus runs at AXI clock speed, and the generated synchronous clock (EXPCLK) is treated as a synchronizing pulse enable for the programmable timing counters.

Figure 4-11 Expansion Bus Clock Generation



4.4.6 Expansion Bus Soft Reset

Asynchronous reset is not used to reset the block's internal logic. This reset may be a combination of the hardware and software resets provided by the chip and is synchronized externally to the AXI clock. A self-clear soft reset can be generated by the block's internal configuration logic when asserted by software. This self-clear reset resets the entire block's logic synchronously. Configuration register are not affected by the block's soft-reset.

4.4.7 Expansion Bus Timing Diagram

Figure 4-12 describes the expansion interface AC timing parameters.

Figure 4-12 Expansion Bus Timing Diagram

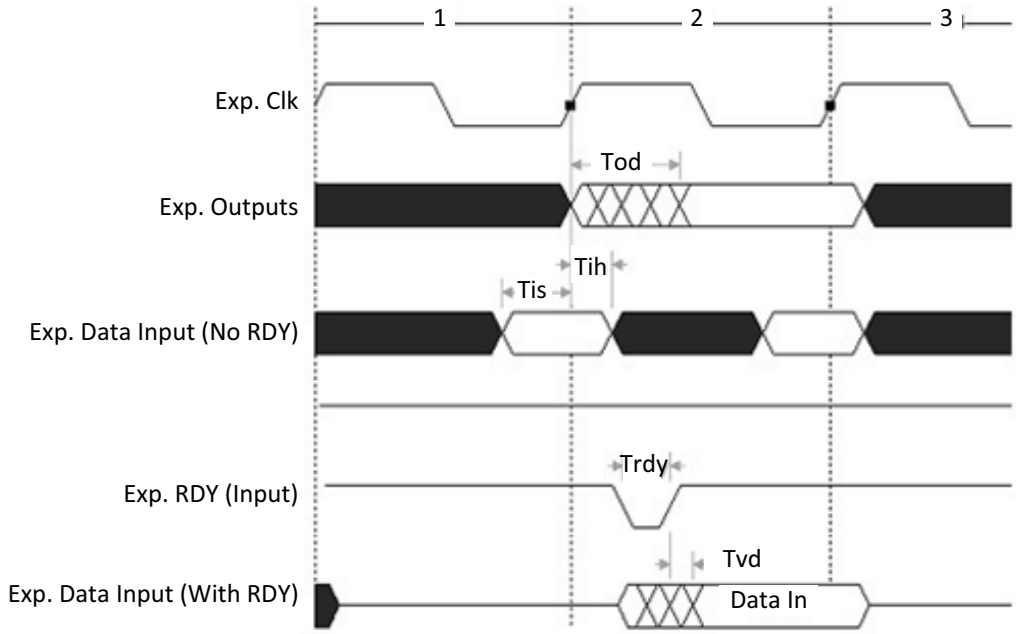


Table 4-2 lists the Expansion Bus timing parameters.

Table 4-2 Expansion Bus Timing Parameters

Symbol	Parameter	Min.	Max.	Units	Notes
	EXP_CLK (Frequency)	23.6	66	MHz	
	EXP_CLK Duty cycle	40	60	%	
Tod	Expansion Outputs relative the rising edge of the EXP_CLK (Output Delay Time)				
	valid to valid	0	6	ns	(1)
	tri-state to valid	0	6	ns	(1)
	valid to tri-state	0	10	ns	(1)
Tz	Expansion Outputs Valid to tri-state				
Tis	Expansion Inputs Setup Time for read data with respect to the rising edge (When Trdy is not used)	1		Cycle	(2)
Tih	Expansion Inputs Hold Time for read data with respect to the rising edge (When Trdy is not used)	0		ns	(3)
Trdy	Ready Input required pulse width	10		ns	(4)
Tvd	Expected valid data after the rising/falling edge of the RDY Pulse. Since the active low RDY edge detection is configurable.		0	ns	(5)

NOTES:
1) Test Load 50pF.
2) Tis (min) value should be configured to be at least 1 EXP_CLK cycle.
3) Tih timing is relevant to the cycle in which CS and/or RE is deasserted.
4) RDY is sampled and synchronized by HCLK.
5) Due to RDY synchronization logic before valid input data latching.

NOTE: For details about Expansion Bus signals, refer to "Expansion Bus Signals" on page 30.

4.5 Bootstrap Synchronization

The device supports 26 input bootstrap pins. During reset EXP_A[25:0] are not driven by LS1024A and they can be set to any configured value through external pull-ups or internal pull-downs. Note that, as listed above, these I/O pads have internal pull-down resistors so an external pull-up is required only if the default value made by the internal pull-down is not the desired one. See Section 31, Hardware Initialization for more detail.

Following reset, the device drives these pins to support Expansion Bus access. The previous latched value is already stored in a software accessible register from which the value can be read but not changed.

NOTE: In case PS_XI/XO is the selected clock source then for proper operation this bootstrap should be set to same value as "SerDes OSC PAD" bootstrap (bit [7])"

4.6 Asynchronous Interface

For an example of asynchronous timing, see Figure 4-3, Normal Mode Timing Diagram (RDY_EN = 1).

1. When Expansion output signals are changing on the same clock edge, the delay between these signals is considered to be between 0 -11 (ns).
2. When Expansion output signals are changing on different clock cycles, the maximum delay between these signals is considered to be: Unexpired of EXP_CLK)-11 (ns) to Unexpired of EXP_CLK)+11 (ns) where N depends on the configured parameters.
3. The read data (if expired is not used) relative to rising edge of CS or RE (whichever deasserted first) should be at least (EXP_CLK Period)+11 (ns).
4. Upon EXP_RDY deassertion state, expansion transaction may be completed within 2 EXP_CLK cycles when relative configuration parameters are set to minimum values.
5. The cycle in which the read data is sampled upon deassertion of RE and/or CS whichever comes first.

While in Asynchronous mode (when RDY is used), the design does not guarantee the relationship between the CS and RE/WE signals. Since the detection of RDY pulse will cause the deassertion of the CS and RE/WE signals simultaneously.

5 DDR3 Controller

This section describes the LS1024A DDR3 SDRAM controller.

5.1 Introduction

The LS1024A provides 16/32-bit DDR3 memory interfaces with optional ECC support. The Memory Controller is programmable for DDR3 SDRAM timing parameters and memory size. The DDR3 controller allows data flow through 4 AXI fabric ports to and from external DDR3 SDRAM memory in burst mode.

5.2 DDR3 Controller Features

The DDR3 interface provides the following features:

- DDR3 support
- Up to 533 MHz (DDR3-1066) with optional clock dithering function
- 16/32-bit support (selection by software)
- Four 64-bit AXI ports
- Address bus supports up to 2G Byte of memory
- Two memory ranks
- 15 address bits (16 in case one rank is used)
- Configurable termination options
- ECC is supported (enabled by configuration)
- 256 Mb to 4 Gb devices with x8/x16 data ports
- Coherency between transactions over different ports of the controller is guaranteed
- Supports low power option including power down and self refresh
- Configurable drive strengths

5.3 Supported Memory Configurations

Table 5-1 lists the supported memory configurations. A maximum of 6 devices are supported.

Table 5-1 Supported Memory Configurations

Address Space	1 Memory Rank		2 Memory Ranks	
	32-bit Bus Mode	16-bit Bus Mode	32-bit Bus Mode	16-bit Bus Mode
32 MB	N/A	1 * (256 Mb, x16) 1 * (256 Mb, x8) for ECC	N/A	N/A
64 MB	2 * (256 Mb, x16) 1 * (256 Mb, x8) for ECC	1 * (512 Mb, x16) 1 * (256 Mb, x8) for ECC	N/A	2 * (256 Mb, x16) 2 * (256 Mb, x8) for ECC
		2 * (256 Mb, x8) 1 * (256 Mb, x8) for ECC		

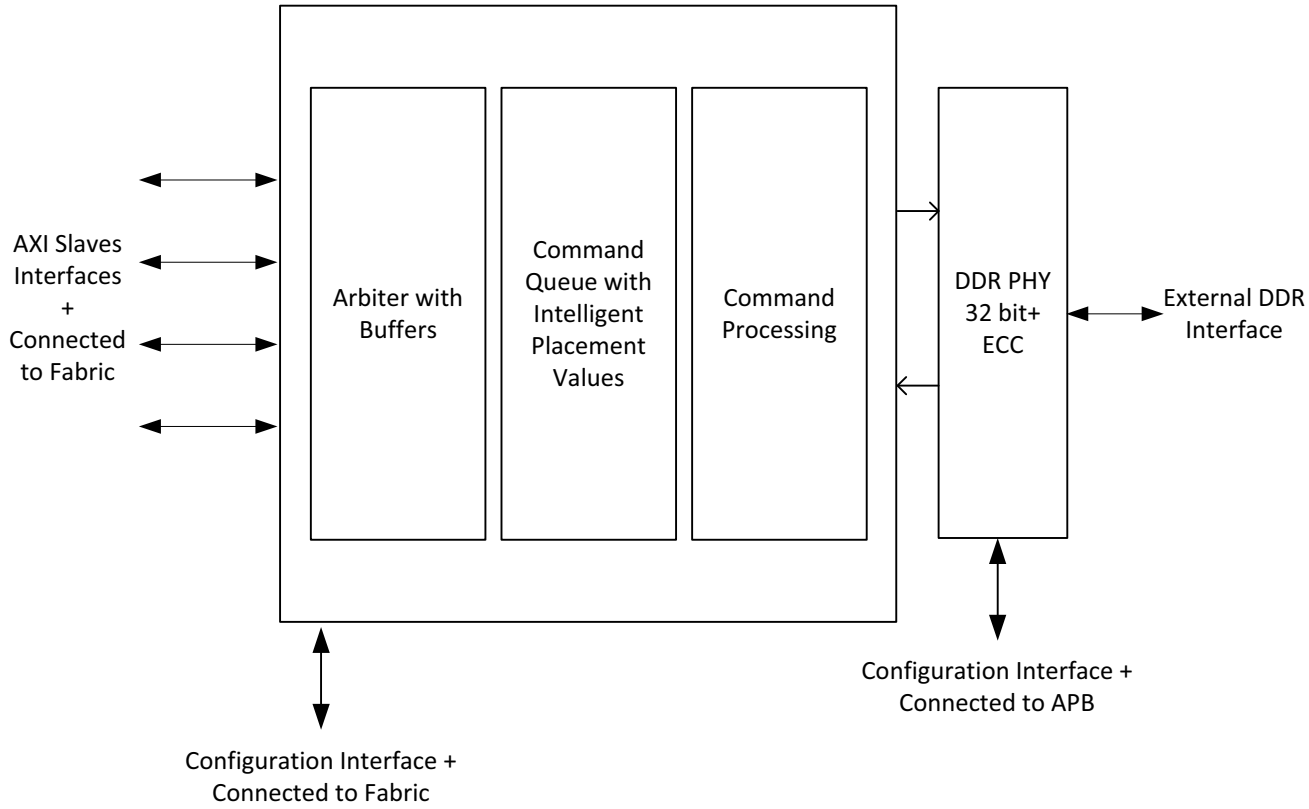
Table 5-1 Supported Memory Configurations (continued)

Address Space	1 Memory Rank		2 Memory Ranks	
	32-bit Bus Mode	16-bit Bus Mode	32-bit Bus Mode	16-bit Bus Mode
128 MB	2 * (512 Mb, x16) 1 * (256 Mb, x8) for ECC	1 * (1 Gb, x16) 1 * (512 Mb, x8) for ECC	4 * (256 Mb, x16) 2 * (256Mb, x8) for ECC	2 * (512 Mb, x16) 2 * (256 Mb, x8) for ECC
	4 * (256 Mb, x8) 1 * (256 Mb, x8) for ECC	2 * (512 Mb, x8) 1 * (512 Mb, x8) for ECC		4 * (256 Mb, x8) 2 * (256 Mb, x8) for ECC
256 MB	2 * (1 Gb, x16) 1 * (512 Mb, x8) for ECC	1 * (2 Gb, x16) 1 * (1 Gb, x8) for ECC	4 * (512 Mb, x16) 2 * (256 Mb, x8) for ECC	2 * (1 Gb, x16) 2 * (512 Mb, x8) for ECC
	4 * (512 Mb, x8) 1 * (512 Mb, x8) for ECC	2 * (1 Gb, x8) 1 * (1 Gb, x8) for ECC		4 * (512 Mb, x8) 2 * (512 Mb, x8) for ECC
512 MB	2 * (2 Gb, x16) 1 * (1 Gb, x8) for ECC	1 * (4 Gb, x16) 1 * (2 Gb, x8) for ECC	4 * (1 Gb, x16) 2 * (512 Mb, x8) for ECC	2 * (2 Gb, x16) 2 * (1 Gb, x8) for ECC
	4 * (1 Gb, x8) 1 * (1 Gb, x8) for ECC	2 * (2 Gb, x8) 1 * (2 Gb, x8) for ECC		4 * (1 Gb, x8) 2 * (1 Gb, x8) for ECC
1 GB	2 * (4 Gb, x16) 1 * (2 Gb, x8) for ECC	2 * (4 Gb, x8) 1 * (4 Gb, x8) for ECC	4 * (2 Gb, x16) 2 * (1 Gb, x8) for ECC	2 * (4 Gb, x16) 2 * (2 Gb, x8) for ECC
	4 * (2 Gb, x8) 1 * (2 Gb, x8) for ECC			4 * (2 Gb, x8) 2 * (2 Gb, x8) for ECC
2 GB	4 * (4 Gb, x8) 1 * (4 Gb, x8) for ECC	N/A	4 * (4 Gb, x16) 2 * (2 Gb, x8) for ECC	N/A

5.4 Functional Description

The DDR3 Memory Controller is a high performance component capable of operating DDR3 SDRAMs with data rates up to 1066 Mb/s for DDR3. The multi-port memory controller accepts memory access requests from up to 4 application-side AXI ports. It includes software configuration registers that are accessible through an AHB configuration port.

Figure 5-1 DDR3 Controller Block Diagram



To support operation at high data rates, the controller interfaces an internal DDR3 PHY that includes address/command path, data paths, DLL and the SSTL I/Os tailored to DDR SDRAM interfacing.

The controller is designed to control up to two memory ranks. It generates separate chip select and on-die termination for each memory rank. Multiple rank support allows memory depth expansion, while support for wide word interfaces allows data width expansion.

By default there are 15 DDR address lines, which is suitable for most applications. If using one rank, the second chip select CS1 may be used as a16th address line if necessary. Please contact Freescale support for details of configuring this mode.

All critical SDRAM timing parameters are programmable for compatibility with different speed grades and/or different vendors.

The multi-ports AXI interface unit contains FIFOs for commands, read and write data, and processes any clock domain crossings. From the port interface blocks, commands are filtered through an arbiter which feeds single commands to the command queue. The command queue uses a placement algorithm to determine the order in which commands execute in the controller. The placement logic follows many rules to determine where new commands should be inserted into the queue, relative to the contents of the command queue at the time.

Placement is determined by considering address collisions, source collisions, data collisions, command types and priorities.The entire command queue is reviewed to determine which banks are to be accessed in the future. The timing is then set to meet the trc and tras_min timing parameters of the memory devices values, which were programmed into the memory controller on initialization. This flexibility allows the memory controller to be tuned to extract the maximum performance out of memory devices.

5.5 DDR3 SDRAM Interface Bus Timing

Figure 5-2 and Figure 5-3 illustrate the DDR3 write cycle and read cycle timing respectively. Table 5-2 lists the DDR3 timing parameters.

Figure 5-2 DDR3 Write Cycle Timing

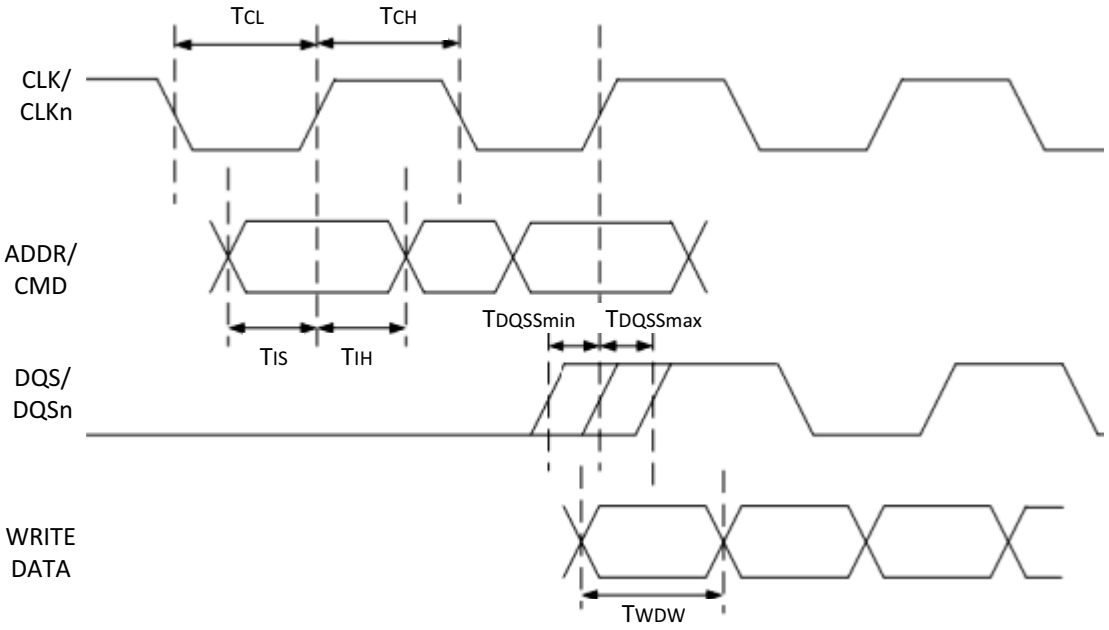


Figure 5-3 DDR3 Read Cycle Timing

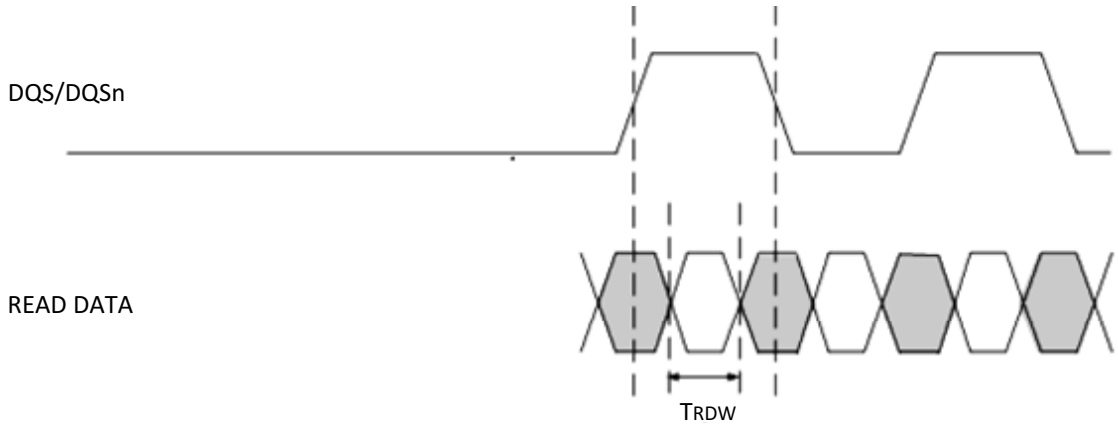


Table 5-2 DDR3 Timing Parameters

Symbol	Parameter	Min.	Max.	Units	Notes
TCH/TCL	Clock high/low level width 533MHz	0.47	0.53	tck(avg)	
TIS	Setup time for address and command signals to rising edge of clock 533MHz	320		ps	1

Table 5-2 DDR3 Timing Parameters (continued)

Symbol	Parameter	Min.	Max.	Units	Notes
TIH	Hold time for address and command signals to rising edge of clock 533MHz	500		ps	1
TWDW	Write Data Window – the minimum time the output data is stable 533MHz	475		ps	2
TDQSS	DQS, DQSn rising edge to CK, CKn rising edge	0.15	0.15	tck(avg)	
TRDW	Read Data Window - the minimum time read data must be stable 533MHz	450		ps	3

General Notes

- Specified timing is for full drive strength operation.
- All values were measured from vref to vref, unless otherwise is specified.
- All timing parameters with CLK signal are defined on CLK-CLKn crossing point.
- All timing parameters with DQS signal are defined on DQS-DQSn crossing point.

Notes

1. Assuming 1V/ns slew rate for address and command signals at the input to the DRAM.
2. The timing is for each 8 data bits and 1 mask bit, measured at the input to the DRAM with 2 inch trace length.
3. The read data window combines the setup and hold timing requirement at input of the LS1024A device.

NOTE: For details about DDR signals, refer to "DDR3 Signals" on page 34.

6 General Purpose Input Output

This section describes the LS1024A GPIO features, capabilities and timing parameters.

6.1 Introduction

The LS1024A device provides up to 64 General Purpose Input Output (GPIO) signals. Of those 64, 8 can be programmed to create interrupts on rising, falling or both edges of input signals. The interface signals are also level sensitive and can generate an interrupt as long as the input is high. The GPIO block holds the configuration registers for the GPIO lines as well as configuration registers for other blocks and input signals.

6.2 Features and Functions

The GPIO interfaces directly to the internal APB bus, which can be accessed by all the CPUs. GPIO interface provides the following features:

- 16 (GPIO[15:0]) dedicated general purpose I/O interface signals for specific control, monitoring signaling purpose.
- GPIO[7:0] can be programmed to create interrupts with rising or falling edges or can be level (high) sensitive
- Additional 48 (GPIO[63:16]) GPIOs are muxed with other functional pins and can only be used in case the other functionality is not used. Muxing selection is in most of the cases per pin. See Table 3-2, Muxing Table.
- At least 16 GPIO pins are capable of driving 10mA of current, which is sufficient for direct LED control.

6.2.1 GPIO Function and Pin Select

There are 64 GPIO signals. Each GPIO has an associated enable bit in the GPIO output enable register. Writing a '1' to the output enable bit will configure the GPIO to be an output. Writing a '0' will configure the GPIO to be read only. GPIO inputs are read via the GPIO input status register.

GPIO pin select registers are used to choose between GPIO and alternate functionality. Pad configuration registers are provided to control slew rates, Schmitt triggers inputs, pull up/down I/O and drive strength.

6.2.2 GPIO Interrupt (0x4, 0x8)

GPIO[7:0] input signals can be programmed to generate 8 interrupts to CPU by setting the corresponding GPIO rising or falling edge interrupt enable register bits. At the chip level the interrupts are provided to A9 IRQ and to PMU IRQ (which is in GPIO and is connected to Util-PE and CSS blocks).

In order to use this logic:

- Set the GPIO signal(s) that should be used as interrupts as input (via output enable register).
- Choose the appropriate triggering for the "Interrupt configuration" registers.
- Interrupt signals are generated based on transition/value of input GPIO signals.

6.2.3 GPIO Timing Diagram

Figure 6-1 illustrates the GPIO timing waveform. Table 6-1 lists the GPIO timing parameters.

Figure 6-1 GPIO Timing Diagram

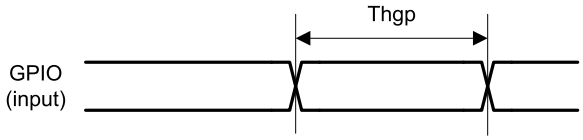


Table 6-1 GPIO Timing Parameters

Symbol	Description	Min	Max	Units	Notes
Thgp	GPIO pulse duration	10		ns	This is the minimal pulse width time for a GPIO (as an input) that is guaranteed to internally register a change. The minimum width must be larger than Fabric clock period. For the slowest fabric clock frequency of 125 MHz, the minimum pulse width detected is 10 ns.

NOTE: For details about GPIO signals, refer to "GPIO Signals" on page 35.

7 Clock and Reset

This section describes the LS1024A clock and reset details.

7.1 Clock Features

The clock features are as follows:

- Four PLLs are available: PLLs 0,1 and 2 have 2 GHz VCO, while PLL3 has a 1.2 HGz VCO with dithering function.
- Two Numerically Controlled Oscillators are available to generate fractional clocks for network timing, like TDM, ZDS and MSIF interface output clocks, and GEMAC Time Stamp Unit internal clock.
- Generation of 125 MHz RGMII TX clock outputs, and three reference clock outputs for external PHYs/switches with programmable rates. If intending to use these clocks with an external switch/PHY, please discuss with Freescale technical support.
- Generation of differential reference clock outputs, derived from PCIe reference clock input, PCIe pipe clock, or internal PLL.
- PCIe 100 MHz SSC reference clock output provided for each PCIe SerDes.
- Support for DDR clock dithering when DDR DFI clock is generated from PLL3. In this mode, PLL3 should not be used for generation of internal system clocks.
- I^2C, SPI, I^2S, UART Baud rate, and Expansion bus interface clock outputs are derived from internal AXI fabric clock.
- Generated clocks for Cortex®-A9, L2cc, PPFE, AXI, DDR support both synchronous or asynchronous relationships.
- Generation of asynchronous clocks for DECT, Crypto engine and CoreSight.
- All generated clocks have programmable rate, divided down from any of the internal PLLs. Clocks can be sourced from the same PLL for synchronous relationship, or from different PLLs if clock decoupling is desired. PLL0 is the PLL used for synchronous operation mode.
- Several options for dynamic clock rate changes. PLL0 and PLL1 have clock dividers at their outputs for on the-fly global clock rate reduction of all clocks sourced from them. Switching clock sources from one PLL to another can be done quickly and is glitch-free.
- All generated clocks are active during reset running at the reference clock frequency. After reset, clocks can be shut down or stay active based on their enable bits default values.
- Internally generated TDM clock is bypassed in reset by refclk divided down to the 1.56 MHz range to avoid interface over clocking. The divide ratio is automatically adjusted based on the reference clock rate selected option. Switching between the divided reference clock and generated TDM clock is done through glitch-less configuration. The divider is not reset by Hardware Reset.
- 50% duty cycle is targeted for all clocks
- All clocks can have the ability to individually shut down, which reduces power consumption when any of them are disabled.
- Several options for the system PLLs and SerDes reference clocks: dedicated, shared or differential. This lowers the board cost and provides more flexibility for the board design based on the target application.

7.2 Reset Features

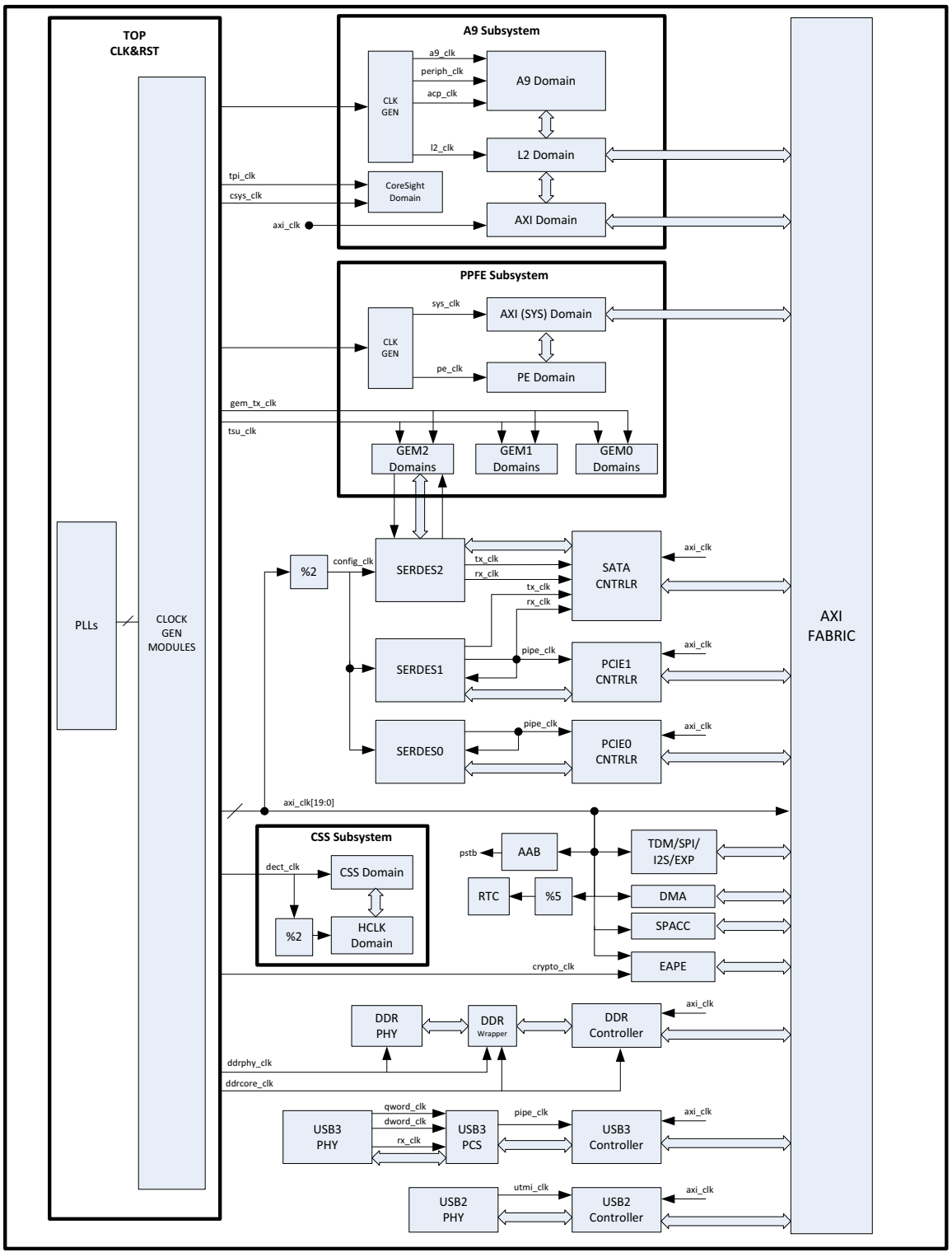
The Reset features are as follows:

- Active low asynchronous external hardware reset globally resets the device; reference clock should be active while reset is asserted, since some logic portions in the device use synchronous reset schemes.
- Software Reset options - Global reset including clock and reset modules, or cluster logic without clock and reset modules. Reset for CoreSight and CA9 debug logic can be separately controlled by software, enabling debug of boot-up sequence.
- All blocks have block software reset with a default value of being in reset, except the blocks that are needed for boot up.
- Several WatchDog reset schemes are implemented to reset each of the CPUs or the whole device.

7.3 Clock Functional Description

Figure 7-1 shows the general clock diagram.

Figure 7-1 General Clock Diagram



7.3.1 Clock Generation

The top level clock and reset block instantiates four analog PLLs (one of them dithered), all sharing one input reference clock. For each clock domain in the device, the PLLs outputs are muxed and optionally divided down to generate the required clock rate. The output of each clock divider is split into several branches, to be distributed to blocks that run at the same rate, and each branch is gated for shut down options. This provides the option to shut down clocks of individual blocks when they are not in use.

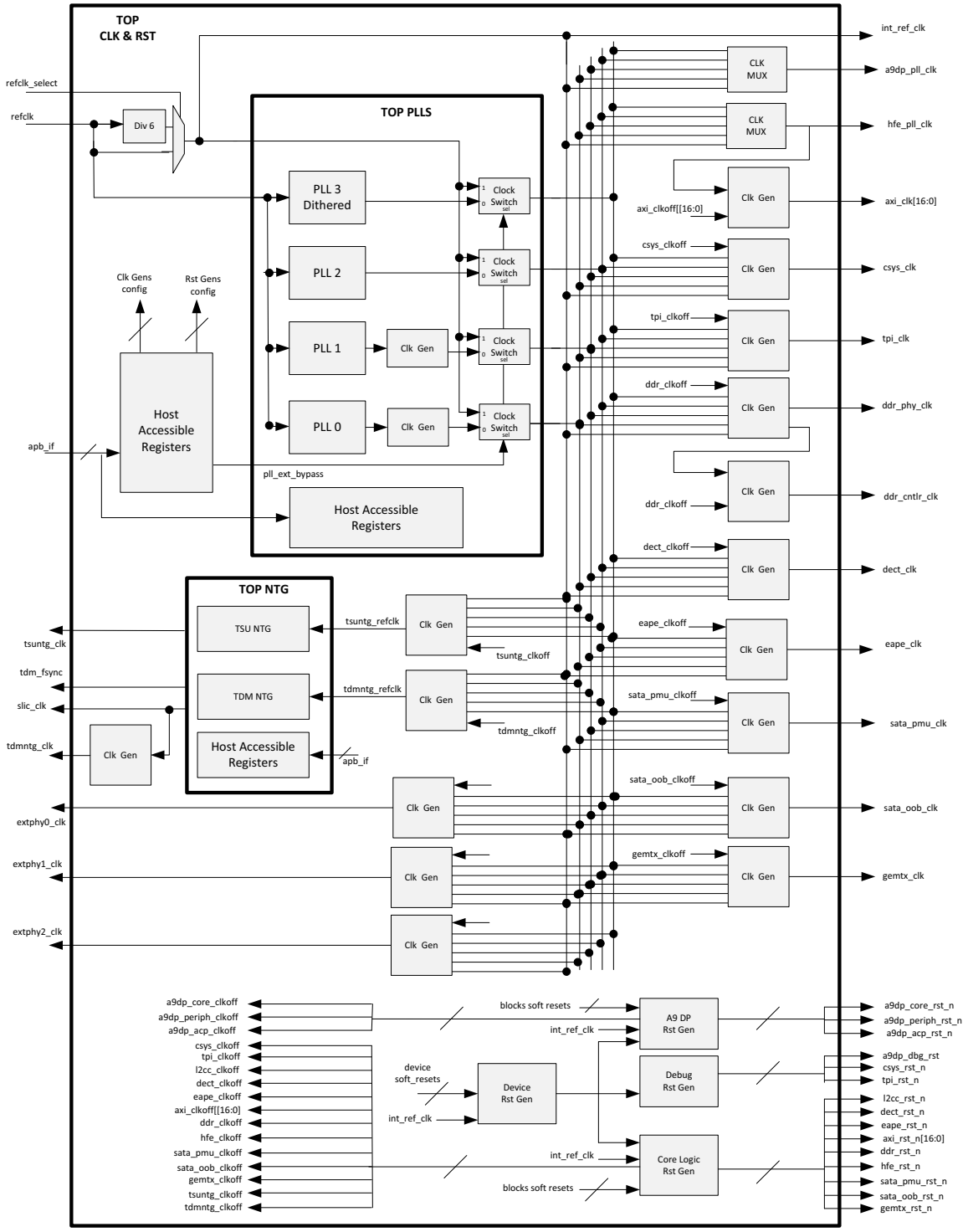
Clock dividers of synchronous clocks run in parallel rather than cascaded. This enables the support of half-integer multiples (3:2, 6:4, and so on.) where needed. For example, to achieve a 1:2 and 1:4 clocks, a divide by 2 and a divide by 4 can be sourced from the same main clock.

To achieve phase alignment when two or more clock dividers are running in parallel from the same PLL, a synchronization procedure needs to be followed. The clock generation module also generates the "clock enable" signals required to regulate data flow between clocks that are multiples but synchronous to each others. Integer and half integer multiples shall be supported, 1:1, 2:3, 1:2 and so on.

For each clock branch, a dedicated reset signal is provided that is controlled by software. Based on the reference clock selection bootstrap pin (125 MHz or 48/24 MHz), the Reference Clock input is either used as is or divided down automatically. This is to limit the internal clock used during boot-up (PLL bypass) to a maximum of 48 MHz. The PLLs always work with the raw undivided reference clock.

Table 7-2 illustrates the top level clocking generation.

Figure 7-2 Top Level Clocking Generation

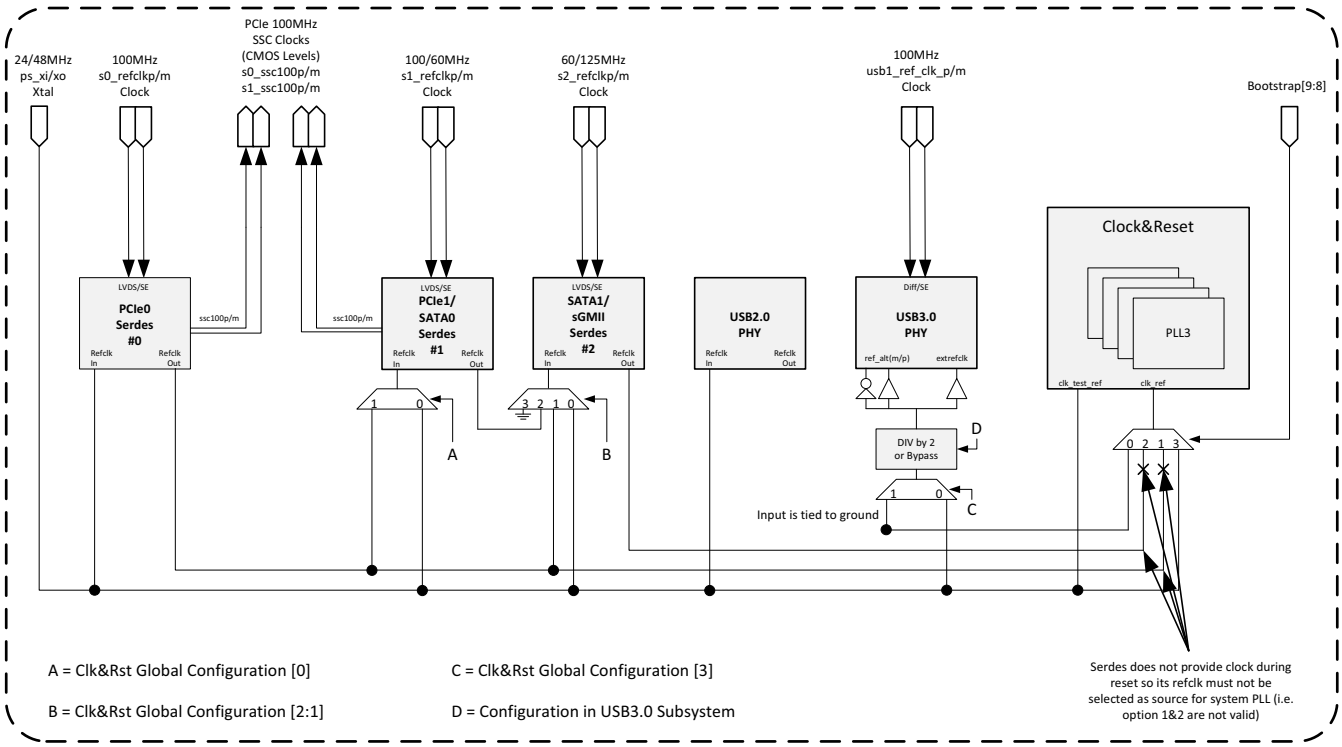


7.3.2 Reference Clocks

7.3.2.1 Input Reference Clocks

Figure 7-3 shows the SerDes, PHY and PLL reference clocks connection.

Figure 7-3 SerDes, PHY and PLL Reference Clocks



- PS_XI — Device Reference Clock (24 MHz or 48 MHz - 48 MHz is recommended)
- RTC_XI — Crystal for RTC (32.768 KHz) - Only required if function is used
- DECT_XI — Crystal for CSS (13.824 MHz) - Only required if function is used
- Differential input clock per SerDes
  - 100 MHz (optionally SSC) for PCIe[1]
  - 60 MHz for SATA[2]
  - 125 MHz for SGMII
- Differential USB3.0 PHY clock input
  - 20, 24, 100 MHz (optionally SSC if USB2.0 function uses an internal refclk)
- UP_XI - Tie to ground.

NOTE:

1. If the SerDes port is used for PCIe Gen2, it is mandatory to supply an appropriate 100 MHz clock to the SerDes clock input.
2. If the SerDes port is used for SATA boot from IBR (BOOT_OP[2:0]=101), an external 60 MHz clock must be provided.

7.3.2.2 Output Reference Clocks

- GEM PHY — three GEM clocks (two if SGMII is used) at 25 or 50 MHz
- DECT BCLK — output clock for external RF module. A weak driver is used but external component is needed in order to create a sinusoidal clock
- PCIe —Differential CMOS Level (from 1.1V VDDA) 100 MHz (optional SSC) from each SerDes

7.3.3 Functional Clocking Modes

The device is designed to work in two clocking modes, and under different operating voltages. Maximum Clock frequencies for A9, L2, AXI Bus, PPFE PE, PPFE SYS, and DDR, depend on the selected mode of operation.

Below are system clocking modes:

- Synchronous Mode — L2 Cache is synchronous to AXI Bus. The two are sourced from PLL0 and their clock ratios can be full or half-integer (1:1, 1:1.5, 1:2, 1:3, 1:4, …), with AXI always assumed to be less or equal to L2. Support for Half-integer 1:1.5 only.
- Asynchronous Mode — L2 Cache and AXI Bus are asynchronous: their clock rates and PLL source are completely independent. It is recommended to use PLL2 or PLL0 for A9 clocking at maximum frequency to match the Static Timing Analysis.
- DDR Asynchronous Mode — DDR Core and AXI Bus are asynchronous. Their clock rates and PLL source are completely independent. If DDR clock dithering is required, PLL3 must be used in that case. DDR async mode and L2-AXI sync/async mode are independent.
- DDR Synchronous Mode — DDR Core and AXI Bus are synchronous with 1:1 ratio, and they are both sourced from PLL0. DDR Clock dithering will not be supported in this case. DDR sync mode and L2-AXI sync/async mode are independent.

7.3.4 Device PLLs

The device has a total of 4 PLLs. Three of them are regular PLLs with a 2 GHz maximum VCO frequency, and one is a dithered PLL with 1.2 GHz maximum VCO frequency.

Table 7-1 lists the LS1024A PLLs.

Table 7-1 LS1024A PLLs

PLL	Description	Clock Output			Lock Time (Max)
		Rate (MHz)[2]	Jitter (p-p)	Duty Cycle(1)	
PLL0	L4LP 1.1V 2GHz FSPLL	1800	6%VCO	40-60%	400 us
PLL1	L4LP 1.1V 2GHz FSPLL	1500	6%VCO	40-60%	400 us
PLL2	L4LP 1.1V 2GHz FSPLL	1800	6%VCO	40-60%	400 us
PLL3	L4LP 1.1V 1.2GHz Dithered PLL	1066	6%VCO	40-60%	750 us

Note:
1. Worst case duty cycle when VCO output divider (S) equals zero.
2. Clock rate is the maximum rate used in this device, not PLL maximum rate.

7.4 Reset Functional Description

7.4.1 Global Resets

The LS1024A provides the following global resets:

- External Hardware Reset

  Asynchronous active low input that resets the whole device. Once activated, it reaches all flops without any synchronization and triggers a reset sequence that finishes after 140 reference clocks. The clocking logic is taken out of reset first, followed by the core functional blocks, and lastly the CortexA9 processor.

  The system reset signal RESET_N should remain asserted (low) at least for 10 µs after all power supplies are established and the chosen reference clock is running.

- Watchdog Reset

  When the watchdog timer expires, it resets all the blocks, clock and reset modules, PLLs, and including itself after some synchronization delay in the reset block. It behaves similarly to the external hard reset. In addition to the global watchdog timer, each CPU has an internal watchdog timer that can reset only the corresponding CPU. All watchdog resets can be masked by software.

- Global Software Reset

  The top clock and reset block has a self-clear global software register. It behaves exactly as the external Hardware Reset.

- Functional Software Reset

  Functional Software reset shall reset all functional blocks, that is, all blocks except: PLLs, clock and reset modules, and all debug logic circuitry. This allows for debugging the boot up sequence, by setting up the debug circuitry and then issuing a functional reset to trace the boot up sequence. Two types of functional resets are available: Self-Clear and Static resets.

- Debug Reset

  A static configuration bit in the top level clock and reset shall keep all debug logic circuitry in reset. This includes the CoreSight logic, as well as the ARM debug logic. The ARM debug logic can be put in reset individually by configuration bits within the System cluster clock and reset. By default, all debug reset configuration bits are in the inactive state (no reset).

Figure 7-4 shows the Reset timing diagram.

Figure 7-4 Reset Timing Diagram

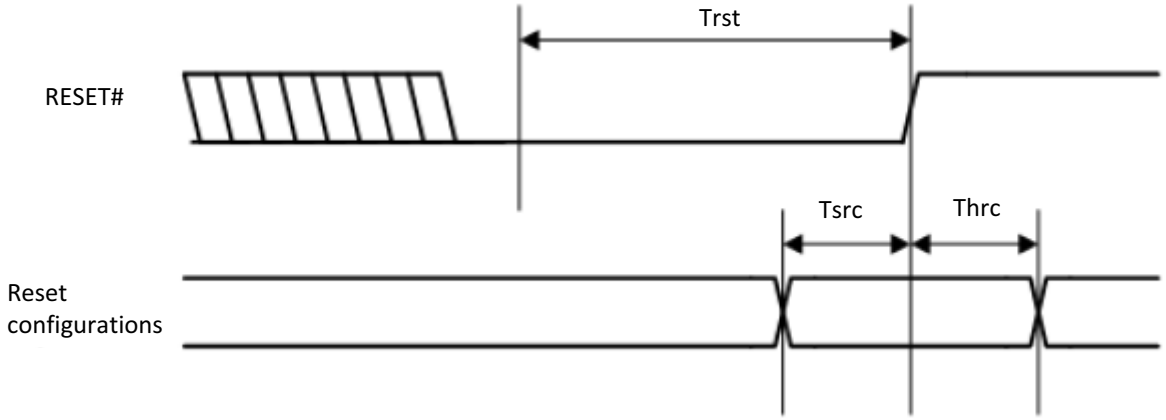


Table 7-2 lists the Reset timing parameters.

Table 7-2 Reset Timing Parameters

Symbol	Description	Min	Max	Units
Trst	Reset duration	100		us
Tsrc	Bootstrap configurations setup time	400		ns
Thrc	Bootstrap configurations hold time	0		ns

7.4.2 Block Resets

Each clock domain has a dedicated reset that is synchronised to it. A global reset control bit shall reset the whole clock domain, including all branches. For each branch of the clock domain, a configuration bit shall reset that specific branch.

7.5 Timing Parameters

7.5.1 Input Reference Clocks

Table 7-3 lists the AC timing parameters of SerDes, USB, PHY and PLL reference clock.

Table 7-3 AC Timing Parameters - SerDes, USB, PHY and PLL Reference Clock

Symbol	Description	Min	Typ	Max	Units
	Clock frequency Option 1 (Default) Option 2		 48 24		 MHz MHz
	Clock duty cycle	40		60	%
	Clock accuracy	-50		50	ppm

If DECT functions are used, an additional DECT reference clock (13.824 MHz) is required. Table 7-4 lists the AC timing parameters of DECT reference clock.

Table 7-4 AC Timing Parameters - DECT Reference Clock

Symbol	Description	Min	Typ	Max	Units
	Clock frequency		13.824		MHz
	Clock duty cycle	45		55	%
	Clock accuracy	-10		10	ppm

If RTC functions are used, an additional RTC reference clock (32.768 MHz) is required. Table 7-5 lists the AC timing parameters of RTC reference clock.

Table 7-5 AC Timing Parameters - RTC Reference Clock

Symbol	Description	Min	Typ	Max	Units
	Clock frequency		32.768		KHz
	Clock duty cycle	30		70	%
	Clock accuracy	-50		50	ppm

7.5.2 Output Reference Clocks

Table 7-6 lists the AC timing parameters of TDM reference clock.

Table 7-6 AC Timing Parameters - TDM Output Reference Clock

Symbol	Description	Min	Max	Units
	Frequency resolution 1.536 MHz 1.544 MHz 2.048 MHz 4.096 MHz 8.192 MHz 16.384 MHz 18.432 MHz 24.576 MHz 49.152		 0.1136 0.0758 0.0568 0.0284 0.0142 0.0072 0.00632 0.00474 0.00236	ppm
	Duty cycle All clocks	40	60	%

Table 7-7 lists the AC timing parameters of Ethernet reference clock.

Table 7-7 AC Timing Parameters - Ethernet Output Reference Clock

Symbol	Description	Min	Typ	Max	Units
	Clock frequency, to be used by: RGMII PHYs RMII PHYs		 25 50		 MHz MHz
	Duty cycle All clocks	45		55	%
	Clock accuracy	-50		50	ppm

NOTE:

1. Achievable only if using a ±50ppm (or better) crystal. In general, reference clock accuracy corresponds to crystal's accuracy.
2. Reference clocks are not defined by the RGMII specification. They are provided as a convenience to the system designer for use by external RGMII PHY/Switches.

7.5.3 Crystal Requirements

Figure 7-5 Crystal Requirements

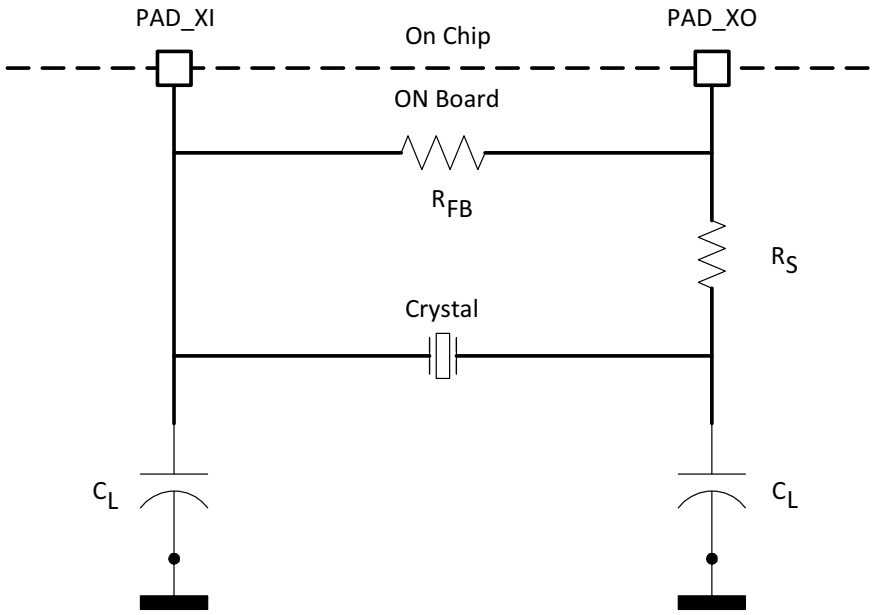


Table 7-8 Approximate System Values for Crystal Circuits

Parameter	Reference Clock		RTC	DECT
	24 MHz	48 MHz	32.768 KHz	13.824 MHz
R_{FB} (ohms) (Feedback Resistor)	5 M	100 k	5 M	5 M
R_S (ohms) (Series Resistor)	0 - 1K	0 - .5K	330k	0

Table 7-8 Approximate System Values for Crystal Circuits (continued)

Parameter	Reference Clock		RTC	DECT
	24 MHz	48 MHz	32.768 KHz	13.824 MHz
C_L (farads) (Load Capacitor)	14 p	14 p	14 p	14 p
Accuracy	+/- 50 ppm	+/- 50 ppm	+/- 50 ppm	+/- 10 ppm

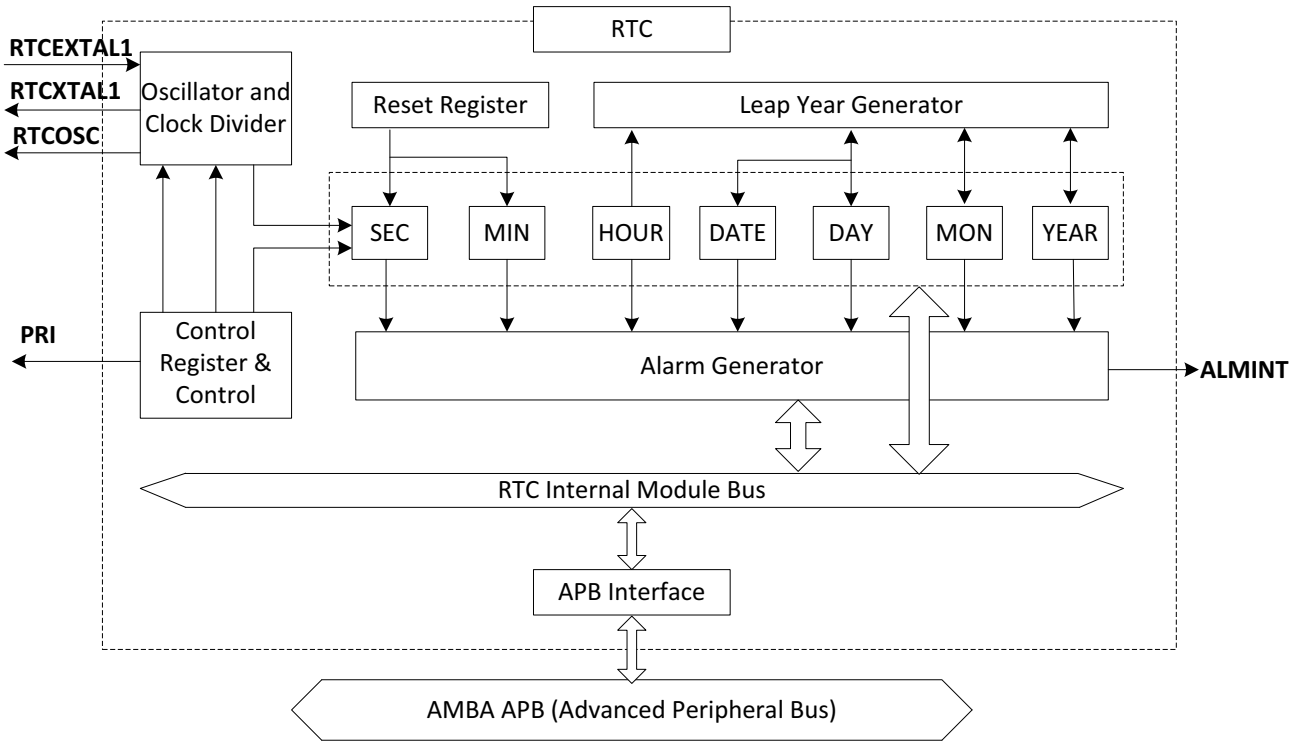
Note:
1. The values of Rfb, Rs, and CL may be further refined to meet the frequency requirements of the system.
2. Regulation agencies may require +/-5ppm accuracy for DECT certification.

8 Real Time Clock

This section describes the LS1024A Real Time Clock (RTC).

The RTC unit will operate by the backup battery when the system power is off. The RTC returns data to CPU as Binary Coded Decimal (BCD) values. The data includes second, minute, hour, date, day of the week, month, and year. The RTC unit works with an external 32.768 kHz crystal and also can perform the alarm function. Figure 8-1 shows the RTC block diagram.

Figure 8-1 RTC Block Diagram



8.1 Features

The following are the RTC features:

- Clock and calendar functions (BCD display)
  - seconds, minutes, hours, date, day of week, month, year
- Leap year generator
- Alarm interrupt (ALMINT) function
- Cyclic interrupts: the interrupt cycle may be 1/256 second, 1/64 second, 1/16second, 1/4 second, 1/2 second, or 1 second
- Operate by the backup battery 3V even when system power is off

The RTC Bridge passes the APB request on the LS1024A APB bus to the RTC APB interface which is running at a slower clock. The RTC Bridge is responsible for the following two operations:

- Write Operation — The write operation is done in a single APB write request

- Read Operation — Since there is no flow control on the APB bus and the RTC APB interface is running at a slower clock, the read operation for RTC on APB bus is divided into two operations

8.2 Function Description

8.2.1 Leap Year Generator

The leap year generator calculates the last date of each month as 28, 29, 30 or 31 based on the data from BCDDAY, BCDMON, and BCDYEAR. This also considers leap years in deciding the last date. A 16-bit counter can just represent four BCD digits, so it can decide whether any year is a leap year or not.

8.2.2 Clock Function

It is required to set to "1" of the RTCCON[1] register for interfacing between CPU and RTC logic. One second error can occur when the CPU reads or writes data into BCD counters and this can cause the change of the higher time units. When the CPU reads/writes data to/from the BCD counters, another time unit may be changed if BCDSEC register is overflowed. To avoid this problem, the CPU should reset BCDSEC register to 00h. The reading sequence of the BCD counters is BCDYEAR, BCDMON, BCDDATE, BCDDAY, BCDHOUR, BCDMIN, and BCDSEC. It is required to read it again from BCDYEAR to BCDSEC if BCDSEC is zero.

8.2.3 Backup Battery Operation

The RTC logic is driven by backup battery if the system power turns off. The interfaces of the CPU and RTC logic are blocked and the battery drives the oscillation circuit, clock divider (DIVIDER), and BCD counters (RTCFCN) to minimize power dissipation.

The RTC_VDD pin must never be left floating. If the RTC is not used, the RTC_VDD pin can be connected to 3.3V. If the RTC function is used, logic should be included to allow RTC_VDD to connect to 3.3V while powered up and a 3V battery when powered down.

8.2.4 Alarm Function

The RTC generates an alarm signal at a specified time. The RTC alarm register, RTCALM, determines the alarm enable and the condition of the alarm time setting.

8.3 RTC Operation

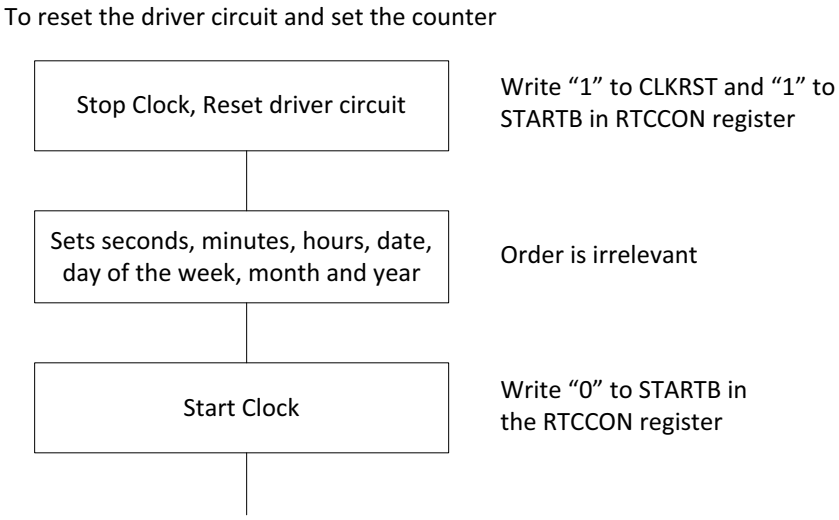
8.3.1 Initial Settings of Registers after Power-on

All the registers should be set after the power is turned on.

8.3.2 Setting the Time

Figure 8-2 shows how to set the time when clock is stopped. This works when the entire calendar or clock is to be set.

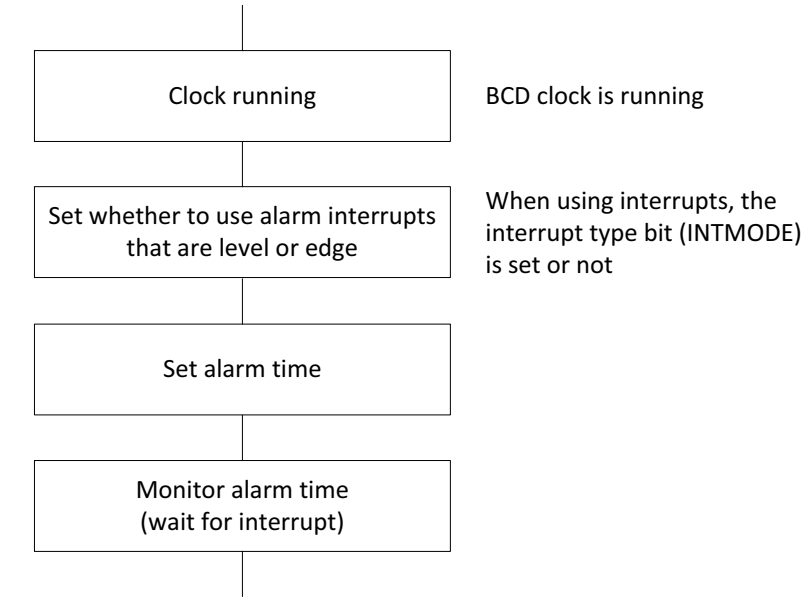
Figure 8-2 Setting Time



8.3.3 Alarm Function

Figure 8-3 shows how to use the alarm function.

Figure 8-3 Alarm Functions



Alarms can be generated using the seconds, minutes, hours, days of week, date, month, year or any combination of these. Set the ALMEN bit (bit 7) in the register on which the alarm is placed to "1", and then set the alarm time. Clear the ALMEN bit in the register on which the alarm is placed to "0".

When the INTMODE bit of RTCIM register is high, and the clock and alarm times match, "1" is set in the PEND bit of RTCPEND register. The detection of alarm can be checked with reading the PEND bit.

9 Low Speed SPI

This section describes the LS1024A Serial Peripheral Interface (SPI) interface.

9.1 Overview

On a LS1024A device, the SPI typically works with TDM and interfaces with SLIC/SLAC devices to connect to standard POTS telephone equipment. It can also be used to access or boot from external serial memory.

The multi-chain SPI provides a common interface mechanism to SLICs from multiple vendors and is used to setup such parameters as μ-law / a-law PCM conversion. For a view of the SPI within the top-level block diagram, see Figure 9-1.

9.2 Features

- Serial interface operation
- Clock bit-rate - User can dynamically control the serial bit rate of the data transfer.
- Serial Master - Enables serial communication with serial slave peripheral devices.
- Independent masking of interrupts - transmit FIFO overflow, transmit FIFO empty, receive FIFO full, receive FIFO underflow, and receive FIFO overflow interrupts can all be masked independently.
- Data frame size (4 to 16 bits) - The frame size of each data transfer is under the control of the programmer.
- FIFO depth - The depth of the transmit and receive FIFO buffers is 8 words deep. The FIFO width is fixed at 16 bits.
- Number of slave select outputs - 4 serial slave select output signals are provided.
- Hardware/software slave-select - Dedicated hardware slave-select lines can be used or software control can be used to target the serial slave device.

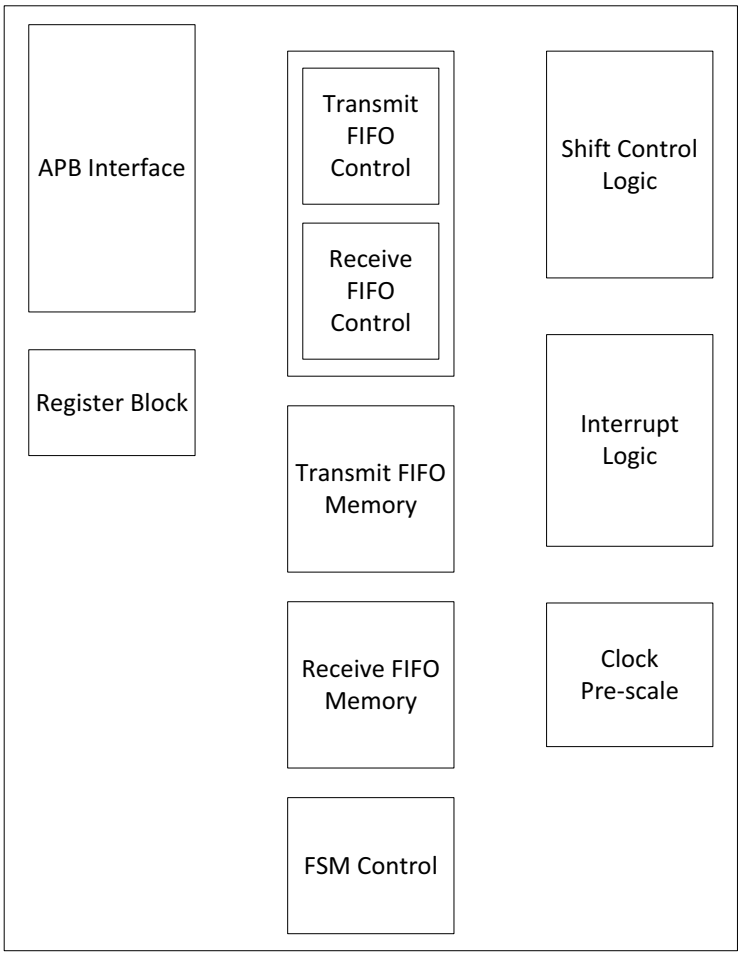
NOTE: The SPI interlace signals are multiplexed with GPIOs:

- SPI_SCLK (muxed with GPIO31)
- SPI_TXD (muxed with GPIO30)
- SPI_RXD (muxed with GPIO32)
- SPI_SS0_N (muxed with GPIO18)
- SPI_SS1_N (muxed with GPIO19)
- SPI_SS2_N (muxed with GPIO21)
- SPI_SS3_N (muxed with GPIO22)

9.3 Functional Description

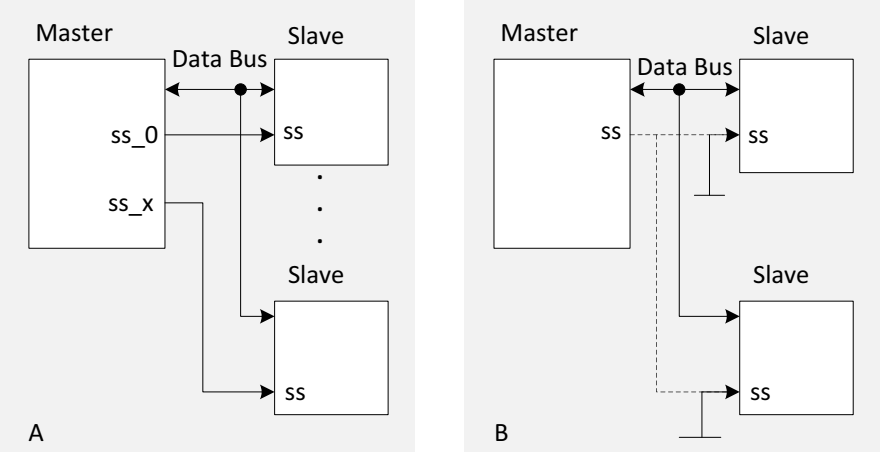
The LS1024A SPI interface can connect to any serial slave peripheral device that supports Motorola Serial Peripheral Interface – a four-wire, full-duplex, serial protocol. There are four possible combinations for the serial clock's phase and polarity. The clock phase (SCPH) determines whether the serial transfer begins with the falling edge of the slave select signal or the first edge of the serial clock. The slave select line is held high when the SPI interface is idle or disabled. Figure 9-1 presents a high-level block diagram of the LS1024A SPI Interface.

Figure 9-1 SPI Block Diagram



The LS1024A SPI interface allows for serial slave to be selected/addressed using either hardware or software. When implemented in hardware, serial slaves are selected under the control of dedicated hardware select lines. The number of select lines generated from the serial master is equal to the number of serial slaves present on the bus. The serial master device asserts the select line of the target serial slave before data transfer begins. This architecture is illustrated in Figure 9-2 A.

Figure 9-2 Hardware/Software Slave Selection



ss = slave select line

When implemented in software, the input select line of each serial slave can either originate for a single slave select output pin on the serial master (user must configure the master to have one slave select output) or be permanently grounded. The main program in the software domain controls the selection of the target slave device. This architecture is illustrated in Figure 9-2 B. The LS1024A SPI interface does not enforce hardware or software control, the user can configure the interface for either implementation.

9.3.1 Serial Peripheral Interface

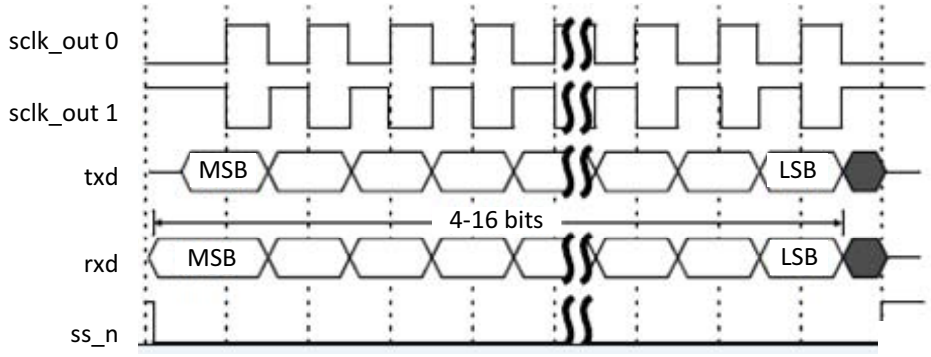
With SPI, the clock polarity (SCPOL) determines whether the inactive state of the serial clock is high or low. To transmit data, both SPI peripherals must have identical SCPH and SCPOL values. The data frame can be 4 to 16 bits in length.

When the SCPH = 0, data transmission begins on the falling edge of the slave select signal. The first data bit is captured by the master and slave peripherals on the first edge of the serial clock, therefore, valid data must be present on the txd and rxd lines prior to the first serial clock edge. Figure 9-3 shows a timing diagram for a single SPI data transfer with SCPH = 0. The serial clock is shown for SCPOL = 0 and SCPOL = 1.

The following signals are illustrated in the timing diagrams in this section:

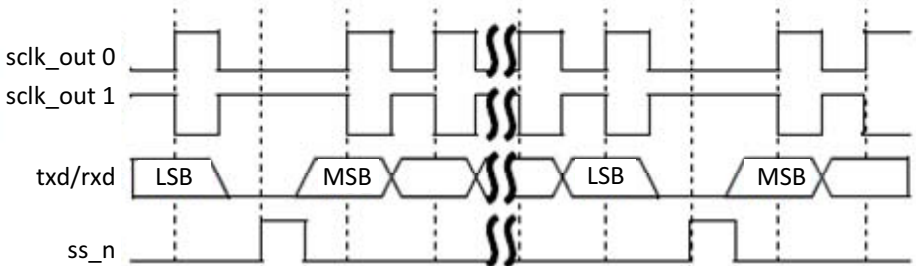
- sclk_out — serial clock from SPI interface master
- ss_n — slave select signal from SPI interface master
- txd — transmit data line for the SPI interface master/slave
- rxd — receive data line for the SPI interface master/slave

Figure 9-3 SPI Serial Format (SCPH = 0)



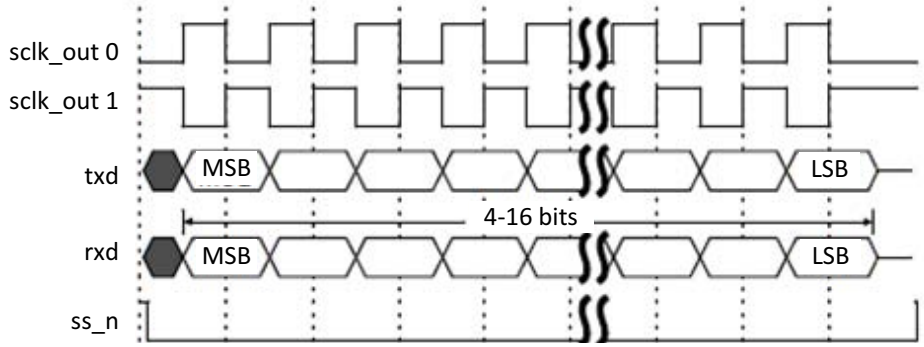
As data transmission starts on the falling edge of the slave select signal when SCPH = 0, continuous data transfers require the slave select signal to toggle before beginning the next data frame. This is illustrated in Figure 9-4.

Figure 9-4 SPI Serial Format Continuous Transfers (SCPH = 0)



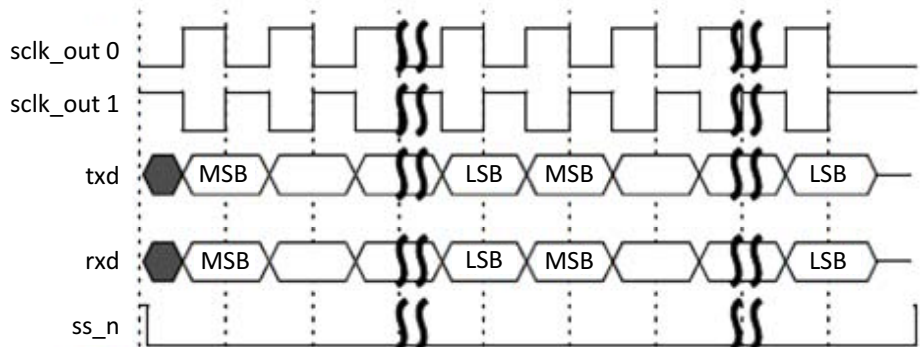
When SCPH = 1, both master and slave peripherals begin transmitting data on the first serial clock edge after the slave select line is activated. The first data bit is captured on the second serial clock edge. During continuous data frame transfers, the slave select line may be held active low until the last bit of the last frame has been captured. Figure 9-5 shows the timing diagram for the SPI format when SCPH = 1.

Figure 9-5 SPI Serial Format (SCPH = 1)



Continuous data frames are transferred in the same as single frames, with the MSB of the next frame following directly after the least significant bit (LSB) of the current frame. The slave-select signal is held active for the duration of the transfer. Figure 9-6 shows the timing diagram for continuous SPI transfers when SCPH=1.

Figure 9-6 SPI Serial Format Continuous Transfer (SCPH = 1)



9.4 Timing Parameters

Figure 9-7 shows the timing diagram of SPI interface.

Figure 9-7 LS-SPI Timing Diagram

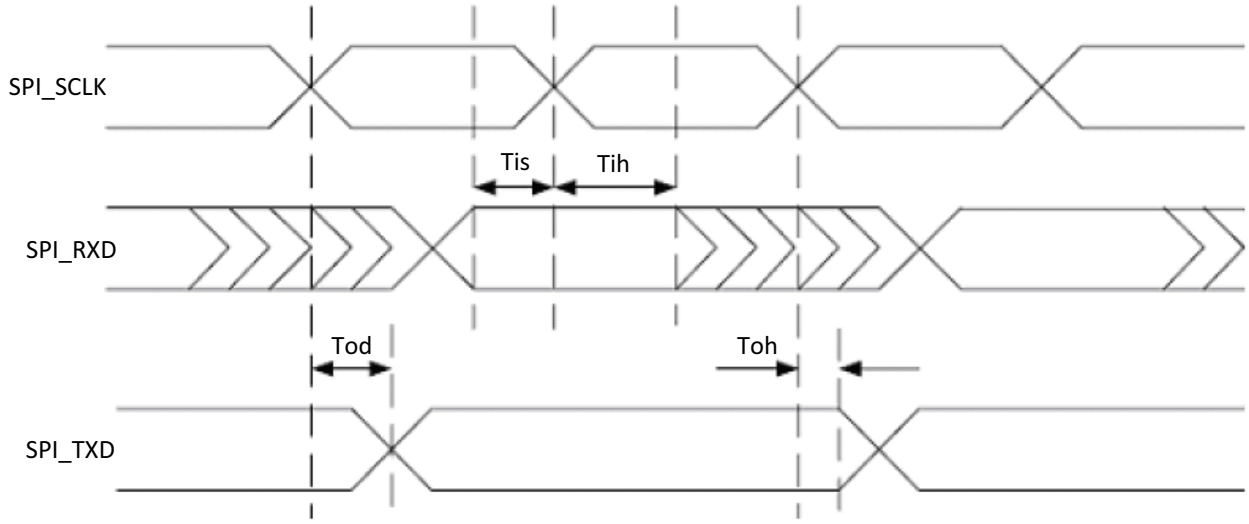


Table 9-1 lists the timing parameters of LS-SPI interface.

Table 9-1 LS-SPI Timing Parameters

Symbol	Parameter	Min.	Max.	Units	Notes
	Clock edge rate (all clocks)	0.25	2	V/ns	5
	SPI_SCLK Frequency		16	MHz	
			14	MHz	3,6
	Clock Duty Cycle (all clocks)	40	60	%	

Table 9-1 LS-SPI Timing Parameters (continued)

Symbol	Parameter	Min.	Max.	Units	Notes
Tis	Input Setup Time	11		ns	1
		12.5			3,6
Tih	Input Hold Time	2		ns	1
Tod	Output Delay Time		5	ns	1,2,3
Toh	Output Hold Time	-5		ns	1,2,4

NOTES:
1. Input can be referenced to either rising or falling edge of the clock. Output is always referenced to the opposite edge than that of the input.
2. SPI_SS# signals are configured when output clock is not active, thus have no AC requirements. In STA we need to verify that its output delay is ±5ns of delay of other output signals.
3. Max load is 50 pF.
4. Min load is 5 pF.
5. Values guaranteed by characterization; not 100% tested in production.
6. The maximum frequency is lower frequency than 16 MHz when max load is used.
7. In order to use the interface at max frequency with max load, the IO pads should be configured to max driving strength (i.e. x4).

NOTE: For details about Low Speed SPI signals, refer to "Low Speed SPI Signals" on page 29.

10 Timer

This section describes the LS1024A timer capabilities and features.

10.1 Introduction

The LS1024A timer block includes six Pulse Width Modulation (PWM) timers that can be used to drive external LEDs. It includes six general purpose timers, each of which can generate an interrupt when the upper limit is reached. Two of the general purpose timers can link to I/O pins and either drive an external output or allow external signals to increment the timer. This block also contains TDM frame sync timer and a watchdog timer.

10.2 Features

- General Purpose Timers
  - Six 32-bit timers (timer0, timer1, timer2, timer3, timer4, timer5) are used to provide interrupts.
  - Six interrupts, one interrupt per timer.
  - A secondary interrupt status register to indicate which of the timers had issued a pulse.
  - Timer3 drives TIM_EVNT0 and timer5 drives TIM_EVNT1 when these pins are configured as outputs. When a timer reaches its high bound value, the corresponding pin is switched.
  - Timer1 counts the changes on TIM_EVNT0 and timer4 counts changes on TIM_EVNT1 when these pins are configured as inputs.
  - A timer2 control register can be programmed to chain timer0 and timer2 together.
  - A timer3 control register can be programmed to chain timer1 and timer3 together.
  - A timer5 control register can be programmed to chain timer4 and timer5 together.
  - Timer2, timer3 and timer5 have programmable low and high bound registers.
  - Timer0, timer1 and timer4 can be written with specific values if needed.
- TDM Frame Sync Timers
  - One 16-bit TDM timer driven by TDM frame sync timing, providing glitch-less pulses to the interrupt controller.
  - One TDM timer interrupt can be programmed from one or more of the two timer pulses.
  - A secondary TDM timer interrupt status register to indicate which of the timers had issued a pulse.
- Watch Dog Timer
  - One 32-bit watch dog timer driven by hclk, providing glitch-less level hard reset to reset the device.
- PWM Timers
  - Six timers

10.3 Functional Description

There are six general-purpose timers in the timer block. Each timer consists of two sections, a high/low bound register and a count-up counter. Every time the high or the low bound registers are configured, the counter is reloaded with the low bound value. Therefore, it is recommended to first configure the high bound register and then the low bound register. In normal mode, the general purpose counters increment on every rising edge of hclk. Once

the counter reaches the high bound value, it asserts the interrupt if the interrupt is enabled and is reloaded with the low bound value again.

The TDM Frame SYNC counters can be configured to count RX Frame SYNC or TX frame SYNC. In normal mode, the TDM timers increment on rising edge of HCLK only when TDM Frame Sync is high.

For TIM_EVENT mode, refer to Table 10-1 and Table 10-2.

In chained mode, timer2 increments when timer0 times out, timer3 increments when timer1 times out, timer5 increments when timer4 times out. An interrupt is asserted when timer2, timer3 or timer5 times out.

10.3.1 PWM Module

The PWM module generates up-to 6 PWM events. Each event has independent configurable period and duty cycle. These events can be used to control the brightness of an LED. For LEDs:

- The output frequency should be between 300 Hz (so human eye will not notice the flickering) to 1 MHz (to minimize inductor noise)
- Minimum duty cycle that is supported by driver circuitry is approximately 1µsec

A global clock divider divides the APB clock. When enabled (setting bit 31 at offset 0x00), the divider generates a pulse whenever its value equals the configurable value (bits 7:0 at offset 0x00) and then it restarts itself. That is, starts counting from 0.

The PWM counters are incremented whenever the clock divider pulse is being generated. When PWM counter reaches the maximum configurable value it resets itself to zero (also happens if clock divider or specific PWM registers are written).

The PWM event is set to '1' when timer is enabled and timer value equals the Low Duty Cycle value. It is set to '0' when the counter wraps around to zero (if reaches maximum value or configuration was written) or if timer is disabled.

NOTE: Take into account that counters are 0-base. For example, if MAX=0d32 and Low DutyCycle=0d16, then the real duty cycle is not 50% but ((16+1)/(32+1))=51.52%

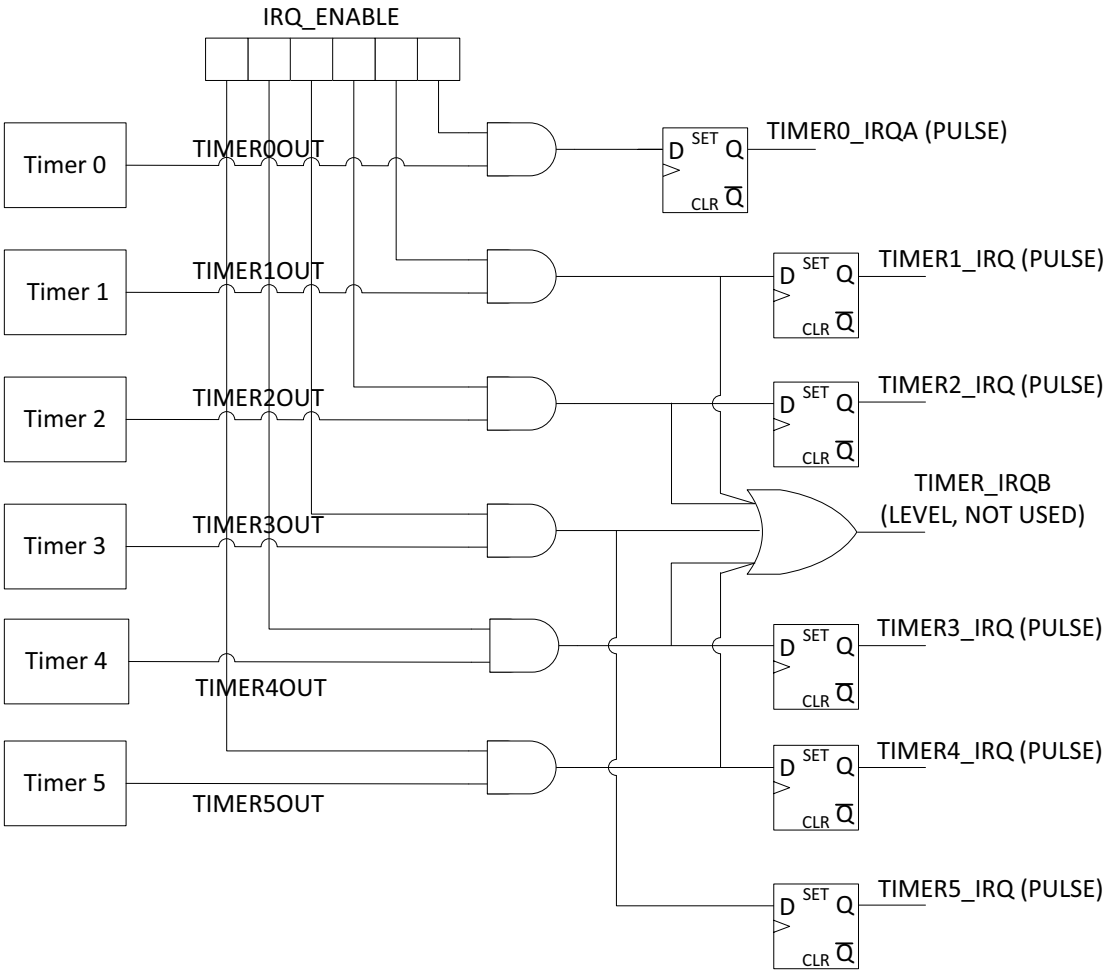
PWM Period = AHB Clock Period * (Clock Divider + 1) * (Max Value + 1)

PWM low DC = (Low Value + 1) / (Max Value + 1)

10.3.2 Interrupt Generation

As shown in Figure 10-1, the IRQ mask registers are used to selectively enable the timeout pulses to generate the IRQA and timers 1 to 5 IRQ interrupts. An Interrupt status register in the timer block can be read to check which of the timers had generated a timeout. This information can also be read from the interrupt controller, since all timers IRQ are being output.

Figure 10-1 General Purpose Timer Top-level Block Diagram



10.3.3 Counting or Driving TIM_EVNT0 and TIM_EVNT1

These two pins can be either input or output, depending on the configuration. Table 10-1 and Table 10-2 describe the behavior of timers.

Table 10-1 Counting / Driving TIM_EVNT0

Pin	Chain-mode	Non chain-mode
TIM_EVNT0 is input and is not ignored in the timer block	Timer1 counts rising or falling edge on TIM_EVNT0. Timer 3 is clocked by timer1's timeout.	Timer1 counts rising or falling edge on TIM_EVNT0. Timer3 is clocked by HCLK.
TIM_EVNT0 is output	Timer3 is clocked by timer1's timeout. TIM_EVNT0 is toggled by timer3's timeout.	Timer3 is clocked by HCLK. TIM_EVNT0 is toggled by timer3's timeout. Timer1 counts with HCLK and does not affect TIM_EVNT0.

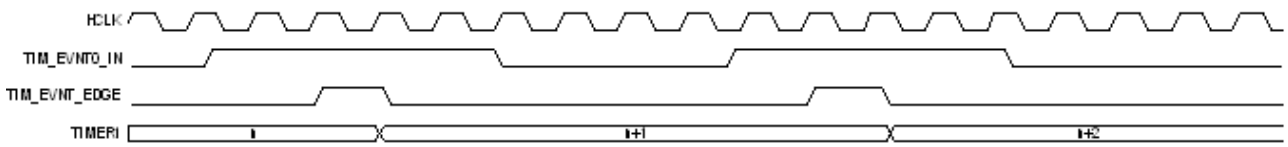
Table 10-2 Counting / Driving TIM_EVNT1

Pin	Chain-mode	Non chain-mode
TIM_EVNT1 is input and is not ignored in the timer block	Timer4 counts rising or falling edge on TIM_EVNT1. Timer 5 is clocked by Timer4's timeout	Timer4 counts rising or falling edge on TIM_EVNT1. Timer5 is clocked by HCLK.
TIM_EVNT1 is output	Timer5 is clocked by Timer4's timeout. TIM_EVNT1 is toggled by timer5's timeout.	Timer5 is clocked by HCLK. TIM_EVNT1 is toggled by Timer5's timeout. Timer4 counts with HCLK and does not affect TIM_EVNT1.

When TIM_EVNT0 or TIM_EVNT1 is configured as input and the timer block is configured to count the changes on these pins, the input first goes through two rising edge flip-flops for synchronization purpose and then it goes through an edge detection circuit. The output of the edge detection circuit increments the timer. An example of counting TIM_EVNT0 rising edge is shown in Figure 10-2.

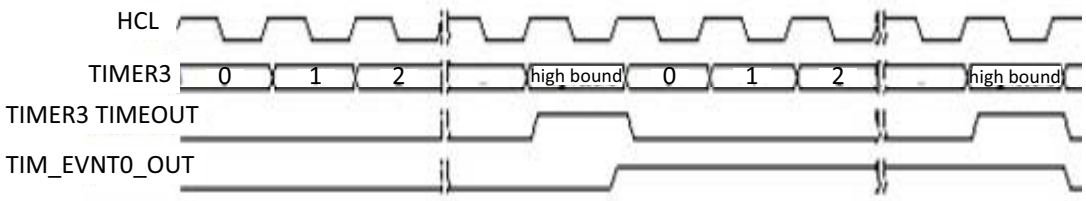
NOTE: In order for the timer to catch the rising or falling edge on TIM_EVNT0 or TIM_EVNT1, TIM_EVNT0 or TIM_EVNT1 has to stay high or low for at least 1 HCLK cycle plus 3 ns.

Figure 10-2 TIM_EVNT0 as Input



When TIM_EVNT0 or TIM_EVNT1 is configured as output, it toggles when the corresponding timer reaches its high bound value. An example of driving TIM_EVNT0 is shown in Figure 10-3.

Figure 10-3 TIM_EVNT0 as Output



11 One Time Programmable Memory

This section describes the One Time Programmable (OTP) features and functions.

11.1 Features

- 8K bits
- Readable by software
- First 8 bits are used for secure mode
- One-time writable by software (different bits can be written at different time)
- The memory supports the "Write Security Lock" feature as documented in the Test Methodology Design Guide document. Once "Security Lock" is programmed, the OTP memory becomes permanently "read only".
- Internal charge pumps generate the necessary program voltages.
- Data bus interface (density dependent)
  - Program: x1 bit
  - Read: x8 bits
- Memory array "0" by default; only need to program the "1" bits
- High reliability: Data retention: >10 years
- Redundancy built-in
  - Each addressable bit has 2 bits logically ORed.

11.2 Functional Description

The initial value of OTP memory is all zeroes. Only addresses that require a value of one need to be programmed. Voltages required to program the OTP are generated internally with charge pumps. External Vpp voltages are not required to program the OTP memory.

The memory can be programmed, read, or be placed in standby mode for low power applications.

The OTP can be controlled by configuring registers that controls the block interface. The block provides write protection logic to avoid accidental programming of the memory. Programming is performed 1 bit at a time while read operations output 8 bits at a time.

11.2.1 OTP IP I/O Description

Table 11-1lists the OTP Block I/O description. These signals are all available through registers.

Table 11-1 OTP Block I/O Description

Pin Name	Type	Description
A[13:0]	Input	These address pins are divided into several groups (row address, column address, etc) according to the block size and bit map. A[13] is used for Test Mode.
CEB	Input	CEB (active low) enables to control power and should be used for block selection. When CEB is high, the module is in standby mode.

Table 11-1 OTP Block I/O Description (continued)

CLE	Input	CLE (active high) enables test mode command entry. User can write to the test mode command registers using test mode command sequence. Please refer to Application Note.
DLE	Input	DLE (active high) enables data input buffers and allows program data patterns to be written into these buffers. This signal is combined with others during program mode.
PGMEN	Input	PGMEN (active high) is needed to enable the high voltage circuit on chip for programming. Please refer to program command sequence for correct waveforms.
READEN	Input	READEN (active high) must be high during read mode and low during program mode.
RSTB	Input	RSTB (active low) will reset all test command registers and data input buffers. This pin must be toggled before any test mode entry and toggled to clear the old setting and old data before entering the normal program mode or normal read mode. RSTB is required for when CEB is selected.
WEB	Input	WEB (active low) is a negative pulse, which allows the device to perform a command sequence and program data sequence in test mode and programming mode respectively.
CPUMPEN	Input	CPUMPEN (active high) enables the charge pump during internal charge pump programming mode. CPUMPEN allows VPP to pass through during external VPP programming mode. CPUMPEN must remain low in read mode.
DIN	Input	The 1-bit program data bus interface
D[7:0]	Output	The 8-bit read data bus interface
LOCK	Output	LOCK output is normally low indicating the OTP memory can be accessed for both read and program operations. Once "Security Lock" is programmed, the LOCK output will be "1" and the OTP memory becomes permanently "read only" memory.

11.2.2 Clocks

OTP logic uses only AXI CLK.

11.2.3 Reset

OTP logic uses an active low reset that is synchronized to AXI CLK. The synchronization is done outside the OTP block. The OTP logic has a dedicated reset to take the block out of the reset mode before the rest of the chip.

11.2.4 Write Protection

To avoid an accidental programming of the memory, the block has two lock registers that are written with a specific value and in a specific sequence to enable a write to the CEB signal register. When the CEB input is high, registers cannot be modified as the memory is in standby mode.

11.2.5 Hardware Secure Mode

After reset, software performs a read from the 1st address of the OTP in order to know if a secure boot is required.

The value of the 1st read will be output on the Hardware Secure Mode Field, o_mem_addr0_data output. Its value depends on ‘ secure_val_sel input.

- If '0' then value of 'o_mem_addr0_data' is all zeroes regardless of value read from OTP
- If '1' then default value 'o_mem_addr0_data' is all ones

Once the read is done, the value at address 0 of the OTP is locked into ‘o_mem_addr0_data’ and the corresponding valid bit is asserted. Future reads will not change the output value. Software uses this value to decide if the device is in secure mode or not.See Section 31.1.3, Secure Boot Settings .

NOTE: For more details on OTP read/write access and programming algorithms, see OTP Application Note.

12 PCI Express Interface

This section describes the PCIe Controller capabilities and features.

12.1 Introduction

The LS1024A device includes two PCI Express (PCIe) interface controllers, each of which supports a single lane. The PCIe interfaces are compatible with the PCIe Base Specification rev 2.1. There are three SerDes, which are shared between the (2 PCIe, 2 SATA, 1 SGMII) and only 3 can be active at any one time.

12.2 Features

The Peripheral Component Interface Express Controller provides the following features:

- Supports internal sourced reference clock, as well as external reference clock. See Section 7.3.2, Reference Clocks.
- Two independent ports, single lane
- Compliant with “PCI Express Base 2.1 Specification”
- Support Gen1 (2.5 G) and Gen2 (5 G)
- Hotplug support
- Configurable for root port or endpoint
- One AXI master interface (data and control) and two AXI slave interfaces (for direct access and for configuration)
- PCIe max payload size supported is 4 KB
- Outbound requests - max payload size is 128 B (8 B bus width * 16 max burst length)
- Inbound requests - max payload size is 4096 B
- Remote max read request size is 512 B
- ECRC generation and checking
- Supports MSI and Legacy interrupts
- 6 Configurable BAR filtering, I/O filtering, configuration filtering and Completion lookup/timeout
- Includes PCI Power Management
- Supports Windowing mode where remote device initiates write and read operations from LS1024A internal address space
- Direct memory-mapped mode through AXI slave interface for direct read or write of remote devices
- Internal address translation unit (not related to the PCI-SIG ATS specification) with 8 entries (regions) for inbound traffic and 8 for outbound. Region's type (for example IO/MEM/CFG) is configurable.
- Differential clock generation for off-chip use, compliant to the PCIe requirements (and specifically jitter requirements).

  Note: Use external reference clock source for PCIe Gen2 applications.

NOTE:	It is recommended to use an external reference clock source for PCIe Gen2 applications, and internal reference clock source for PCIe Gen1 applications.

12.3 PCI Express Electrical Specifications

Table 12-1 and Table 12-2 show the RX and TX electrical specifications. Table 12-3 shows the External Reference Input Clock Requirements.Table 12-4 and Table 12-5 show the SerDes TX and RX Specifications. Table 12-6 shows the Reference Clock Output Specifications.

Table 12-1 PCIe RX Electrical Specifications

Parameter	Conditions	Min	Typ	Max	Unit
Differential Input Peak to Peak Voltage		50		2000	mV_{diffpp}
Input transition time		0.15		0.40	UI
Differential DC return loss		18			dB
Differential AC return loss (standard specific)		8		16	dB
Common mode DC return loss		12			dB
Common mode AC return loss (standard specific)		6		22	dB
DC input differential termination		90		110	Ω
DC input common mode termination		22.5		27.5	Ω
Power down DC input impedance		200			kΩ
Input common mode AC voltage peak-peak				300	mV
Input common mode frequency		2		200	MHz
Jitter Tolerance (TJ) (standard specific)	LPF: F-3 dB=1.5 MHz (Gen1), n/a (Gen2)			0.6	UIpp

Table 12-2 PCIe TX Electrical Specifications

Parameter	Conditions	Min	Typ	Max	Unit
Differential Output Peak to Peak Voltage		150		1200	mV_{diffpp}
20-80% Rise/Fall Time		30		110	ps
Differential DC return loss		15			dB
Differential AC return loss (1GHz-6GHz)		6		13	dB
Common mode DC return loss		12			dB
Common mode AC return loss (standard specific)		5		13	dB
DC output differential termination		90		110	Ω
DC output common mode termination		22.5		27.5	Ω
Programmable coarse de-emphasis			-3.5 ± 3.5		dB
Fine de-emphasis			0.5		dB
Precursor (N+1)			-14		dB
Postcursor (N-1)			-4.4		dB
Total Jitter (TJ) (standard specific)	LPF: F-3 dB=1.5 MHz (Gen1), Step BPF: 10 kHz - 1.5 MHz (Gen2)			0.25	UIpp

Table 12-3 External Reference Input Clock Requirements

Parameter	Description	Min	Typ	Max	Unit
Frequency	Reference clock operating frequency range		100		MHz
RCUI	Reference clock unit interval				ns
Duty Cycle	Duty Cycle	40	50	60	%
T_R/T_F	Rise and falling edge rate		0.2	0.25	RCUI
Skew	Skew between REFCLKP and REFCLKM			0.05	RCUI
FT	Frequency tolerance	-300		300	ppm
Z_{C-DC}	Clock source output DC impedance	40		60	Ω
V_{DIFF}	LVDS Differential Voltage	250		400	mV
V_{CM}	LVDS	1		1.4	V

Table 12-4 SerDes TX Electrical Specifications

Parameter	Conditions	Min	Typ	Max	Unit
Differential Output Peak to Peak Voltage		150		1200	mV_{diffpp}
20-80% Rise/Fall Time		30		110	ps
Differential DC return loss		15			dB
Differential AC return loss (1GHz- 6GHz)		6		13	dB
Common mode DC return loss		12			dB
Common mode AC return loss (standard specific)		5		13	dB
DC output differential termination		90		110	
DC output common mode termination		22.5		27.5	
Programmable coarse deemphasis			-3.5 ± 3.5		dB
Fine de-emphasis			0.5		dB
Precursor (N+1)			-14		dB
Postcursor (N-1)			-4.4		dB

Table 12-4 SerDes TX Electrical Specifications (continued)

Parameter	Conditions	Min	Typ	Max	Unit
Total Jitter (TJ) (standard specific)	LPF: Fbaud/1667			data rate dependent	ps_{p-p}
Random Jitter (RJ) (standard specific)	LPF: Fbaud/1667			data rate dependent	ps_{p-p}
Deterministic Jitter (DJ) (standard specific)	LPF: Fbaud/1667			data rate dependent	ps_{p-p}

Table 12-5 SerDes RX Electrical Specifications

Parameter	Conditions	Min	Typ	Max	Unit
Differential Input Peak to Peak Voltage		50		2000	mV_{diffpp}
Input transition time		0.15		0.40	UI
Differential DC return loss		18			dB
Differential AC return loss (standard specific)		8		16	dB
Common mode DC return loss		12			dB
Common mode AC return loss (standard specific)		6		22	dB
DC input differential termination		90		110	Ω
DC input common mode termination		22.5		27.5	Ω
Power down DC input impedance		200			kΩ
Input common mode AC voltage peak-peak				300	mV
Input common mode frequency		2		200	MHz
Jitter Tolerance (TJ) (standard specific)	LPF: Fbaud/1667	0.65			UIpp

In the PCIe modes (Gen1 or Gen2), the PCIe SerDes provides a differential 100 MHz reference clock output. This reference clock, if enabled, can provide spreading according to the SSC specification requirement of the PCIe standard. The 100 MHz SSC reference clock outputs are available through the pins **S#_ck_100p/m**.

The output levels are CMOS levels at the supply S#_VDDA (1.1V).

Table 12-6 lists the Reference Clock Output Specifications.

Table 12-6 100MHz SSC Reference Clock Output Specification

Description	Min	Typical	Max	Unit
Output voltage level - CMOS	0	1.1V	1.21	V
Duty Cycle	40	50	60	%

NOTE: To minimize jitter accumulation, the reference clock outputs should be routed and sourced to other devices as differential signals.

13 Dual Core SMP ARM® Cortex®-A9

This section describes the ARM Cortex features.

13.1 Overview

The LS1024A contains dual Cortex-A9 CPU (up to 1.2 GHz) with Neon and Snoop Control Unit (SCU). The Cortex-A9 processor is an ARMv7 architecture delivering 2.5 DMIPS/MHz per core. The LS1024A is capable of either SMP or AMP operation to allow full flexibility of different software architectures. 32KB of L1 instruction cache and 32 KB of L1 data cache for each core along with 256 KB of L2 cache. For added debugability and security, Coresight and Trustzone are supported.

13.2 ARM Cortex-A9 Features

The features of ARM Cortex-A9 are:

- Dual Cortex-A9 CPU with Snoop Control Unit (SCU)
- Capable of AMP or SMP configurations
- 2.50 DMIPS/MHz/core
- High efficiency, dynamic length, multi-issue superscalar, out-of-order, speculating 8-stage pipeline
- Core clock is operational at 650 MHz, 900 MHz, or 1.2 GHz
- 32 KB data and instruction L1 caches
- Speculative Read is supported
- L1 Parity check is supported (statuses are stored in GPIO)
- TLB size: 128
- Neon with floating point processing engine
- Two 64-bit AXI ports
- Generic Interrupt Controller is included in SCU with support for 64 IRQS
- Timer is included in SCU
- Accelerator Coherency Port (ACP) is supported
- Power down modes are supported including
  - Stand By
  - Power down each CPU independently or both (Power Island)

13.3 L2 Cache Features

The features of L2 Cache are:

- 256 KB
- 8 ways
- 2 AXI 64-bit buses with CPU
- Core clock frequency is half the frequency of Cortex-A9 clock

- 2 AXI 64-bit buses
- L2CC and AXI fabric clocks can be synchronous or asynchronous (selection via bootstrap)
- Address Filtering option is enabled - when enabled, port 1 is used to access specific address region and port 0 for the rest; when disabled, both ports work in round-robin fashion
- Support line and way lock down options
- Support master lock down option (where following masters are supported: CPU=000, CPU1=001, ACP=100
- Parity is supported

13.4 A9 Interrupt Controller

Table 13-1 lists the A9 interrupt controller.

Table 13-1 A9 Interrupt Controller

Bit	Interrupt			P/L[1]
0	PTP0_IRQ	Processor to Processor Interrupt (set under firmware control) – Set via register at offset 0x9C and clear at 0x98	GPIO	L
1	PTP1_IRQ		GPIO	L
2	PTP2_IRQ		GPIO	L
3	PTP3_IRQ		GPIO	L
4	HFE_0_IRQ	PPFE's HIF Interrupt Indication	PPFE	L
5	HFE_1_IRQ	PPFE's HIF No Copy Interrupt Indication	PPFE	L
6	HFE_2_IRQ	PPFE's GPT Timer Interrupt Indication	PPFE	L
7	FABRIC_IRQ	Fabric Interrupt Indication	FABRIC	L
8	A9_L1_PAR_IRQ	A9 L1 Parity Fail Interrupt Indication	GPIO	L
9	A9_PMU0_IRQ	A9 PMU CPU0 Interrupt Indication	A9	L
10	A9_PMU1_IRQ	A9 PMU CPU1 Interrupt Indication	A9	L
11	L2_IRQ	L2 Interrupt Indication	L2	L
12	EAPE_IRQ	Crypto Engine – EAPE Interrupt Indication		L
13	SPACC_IRQ	Crypto Engine – SPACC Interrupt Indication		L
14	CIE_IRQ	DPI – CIE Interrupt Indication		L
15	DEC_IRQ	DPI – DECOMP Interrupt Indication		P
16	SATA_IRQ	SATA Controller Interrupt Indication	SATAC	L
17	CSS_0_IRQ	css_gp_out[15:12] field in CSS_SYS_CFG_OUT_CNTRL register	CSS	L
18	CSS_1_IRQ		CSS	L
19	CSS_2_IRQ		CSS	L
20	CSS_3_IRQ		CSS	L
21	USB2p0_IRQ	USB2.0 Controller Interrupt Indication	USBC0	L
22	USB3p0_IRQ	USB3.0 Controller Interrupt Indication	USB3SubS	PL
23	SATA_MSI_IRQ	SATA Controller msi_req Interrupt Indication	SATAC	L
24	CSS_IRQ	CSS internal interrupt controller Indication	CSS	L

Table 13-1 A9 Interrupt Controller (continued)

Bit	Interrupt			P/L[1]
25	DUS_DMAC_IRQ	DMAC Interrupt Indication	DUS	L
26	DUS_UART0_IRQ	UART0 Interrupt Indication	DUS	L
27	DUS_UART0_IRQ UART_S2_IRQ	UART1 Interrupt Indication or LS UART Interrupt Indication[2]	DUS UARTCORE	L L
28	DUS_SPI_IRQ	HS SPI Interrupt Indication	DUS	L
29	SPI_LS_IRQ	LS SPI Interrupt Indication	SPCORE	L
30	I2C_IRQ	I2C Interrupt Indication	SPCORE	L
31	HFE_3_IRQ	PPFE's UPE Interrupt Indication	PPFE	L
32	DDRC_IRQ	DDR Interrupt Indication	DDRC	L
33	TDMA_TX_IRQ	TDM TX Buffer Interrupt Indication (no mask)	TDMA	P
34	TDMA_RX_IRQ	TDM RX Buffer Interrupt Indication (no mask)	TDMA	P
35	TDMA_RxTxErr_IRQ	RX or TX AHB Error (no mask)	TDMA	P
36	HFE_4_IRQ	PPFE's UPE Timer Interrupt Indication	PPFE	L
37	TDMA_IRQ	Interrupt Indication (result of OR between override, under-run, empty and full TDMA interrupts)	TDMA	L
38	ZDS_IRQ or MSIF_IRQ	Interrupt indication on the Le88536 external device or ProSLIC external device	ZDS MSIF	L
39	MDMA_M2IO_IRQ	DMA's MEM to I/O Interrupt Indication	MDMA	L
40	MDMA_IO2M_IRQ	DMA's I/O to MEM Interrupt Indication	MDMA	L
41	MDMA_AXIW_IRQ	AXI bus error on a write access (no mask)	MDMA	P
42	MDMA_AXIR_IRQ	AXI bus error on a read access (no mask)	MDMA	P
43	PCIe0_IRQ	PCIe 0 Controller Interrupt Indication	PCIEC	L
44	PCIe1_IRQ	PCIe 1 Controller Interrupt Indication	PCIEC	L
45	GPIO0_IRQ	General IRQ 0 also can be set by GPIO 0 change	GPIO	P/L
46	GPIO1_IRQ	General IRQ 1 also can be set by GPIO 1 change	GPIO	P/L
47	GPIO2_IRQ	General IRQ 2 also can be set by GPIO 2 change	GPIO	P/L
48	GPIO3_IRQ	General IRQ 3 also can be set by GPIO 3 change	GPIO	P/L
49	GPIO4_IRQ	General IRQ 4 also can be set by GPIO 4 change	GPIO	P/L
50	GPIO5_IRQ	General IRQ 5 also can be set by GPIO 5 change	GPIO	P/L
51	GPIO6_IRQ	General IRQ 6 also can be set by GPIO 6 change	GPIO	P/L
52	GPIO7_IRQ	General IRQ 7 also can be set by GPIO 7 change	GPIO	P/L
53	WOL_IRQ	Wakeup on LAN Interrupt Indication from all GEM	PPFE	P
54	USB3p0_PM	USB3.0 PME Interrupt Indication	USB3SubS	L
55	TIMER0_IRQ	General Purpose Timer 0 Interrupt Indication	TIM	P
56	TIMER1_IRQ	General Purpose Timer 1 Interrupt Indication	TIM	P
57	TIMER2_IRQ	General Purpose Timer 2 Interrupt Indication	TIM	P
58	TIMER3_IRQ	General Purpose Timer 3 Interrupt Indication	TIM	P

Table 13-1 A9 Interrupt Controller (continued)

Bit	Interrupt			P/L[1]
59	TIMER4_IRQ	General Purpose Timer 4 Interrupt Indication	TIM	P
60	TIMER5_IRQ	General Purpose Timer 4 Interrupt Indication	TIM	P
61	TIMER6_IRQ	TDM Fsync Timer Interrupt Indication	TIM	P
62	RTC_ALM_IRQ	RTC – ALM	RTC	P/L
63	RTC_PRI_IRQ	RTC – PRI	RTC	L

NOTE:
1. P/L indicates whether interrupt type is Pulse (P), Level (L) or both (P/L)
2. UART1 or UART_S2 is selected based on Misc Pin Select Register (bits [1:0] in GPIO block

14 AXI / AHB Cross Connect Fabric

This section describes the AXI / AHB Cross Connect Fabric of LS1024A device.

The LS1024A fabric provides a central bus through which all AXI/AHB masters access AXI/AHB/APB slaves. The main fabric is a multi-layer interconnect implementation of the AXI protocol, which is designed for high-performance, high-frequency system, where simultaneous transfers between different masters and slaves can occur.

14.1 Features

The block has the following basic functionality and features:

- Multi-master fixed system with an increased available bus bandwidth. Fixed system means that the muxing cannot be set differently by changing configuration and dynamic muxing (e.g. master uses other port of DDRC if they are available) is not available except for USB3, SATA and PCIe0 which can be configured (independently) to use DDR port 2 or 3
- Multiple layers with round-robin arbitration. All masters have dedicated layer to each slave channel. A master competes with another master only when they both access the same slave channel
- 64-bit data bus for most Master/Slaves
- Remapping address regions—The ability to remap the lower address space to either: External Boot ROM (Expansion address space), Internal Boot ROM (IBR address space) or DDR memory space (when remapping is off). The selection is done based on boot option pins and remapping enable/disable configuration
- CA9 and PPFE can access any address space
- Support for Trust Zone

The fabric also includes an AHB/AXI to APB Bus Bridge (AAB). The bridge converts AHB/AXI transfers into a suitable APB format for accessing configuration and status registers of many slave blocks.

14.2 Trust Zone

The fabric supports a trust zone feature. A trusted transaction is indicated by a master by driving zero on PROT[1] bit. Only masters that are defined as trusted masters can do trusted transactions.

The slaves have the option to be configured as trusted or not.

In case a non-trusted transaction destination is a trusted slave, the transaction is diverted to the default slave inside the fabric and does not reach the destination slave.

A Trust Zone block holds all needed configurations for master and slave blocks. A general configuration option is available to disable this feature.

The default value of the system is non-trusted mode. All masters and slaves are configured to be in non-trusted modes.

14.2.1 Feature List

- Support for trust zone for all masters.
- Support for trust zone for all AXI configuration port slaves and for DPI, DECT, DDR, Trust Zone and DUSDMA AHB configuration port slaves.

- Support for trust zone for all AAB peripherals.
- Support for fully trusted/non-trusted configuration (either the whole block is trusted or not) for ACP and PCIe AXI slaves.
- Support for partly trusted/non-trusted (1 partial section of the block) for DDR, IRAM and EXP AXI slaves with restrictions on minimum section size. Maximum size supported for the whole slave address range.
- Support to resolve aliasing access problem.
- Default setting for the system is all masters and slaves are set to non-trusted.

14.2.2 Masters

- All blocks in the device have the option to be configured as trusted or non-trusted master.
- A trusted master does only trusted transactions while non-trusted master does only non-trusted transaction.
- The control is done by driving PROT[1] of the master as ‘1’ or’0’ according to the trusted/non-trusted configuration. PROT[1] =’0’ indicates a trusted transaction while PROT[1]=’1’ indicates non-trusted transaction.

These features are implemented to all masters except the A9, which drives the PROT signals itself.

14.2.3 Slaves

- Some of the AXI slaves and some of the AHB slaves need to have the option configured to be trusted/non-trusted slaves.
- Some of the slaves are configured to be either fully trusted or fully non-trusted, while some are configured to have one region which is defined as trusted and the rest of the access region as non-trusted.

14.2.3.1 AXI Slaves

The options to be configured to either trusted or non-trusted:

- USB3 config
- PPFE config
- SPAcc config
- EspAh config
- PCIe0 config
- PCIe1 config
- SATA config
- DECT config
- ACP
- PCIe0
- PCIe1

The following slaves have one region which can be defined as trusted. The region can start from any offset but must be a continuous region. The low threshold and high threshold is configured in the trust zone block:

- DDR (2 GB max, 1 MB min).
- IRAM (64 KB max, 8 KB min)
- EXP (64 MB max, 1 MB min)

To handle the case of a non-trusted burst that starts in a non-trusted zone and can go into a trusted zone, the boundary of the trusted zone configured is expanded by 128 bytes from below. Therefore, if the low threshold is configured to address ‘X’ the effective low threshold starts at address ‘X – 128 B’. Every non-trusted transaction to addresses between ‘X – 128 B’ is also rejected.

The reason for 128 bytes is that this is the longest possible burst (8 B bus X length of 16). In case the low threshold is configured to value 0x0, the threshold is not decremented by 128.

For DDR and IRAM slaves, as the whole address range is defined as trusted or non-trusted, an aliasing issue can occur. In this case, a non-trusted access to an address above the maximum address of the slave is mapped to the aliased lower address so the non-trusted access can gain access to a zone which is defined as trusted. To overcome the problem, Hardware looks only at the address bits that consist of the maximum size of the slave (fixed for IRAM and configurable by the ‘DDR Mask’ register for DDR).

In the case of EXP block, the range of each CS is set by software and any access outside that range results in an ERROR, hence no aliasing problem.

14.2.3.2 AHB Slaves

The following slaves need to have trust zone configuration:

- DDR config
- DPI0 config
- DPI1 config
- Trust Zone
- DUSDMA config
- AAB (All clients can be configured to trusted or non-trusted)

The AAB block as a slave is defined as non-trusted slave and the blocking of the access is done in the AAB block itself.

AAB Implementation

The AAB block receives HPROT[1] requests from clients, which indicates whether the transaction is trusted or non-trusted and it blocks the PSEL if non-trusted.

The register for AAB has 33 bits implemented in hardware, however, not all bits are used.

As the write data bus is only 32 bits, these bits control the lower 32 bits of the register while the access to the register have 2 addresses. A write to the low address results in a ‘0’ to be written to the 33rd bit of the register, while a write to the high address results in a ‘1’ to be written to the 33rd bit.

Read access of the low address reads the lower 32 bits of the register, while read access of the high address reads the 33rd bit of the register.

14.2.4 Error Interrupt

All AHB masters (except DECT) pass error responses from the AHB bus to AXI in the read case. For write cases, there are two interrupts: ‘XWSLVERR’ and ‘XWDECERR’.

To know if an error occurred in the write transaction, the interrupts are captured by an interrupt status register in the Trust Zone block. Each interrupt has an enable bit to enable/disable it from generating a global interrupt to the A9.

To clear the interrupts, each pair of ‘SLV’ and ‘DEC’ error interrupts have a clear bit. This bit, which is a self clear register, writes a ‘1’ to clear itself.

15 DUSI Subsystem

This section describes the DUSI (DMAC, UART, HS-SPI and I^2S) subsystem specification of LS1024A device.

15.1 Features

15.1.1 DMA

DMA provides the following features:

- AHB-Central DMA Controller core that transfers data from/to HS SPI, UART and I^2S peripheral blocks from/to DDR or IRAM
- AHB master interface for data transfer
- AHB slave interface is used to configure the DMA and also provide a direct access to the peripheral registers
- Up to eight channels, one per source and destination pair
  - Unidirectional channels - data transfers in one direction only
  - Programmable channel priority
- Hardware handshaking interfaces for source and destination peripherals
- Enabling and disabling of individual DMA handshaking interfaces
- Programmable flow control at block transfer level

15.1.2 HS-SPI

A multi-chain SPI provides a common interface mechanism for controlling peripheral devices. For example, SLICs from multiple vendors can be controlled on the SPI Bus. The DMA was added so that the interface can work at a higher frequency than LS-SPI and support data transfer speed up to 50MHz. HS-SPI can also be used for booting provided the chip select 0 is connected to the external flash.

- Serial interface operation - Motorola SPI
- Can be controlled by the DMA unit or directly by CPU via the DMA slave port
- Support for clock rates up to 50 MHz
- Clock bit-rate - user can dynamically control the serial bit rate of the data transfer
- Data frame size (4 to 16 bits) - The frame size of each data transfer is under the control of the programmer
- Depth of transmit and receive FIFO buffers is 32 words deep. The FIFO width is fixed at 16 bits
- 2 serial slave select outputs
- Master only without multi-master support
- Includes logic to allow a programmable delay on the sample time of the rxd input signal - up-to 10 AHB clock cycles

15.1.3 UART

The LS1024A device provides two independent UART interfaces. The RX and TX signals are provided, which can be connected to an RS232 driver for standard serial port operation. The UART interfaces provide a useful console port and can also be used as a software debug port. It is recommended to connect the UART pins to standard connectors such as DB9 or RJ45 for easy access.

Each Serial Interface Port provides the following features:

- Can be controlled by the DMA unit or directly by the CPU through the DMA slave port
- Programmable character properties, such as number of data bits per character (5-8), optional parity bit (with odd or even select), number of stop bits (1, 1.5 or 2) and line break generation and detection
- DMA signaling with two programmable modes
- Transmit and receive FIFO
- Transmitter adds start, stop, parity bits to the serial data
- Programmable serial data baud rate
- Port 0 includes flow control signaling (RTS and CTS)
- Port 0 supports up to 3 Mbps throughput
- Port 0 is muxed with GPIO and by default GPIO functionality is selected

NOTE: UART1 is used as console port in U-Boot. For details about Fast UART signals, refer to "Fast UART Signals" on page 36.

15.1.4 I^2S

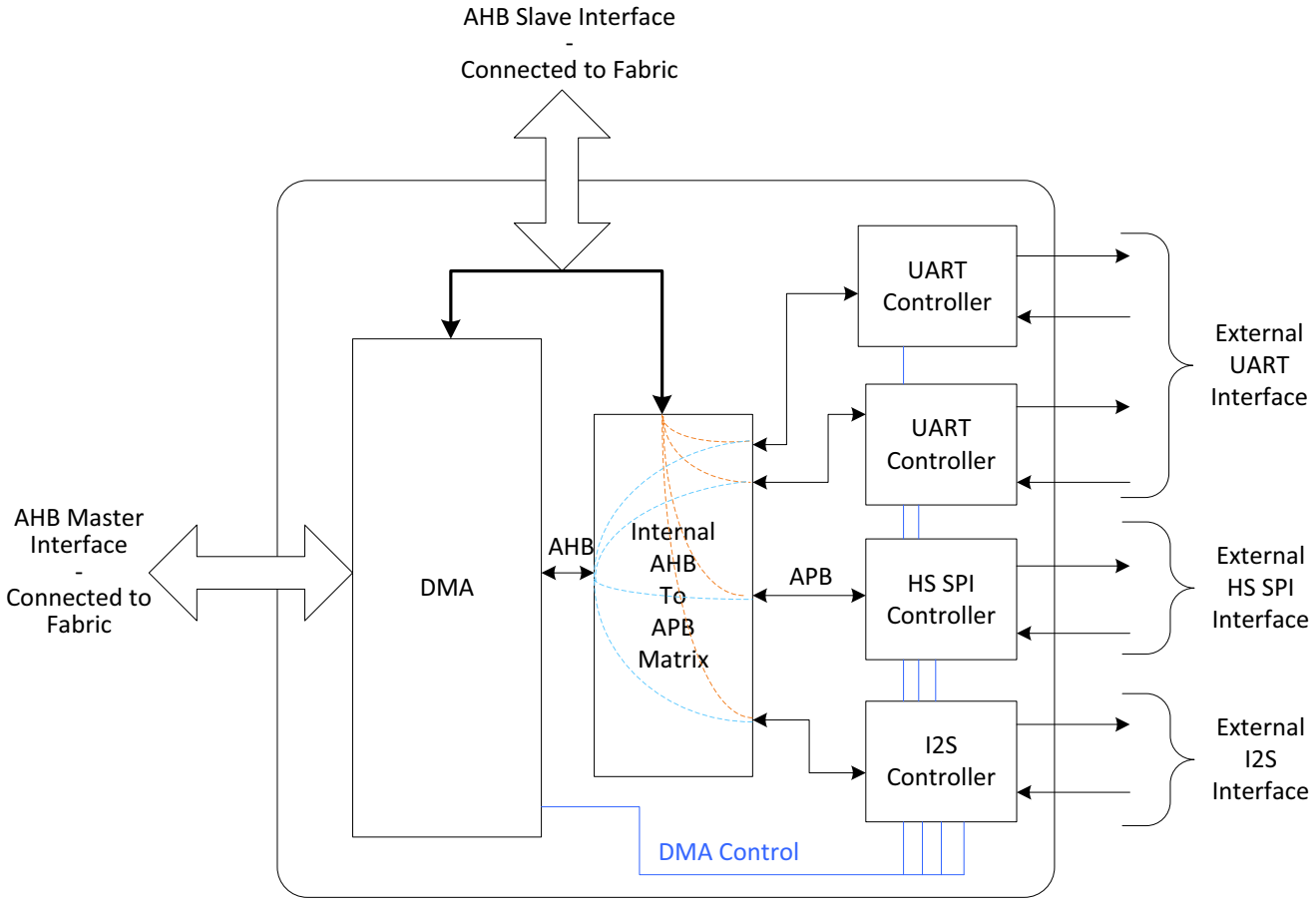
The I2S controller supports streaming serial audio data between an external I^2S Codec (ADC/DAC) and the processor. It consists of one transmitter channel and one receive channel. The transmit and the receive channels are independent of each other and can work simultaneously.

- DMA Support: Can be controlled by the DMA unit or directly by CPU via the DMA's slave port
- Controller interface can be configured to work in three modes
  - Internal Master mode: The clock source to the I^2S controller is AHB clock. The Bit clock 'I2S_BCLK' and the word select signal 'I2S_LRCLK' is generated internally from the AHB clock.
  - External Master mode: The clock source to the I^2S controller is an external Codec Clock. The Bit clock 'I2SBCLK' and the word select signal 'I2S_LRCLK' is generated internally from I2S_CODCLKI.
  - Slave Mode: The clock source to the I^2S controller is AHB clock. The Bit clock 'I2S_BCLK' and the word select signal 'I2S_LRCLK' is also supplied to the I^2S Controller from an external source.
- Word Length: 8-bit, 16-bit, 24-bit per channel
- Format: I^2S Justified, Left Justified (MSB), Right Justified (LSB)
- Transmission type: Simultaneous TX and RX, TX only, RX only
- Sampling Frequency: 8 KHz, 11.025 KHz, 16 KHz, 22.050 KHz, 32 KHz, 44.1 KHz, 48 KHz, 64 KHz, 88.2 KHz or 96 KHz
- Programmable left/right word clock polarity

15.2 DUSI Block Diagram

Figure 15-1 shows the block diagram of DUSI subsystem.

Figure 15-1 DUSI Subsystem



15.3 Functional Description

15.3.1 I²S Functional Description

The I²S Controller is very feature rich and works in slave mode, external master mode, or internal master mode (as a Transmitter or Receiver). In the Master mode, the Output Codec Clock (RCLK) to the External codec and the BCLKm is generated in the controller by dividing down the AXI clock or the input Codec clock. The Audio Channel Clock is then derived from the BCLKm in the I²S Channel Generator Block.

In the Slave Mode BCLK and LRCLK is supplied from an external master.

After the power on reset the I²S controller must be configured for I²S Access. The configuration is done by accessing I²S' APB internal interface via the DMA's AHB slave interface. As part of this process TX and RX FIFOs should be flushed before any valid I²S transactions occur. Then I2S Data is written directly via the APB interface or by the DMA block into the TX FIFO. After enabling the I²S operation, the data from TX FIFO is fetched and provided to the internal channel generator block.

The I²S Channel Generator Block uses the BITCLK to generate the Channel Clock and the Parallel to serial load transfer control signals for the TX SFTR Block. The Holding Register inside the TX SFTR holds the incoming Parallel data and passes it onto I2SSDO bit aligned with BITCLK. The Channel Clock LRCLK is also passed along with Channel Clock enable.

During the Receive phase, a change on the Channel clock is interpreted as incoming data on the I2SSDI line and is latched on the positive edge of BCLK in the RX SFTR.

With the help of BCLK and LRCLK, the Channel Generator block generates a Serial to Parallel load indication and latches the Left channel data and Right channel data. The data is then written into the RX FIFO where it is stored in subsequent locations. The data can be fetched from the FIFO by reading it via the APB interface or by the DMA block. The Channel Generator block waits for the Left Channel data and the Right Channel data and passes it onto the RX FIFO Block where it is stored in subsequent locations. Any read from the APB is provided the stored data.

15.3.1.1 IIS-Bus Format

The I^2S bus has four lines including serial data input I2SSDI, serial data output I2SSDO, left/right channel select clock I2SLRCLK, and serial bit clock I2SBCLK; the device generating I2SLRCLK and I2SBCLK is the master.

Serial data is transmitted in 2's complement with the MSB first with a fixed position, whereas the position of the LSB depends on the word length. The transmitter sends the MSB of the next word one clock period after the I2SLRCLK is changed. Serial data sent by the transmitter may be synchronized with either the trailing or the leading edge of the clock signal. However, the serial data must be latched into the receiver on the leading edge of the serial clock signal, so there are some restrictions when transmitting data that is synchronized with the leading edge.

The LR channel select line indicates the channel being transmitted. I2SLRCLK may be changed on either a trailing or leading edge of the serial clock, but it does not need to be symmetrical. In the slave, this signal is latched on the leading edge of the clock signal. The I2SLRCLK line changes one clock period before the MSB is transmitted. This allows the slave transmitter to derive synchronous timing of the serial data that is set up for transmission. Furthermore, it enables the receiver to store the previous word and clear the input for the next word.

15.3.1.1.1 MSB (LEFT) JUSTIFIED

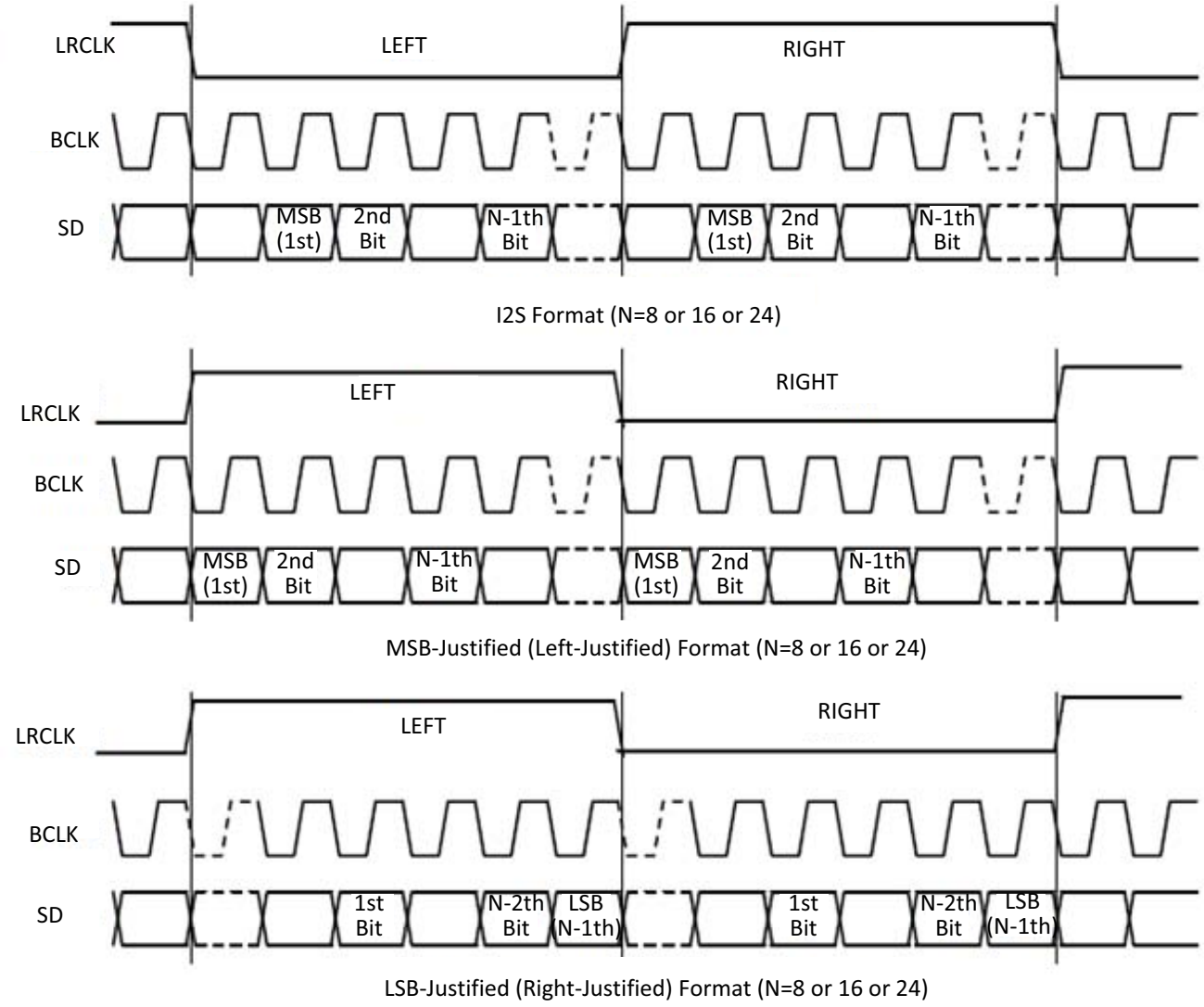
MSB-Justified (Left-Justified) format is similar to I^2S bus format, except that in MSB-justified format, the transmitter always sends the MSB of the next word at the same time whenever the I2SLRCLK is changed.

15.3.1.1.2 LSB (RIGHT) JUSTIFIED

LSB-Justified (Right-Justified) format is opposite to the MSB-justified format. In other words, the transferring serial data is aligned with ending point of I2SLRCLK transition.

Figure 15-2 shows the audio serial timing in I^2S, MSB-justified, and LSB-justified formats. Note that the word length is 16-bit and I2SLRCLK makes transition every 24 cycle of I2SBCLK (BFS is 48 fs, where fs is sampling frequency; I2SLRCLK frequency).

Figure 15-2 I2S Audio Serial Data Formats



15.3.2 HS-SPI Functional Description

The operation of HS-SPI is similar to LS SPI with the only difference that the DMA function allows faster data transfer. For more details, refer to Chapter 9, Low Speed SPI.

15.4 Timing Parameters

15.4.1 HS-SPI Timing Diagram and Parameters

Figure 15-3 shows the timing diagram of SPI interface.

Figure 15-3 SPI Timing Diagram

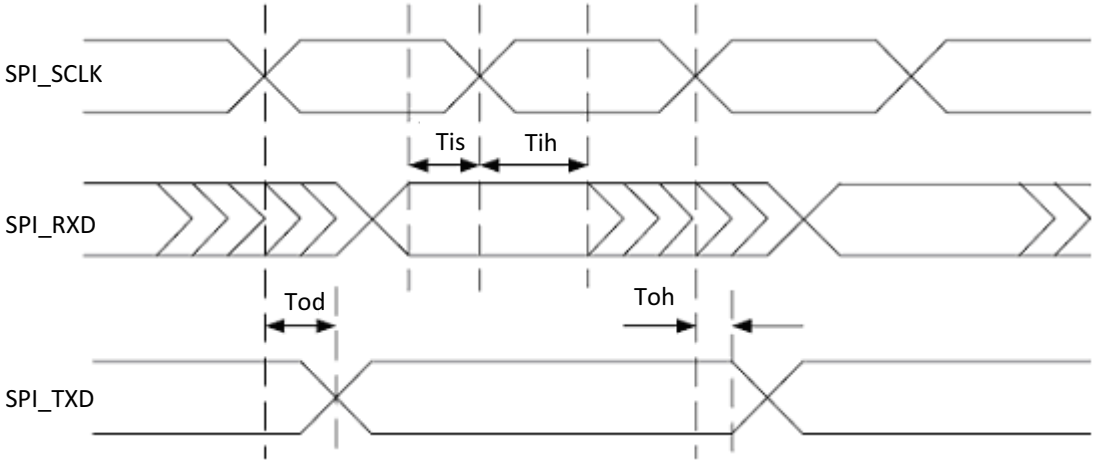


Table 15-1 lists the timing parameters of HS-SPI interface.

Table 15-1 HS-SPI Timing Parameters

Symbol	Parameter	Min.	Max.	Units	Notes
	Clock edge rate (all clocks)	0.1	2	V/ns	6
	SPI_2_SCLK Frequency All except READ instruction READ instruction		 50 50	 MHz	
	Clock Duty Cycle (all clocks)	46	53	%	
Tis	Input Setup Time	**		ns	1,5
Tih	Input Hold Time	**		ns	1,5
Tod	Output Delay Time		1.5	ns	1,2,3
Toh	Output Hold Time	-0.5		ns	1,2,4

NOTES:
1. Input can be referenced to either rising or falling edge of the clock. Output is always referenced to the opposite edge than that of the input.
2. SPI_SS# signals are configured when output clock is not active, thus have no AC requirements.
3. Max load is 15pF.
4. Min load is 5pF.
5. During board design the user needs to take into account the output delay of external device (because it is based on input clock) and the round trip delay. Logically LS1024A's SPI module allows a programmable delay on the sample time of the rxd input signal - up to 10 AHB clock cycles.
6. Values guaranteed by characterization; not 100% tested in production.
7. **A training sequence is needed to select the right delay element that should be used. In order to have reliable operation the training sequence would need to have at least 3 good sampling points so a mid point can be selected. For 250 MHz AXI clock that means a valid window of at least 13ns.

NOTE: For details about High Speed SPI signals, refer to "High Speed SPI Signals" on page 36.

15.4.2 I²S Timing Parameters

Table 15-2 describes the I²S bus timing details.

Table 15-2 I²S Bus Timing

Symbol	Parameter	Min.	Type	Max.	Units	Notes
	CODCLKI and CODCLKO edge rate	0.25		2	V/ns	3
	CODCLKI and CODCLKO Frequency		36.864	41	MHz	
	CODCLKI and CODCLKO Duty Cycle	40		60	%	
Tpcy	BCLK Frequency		4.608	5.12	MHz	
Thc, Tlc	BCLK Duty Cycle	35		65		
Tod	SDO and LRCLK output delay	-25		15		1,2,4
Tis	SDI and LRCLK input setup	25				1
Tih	SDI and LRCLK hold	0				1

NOTES:
1. SDI (and LRCLK in) is referenced to raising of the BCLK (driven at falling edge). SDO (and LRCLK out) is referenced to the falling edge of BCLK (sampled at rising edge)
2. Maximum load is 30 pF, Min load is 5 pF
3. Assuming maximum 10 ns round trip delay when external device generates BCLK
4. General: In order to use the interface at max frequency with maximum load, the I/O pads should be configured to max driving strength

NOTE: For details about I²S signals, refer to "I2S Signals" on page 36.

16 Deep Packet Inspection

This section describes the CIE and Decomp capabilities, pin list and features.

The DPI engine consists of two engines:

- Content Inspection Engine (CIE)
- Decompression Engine (Decomp)

16.1 Content Inspection Engine (CIE)

The DPI CIE Engine is a layer 7 content inspection core; supporting layer-7 applications and has become a demanding requirement for current security/ content-aware network equipment. Many such applications rely on content inspection (Deep packet inspection) to achieve their functionality such as anti-virus, IPS, traffic classification, and so on. The engine supports pattern matching for in-bound and out-bound data and utilizes patented technologies to provide excellent performance with minimal memory and signature maintenance requirements.

The CIE engine supports pattern matching of incoming data which could be in the following forms:

- Single packet/file,
- Portions of a packet/file, or
- Concatenation of several packets/files.

A list of regular expressions is used to represent the patterns to be matched. To perform pattern matching operations, the regular expressions are compiled (or translated) first and then downloaded as the inspection codes produced by the compiler into the core.

The core offloads content inspection so that system can have better performance and be more cost effective to meet stringent requirements for performance, availability and reliability in Small Office Home Office (SOHO) and Small and Medium Business (SMB). This chip provides deep packet inspection at all OSI layers, including the payload, 200 Mbps aggregate throughput.

The Deep Packet Inspection provides the following features:

- Support 64 sets of rules, each maximum of 256 K rules.
- Supports Regular expression and plain string patterns.
- Optimized for plain string patterns to reduce inspection code size (6.6 MB for 100 K).
- Can achieve 200 Mbps.
- Cross packet search with minimal overhead.
- Support 64-bit addressing.

16.2 Decompression Engine (Decomp)

The Decompression Engine is compliant with "RFC1951" and provides hardware acceleration and processor offload for examining compressed data.

The Decompression Engine provides the following features:

- Supports deflate algorithm
- Supports store, fixed Huffman or dynamic Huffman methods
- Supports decompression across input data boundary

17 PPFE (Ethernet Interface)

This section describes the Programmable Packet Forwarding Engine (PPFE) signals, capabilities, functioning, timing parameters and features.

17.1 Introduction

The LS1024A uses a Hardware packet forwarding engine to provide high performance Ethernet interfaces. The device includes three Ethernet ports: WAN, LAN and the third typically used for a DMZ port or backup WAN. All three Ethernet ports support RMII and RGMII. One port also has the option to support SGMII (1G speed only). These configurations conform to IEEE 802.3 and support full-duplex and half-duplex operation at 10/100/1000 Mbps. All ports are IEEE Standard 1588-2007 PTP V2 and 802.1AS compliant.

17.2 Features

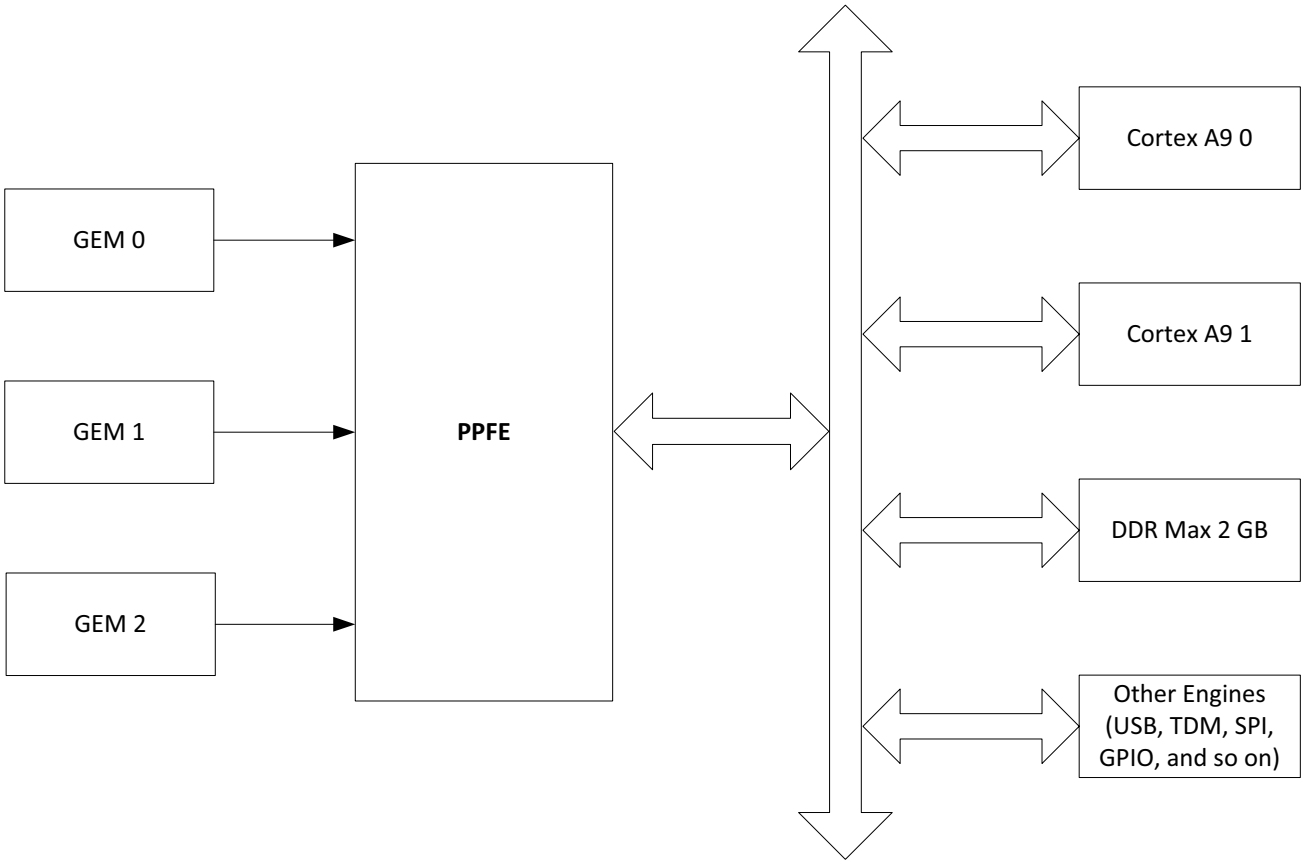
The Programmable Packet Forwarding Engine (PPFE) provides the following features:

- Performs the IEEE 802.3 protocol for 10/100/1000 Mbps (SGMII is 1000 Mbps only)
- Supports packet sizes from 64 bytes up to 10240 bytes for jumbo frames
- VLAN Packet Identification and tagging
- Address Recognition Circuit for efficient bridging. 32 specific address registers for filtering
- Capable of autonomously handling all packets belonging to a given stream, without Host CPU intervention, following stream creation
- Capable of addressing DDR, security co-processor and internal on-chip memory
- Capable of routing/bridging an aggregate of 2 Gbps of traffic, at any packet size, must support 2Gbps for IPv4/NAT and IPv6 for a singe connection
- QoS Compliant with HGI 2.0 at any packet size
- 3 independent GEMAC ports:
  - Port 0 supports RGMII/RMII
  - Port 1 supports RGMII/RMII
  - Port 2 supports RGMII/RMII/SGMII
- Includes JTAG and UART interfaces for debugging

17.3 Functional Description

Figure 17-1 illustrates the PPFE block diagram.

Figure 17-1 PPFE Block Diagram



17.4 Ethernet Interface Bus Timing

NOTE:

1. RMII was verified with 3.3 V devices and supplies.
2. RGMII was verified with 2.5 V devices and supplies.
3. MDIO works with 3.3V devices and supplies.

17.4.1 RMII Interface Timing

Figure 17-2 illustrates the RMII interface AC timing.

Figure 17-2 RMII Interface AC Timing

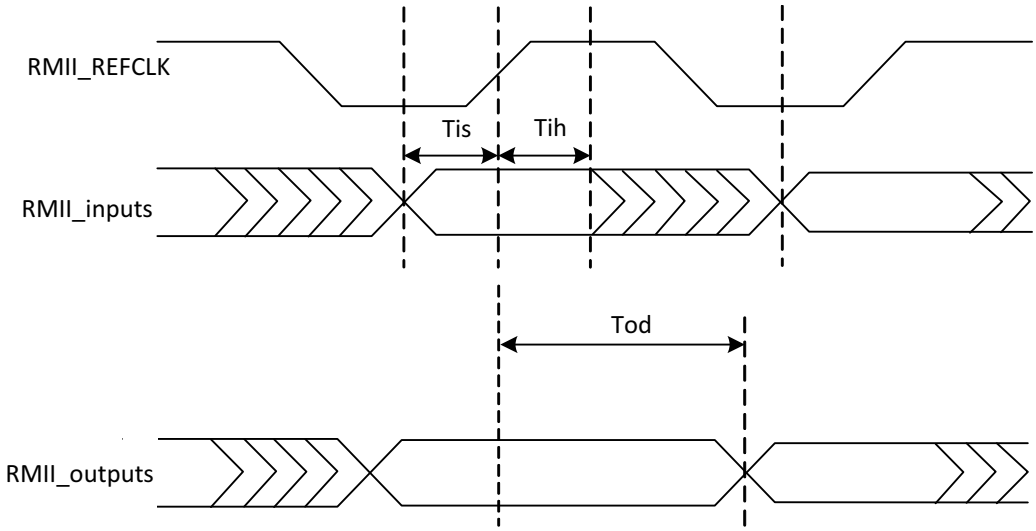


Table 17-1 lists the RMII interface AC timing parameters.

Table 17-1 RMII Interface AC Timing Parameters

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
	Rise and fall times (signals and clock)	1		5	ns	1
	RMII_REFCLK Frequency		50		MHz	
	RMII_REFCLK Accuracy	-50		50	ppm	
	RMII_REFCLK Duty Cycle	35		65	%	
Tis	Input Setup Time	4			ns	2
Tih	Input Hold Time	2			ns	2
Tod	Output Delay Time	2		14	ns	2,3

NOTES:
1. Measured between the points on the waveform, which cross 0.8 V and 2.0 V.
2. Reference to clock level of 1.4 V.
3. Output drivers shall be capable of meeting the output requirements while driving a 25 pF load.

NOTE: For details about RMII signals, refer to “RMII Mode” on page 37.

17.4.2 RGMII Interface Timing

Figure 17-3 illustrates the RGMII interface AC timing.

Figure 17-3 RGMII Interface AC Timing

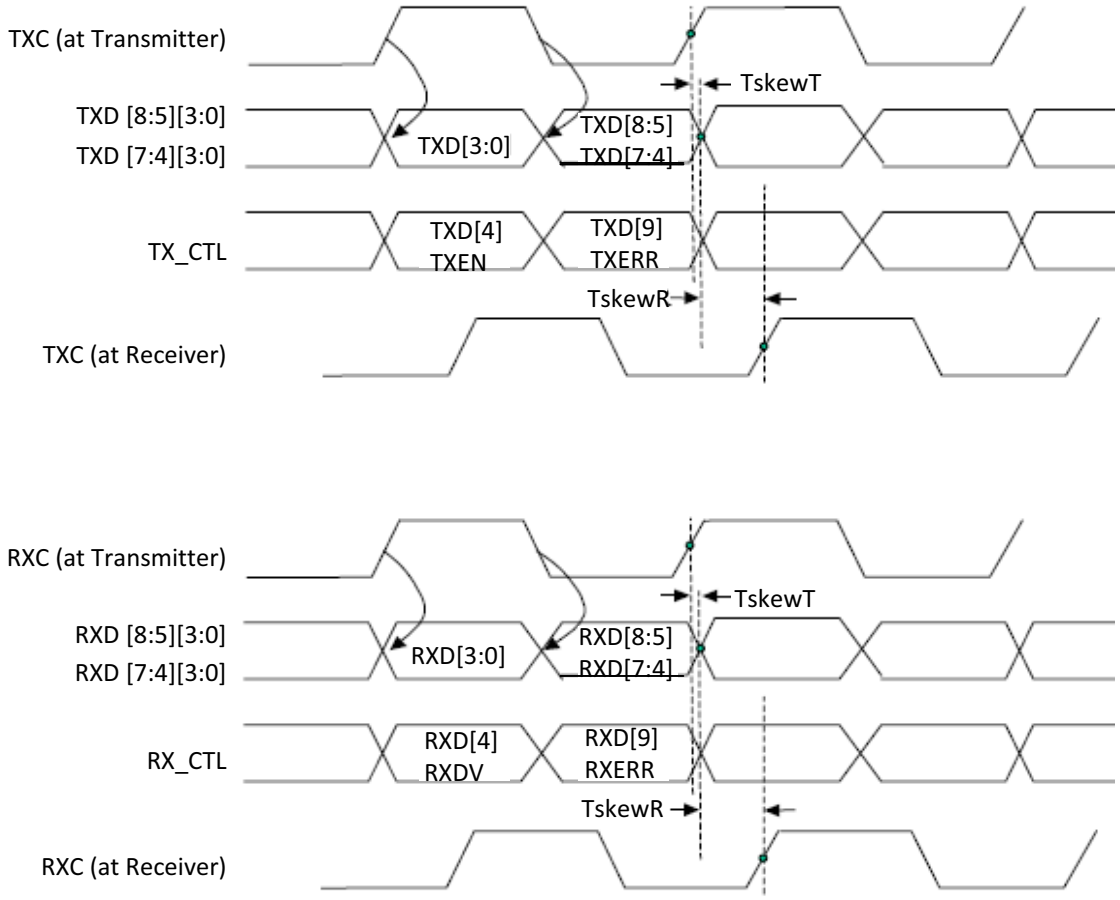


Table 17-2 lists the RGMII interface AC timing parameters.

Table 17-2 RGMII Interface AC Timing Parameters

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
TskewT	Data to Clock output Skew (at Transmitter)	-500	0	500	ps	1,2,7
TskewR	Data to Clock input Skew (at Receiver)	1		2.6	ns	1,3,7
Tcyc	Clock Cycle Duration (1000 Mbps)	7.2	8	8.8	ns	4,7
Tcyc	Clock Cycle Duration (100 Mbps)	36	40	44	ns	4,7
Tcyc	Clock Cycle Duration (10 Mbps)	360	400	440	ns	4,7
	Clock Accuracy	-50		50	ppm	7
Duty_G	Duty Cycle for Gigabit	45	50	55	%	5,6,7
Duty_T	Duty Cycle for 10/100T	40	50	60	%	5,6,7
Tr / Tf	Rise / Fall Time (20-80%)			.75	ns	7

Table 17-2 RGMII Interface AC Timing Parameters (continued)

NOTES:

1. The skew at the transmitter is specified for 15 pF clock and data loads. If the load is significantly different on the board, it is the responsibility of the board designer to characterize the output skew and to account for it. Parallel and serial terminations are required and circuit simulation is highly recommended (application note should be made available on this subject).
2. It is recommended that the PHY/switch connected over this interface includes internal clock delays (for both receive and transmit directions), in order to overcome the difference introduced between TskewT and TskewR. An alternative option of additional trace delay on the board is not recommended due to the additional load it introduces. For 10/100, the maximum value is unspecified.
3. For 10 Mbps and 100 Mbps, Tcyc will scale to 400 ns ± 40 ns and 40 ns ± 4 ns respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domain as long as minimum duty cycle is not violated and stretching occurs for no more than three Tcyc of the lowest speed transitioned between.
5. Cycle values are defined in percentages of the nominal clock period so to make this table speed independent.
6. Needs to be compliant with RGMII v1.3 (thus based upon 3.3V/2.5 V CMOS interface voltages as defined by JEDEC EIA/JESD8-5), and not compliant with RGMII v2.0 (specifically, not based upon 1.5 V HSTL interface voltages as defined by JEDEC EIA/JESD8-6).
7. Applies to cases where external delay on TXC/RXC is enabled (delay of greater than 1.5ns and less than 2.0 ns)
8. As per the test load condition specified by the RGMII v2.0 spec., in the normal board environment of 15 pF load, the maximum rise and fall time can be up to 1250 pS.

NOTE: For details about RGMII signals, refer to "RGMII Mode" on page 38.

17.4.3 SGMII Interface Timing

Table 17-3 and Table 17-4 shows the RX and TX timing parameters. Table 17-5 shows External Reference Input Clock Requirements.

Table 17-3 SGMII RX Electrical Specifications

Parameter	Conditions	Min	Typ	Max	Unit
Differential Input Peak to Peak Voltage		50		2000	mV_{diffpp}
Input transition time		0.15		0.40	UI
Differential DC return loss		18			dB
Differential AC return loss (standard specific)		8		16	dB
Common mode DC return loss		12			dB
Common mode AC return loss (standard specific)		6		22	dB
DC input differential termination		90		110	Ω
DC input common mode termination		22.5		27.5	Ω
Power down DC input impedance		200			kΩ
Input common mode AC voltage peak-peak				300	mV
Input common mode frequency		2		200	MHz
Jitter Tolerance (TJ) (standard specific)	LPF: F-3 dB=1.5 MHz (Gen1), n/a (Gen2)			0.6	UIpp

Table 17-4 SGMII TX Electrical Specifications

Parameter	Conditions	Min	Typ	Max	Unit
Differential Output Peak to Peak Voltage		150		1200	mV_{diffpp}
20-80% Rise/Fall Time		30		110	ps
Differential DC return loss		15			dB
Differential AC return loss (1GHz-6GHz)		6		13	dB
Common mode DC return loss		12			dB
Common mode AC return loss (standard specific)		5		13	dB
DC output differential termination		90		110	Ω
DC output common mode termination		22.5		27.5	Ω
Programmable coarse de-emphasis			-3.5 ± 3.5		dB
Fine de-emphasis			0.5		dB
Precursor (N+1)			-14		dB
Postcursor (N-1)			-4.4		dB
Total Jitter (TJ) (standard specific)	LPF: F-3dB=1.5MHz (Gen1), Step BPF: 10kHz - 1.5MHz (Gen2)			0.25	UIpp

Table 17-5 External Reference Input Clock Requirements

Parameter	Description	Min	Typ	Max	Unit
Frequency	Reference clock operating frequency range		125		MHz
RCUI	Reference clock unit interval		8		ns
Duty Cycle	Duty Cycle	40	50	60	%
T_R/T_F	Rise and falling edge rate		0.2	0.25	RCUI
Skew	Skew between REFCLKP and REFCLKM			0.05	RCUI
FT	Frequency tolerance	-300		300	ppm
Z_{C-DC}	Clock source output DC impedance	40		60	Ω
V_{DIFF}	LVDS Differential Voltage	250		400	mV
V_{CM}	LVDS	1		1.4	V

17.4.4 MDIO Interface Timing

Figure 17-4 illustrates the MDIO interface AC timing.

Figure 17-4 MDIO Interface AC Timing

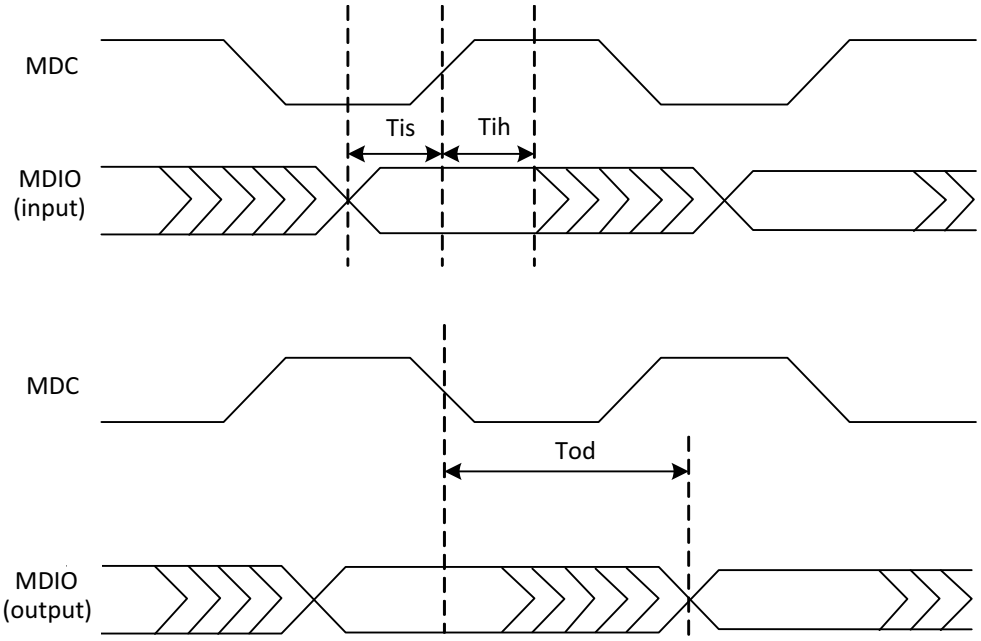


Table 17-6 lists the MDIO interface AC timing parameters.

Table 17-6 MDIO Interface AC Timing Parameters

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
	Clock edge rate (All Clocks)	0.25		2	V/ns	1
	MDC Frequency			2.5	MHz	
	MDC Duty Cycle	40		60	%	
Tis	MDIO Input Setup Time	20			ns	
Tih	MDIO Input Hold Time	0			ns	
Tod	MDIO Output Delay Time	-10		10	ns	

NOTES
The rise and fall times are determined by the edge rate in V/ns. A “Max” edge rate is the fastest rate at which a clock transitions.

18 DECT Communication Sub-System

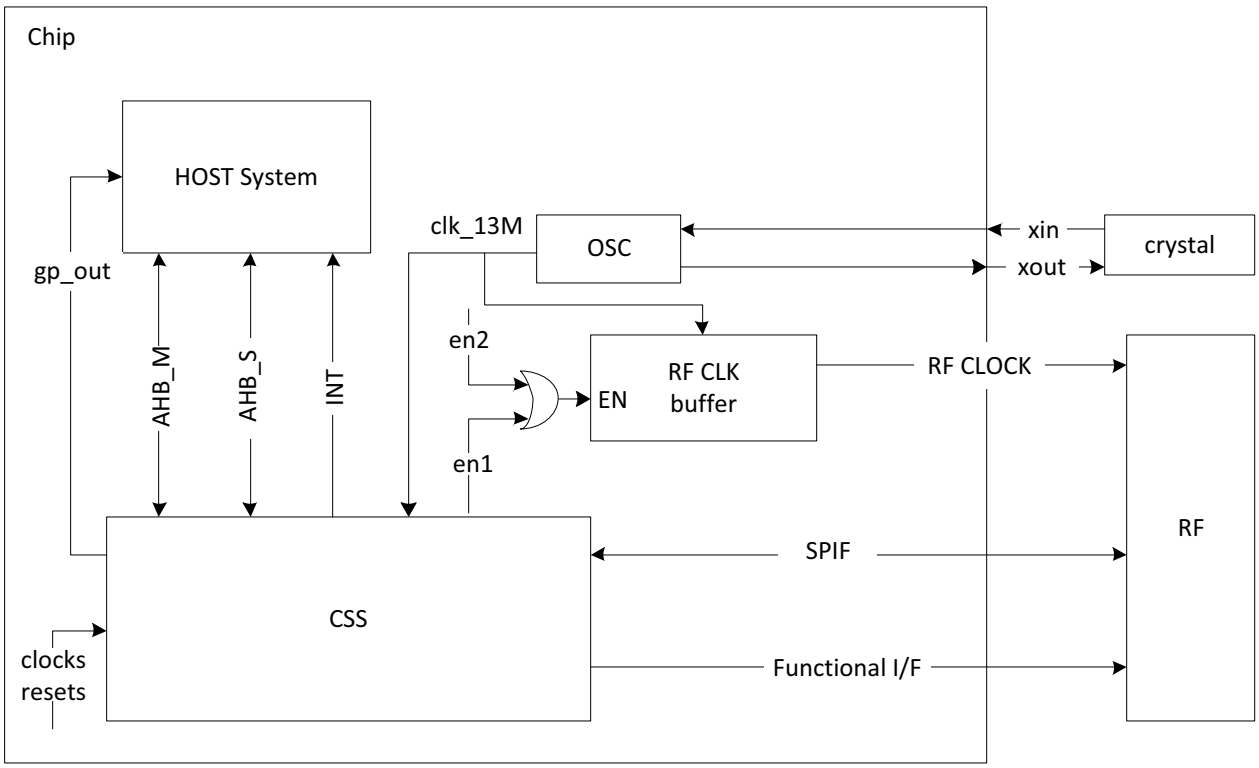
This section describes the CSS capabilities, external pin list, timing parameters and features of LS1024A device.

18.1 Introduction

The Communication Sub-System (CSS) block is the digital portion of Digital Enhanced Cordless Telecommunications (DECT) interface. The CSS block is integrated into the LS1024A DECT interface. An external RF module is needed to support DECT functionality. The CSS is CAT-iq 2.1 capable and is software upgradable for future enhancements.

Figure 18-1 illustrates the CSS block diagram.

Figure 18-1 CSS Block Diagram



18.2 Features

The CSS provide the following features:

- Full featured DECT base station
- Cat-iq 2.1 capable (Software upgradable for future enhancements)
- Minimal impact on Host CPU for DECT-side low-level support
- CSS includes memories for storing Instruction code (128 KB) and Data (32 KB)
- ARM926: 16 KB Instruction cache and 16 KB Data cache

- Includes JTAG for debugging

18.3 Timing Parameters

Table 18-1 lists the timing parameters of CSS.

Table 18-1 CSS Timing Parameters

Symbol	Parameter	Min.	Typ	Max	Units	Notes
	SCLK and BCLK Clock edge rate	0.25		2	V/ns	4,6
	SCLK and BCLK Frequency		13.824		MHz	
	SCLK and BCLK Clock Duty Cycle	40		60	%	
Tis	SDATA In Setup Time	9			ns	1,5
Tih	SDATA In Hold Time	0			ns	1,5
Tod	SDATA output Delay	-12		12	ns	1,2,3,4

- RSTN is related to internal clock and has no AC spec parameter (i.e. asynchronous)
- TR_DATA, SYM_REC_DEBUG, SYN_MATCH, RADIO_EN and SLOT_CTRL have no AC spec parameter (i.e. asynchronous)
- SEN changes while output clock is not active. Thus it does not have AC requirements.

NOTES:

1. SDATA In is referenced to falling of the SCLK (driven at rising by RF device). SDATA Out is referenced to the rising edge of SCLK (sampled at falling by RF device.
2. Max load is 30pF.
3. Min load is 5pF.
4. Values guaranteed by characterization; not 100% tested in production.
5. Max round trip delay is 5ns.
6. BCLK is used as reference clock of RF module. A weak driver is used but external component might be needed in order create a sinusoidal clock.
7. In order to use the interface at max frequency with max load, the IO pads should be configured to max driving strength (i.e. x4).

NOTE: For details about CSS signals, refer to “CSS Signals” on page 38.

19 Security Accelerator

This section describes the LS1024A Security accelerator interface.

19.1 Overview

The IPSec Engine provides cryptographic functionality. It accelerates IPSec protocol processing by combining hash and ciphering engines, a special purpose DMA engine, ESP / AH packet processing logic, and interrupt mitigation. The LS1024A hardware architecture provides direct access to the IPSec Engine's slave interface, hence supporting software control of the raw cryptographic mode.

19.2 Features

19.2.1 IPSec Features

- Data Encryption Standard Execution
  - AES, DES, and 3DES algorithms
  - ECB and CBC modes for DES and 3DES
  - CTR and CBC mode for AES (128-bit,192-bit, 256-bit)
  - AES-CBC mode cipher. 128, 192, 256 bit key sizes
  - DES-CBC mode cipher. 56 and 168 bit (3DES) key sizes
- Message digest execution
  - SHA1, SHA-256 with 160- or 256-bit message digest
  - MD5 with 128-bit message digest
  - HMAC with either algorithm
  - HMAC-MD5 mode hash
  - HMAC-SHA1 mode hash
  - HMAC-SHA256 mode hash
- Raw Hashing Mode:MD5, SHA-1, SHA-256, SHA-384, SHA-512
- AH mode processing
- ESP mode processing
- Transport mode processing
- Tunnel mode processing
- IPv4 and IPv6 processing
- Extended Sequence Numbers
- DDT based packet memory architecture
- SA bundles and nested tunnels are not handled explicitly by the hardware. They may be constructed by sequencing the same packet through the EAOE multiple times via software.
- Provides 64 entries long (per IN/OUT direction) control FIFOs holding multiple configurations to be written to IPSEC configurations registers

- Provides 64 entries long (per IN/OUT direction) status FIFOs holding multiple status reads from IPSEC status registers
- ARM interrupt mitigation
- Allows access to slave interface, in order to support software-controlled raw cryptographic mode
- IKEv 2 Support
- SNOW3G support
- Kasumi support

19.2.2 SSL Support Features

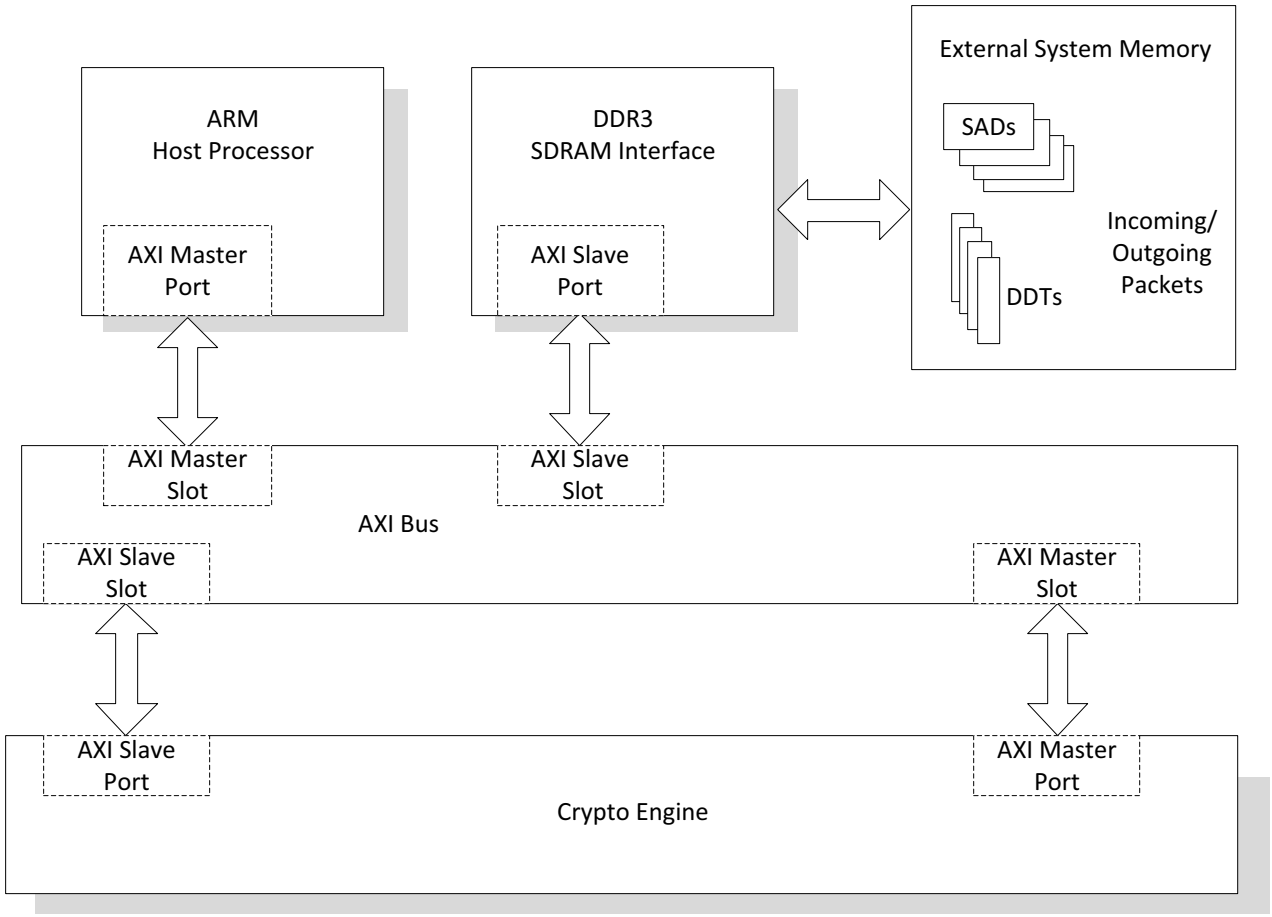
- RC4 and AES support
- Support for simultaneous sessions
- Concurrent support for SSL sessions and IPSec tunnels
- Hardware-based random-number generation
- Hardware-based public key acceleration engine
- Raw Hashing Mode: MD5, SHA-1, SHA-256, SHA-384, SHA-512

19.3 Functional Description

As shown in Figure 19-1, the IPSec Engine consists of an Offload Interface and an (ESP/AH) core. The IPSec Engine bridges the gap between raw cryptographic offload and complete IPSec offload. By combining hash and ciphering engines, a special purpose DMA engine, and ESP/AH packet processing logic, the IPSec engine allows all the mathematically intensive IPSec operations to be off-loaded from the host ARM processor. With the Offload Interface, host processor responsibilities are minimized.

Beside the ESP/AH core for IPSec processing, the LS1024A provides several hardware-based engines to accelerate the SSL/TCL and other security standards. In addition to AES, DES, and hash cores, the device includes a RC4 engine to support the SSL standard, a PKA engine and a hardware-based true random generator.

Figure 19-1 IPSec Engine Operations Overview



The standard algorithms supported are:

- AH-SHA-1
- AH MD5
- ESP DES/NULL
- ESP DES/SHA-1
- ESP 3DES/MD5
- ESP 3DES/NULL
- ESP 3DES/SHA-1
- ESP 3DES/MD5
- ESP AES128/NULL
- ESP AES128/SHA-1
- ESP 3DES/NULL
- ESP 3DES/SHA-1
- ESP 3DES/MD5
- ESP AES128/NULL
- ESP AES128/SHA-1

- ESP AES256/MD5

20 TDM Bus Interface

This section describes the LS1024A TDM bus interface.

20.1 Overview

The TDM Bus interface provides a full-duplex, serial TDM bus for digital data transfer between the Network Interface device such as T1/E1 Framer, Time Slot Interchanger, SLIC, and the LS1024A. This section presents TDM Bus features, functional description, and interface timing.

20.2 Features

- Full-duplex, serial time division multiplexed bus for digital transfer with network interface device. For example, T1/E1 framer, time slot interchanger and so on.
- A single TDM bus providing a maximum of 24/32/64/128 time slots (running at 1.536 or 1.544 MHz, 2.048 MHz, 4.096 MHz, or 8.192 MHz, accordingly), or any configured number when running off another clock.
- Clock rate can be x1 or x2 data rate (going up 16.384 MHz for x2). In x2 mode, data is sampled every two clock cycles.
- Provides a programmable timing parameters interface.
- Data can optionally not be driven during inactive timeslot.
- Internal loopback of TDM DX to TDM DR (uses TDM_CK and TDM_FS).
- External loopback of TDM DR to TDM DX (see Section 20.6 TDM Loopback Timing).
- TDM_CK and TDM_FS may be sourced by the LS1024A device.

When sourced externally, TDM_CK and TDM_FS must be stable and within specification before taking the TDM block out of reset.

20.3 Functional Description

The TDM bus supports speeds of 1.536 MHz to 8.192 MHz, allowing between 24 and 128 timeslots. The device processing throughput is not designed to uphold processing of many active channels. Dual rate clock is also supported (up to 16.384 MHz), where data is held for 2 clock cycles. Support is also included for 1.544 MHz clock (193 bit frame) through configuration allowing ignore of the first bit in a frame.

The TDM interface can be set to support both internal and external loopback testing through a GPIO register setting. The parameters of the TDM bus are configurable. The FS, DX, and DR can be sampled on falling or rising edges controlled by parameters FE, XCE and RCE respectively. Data transmission can begin on any clock cycle relative to cycle 0 by programming the appropriate cycle value in the CYCX and CYCR parameters; and the interface can operate in single-clock or double-clock mode where one data bit is transmitted or received every TDM_CK period or every two TDM_CK periods.

The TDM DMA (TDMA) controller manages the flow of data between the TDM bus interface and external system memory through the AMBA AHB Bus and the DDR SDRAM controller. Both the TDM bus interface and the TDMA registers are configured through the APB.

20.4 TDM Bus Interface Timing

Figure 20-1 to Figure 20-8 show the TDM Bus timing and how clock edges are counted in cycles. Cycles are defined as always beginning (with cycle 0) on the rising TDM_CK edge relative to the clock edge on which TDM_FS is sampled. Data transmission can begin on any clock cycle relative to cycle 0 by programming the appropriate cycle value in the CYCX parameter in the Transmitter Operating Configuration Register and CYCR parameter in the Receiver Operating Configuration Register. The TDM Bus interface can operate in single-clock or double-clock mode. One data bit is transmitted or received every TDM_CK period or every two TDM_CK periods as programmed by the CMSX bit in the Transmitter Operating Configuration Register and CMSR bit in the Receiver Operating Configuration Register.

Figure 20-1 Transmit Timing (FE = 1, CMSX = 0)

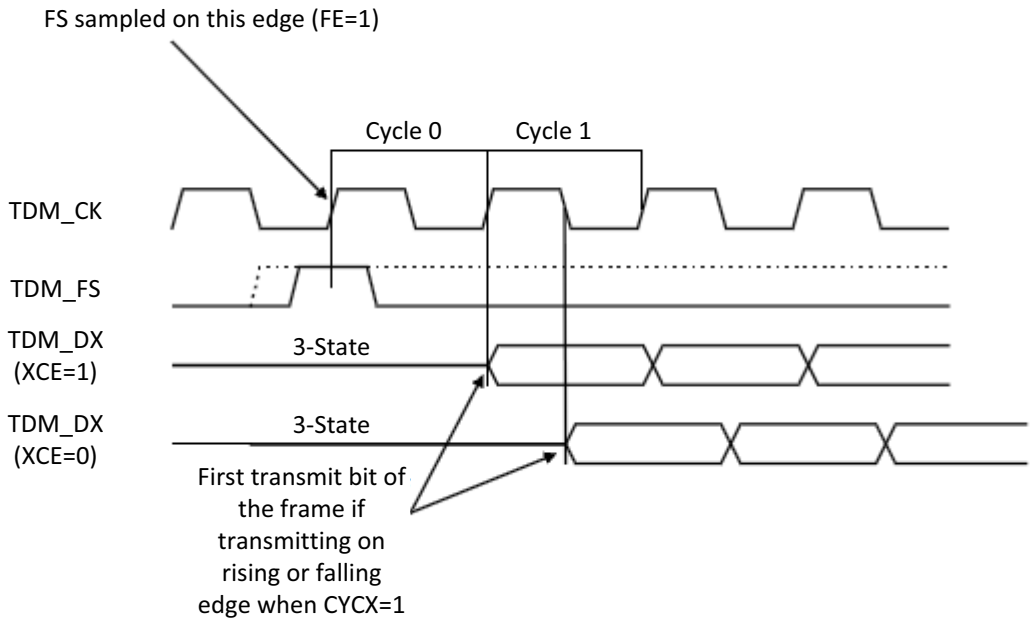


Figure 20-2 Transmit Timing (FE = 0, CMSX = 0)

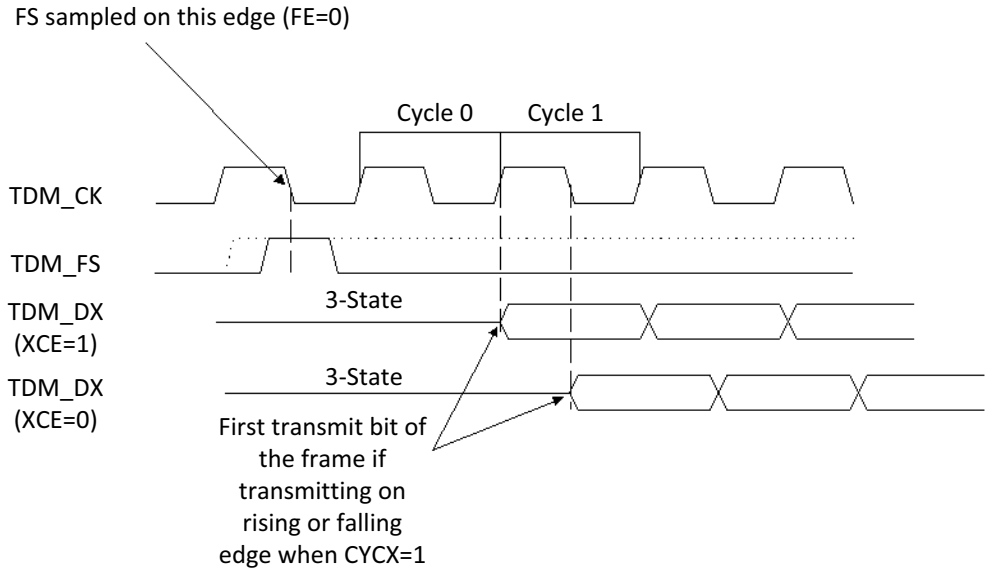


Figure 20-3 Received Timing (FE = 1, CMSR = 0)

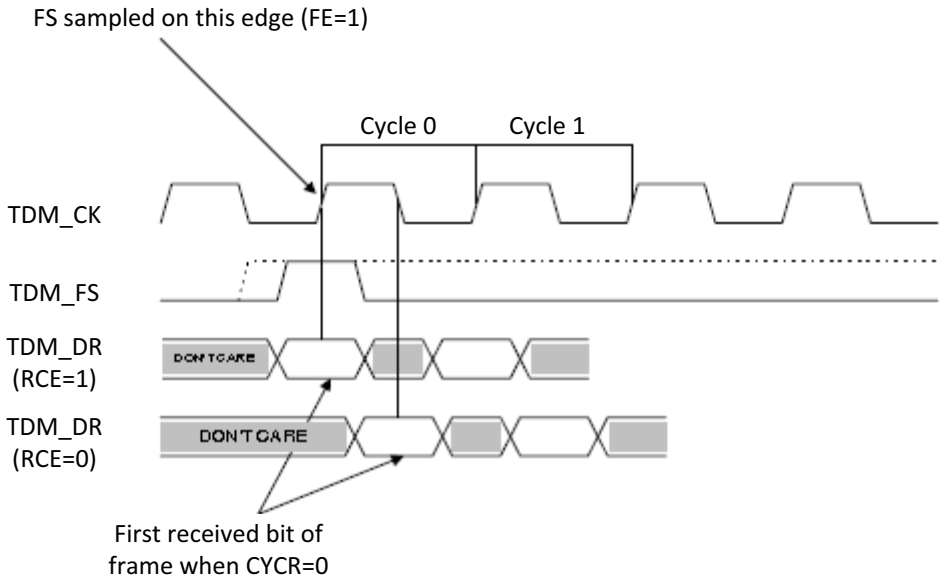


Figure 20-4 Received Timing (FE = 0, CMSR = 0)

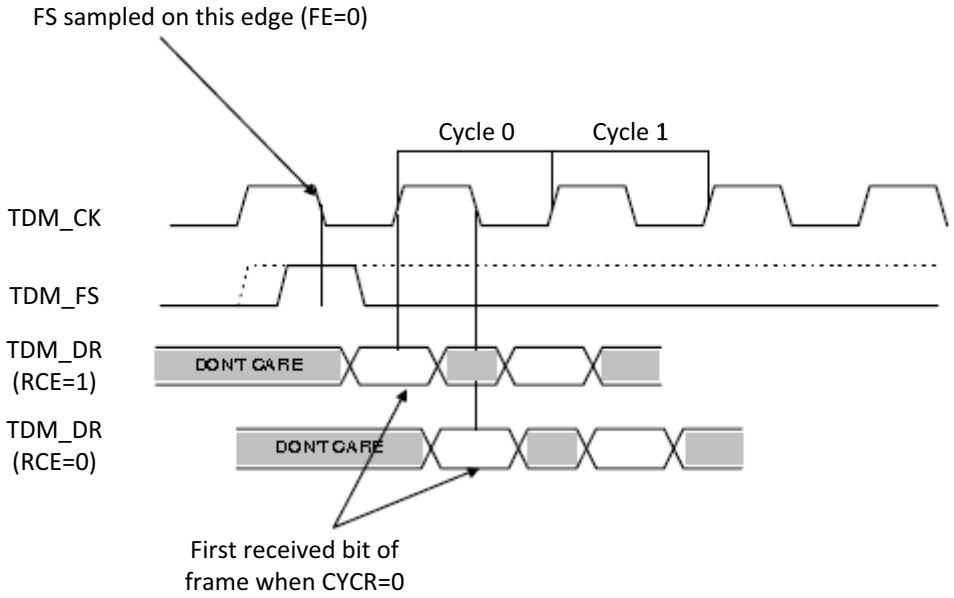


Figure 20-5 Transmit Timing (FE = 1, CMSX = 1)

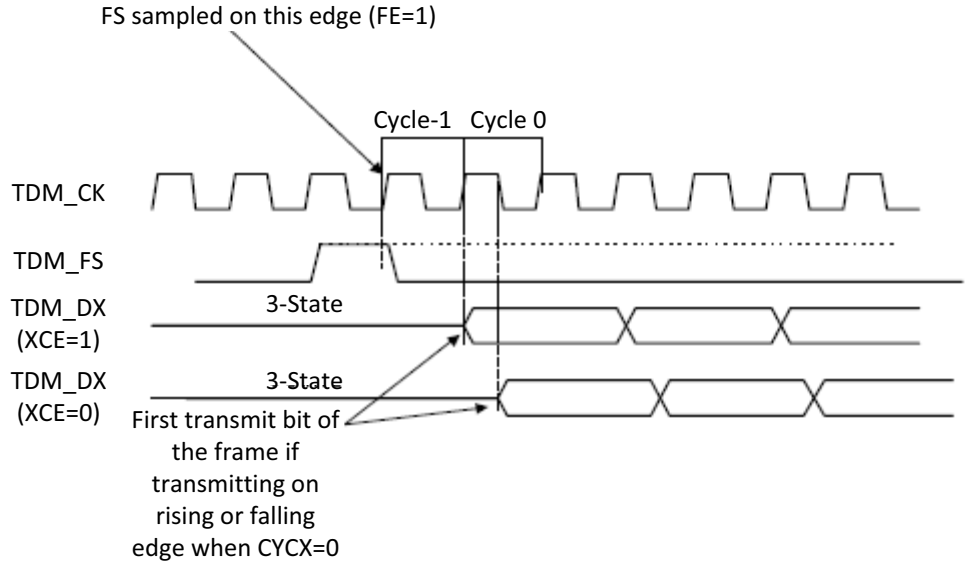


Figure 20-6 Transmit Timing (FE = 0, CMSX = 1)

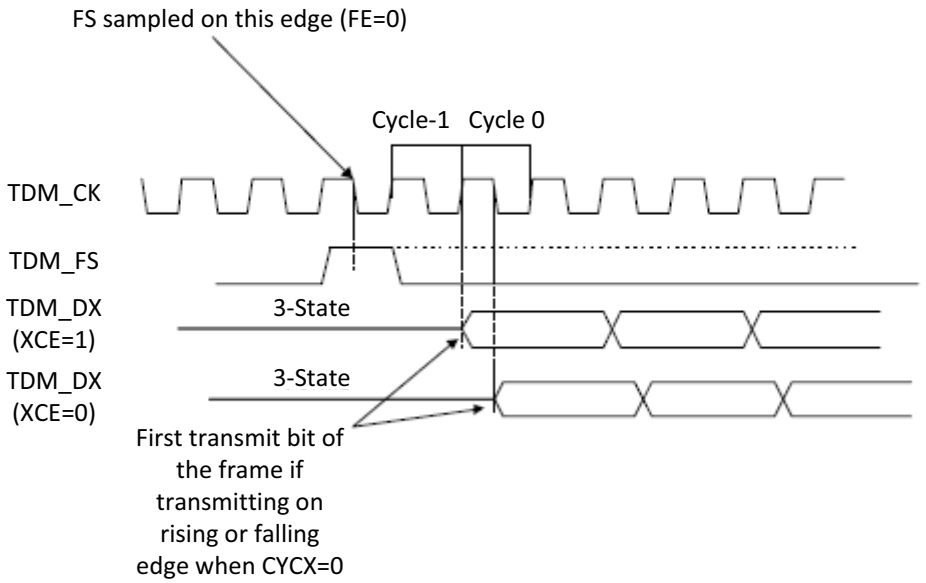


Figure 20-7 Received Timing (FE = 1, CMSR = 1)

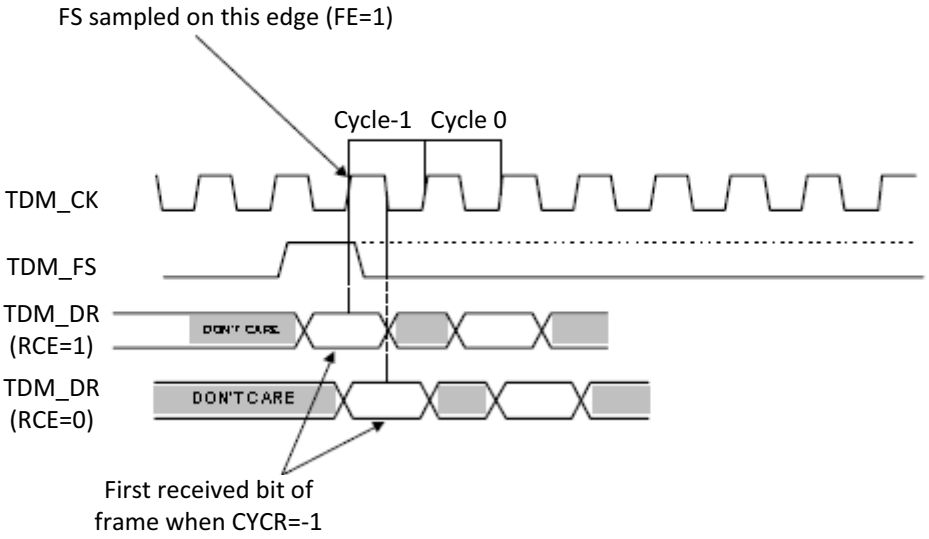
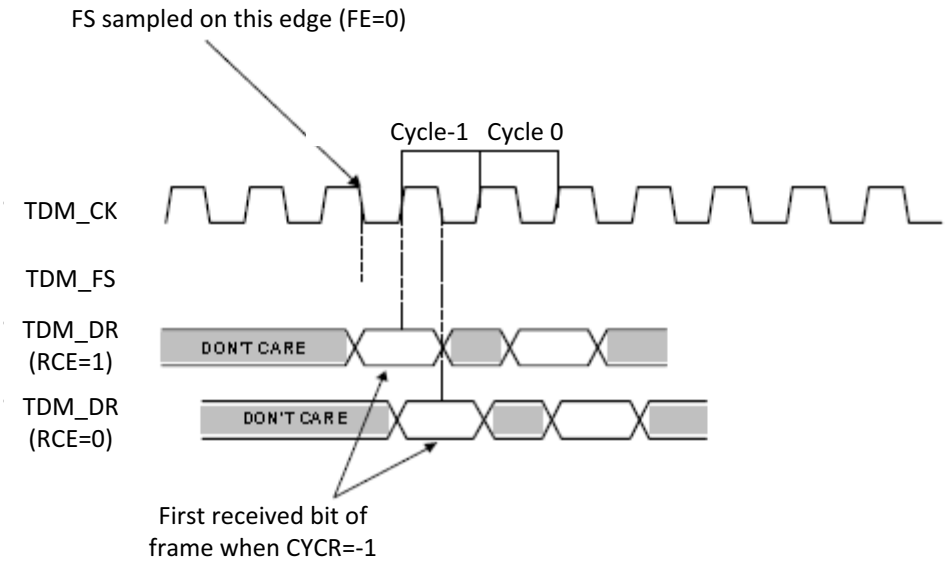


Figure 20-8 Received Timing (FE = 0, CMSR = 1)



20.5 TDM Interface Timing

The TDM Interface timing parameters are programmable and can be configured for H.100, H110, and H-MVIP bus standards using the SUPVSR_SET_TDM_PARAMS message. Figure 20-9 illustrates the TDM bus timing.

Figure 20-9 TDM Bus Timing

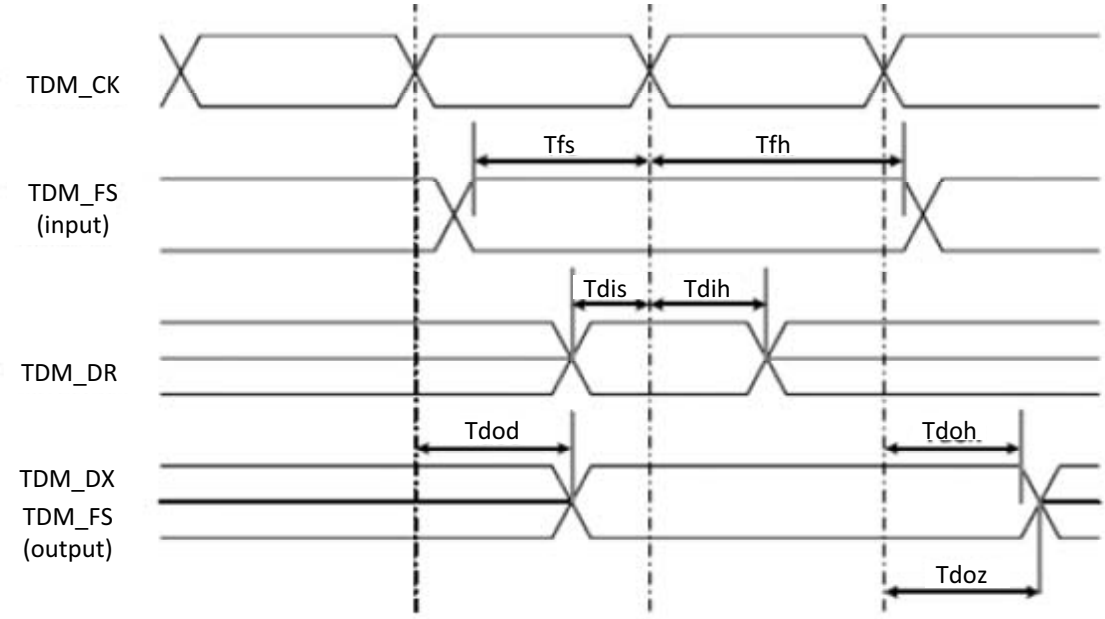


Table 20-1 describes the TDM bus timing details.

Table 20-1 TDM Bus Timing

Symbol	Parameter	Min.	Max.	Units	Notes
	Clock edge rate (All Clocks)	0.25	2	V/ns	1
Tcp	CK Clock Period 1:1 clock to data rate ratio 2:1 clock to data rate ratio	 122 61		ns	
Tch	CK Clock Duty Cycle	40	60	%	
Tfs	Frame Synch Input Setup Time	20		ns	4, 5, 6
Tfh	Frame Synch Input Hold Time	20		ns	4, 5, 6
Tdis	DR Input Setup Time	25		ns	3, 4
Tdih	DR Input Hold Time	4		ns	2, 4
Tdod	DX/FS Output Delay Time	—	20	ns	2,4,6
Tdoh	DX/FS Output Hold Time	0		ns	2,4,6
Tdoz	DX Output Hi Z Time	2	20	ns	2,4,6

NOTES:

1. The rise and fall times are determined by the edge rate in V/ns. A “Max” edge rate is the fastest rate at which a clock transitions.
2. Measured at the transmitter.
3. Measured at the receiver.
4. All inputs can be programmed to be sampled at either rising or falling edge of the clock. All outputs can be independently programmed to be generated at either rising or falling edge of the clock
5. The Frame Synch can be programmed as either active low or active high.
6. TDM_FS may be either input or output. If input, Tfs and Tth apply. If output, Tdod and Tdoh apply.

NOTE: For details about TDM signals, refer to “TDM Signals” on page 37.

20.6 TDM Loopback Timing

This is an external, remote loopback. When enabled, TDM_DR is looped back to TDM_DX without any sampling. Figure 20-10 illustrates the TDM lookpback timing.

Figure 20-10 TDM Loopback Timing

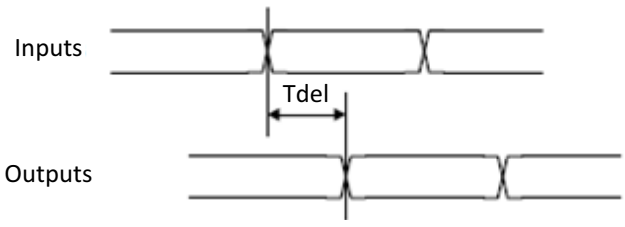


Table 20-2 TDM Loopback Setup and Hold Times

Symbol	Parameter	Min.	Typ.	Max.	Units
Tdel	Input to output delay	2	—	20	ns

21 Microsemi ZSI Interface

LS1024A has internal SLIC Unit (ZDS) block which converts the typical VE880 SLAC MPI and PCM interfaces into a 4- pin proprietary Microsemi Serial Interface (ZSI) to reduce pin count on the host and SLAC devices and allow isolators to be easily utilized.

The use of ZSI corresponds to ZDS mode in LS1024A, which is controlled through GPIO register offset 0x60. In the Legacy mode or TDM mode the ZSI interface acts like a normal TDM interface

21.1 Features

The ZSI Interface provides the following features:

- Supports communication to Microsemi SLIC/SLAC device, such as Le88264 and ZL886x, which supports ZSI interface over the 4-wire ZSI
- Receives a 49.152 MHz clock (Internally generated SLIC clock) and TDM clock (divided down from SLIC clock)
- Supports TDM clock up to 8.192 MHz (1.024 MHz is minimum)
- Supports SPI clock up to 8.192 MHz
- Internally interfaces TDM block and LS-SPI blocks
- In ZDS mode, the active low interrupt is inverted and synchronized from SLIC clock domain to AXI/AHB domain and then gets connected to the A9 IRQ bus

When the block is used, ZSI signals are brought out through TDM pins. SPI CS#3 is used internally. No external device should be connected to it.

21.2 ZSI initialization

ZSI initialization primarily involves the following actions:

1. Configuring clock & reset block
2. Taking TDM out of reset and configuring TDMA and TDM
3. Configuring SPI
4. Taking ZDS block out of reset
5. Enabling TDM receiver and transmitter

21.2.1 Configuring clock & reset block

While TDM and ZDS blocks are in reset, perform the following steps:

1. Select ZDS mode (GPIO register - offset 0x60)
2. Configure clock&reset block to generate SLIC and TDM clocks and FSYNC
3. Make sure that clock toward external SLIC does not exceed its max frequency

21.2.2 Configuring TDMA and TDM

Take TDM out of reset and configure TDMA and TDM (PSEL0 in APB space). Configure the number of time slot based on external SLIC frequency.

21.2.3 Configuring SPI

To configure SPI, generate a clock which is 8.192MHz (or lower). The ZDS block samples inputs data at the rising edge and drives data at rising edge.

Frame size (DFS) is 8bit, Serial clock polarity (SCPOL) =0 and Serial clock phase (SCPH) =0

22 SiLabs Integrated Serial Interface

The ProSLIC Integrated Serial Interface (ISI) is an IP block that enables the smallest and most cost-effective implementation of a ProSLIC solution. This block enables a simplified three-pin interface to supported ProSLIC ICs and internally connects to standard TDM/SPI buses.

The use of ISI interface corresponds to MSIF mode in LS1024A, which is controlled through GPIO register offset 0x60.

22.1 Features

Integrated Serial Interface provides the following features:

- Receives a 24MHz clock (SLIC clock) and TDM clock (divided down from SLIC clock).
- Supports SPI clock up to 4 MHz (3MHz is minimum).
- Supports TDM clock up to 2.048 MHz (1.536MHz is minimum).
- Efficient 3-pin interface to support ProSLIC ICs.
- Eliminates up to six pads in SoC.
- No analog or memory cells required.
- Minimal silicon area.
- Internally interfaces TDM block and SPI blocks.

When this block is used, ISI signals are brought out via TDM pins and SPI CS#3 are used internally and no external device needs to be connected to it.

NOTE: ISI pins are muxed with the TDM interface so that only one interface can be used at one time (ISI, ZSI, or TDM).

22.2 ISI Initialization

User needs to perform the following actions to initialize the Integrated Serial Interface.

1. Select MSIF mode (GPIO register - offset 0x60)
2. Configure clock&reset block to generate SLIC (24.576/18.528/18.432MHz), TDM clocks (divide by 12) and FSsync
3. Configure SPI controller: frequency 3-4MHz, 9bit frame, CPH=1, CPL=0

Ensure that Writes: least significant bit of written data is 0, and Reads: least significant bit of read data is ignored.

There needs to be a specified minimum time between consecutive operations (even between control, address and data phases) so that S/W does not write more than one data to SPI FIFO. The next write should be done only after it confirms that the FIFO is empty.

23 SATA Interface

This section describes the LS1024A SATA controller configuration options and features.

23.1 Features

The SATA Controller consists of the following features:

- One controller for two independent ports
- SATA 1.5 Gb/s, SATA 3.0 Gb/s speeds
- 8b/10b encoding/decoding
- Compliant with the following specifications:
  - Serial ATA II
  - AHCI Revision 1.3
- OOB signaling detection and generation
  - OOB clock frequency (generated internally) is 125 MHz
  - SATA 1.5 Gb/s, SATA 3.0 Gb/s speed negotiation
  - Asynchronous signal recovery, including retry polling
  - Digital support of device hot-plugging
- AXI interface (one master and one slave)
- Internal DMA engine per port
- All ports combined have 16 max outstanding write requests and 16 outstanding read requests
- Power management features including automatic partial-to-slumber transition
- Disabling RX and TX Data clocks during power down modes
- Uses a two-tiered interrupt structure defined in the AHCI specification

23.2 Functional Description

The SATA controller is a two port AHCI-Compliance Host Bus Adaptor. The controller supports Native Command Queueing (NCQ) with up to 32 outstanding commands as defined in SATA II standard. It supports Port Multiplier functionality with command based switching, Hot Plug capability and Slumber and Partial power down states.

The controller combining with the SerDes implement the PHY, Link and Transport layers of the SATA protocol. At each port, the Controller provides two FIFO to buffer data for transferring to and from the system memory, a set of registers for Task-file list, DMA and bus interface unit to interface to the system bus and memory.

Data for an ATA/ATAPI command resides in the system memory in the form of one or more Physical Region Descriptors (PRD). PRD entries describe the physical location and length of data to be transferred. Each PRD entry is read by the Port DMA from the system memory before transferring the block of data associated with this entry. The Port DMA transfers the PRD data block between the system memory and its FIFOs using one or more DMA transaction. The DMA transaction size can be set by software independently for each port. The SATA transport, link and phy state machine generates and sends the command to the device to request and to complete the data transfer.

SATA 0 and SATA 1 signals are muxed with GPIO signals: sata0/1_act_led and sata0/1_cp_pod. See Table 3-2, Muxing Table.

- sata0/1_act_led drives an external LED based on port activity.
- sata0/1_cp_pod is used for cold presence Power-on device, which enables power to the external device when asserted.

23.3 SATA Interface Timing

Table 23-1 and Table 23-2 list the RX and TX SATA Electrical Specifications respectively. Table 23-3 lists the External Reference Input Clock Requirements.

Table 23-1 SATA RX Electrical Specifications

Parameter	Conditions	Min	Typ	Max	Unit
Differential Input Peak to Peak Voltage		50		2000	mV_{diffpp}
Input transition time		0.15		0.40	UI
Differential DC return loss		18			dB
Differential AC return loss (standard specific)		8		16	dB
Common mode DC return loss		12			dB
Common mode AC return loss (standard specific)		6		22	dB
DC input differential termination		90		110	Ω
DC input common mode termination		22.5		27.5	Ω
Power down DC input impedance		200			kΩ
Input common mode AC voltage peak-peak				300	mV
Input common mode frequency		2		200	MHz
Jitter Tolerance (TJ) (standard specific)	LPF: F-3 dB=Fbaud/500 (Gen1 and Gen2)			0.65	UIpp

Table 23-2 SATA TX Electrical Specifications

Parameter	Conditions	Min	Typ	Max	Unit
Differential Output Peak to Peak Voltage		150		1200	mV_{diffpp}
20-80% Rise/Fall Time		30		110	ps
Differential DC return loss		15			dB
Differential AC return loss (1GHz-6GHz)		6		13	dB
Common mode DC return loss		12			dB
Common mode AC return loss (standard specific)		5		13	dB
DC output differential termination		90		110	Ω
DC output common mode termination		22.5		27.5	Ω
Programmable coarse de-emphasis			-3.5 ± 3.5		dB
Fine de-emphasis			0.5		dB

Table 23-2 SATA TX Electrical Specifications (continued)

Parameter	Conditions	Min	Typ	Max	Unit
Precursor (N+1)			-14		dB
Postcursor (N-1)			-4.4		dB
Total Jitter (TJ) (standard specific)	LPF: F-3 dB=Fbaud/500 (Gen1 and Gen2)			0.37	UIpp

Table 23-3 External Reference Input Clock Requirements

Parameter	Description	Min	Typ	Max	Unit
Frequency	Reference clock operating frequency range		60		MHz
RCUI	Reference clock unit interval		16.7		ns
Duty Cycle	Duty Cycle	40	50	60	%
T_R/T_F	Rise and falling edge rate		0.2	0.25	RCUI
Skew	Skew between REFCLKP and REFCLKM			0.05	RCUI
FT	Frequency tolerance	-300		300	ppm
Z_{C-DC}	Clock source output DC impedance	40		60	Ω
V_{DIFF}	LVDS Differential Voltage	250		400	mV
V_{CM}	LVDS	1		1.4	V

24 Joint Test Action Group (JTAG)

This section describes the Joint Test Action Group (JTAG) features and functions.

24.1 Introduction

The LS1024A device provides one JTAG interface, which can be used for Boundary Scan when the device is in Test mode, or for accessing the Cortex®-A9, ARM926, PPFE, and USB3 PHY for debug purposes when the device is in normal mode.

24.2 Features

The Joint Test Action Group Port provides the following features:

- Boundary scan Tap compliant to IEEE 1149.1 standard also supports IEEE 1149.6 for AC JTAG for USB 3.0 and SerDes modules
- Single JTAG port for boundary scan or debug
- Debug option for Cortex-A9 or ARM926 in CSS block, PPFE processors excluding TMUs, or USB3 PHY
- Option to permanently block JTAG debug capability based on information stored in OTP, without disabling Boundary Scan for manufacturing and test

NOTE: For details about JTAG signals, refer to "JTAG Interface Signals" on page 39.

24.3 JTAG Muxing Options

Testmode_n and jtag_mode pins choose the modes as shown in Table 24-1.

Table 24-1 JTAG Muxing Options

Testmode_n[2:0]	jtag_mode	Comments
000 (Test)	100	Nand Tree
000 (Test)	101	Tri-state
000 (Test)	000	BSCAN with all PHY
000 (Test)	001	BSCAN with SRDS0
000 (Test)	010	BSCAN with SRDS1
000 (Test)	011	BSCAN with SRDS2
000 (Test)	110	BSCAN with USB3 PHY
000 (Test)	111	BSCAN with no PHY
100 (Normal)		USB3 PHY debug
110 (Normal)		CSS debug
101 (Normal)		PPFE debug
111 (Normal)		Cortex-A9 debug

24.4 JTAG ID

Table 24-2 lists the JTAG ID.

Table 24-2 JTAG ID

Version [31:28]	Part Number[27:12]	Manufacturer identification [11:1]	Mandatory
xxxx	16'b0000_0001_1010_0110(h'01A6)	b'010_0010_1101(h'22D)	1

24.5 Timing Parameters

Figure 24-1 JTAG Timing Diagram

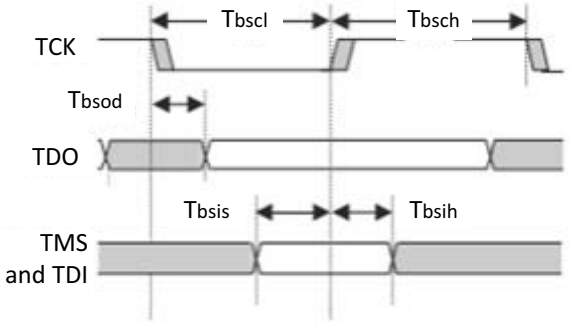


Table 24-3 lists the JTAG Timing parameters.

Table 24-3 JTAG Timing Parameters

Symbol	Parameter	Min.	Max	Units
T_{bscl}	TCK LOW period	50		ns
T_{bsch}	TCK HIGH period	50		ns
T_{bsod}	TDO output delay from TCK (falling)	0	25	ns
T_{bsis}	TDI, TRST_N and TMS setup to TCK (rising)	20		ns
T_{bsih}	TDI, TRST_N and TMS hold from TCK (rising)	10		ns

25 Inter-IC Interface

This section describes the LS1024A I^2C interface.

25.1 Overview

LS1024A devices include a standard I^2C to load boot code and to provide system management communications with other devices.

25.2 Features

The Inter-IC Bus (I^2C) Master/Slave Interface provides the following features:

- Conforms to V2.1 of the I^2C specification.
- Master or slave operation
- Multi-master systems supported
- Supports both 7-bit and 10-bit addressing on the I^2C bus
- Own address and General Call (data broadcast) address detection
- Built in collision detection
- Supports High Speed (3.4 Mbps), Fast (400 kbps) and Standard (100 kbps) transfer rates

NOTE: The I^2C interface signals are multiplexed with GPIOs:

- I^2C SCL (muxed with GPIO16)
- I^2C_SDA (muxed with GPIO17)

25.3 Functional Description

I^2C is a low-bandwidth, short distance protocol for on-board communications. All devices are connected through two wires: Serial Data (SDA) and Serial Clock (SCL). Available Freescale drivers allow LS1024A devices to boot from a serial EEPROM through the I^2C interface. All I^2C devices must have a unique address to identify it on the bus. Slave devices have a predefined address, but the lower bits of the address can be assigned to allow for multiples of the same devices on the bus.

The LS1024A device operates as a master, a slave, or in multi-master mode. It supports all I^2C speeds: standard (100 kbps), fast (400 kbps) and high speed (3.4 Mbps). The LS1024A I^2C interface includes a programmable clock divider to allow adjustment of data speed over a wide range. However, the LS1024A I^2C interface does not include an output signal for direct control of a bridge between fast/standard and high-speed bus segments. Thus, the LS1024A I^2C interface is typically configured to accommodate the slowest device on the bus.

25.4 I^2C Timing

Figure 25-1illustrates the I^2C timing waveform. Table 25-1 lists the I^2C timing parameters.

Figure 25-1 I²C Timing Waveforms

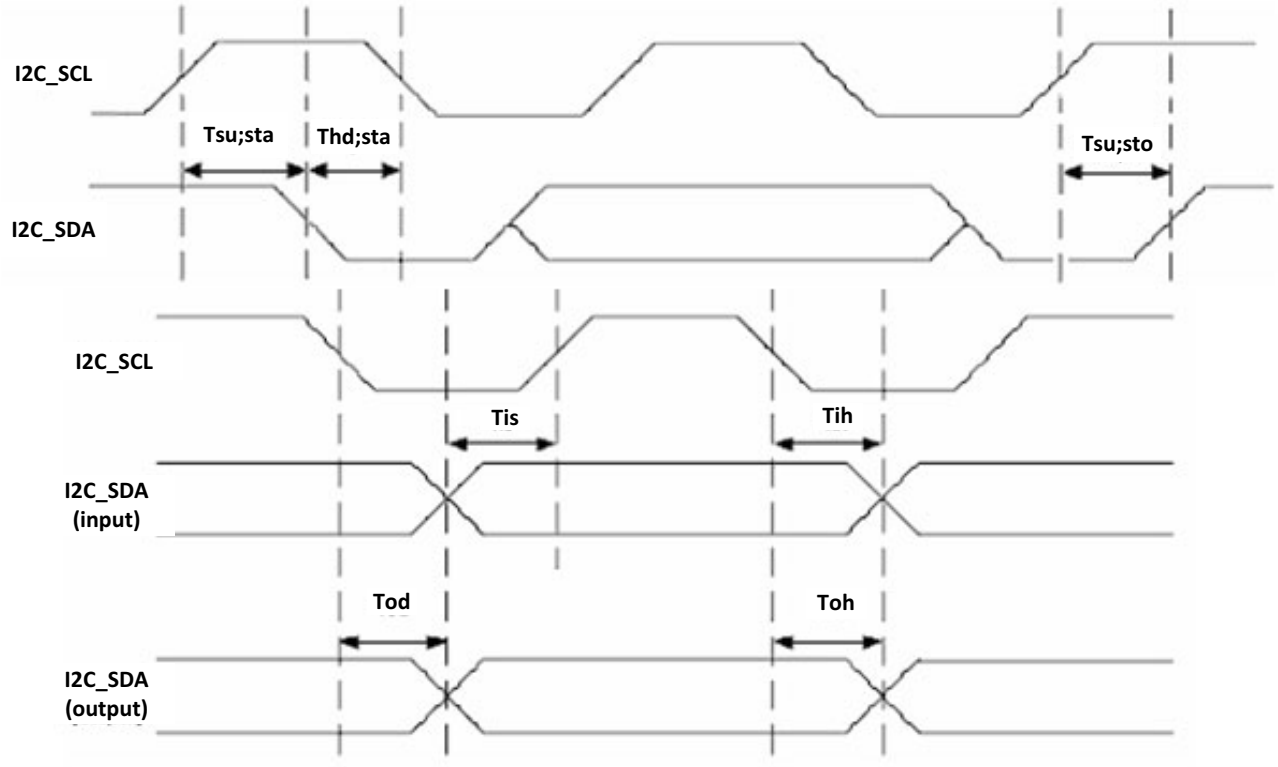


Table 25-1 I²C Timing Parameters

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
	Clock Frequency			3.4	MHz	
	Clock Duty Cycle Low period High period	 160 60			 ns ns	
Tsu;sta	(Repeated) START condition setup time	160			ns	1, 2
Thd;sta	(Repeated) START condition hold time	160			ns	1, 2
Tsu;sto	STOP condition setup time	160			ns	1, 2
Tis	Input Setup Time (I^2C_input)	10			ns	
Tih	Input Hold Time (I^2C_input)	0			ns	
Tod	Output Delay Time (I^2C_output)			60	ns	3, 4
Toh	Output Hold Time (I^2C_output)	0			ns	

Table 25-1 I^2C Timing Parameters (continued)

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
NOTES: 1. These numbers can be extended when using a slower output clock (master mode). 2. This number increases as clock frequency is slower, according to the following formula: Tsu;sta(min) = Thd;sta(min) = Tsu;sto(min) = $2^N * T_{AHB}$ where T_{AHB} is the AHB clock period, and N is a parameter that is used to set the I^2C clock frequency according to the AHB clock frequency 3. Output delay time is not defined in standard. LS1024A value should guarantee meeting the timing at the receiver. 4. This number increases as clock frequency is slower, according to the following formula: Tod(max) = $2^{N+1} * (M+1) * T_{AHB}$ where T_{AHB} is the AHB clock period, and N and M are parameters that are used to set the I^2C clock frequency according to the AHB clock frequency						

NOTE: For details about I^2C signals, refer to "I2C Signals" on page 35.

25.5 High Speed Mode

A Master may arbitrate and select High speed operation by transmitting one of the reserved 7-bit addresses of the form 00001*xxx*b. The first five bits of this address are significant: the remaining three bits may be used to identify different Hs-mode masters on the same I^2C bus.

On detecting a code of this form, the I^2C interface enters High speed mode. It reverts to F/S mode on detection of a STOP condition on the I^2C bus.

25.6 Clock Synchronization

If another device on the I^2C bus drives the clock line when the I^2C interface is in master mode, the I^2C interface synchronizes its clock to the I^2C bus clock. The high period of the clock is determined by the device that generates the shortest high clock period. The low period of the clock is determined by the device that generates the longest low clock period.

When the I^2C interface is in master mode and is communicating with a slow slave, the slave can stretch each bit period by holding the SCL line low until it is ready for the next bit. When the I^2C interface is in slave mode, it holds the SCL line low after each byte has been transferred until the IFLG has been cleared in the CNTL register.

25.7 Bus Arbitration

In master mode, the I^2C interface checks that each transmitted logic 1 appears on the I^2C bus as a logic 1. If another device on the bus over-rules and pulls the SDA line low, arbitration is lost. If arbitration is lost during the transmission of a data byte or a Not ACK bit, the I^2C interface returns to the idle state. If arbitration is lost during the transmission of an address, the I^2C interface switches to slave mode so that it can recognize its own slave address or the general call address.

26 USB 2.0 Interface

This section describes LS1024A USB 2.0 interface.

26.1 Introduction

The Universal Serial Bus (USB) 2.0 interface complies with the USB2.0 standard and is backward compatible with USB1.1. It supports High-Speed (480-Mbps), Full-Speed (12-Mbps) and Low- Speed(1.5-Mbps) modes. The LS1024A device includes one instance of USB2 controller with integrated USB2 PHY.

26.2 Features

The USB2.0 Controller and PHY has the following features.

26.2.1 Controller

- USB 2.0 and USB 1.1 compliance
- Can be configurable to act as host-only or device-only
- LS is not supported in Device mode
- Number of device mode endpoints is six (in addition to control endpoint 0)– Two for Isochronous, two for Interrupt and two for Bulk
- Number of Host Mode Channels is 14
- Supports a generic root hub
- Supports suspend mode
- Internal DMA with scatter/gather option
- Max packet size is: 1024B for Isochronous and Interrupt; 512 B for Bulk
- Link Power Management is supported
- Controller - PHY interface is 8/16 bits (software-selectable for flexibility)UTMI+Level3

26.2.2 PHY

- Supports off-chip charge pump regulator to generate 5 V for VBUS
- Includes the 2.5 V Voltage Regulator
- Fully integrates 45Ω termination, 1.5kΩ pull-up and 15kΩ pull-down resistors, with support for independent control of the pull-down resistors
- Supports 480 Mbps high-speed, 12 Mbps full-speed, and 1.5 Mbps low-speed (Host mode only) data transmission rates
- Supports 8/16-bit unidirectional parallel interfaces for HS, FS, and LS (Host mode only) modes of operation, in accordance with the UTMI+ specification
- Provides dual (HS/FS) mode host support
- Implements logic to support suspend, sleep, resume, and remote wakeup operations
- Implements VBUS threshold comparators

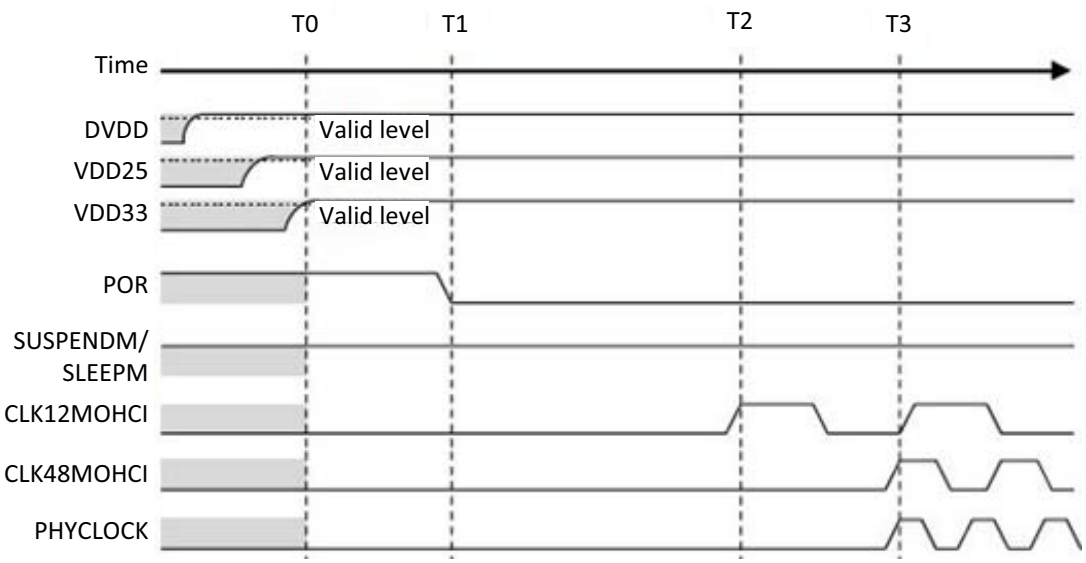
NOTE: For details about USB2.0 signals, refer to "USB2.0 Interface Signals" on page 40.

26.3 Reset and Power Up Control Timing

26.3.1 USB2 PHY Power On Reset Timing

Figure 26-1 specifies the Power-ON Reset (POR) assertion-timing for the USB nanoPHY.

Figure 26-1 USB2 PHY Power-On Reset Timing



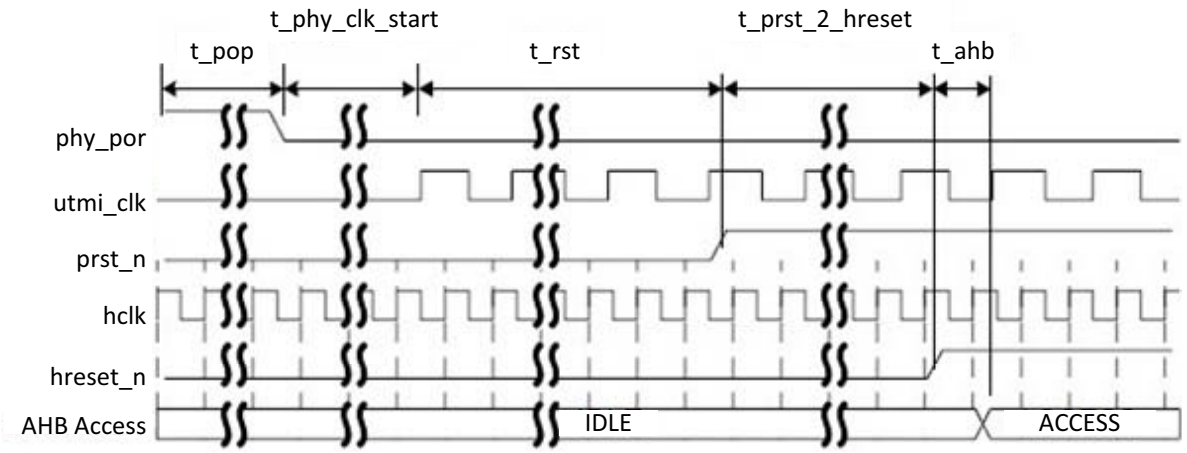
Assert the USB2 PHY POR = 1 for at least 10µs, to properly reset the USB2 PHY IP, before deasserting the reset and enabling it.

The PHYCLOCK (UTMI+ Clock to the OTG Controller) should start within 45 µs of deasserting the Power-On Reset to the PHY.

26.3.2 USB2 Controller Clock-Reset Timing

Figure 26-2 specifies the USB2 PHY and AHB Clock-domain Reset, and AHB Clock-domain Clock timings for the USB2 Controller.

Figure 26-2 USB2 Controller Clock-Reset Timing



The USB2 PHY Power-On Reset (POR) must be asserted for "t_pop(actually 't_por') ≥10µs", before desertion.

The PHY Clock Start (PHYCLOCK/utmi_clk) should be "t_phy_clk_start ≥ 45µs", after PHY power on reset desertion.

The USB2 Controller PHY Clock-domain Reset need to be asserted for period of 't_rst ' ≥(12 cycles of the slowest clock) before desertion.

Considering the AHB Clock = 250 MHz (4 ns period) and the UTMI+ 16-bit PHY Clock = 30 MHz (33.33 ns period) [It is 60 MHz for the 8-bit PHY interface selection]. The t_rst ≥ 12 * 33.3333 ns, meaning t_rst ≥ 0.4 µs (PHY clock is slow clock). After this period after the PHY clock has started, then deassert the PHY clock-domain reset (prst_n) for the Controller. The 'prst_n' must be deasserted synchronously in terms of the PHY 'utmi_clk'.

The 't_prst_2_hreset' ≥ (6 cycles of the slowest clock) which is t_prst_2_hreset ≥ 0.2 µs (meaning 6 * 33.3333 ns). After this period the Controller's AHB clock-domain reset 'hreset_n' need to be deasserted in synchronous to AHB 'hclk'.

Considering t_ahb = 1 AHB Clock period = 4 ns(250 MHz), the USB2 Controller is accessible for operation 1 AHB Clock-cycle after the 'hreset_n' has been deasserted.

26.3.3 USB Controller and PHY Clock-Reset Timing Implementation

Both the hclk to the Controller and the reference clock to the PHY must be running before deasserting any of the resets.

1. Start by initially asserting the USB2 PHY's POR (high) and the Controller's prst_n (low) and hreset_n (low).
2. After approximately 10.1 µs (i.e. > 10 µs), deassert POR.
3. Wait for the PHYCLOCK output ('utmi_clk' input to the Controller) to start, or wait for 45 µs to pass; after deasserting POR.
4. Wait for 12-14 'utmi_clk' cycles, or wait for more than 400 ns; after the 'utmi_clk' has started, and then deassert the 'prst_n' synchronously with respect to 'utmi_clk'.
5. Wait for 6-8 'utmi_clk' cycles, or wait for more than 200 ns; after the 'prst_n' has been deasserted, and then deassert the 'hreset_n' synchronously with respect to 'hclk'.
6. Wait for one 'hclk' cycle (or more than 4 ns) after the 'hreset_n' has been deasserted. The USB2 Controller is ready for operation.

27 USB 3.0 Interface

This section describes LS1024A USB 3.0 interface.

27.1 Introduction

The USB 3.0 Interface, compliant with Universal Serial Bus 3.0 Specification, Revision 1.0, is backward compatible with USB2.0 and USB1.1. It supports Super-Speed (5.0-Gbps), High-Speed (480-Mbps), Full-Speed (12-Mbps) and Low- Speed (1.5-Mbps) modes. The LS1024A device includes one instance of USB3 controller with integrated USB3 PHY.

27.2 Features

The USB 3.0 Controller and PHY has the following features.

27.2.1 Controller

- Can be configurable to act as host-only or device-only
- Isochronous endpoint capability
- Device
  - 8 endpoints including OUT and IN control endpoint 0 which is always present
  - 4 maximum number of Device mode IN endpoints active at any time, including control endpoint 0, which is always present
  - PIPE3 (SS) and UTMI+ (HS) interfaces
  - 8 bits data width for UTMI+ PHY interface
  - Enable Link Power Management (LPM)
- Host
  - Up to 16 devices are supported
  - Compatible with the xHCI Version 0.96 specification and also supports xHCI Version 1.0.

27.2.2 PHY

- Fully compliant with Universal Serial Bus 3.0 Specification, Revision 1.0
  - Supports 5.0-Gbps SuperSpeed (SS) through 3-m cable, 480-Mbps high-speed (HS), 12-Mbps full-speed (FS), and 1.5-Mbps low-speed (LS) serial (Host mode only) data transmission rates
  - Supports beaconing, receiver detection, and electrical idle
  - Four-wire SuperSpeed connection (two TX and two RX unidirectional) with built-in TX and RX equalization
- Single external or internal reference clock input for both USB 3.0 and USB 2.0 operating modes. Wide range of reference clocks supported: 19.2, 20, 24, and 100 MHz
- Built-in VBUS threshold comparators; support for off-chip charge pump regulator to generate 5-V VBUS signals
- Minimal external component cost: only a single external resistor required
- USB3.0 mode includes Spread Spectrum Clock (SSC) generation and absorption

- Supports all power management features
  - Supports SuperSpeed power-down modes: U0, U1, U2, and U3
  - Supports high-speed power modes: suspend, resume, and remote wakeup
- IEEE standards 1149.1 and 1149.6 (JTAG) boundary scan for internal visibility and control
- Built-in Self-Test (BIST) features for production, at-speed, testing on any digital tester SuperSpeed, high-speed, full-speed, and low-speed USB test modes supported
- Advanced, built-in diagnostics including SuperSpeed 5-Gbps on-chip sampling scope for easy debug
- PHY supports a separate 16-bit Control Register (CR) access interface.

NOTE: For details about USB3.0 signals, refer to "USB3.0 Interface Signals" on page 40.

27.3 USB3 PHY Control Register Access

The CR port is a 16-bit data/address parallel port that is provided for on-chip access to the control registers inside the USB 3.0 PHY. While access to these registers is not required for normal PHY operation, this interface enables access to some of the PHY's diagnostic features during normal operation or to override some basic PHY control signals. This interface is completely asynchronous-using a handshake between the cr_cap_addr, cr_cap_data, cr_read, and cr_write input commands with cr_ack acknowledgements and cd_data_out outputs from the PHY. CR port access is divided into address, read, and write transactions, as shown in Figure 27-1, Figure 27-2, and Figure 27-3.

Figure 27-1 CR Bus Address Capture Transaction

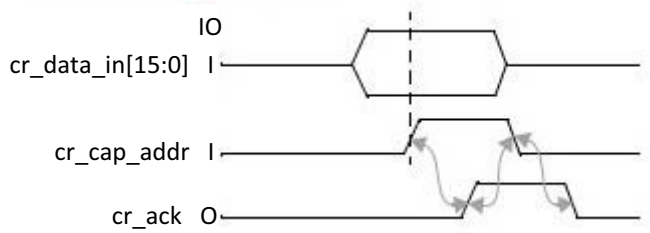


Figure 27-2 CR Bus Read Transaction

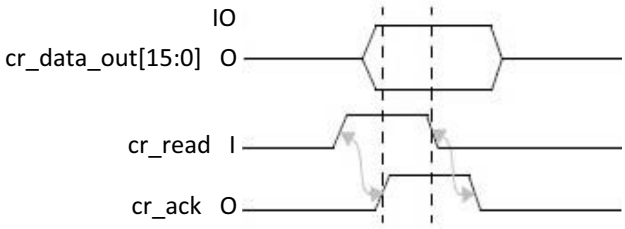
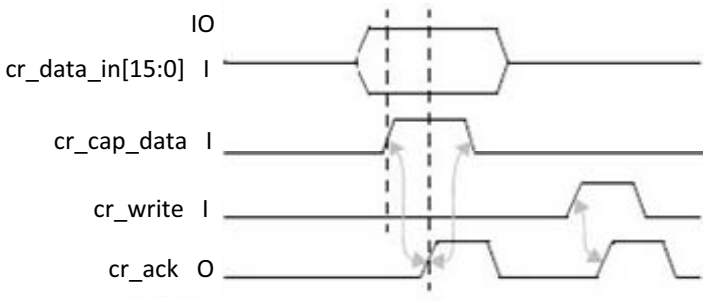


Figure 27-3 CR Bus Write Transaction



27.4 USB3 PHY POR Timing

The USB 3.0 PHY has multiple power supplies:

- 1.1-V: VP, VPTX0, DVDD
- 3.3-V: VPH, VDD330

While the power supplies can be brought up in any sequence provided they come up at relatively the same time, the ASIC must hold the phy_reset pin high until the supplies are within the range specified in Table 27-1 and the reference clock is up and stable.

Figure 27-4 shows power-on reset timing for the USB 3.0 PHY when the HS function is not in Suspend or Sleep mode.

Figure 27-4 POR Timing

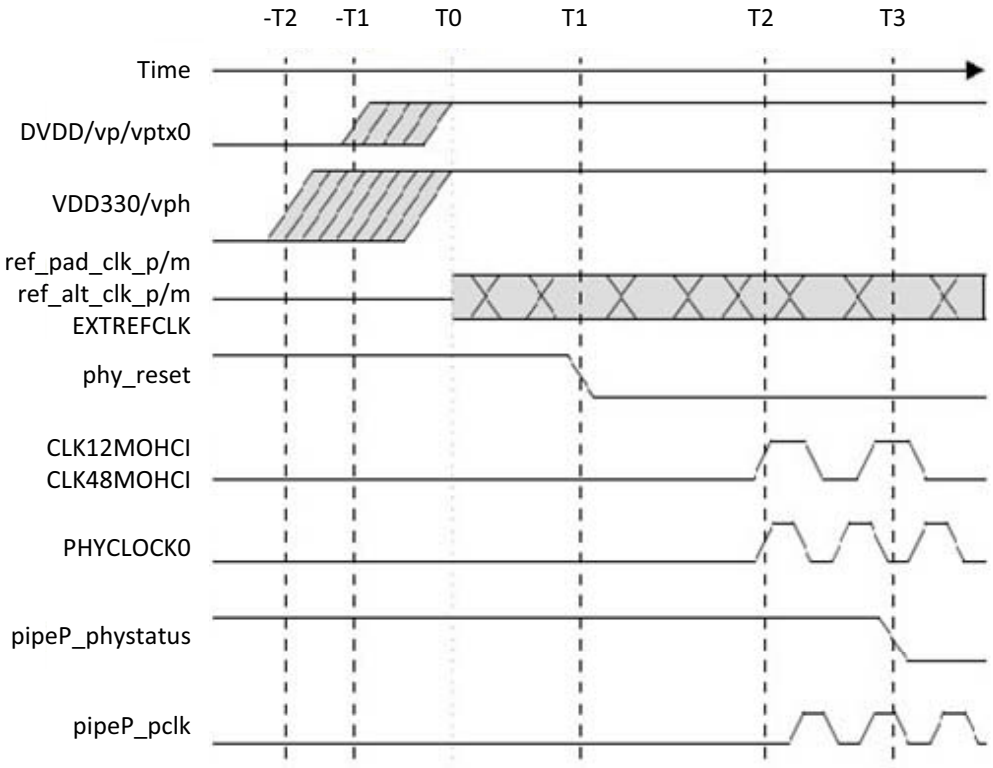


Table 27-1 POR Timing Parameters

Timing Parameter	Description	Value
RefClk	Differential reference clock input into the PHY. is equal to pins ref_alt_clk_p/ref_alt_clk_m or ref_pad_clk_m/ref_pad_clk_p and/or EXTREFCLK depending on the setting of ref_use_pad and REFCLKSEL[1:0]	
-T2 to -T1	Maximum time VDD330/vph is applied before DVDD/vp/vptx	< 10's of ms
T0	Time when supplies are within specified limits and the reference clcok is up and stable.	
T1	Time after T0 when ASIC can remove POR	> 10 µs
T2-T1	Time after T1 when PHYCLOCK, CLK12MOHCI, and CLK48MOHCI are guaranteed to be available for use by ASIC	> 45 µs
T3-T2	Time after T1 when pipeP_phystatus deasserts to indicate that pipeP_pclk is guaranteed to be up and stable.	>120 µs

28 XOR-DMA Controller

This section describes XORDMA subsystem of LS1024A device.

28.1 Features

XORDMA provides the following features:

- Multi-purpose DMA controller
- Independent Inbound and Outbound Frame and Buffer descriptors provide information about the packet to be transferred.
- Frame/Buffer Descriptors can support linked list-transfer operations
- Scatter/Gather
- XOR Function:
  - Block size: 256B, 512B, 1KB, 2KB, 4KB
  - Number of Blocks: 2-15
  - Modes:
    - Encode: XOR all blocks and return parity block
    - Validate: XOR all blocks and verify parity calculation
  - Runs at speed of AXI bus

28.2 DMA Data Structure

The DMA controller exchanges control information and data with the system via three data structures:

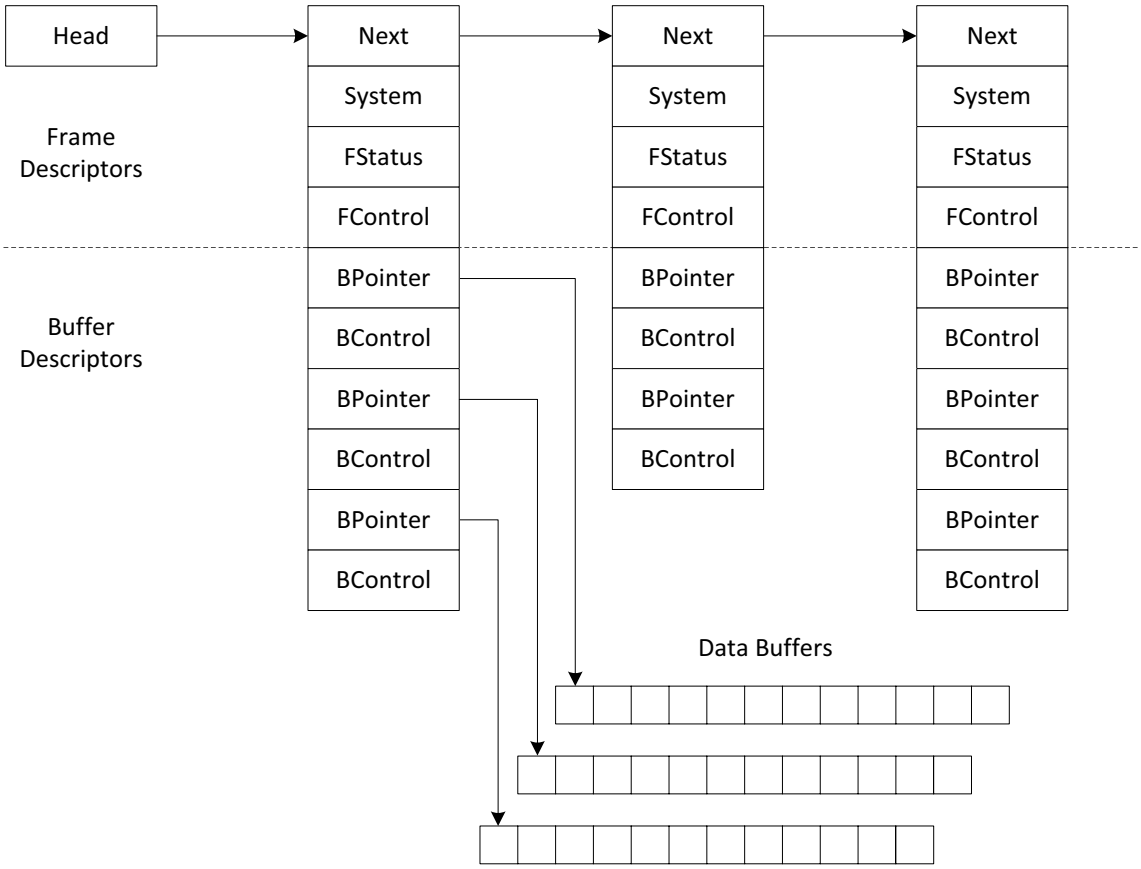
- Frame descriptors
- Buffer descriptors
- Data buffers

Frame descriptors have a four-byte pointer to the next frame, a field for the system or applications program to use exclusively, a frame status field and a control field for the entire frame. Buffer descriptors have a pointer to a data buffer and control field for the buffer. A data buffer is an array of bytes, which can be stored in the memory.

Frame descriptors must be aligned on 16-byte boundaries. Buffer descriptors must be aligned on eight-byte boundaries. The DMA engine supports transfers of data buffer on byte boundaries. Multiple buffer descriptors are used for scattering and gathering.

Figure 28-1 shows how these data structures are related.

Figure 28-1 Relation between Data Structures



29 Electrical and Environmental Specifications

This section describes the Power supply, the voltage requirements, the electrical and environmental specifications of LS1024A device.

29.1 Power Supply

The power supply requirements of the different components of LS1024A device are listed below:

Table 29-1 Power Supply Requirements

Description	Symbol	Typical(V)	Notes
System Supplies			
Core	CORE_VDD_RING	1.1 V	1.1 V for all digital logic except CA9 and PPFE
	VDD_A9	1.1 V, 1.2 V, or 1.24 V	For CA9 Subsystem (Cortex®-A9 and L2)
	VDD_HFE		
PLL	PLL#_AVDD	1.1 V or 1.13 V	Core supply
	PLL#_AVSS		Core ground
GEMAC	GEM#_DVDD (RGMII mode)	2.5 V or 3.3 V	3.3 V operation requires software configuration
	GEM#_DVDD (RMII mode)	3.3 V	
	GEM2_DVDD (DECT/I2S mode)		MDIO is always 3.3 V
USB3.0 PHY	USB3_VDD_RING (PHY DS = VDD330, VPH)	3.3 V	High supply for HS and SS operations
	DVDD	1.1 V of 1.13 V	Analog and digital HS supply:
	VP		Analog and digital SS supply:
	VPTX0		Transmit Supply
USB2.0 PHY	USB0_VDD33_0,USB0_VDD33_1	3.3 V	Analog Power Supply
	USB0_DVDD	1.1 V of 1.13 V	Digital Power Supply
SerDes	S#_VDDHA	2.5 V (or 3.3 V)	High Analog Supply
	S#_VDDT_0	1.1 V of 1.13 V	TX driver Low Analog Supply
	S#_VDDA		Low Analog Supply
OTP	OTP_VDDIO	2.5 V	2.5 V for read operation
	OTP_VDD	1.1 V of 1.13 V	1.1 V for OTP
Digital I/O (GPIO, EXP, Coresight, JTAG)	IO_VDD_RING,E_DVDD	3.3 V	Digital I/O
DDR	DDR_VDDQ, DDR_VDDQZQ	1.5 V (DDR3)	
	DDR_VREF_RING	0.5*DDR_VDDQ	
	DDR_VSSQZQ	Ground Supply	

Table 29-1 Power Supply Requirements (continued)

Description	Symbol	Typical(V)	Notes
RTC (Lithium battery)	RTC_VDD	3 V	
FSOURCE for ECID eFuse	FSOURCE_ECID	1.8 V or O	Normal and other nodes-0 V Programming on tester- 1.8 V
Common ground supply	VSS_RING		
Oscillator pads	DOSC_DVDD, PSOSC_DVDD, UPOSC_DVDD	3.3 V	

Notes:
- Power Supply Tolerance for Core and PLL is 3%.
- Power Supply Tolerance for all other supplies is 5%.

29.2 Operating Conditions

Table 29-2 and Table 29-3 list the operation conditions for LS1024A device.

Table 29-2 Temperature Requirements

Symbol	Parameter	LS1024A			Unit
		Min	Typical	Max	
Ta	Ambient Temperature	-10		70*	^{o}C
Tj	Junction Temperature	—		125	^{o}C

Note:
* Assumes a heatsink for 900 MHz and 1.2 GHz devices under the worst case conditions (all functional blocks are fully active).

Table 29-3 Voltage Requirements

Supply	Symbols	650MHz Devices LS1024ASN7ELA, LS1024ASE7ELA			900MHz Devices LS1024ASN7JLA, LS1024ASE7JLA			1200MHz Devices LS1024ASN7MLA, LS1024ASE7MLA			Unit
		Min	Typical	Max	Min	Typical	Max	Min	Typical	Max	
Core Supply	CORE_VDD_RING, PLL#_AVDD, DVDD, VP, VPTX0, USB0_DVDD, S#_VDDA, S#_VDDT	1.045	1.1	1.155	1.045	1.1	1.155	1.096	1.13	1.164	Volts
A9/HFE Supply	VDD_A9, VDD_HFE	1.045	1.1	1.155	1.14	1.2	1.26	1.203	1.24	1.277	Volts
DDR IO Supply	DDR_VDDQ DDR_VDDQZQ	1.425	1.5	1.575	1.425	1.5	1.575	1.425	1.5	1.575	Volts
DDR Reference	DDR_VREF_RING	DDR_VDDQ * 0.49	DDR_VDDQ * 0.5	DDR_VDDQ * 0.51	DDR_VDDQ * 0.49	DDR_VDDQ * 0.5	DDR_VDDQ * 0.51	DDR_VDDQ * 0.49	DDR_VDDQ * 0.5	DDR_VDDQ * 0.51	Volts
RGMII/SerDes Supply	GEM#_DVDD (2.5V Mode) S#_VDDHA (2.5V Mode) OTP_VDDIO	2.375	2.5	2.625	2.375	2.5	2.625	2.375	2.5	2.625	Volts
RTC Supply	RTC_VDD	2.85	3	3.15	2.85	3	3.15	2.85	3	3.15	Volts
USB/GPIO Supply	GEM#_DVDD(3.3V Mode), S#_VDDHA (3.3V Mode) IO_VDD_RING USB3_VDD_RING USB0_VDD33_#	3.135	3.3	3.465	3.135	3.3	3.465	3.135	3.3	3.465	Volts

NOTE: The core voltage depends on the following:

- Target application — 650 MHz, 900 MHz or 1.2 GHz, single or dual regulators for the 1.1 and 1.2 V domains.
- Power State—Idle or Activepower state of the device

Table 29-4 lists the Voltage tolerance of the LS1024A devices:

Table 29-4 Device Voltage Tolerances

Device Operation	VCore	VHFE/VDD_A9
650 MHz	1.1V ± 5%	1.1V ± 5%
900 MHz	1.1V ± 5%	1.2V ± 5%
1.2 GHz	1.13V ± 3%	1.24V ± 3%

29.3 Absolute Maximum Continuous Ratings

Absolute maximum ratings specify conditions under which there is no device damage, but device operation is not guaranteed.Table 29-5 lists the absolute maximum ratings of LS1024A device.

Table 29-5 Absolute Maximum Ratings

Symbol	Parameter	Rating			Units
		Typical	Minimum	Maximum	
V_{DD}	DC Supply Voltage	2.5 V V_{DD}	-0.5	3.6	V
		3.3 V V_{DD}	-0.5	4.6	
V_{IN}	DC Input Voltage	2.5 V Input Buffer	-0.5	3.6	
		3.3 V Input Buffer	-0.5	4.6	
		3.3 V Interface/5 V Tolerant Input Buffer	-0.5	6.5	
V_{OUT}	DC Output Voltage	2.5 V Output Buffer	-0.5	3.6	
		3.3 V Output Buffer	-0.5	4.6	
		3.3 V Interface/5 V Tolerant Output Buffer	-0.5	6.5	
II/O	In/Out Current		± 20		mA
Ta	Storage Temperature		-65 to 150		°C

29.4 Power Specification

Table 29-6 lists the absolute current (for power regulator sizing) of LS1024A devices.

Table 29-6 LS1024A Absolute Current (for power regulator sizing)

Symbol	Parameter	650MHz Devices LS1024ASN7ELA, LS1024ASE7ELA			900MHz Devices LS1024ASN7JLA, LS1024ASE7JLA			1200MHz Devices LS1024ASN7MLA, LS1024ASE7MLA			Unit
		Min	Typical	Max	Min	Typical	Max	Min	Typical	Max	
I_{core}	Current consumed by 1.1V Core			1200			1400			1500	mA
I_{HFE}	Current by PPPoE (VDD_HFE)			600			900			1000	mA
I_{A9}	Current by A9 (VDD_A9)			1200			1500			2000	mA
I_{DDR}	DDR I/O current (1.5V)			400			450			500	mA
I_{rgmii}	RGMII/SerDes I/O current (2.5V)			150			150			150	mA
I_{gpio}	USB/GPIO I/O current (3.3V)			200			200			200	mA
I_{rtc}	RTC current (3.0V)			7.4			7.4			7.4	uA
Note: Values given in this table are for power supply sizing and should not be used to estimate chip power consumption. Under certain conditions, the Core, A9 and HFE supplies can each experience current transients of up to 4 A for a duration of tbd microseconds.											

29.5 DC Electrical Characteristics

Table 29-7 and Table 29-8 list the DC electrical characteristics of LS1024A device.

Table 29-7 LVCMOS DC Electrical Characteristics

Parameter		Condition		Minimum	Typical	Maximum	Units
V_{tol}	Tolerant external voltage for PAD	V_{DD} Power Off				5.5	V
						3.6	
		VDD Power On (Note 1)	V_{DD}=3.3 V			5.5	V
						3.6	
			V_{DD}=2.5 V			5.5	
						3.6	
V_{ih}	High Level Input Voltage						
	LVCMOS Interface			0.7 V_{DD}		V_{DD}	V
V_{il}	Low Level Input Voltage						
	LVCMOS Interface			0		0.3 V_{DD}	V
ΔV	Hysteresis Voltage			0.1 V_{DD}			V

Table 29-7 LVCMOS DC Electrical Characteristics (continued)

Parameter		Condition	Minimum	Typical	Maximum	Units
I_{ih}	High Level Input Current					
	Input Buffer	$V_{in}=V_{DD}$ (V_{DD}=min)	-10		10	uA
	Input Buffer with pull-down		45 (Note 2)			uA
I_{il}	Low Level Input Current					
	Input Buffer	$V_{in}=V_{SS}$ (V_{ss}=min)	-10		10	uA
	Input Buffer with pull-up				-45 (Note 2)	uA
V_{oh}	Output high Voltage (Note 3)	Ioh=-2 mA	$0.8xV_{DD}$			V
		Ioh=-4 mA				
		Ioh=-8 mA				
		Ioh=-12 mA				
V_{ol}	Output Low Voltage (Note 3)	Iol=2 mA			$0.2xV_{DD}$	V
		Iol=4 mA				
		Iol=8 mA				
		Iol=12 mA				
I_{oz}	Tri-state Output Leakage Current	$V_{out}=V_{SS}$ or V_{DD}	-10		10	uA
C_{IN}	Input Capacitance	Any Input and Bidirectional Buffers			5	pF
C_{OUT}	Output Capacitance	Any Output Buffer			5	pF

NOTES:
1. The V_{tol} max value as 5.5 V in power On mode is for 5 V tolerant I/O (LVCMOS).
   - The V_{tol} max value as 3.6 V in power On mode is for 3.3 V fail-safe I/O (LVCMOS).
2. The values of I_{oh} & I_{ol} are valid only for 3.3 V range.
3. The value of I_{oh} and I_{ol} is for minimum driver strength. The detailed driver strength per LVCMOS cell.

NOTE: For various signal levels of SerDes differential signal and reference clock I/O see Section , Section 17.4 and Section 23.3.

30 Power Management

This section describes the Power Management features.

The Cortex®-A9 and its subsystem (including L2 and Coresight) support power gating options, which allow power-down of each CPU separately, both CPUs, entire A9MP, or the whole A9 subsystem (as in hibernate mode). When the Cortex-A9 are powered down, the PMU can be started.

30.1 Power Management Features

- Clock shut down of major blocks
- Suspend mode for USB/SATA/PCIE PHYs
- DDR self-refresh with automatic memory and controller clock gating
- Dynamic frequency scaling of major system clocks (A9, L2cc, AXI & PPFE and so on)
- Voltage islanding for A9 MPU and PPFE, with support for typical and overdrive operating voltage for each independently
- Power gating of A9 Subsystem and CPU cores
- Support for dynamic voltage switching between typical and overdrive levels
- Software can implement power saving modes, for example sleep or hibernate, as required by the system application

30.2 Power Management Functional Description

30.2.1 Low Power Implementation

30.2.1.1 Block Level Clock Gating

Each major block has separately configurable programmable stop-clock functionality, which can be activated and de-activated dynamically. The software configuration registers are located in clock and reset block.

The DDR controller supports several low power modes, including power down and self-refresh modes, enabled/disabled manually by software, or automatically by hardware when auto mode is enabled. In the deepest low power state, DDR memory is put in self-refresh and clocks to DDR controller and DDR memory are gated off. In auto mode, power down modes are enabled when DDR controller is idle, and exited when a command enters its queue. The software configuration registers for DDR power down are located in the DDR controller.

30.2.1.2 Block Level Power-Down Modes

USB, SATA and PCIe PHYs support suspend and power down mode. In these modes, the PHY PLLs and recovered line clocks are shutdown, major functions are powered off, and power is reduced to minimum leakage.

PCIe supports power management functionality that is described in PCI Bus Power Management Specification 1.2 and Advanced Configuration/Power Management Specification 2.0.

30.2.1.3 Dynamic Frequency Scaling

Frequencies of internally generated clocks (sourced from PLLs in clock and reset block) can be changed, to dynamically adjust clock rates based on block activities.

Separate clock rate control for each clock, but clock ratio relationships between synchronous domains must be maintained as described in clocking section of the device documentation.

30.2.1.4 Voltage Islanding and Power Gating

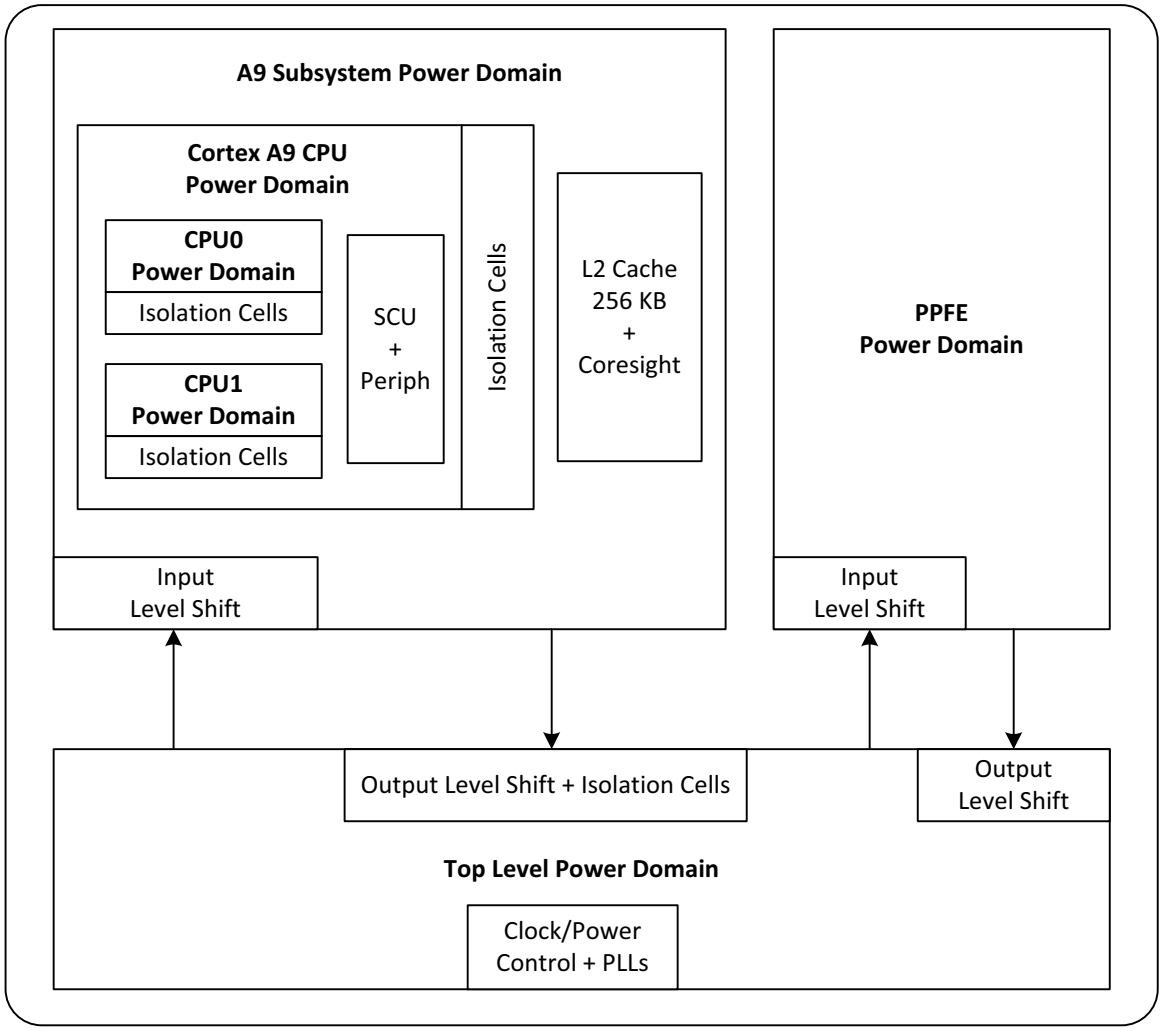
Three voltage islands are implemented: each of the A9 subsystem and PPFE has a dedicated power domain, and the rest of the device has one power domain.

Power gating is implemented for the whole A9 subsystem (including L2 Cache, and Coresight logic), for the Cortex-A9 MPU by itself (CPUs + SCU), and for each of the two CPU cores as well.

Table 30-1 Power Domains Definitions

Block	Domain	Frequency	Voltage (V)	Power Island (Shut-off)	Note	Devices	Tolerance
CPU0/CPU1	A9 VDD	1.2 GHz	1.24	Y (independently)		LS1024AS*x*7MLA	+/- 3%
		900 MHz	1.2	Y (independently)		LS1024AS*x*7JLA	+/- 5%
		650 MHz	1.1	Y (independently)		LS1024AS*x*7ELA	+/- 5%
A9 MPU	A9 VDD		1.13	Y	Incl: CPUs, SCU, A9 Peripherals	LS1024AS*x*7MLA	+/- 3%
			1.1	Y		LS1024AS*x*7JLA	+/- 5%
			1.1	Y		LS1024AS*x*7ELA	+/- 5%
A9 Subsystem	A9 VDD		1.13	Y	Incl: A9 MPU, L2cc, Coresight	LS1024AS*x*7MLA	+/- 3%
			1.1	Y		LS1024AS*x*7JLA	+/- 5%
			1.1	Y		LS1024AS*x*7ELA	+/- 5%
PPFE	PPFE VDD	500 MHz	1.24	N		LS1024AS*x*7MLA	+/- 3%
		500 MHz	1.2	N		LS1024AS*x*7JLA	+/- 5%
		400 MHz	1.1	N		LS1024AS*x*7ELA	+/- 5%
Top Level	Top VDD		1.13	N		LS1024AS*x*7MLA	+/- 3%
			1.1	N		LS1024AS*x*7JLA	+/- 5%
			1.1	N		LS1024AS*x*7ELA	+/- 5%

Figure 30-1 Power Islanding Diagram



30.2.1.5 Dynamic Voltage Scaling

A9 subsystem and PPFE voltage levels can dynamically switch, along with frequency scaling. For example, if A9 MPU is running full capacity at 900 MHz, 1.2 V, it can dynamically switch to 650 MHz (or lower), and reduce supply to 1.1 V, when loading is reduced. Software can control on-board voltage regulators, through GPIO, to adjust the levels based on the desired clock frequencies.

30.2.2 Power Management Unit (PMU) Interrupts

The following triggers are used by the PMU to come out of power down. Each trigger can be separately masked.

- PPFE interrupt (+ Wake-on-LAN)
- PCIe interrupt
- USB interrupt
- SATA interrupt
- UART interrupt

- Any GPIO interrupt
- Timer interrupt

Table 30-2 lists the PMU interrupts.

Table 30-2 PMU Interrupts

Bit	Interrupt			P/L
0	GPIO0_IRQ	GENERAL IRQ 0 also can be set by GPIO 0 change	GPIO	PL
1	GPIO1_IRQ	GENERAL IRQ 1 also can be set by GPIO 1 change	GPIO	PL
2	GPIO2_IRQ	GENERAL IRQ 2 also can be set by GPIO 2 change	GPIO	PL
3	GPIO3_IRQ	GENERAL IRQ 3 also can be set by GPIO 3 change	GPIO	PL
4	GPIO4_IRQ	GENERAL IRQ 4 also can be set by GPIO 4 change	GPIO	PL
5	GPIO5_IRQ	GENERAL IRQ 5 also can be set by GPIO 5 change	GPIO	PL
6	GPIO6_IRQ	GENERAL IRQ 6 also can be set by GPIO 6 change	GPIO	PL
7	GPIO7_IRQ	GENERAL IRQ 7 also can be set by GPIO 7 change	GPIO	PL
8	TIMER0_IRQ	General Purpose Timer 0 Interrupt Indication	TIM	P
9	TIMER1_IRQ	General Purpose Timer 1 Interrupt Indication	TIM	P
10	TIMER2_IRQ	General Purpose Timer 2 Interrupt Indication	TIM	P
11	TIMER3_IRQ	General Purpose Timer 3 Interrupt Indication	TIM	P
12	ZDS_IRQ or MSIF_IRQ	Interrupt indication on the Le88536 external device or ProSLIC external device	ZDS MSIF	L
13	RTC_ALM_IRQ	RTC – ALM	RTC	P/L
14	RTC_PRI_IRQ	RTC – PRI	RTC	L
15	PCIe0_IRQ	PCIe 0 Controller Interrupt Indication	PCIEC	L
16	PCIe1_IRQ	PCIe 1 Controller Interrupt Indication	PCIEC	L
17	SATA_IRQ	SATA Controller Interrupt	SATAC	L
18	SATA_MSI_IRQ	SATA Controller msi_req Interrupt	SATAC	L
19	USB2p0_IRQ	USB2.0 Controller Interrupt	USBC0	L
20	USB3p0_IRQ	USB3.0 Controller Interrupt	USB3SubS	PL
21	HFE_0_IRQ	PPFE’s HIF Interrupt Indication	PPFE	L
22	WOL_IRQ	Wakeup On LAN Interrupt Indication from all GEM	PPFE	P
23	CSS_IRQ	CSS NIRQ internal interrupt controller Indication	CSS	L
24	DUS_DMAC_IRQ	DMAC Interrupt Indication	DUS	L
25	DUS_UART0_IRQ	UART0 Interrupt Indication	DUS	L
26	DUS_UART0_IRQ UART_S2_IRQ	UART1 Interrupt Indication or LS UART Interrupt Indication**	DUS UARTCORE	L L
27	HFE_1_IRQ	PPFE’s HIF No Copy Interrupt Indication	PPFE	L
28	USB3p0_PM	USB3.0 PME Interrupt Indication	USB3SubS	L

Table 30-2 PMU Interrupts (continued)

29	PTP0_IRQ	Processor to Processor Interrupt (set under firmware control) – Set via register at offset 0x164 and clear at 0x160	GPIO	L
30	PTP1_IRQ		GPIO	L
31	PTP2_IRQ		GPIO	L

The status and control registers are located in GPIO block – one set for PPFE and one for CSS.

31 Hardware Initialization

This section describes the boot options and power up sequence of the LS1024A device.

31.1 Internal Boot ROM

This section describes the Internal Boot ROM (IBR) for the LS1024A device. The device has three stage booting:

- 1st Stage - IBR
- 2nd Stage - Microloader
- 3rd Stage - Barebox/U-Boot

After power on Reset, IBR works as First stage Boot Loader. IBR copies the Microloader from the selected Boot Device. The following options for Boot Devices are supported. Selection is done from the Boot Strap Register.

- Low Speed SPI Boot
- I^2C Boot
- NOR Boot
- Fast SPI Boot
- Fast UART Boot
- SATA Boot (Needs external clock)

Microloader is a Second Stage Boot loader. The microloader performs the following functions:

- Low level board initialization (DDR, PLL and Clock Initialization and so on)
- Download 3rd stage boot loader (U-Boot) from the selected boot device. An option to use different boot device by the Microloader to download Barebox/U-Boot is available.
- Microloader supports few or all boot modes supported by IBR as per the requirement and size limitation.

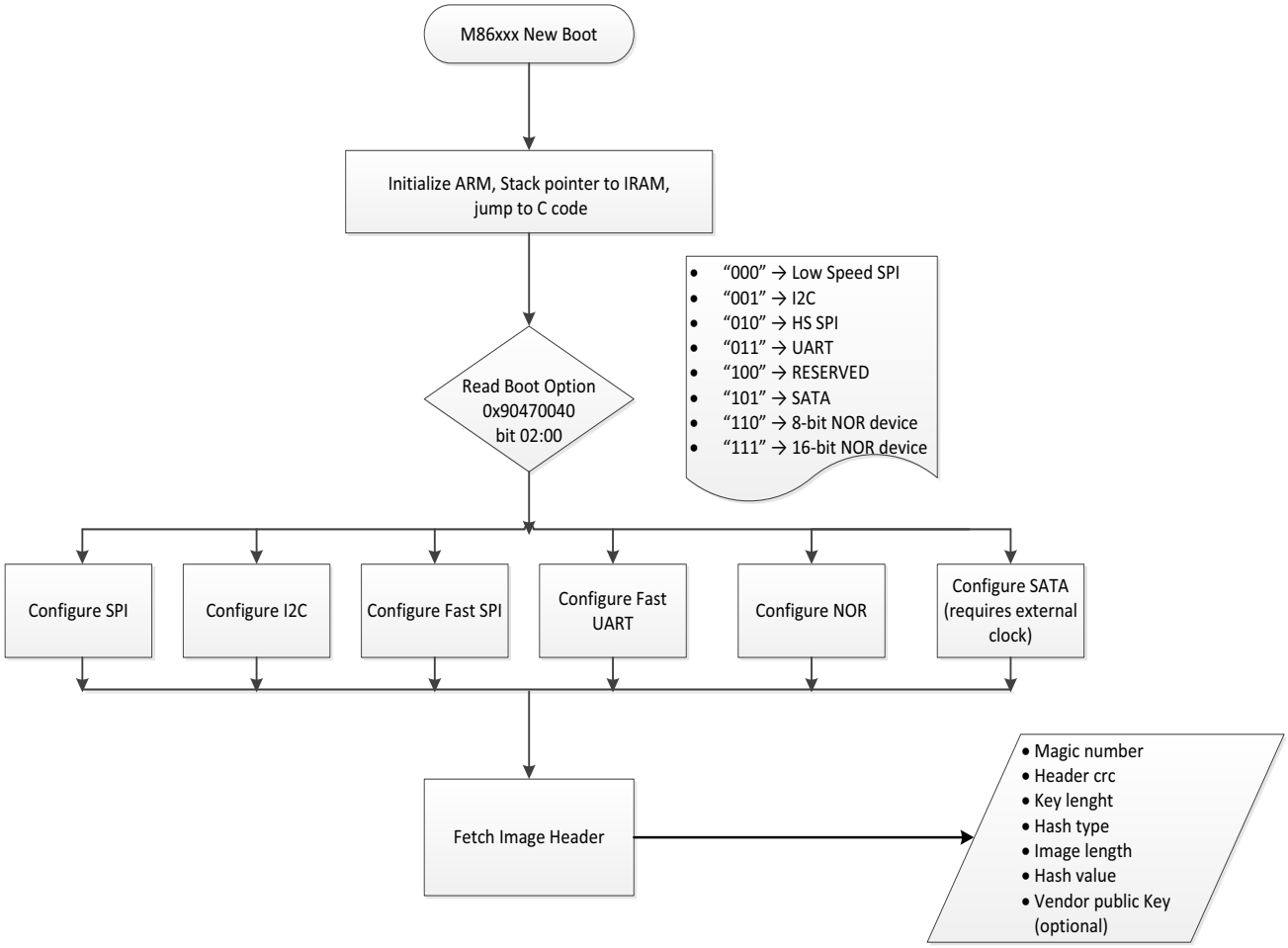
31.1.1 Boot Modes

LS1024A IBR supports the following boot modes:

- Internal Boot Non Secure: This is a normal boot mode where 3 stage booting takes place, but no security is involved.
- Internal Boot Secure: This is a secure boot mode where 3 stage booting takes place, and all the boot images (Microloader / U-Boot / Linux) get authenticated using Security Engine.

Figure 31-1 illustrates LS1024A Boot Flow diagram.

Figure 31-1 LS1024A Boot Flow



31.1.2 LS1024A Boot Options

IBR boot options are selected from expansion bus signals, the device supports 26 input bootstrap pins. EXP_A[25:0] are used as bootstraps for hardware and software. By default, all EXP_A bits are pulled down.

During reset, EXP_A[25:0] are not driven by LS1024A and they can be set to any configured value via external pull-ups or internal pull-downs.

Following reset, the device drives these pins to support Expansion Bus access. The previous latched value is already stored in a software accessible register from which the value can be read but not changed.

31.1.2.1 Hardware Boot Option

Table 31-1 Bootstraps for Hardware

Bits	Bootstraps for Hardware
15	Tri-state Coresight I/F – EXP_A[15] ‘0’ – Drive Interface ‘1’ – Tri-state (useful if interface is not used or when used as GPIO)
14	EXP_DM driving mode – EXP_A[14] ‘0’ – bus is driven only during writes ‘1’ – bus is driven all time
13	GEM2 Mode – EXP_A[13] ‘0’ – GEMAC (PPFE) ‘1’ – I2S/CSS
12	SerDes2 Mode – EXP_A[12] ‘0’ – SATA1 ‘1’ – SGMII
11	SerDes1 Mode – EXP_A[11] ‘0’ – PCIe1 ‘1’ – SATA0
10	L2CC-AXI Sync Mode – EXP_A[10] ‘0’ – L2CC and AXI clocks are Asynchronous ‘1’ – L2CC and AXI clocks are Synchronous and balanced (the exact ratio is configuration option in clock and reset block)
9:8	System PLL Refclk Select – EXP_A[9:8] ‘00’ – Reserved ‘01’ – MUST NOT BE USED FOR PROPER OPERATION ‘10’ – MUST NOT BE USED FOR PROPER OPERATION ‘11’ – SerDes XTAL (PS_XI/XO) is selected clock source (24/48MHz – depends on bit 7)
7	SerDes OSC PAD (PS_XI/XO) – Reference clock frequency selection bootstrap (inverted value of SF1) – EXP_A[7] ‘0’ – 30MHz ~ 50MHz ➔ should be selected when 48MHz crystal/clock is used ‘1’ – 15MHz ~ 30MHz ➔ should be selected when 24MHz crystal/clock is used Note: SF0 is tied to 1 in GPIO block and might later on be controlled during DFT
6	SerDes OSC PAD (PS_XI/XO) – Crystal Enable bootstrap (E0) – EXP_A[6] ‘0’ – Crystal input mode (connect crystal to XI and XO) ‘1’ – Input clock mode (connect clock to XI and leave XO open)
5	Not used. Should be set as bit [7]
4	Reserved
3	TDM CLK OUT Enable bootstrap – EXP_A[3] ‘0’ – TDM clock is driving by external device ‘1’ – TDM clock is driven by C2K
2:0	Status of BOOT_OP bootstrap – EXP_A[2:0]. See table Table 31.1.2

Table 31-2 lists the LS1024A Boot Option Bits.

Table 31-2 LS1024A Boot Option Bits

BOOT_OP[2:0]	Outcome
000	LS SPI
001	I2C
010	Fast SPI
011	UART
100	Reserved
101	SATA
110	8-bit NOR device
111	16-bit NOR device

31.1.2.2 Software Boot Option

31.1.2.2.1 Fast UART Speed

Table 31-3 Extended Boot Option Bits – UART Boot Baud Rate

BIT[16]	Outcome
0	115200
1	921600

31.1.2.2.2 Secure Boot Option

If Debug mode is enabled, then Secure Boot Option is derived from this bit.

Table 31-4 Extended Boot Option Bits – Secure Boot Option

BIT[17]	Outcome
0	Disable
1	Enable

31.1.2.2.3 SPI Address length

LS1024A IBR supports SPI devices supporting 2 byte, 3 byte and 4 byte address cycle.

Table 31-5 Extended Boot Option Bits – SPI Address Length

BOOT_OP[19:18]	Outcome
00	N/A
01	2 Byte Address

Table 31-5 Extended Boot Option Bits – SPI Address Length (continued)

BOOT_OP[19:18]	Outcome
10	3 Byte Address
11	4 Byte Address
NOTES: • LS SPI Boot Mode supports 2/3/4 Byte address SPI devices. • Fast SPI Boot Mode only supports 3 Byte address devices.	

31.1.2.2.4 Extended ID Read Select

Table 31-6 Extended ID Read Select

BOOT_OP[19:18:17]	Outcome
000	32 KB
001	64 KB
010	128 KB
011	256 KB
100	512 KB
101	1024 KB
110	2048 KB
111	2048 KB
NOTE: If Value of Bit[19:17] is greater than 2 and Page size is 512 Byte then Block size is equal to 16 KB.	

31.1.2.2.5 SPI SC Polarity

Table 31-7 Extended Boot Option Bits – SPI SC Polarity

BOOT_OP[20]	Outcome
0	-ve
1	+ve

31.1.2.2.6 Clock Options

LS1024A IBR supports PLL enable as well as disable mode.

Table 31-8 Extended Boot Option Bits – Clock Option

BIT[21]	Outcome
0	PLL Disable
1	PLL Enable

31.1.3 Secure Boot Settings

In this mode, OTP memory byte 0 and byte 1 are read and depending upon the value security settings are applied.

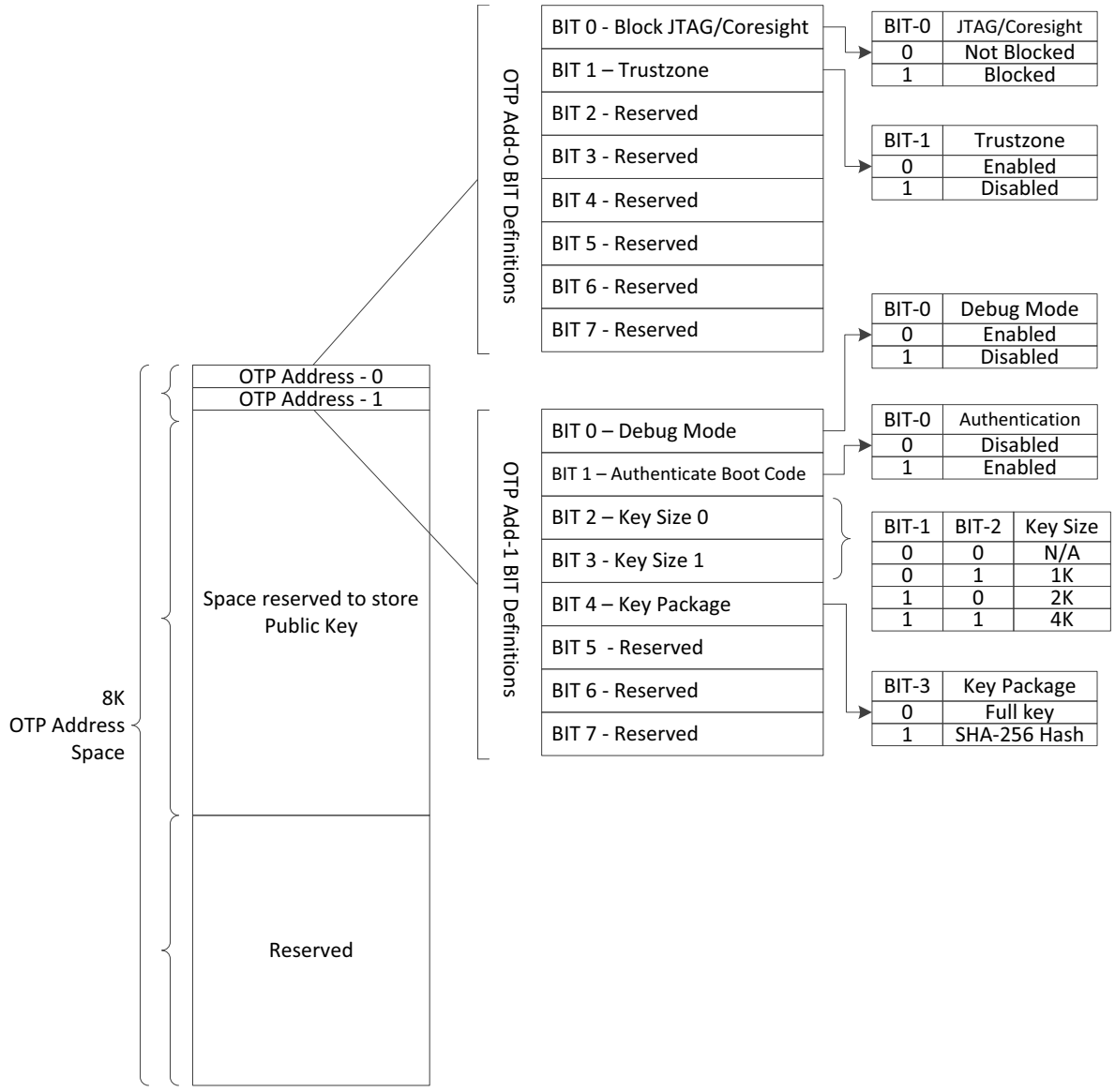
Table 31-9 Secure Boot Configuration Layout

Byte	Bits	Description
Byte 0	Bit [0]	JTAG/Coresight. 0: Not Blocked. 1: Blocked.
	Bit [1]	Trustzone. 0: Disabled. 1: Enabled.
Byte 1	Bit [0]	Debug mode. 0: Enable. 1: Disable.
	Bit [1]	Authenticate boot code. 0: Disable. 1: Enable.
	Bit [3:2]	Key size. 00: N/A. 01: 1K. 10: 2K. 11: 4K.
	Bit [4]	Key Package. 0: Full. 1: SHA-256 hash.

31.1.4 OTP Layout

Figure 31-2 explains the Proposed Layout of OTP area.

Figure 31-2 OTP Layout



31.1.5 Reference Clock Options

LS1024A IBR supports PLL enable as well as disable mode. The following reference clock options are available:

- 24 MHz (SerDes Xtal)
- 48 MHz (SerDes Xtal)

For reference clock option bits, see the bits [10:5] descriptions in Table 31-1.

Table 31-10 Reference Clock Option Bits

	Bit – 5	Bit – 7	Bit – [9:8]
24 MHz	1	1	0x3
48 MHz	0	0	0x3

31.2 Power Sequence

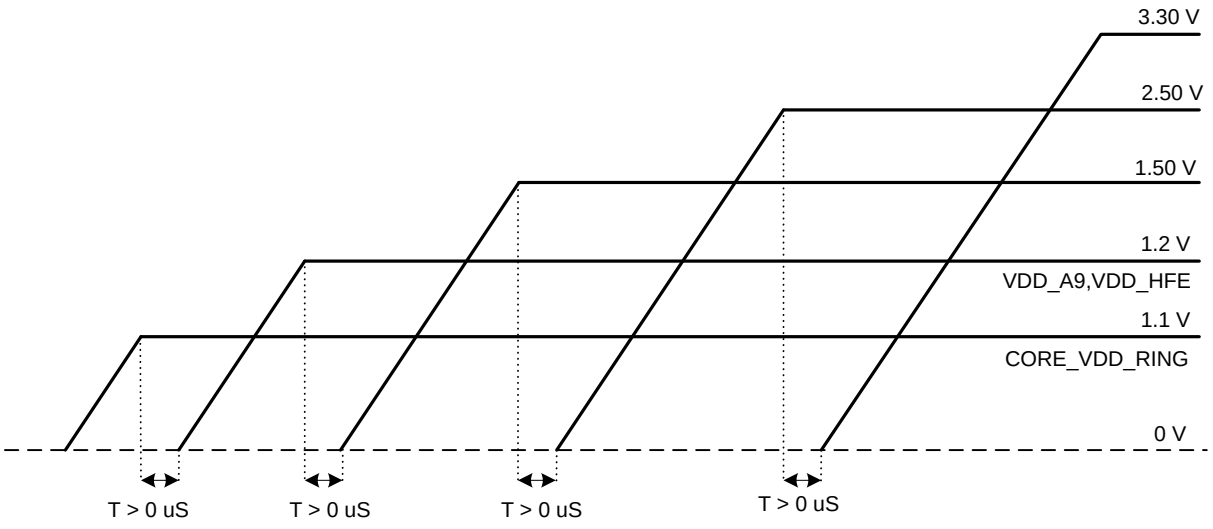
To prevent shoot through current from power supply and glitch on the pads during power-up and power-down periods, following power sequences should be followed.

The system reset signal RESET_N should remain asserted (low) at least for10µs after all power supplies are established and the chosen reference clock is running.

31.2.1 Power Up Sequence

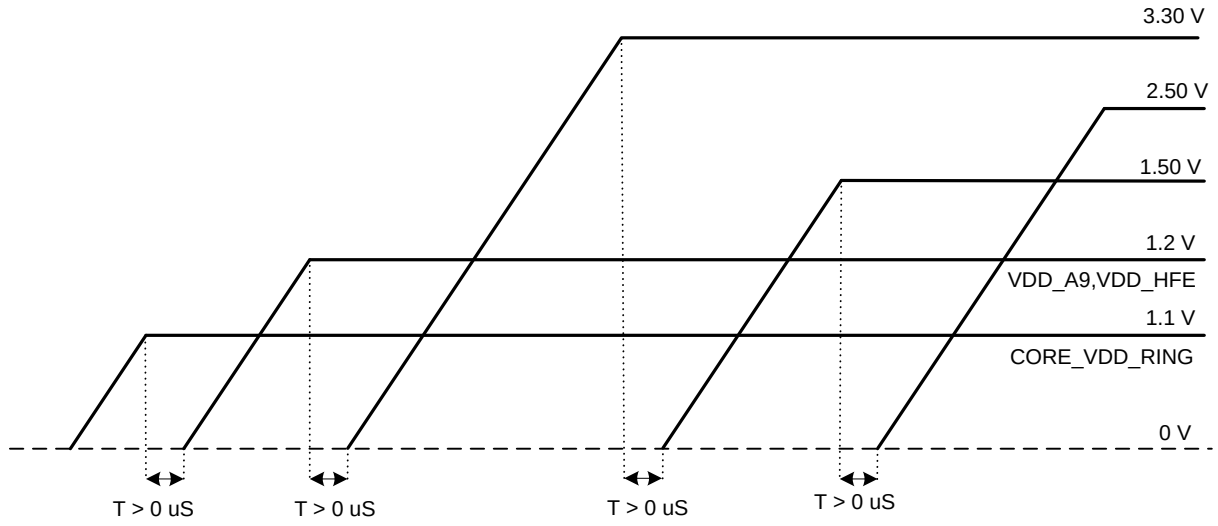
- Recommended Power-up sequence: supplies come up relatively the same time, however follow a low to high voltage sequence such as 1.1, 1.2, 1.50, 2.50, 3.30 V. The time between supplies should be greater than 0 µS. See Figure 31-3, Recommended Power Up Sequence.
- Other options available for Power-up sequence are as follows:
  - 3.3V comes up before 1.5V and no importance on the 1.5 and 2.5 sequence. Supplies come up relatively the same time in the following sequence 1.1, 1.2, 3.3, 1.5, 2.5 or 1.1, 1.2, 3.3, 2.5, 1.5. The time between supplies should be greater than 0 uS. See Figure 31-4, Power up Sequence, 3.3 V before 1.5 V and Figure 31-5, Power Up Sequence, 3.3 V before 2.5 V.
  - 3.3V comes up first in the following sequence 3.3, 1.1, 1.2, 1.5, 2.5. The time between 3.3V stable to 1.1 V stable should be less than 1mS. The remaining supplies should be greater than 0 µS. See Figure 31-6, Power Up Sequence, 3.3 V before 1.1 V.

Figure 31-3 Recommended Power Up Sequence



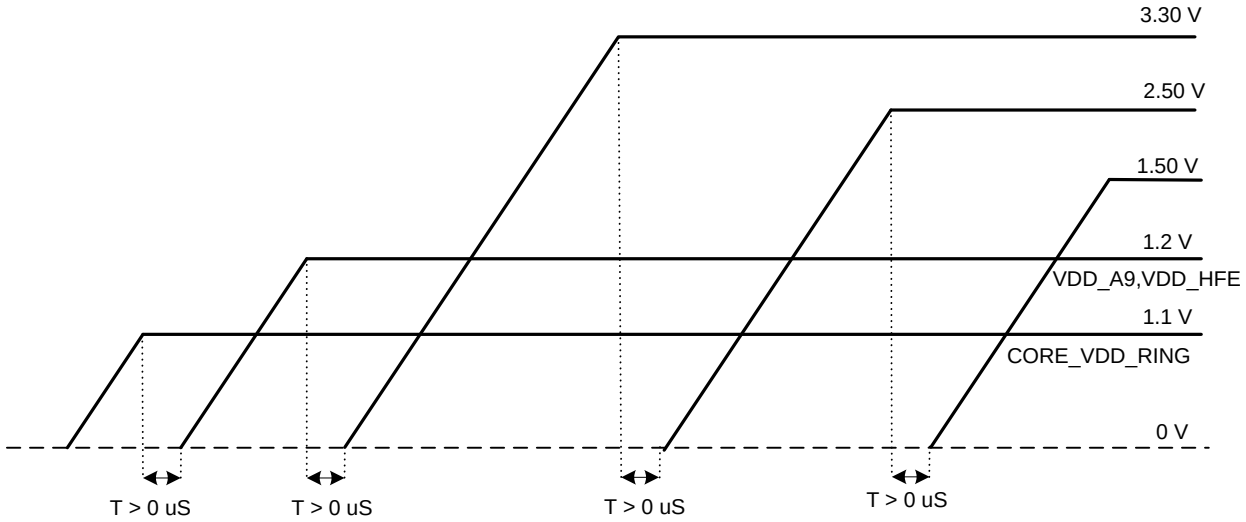
Power Up Sequence, Low To High

Figure 31-4 Power up Sequence, 3.3 V before 1.5 V



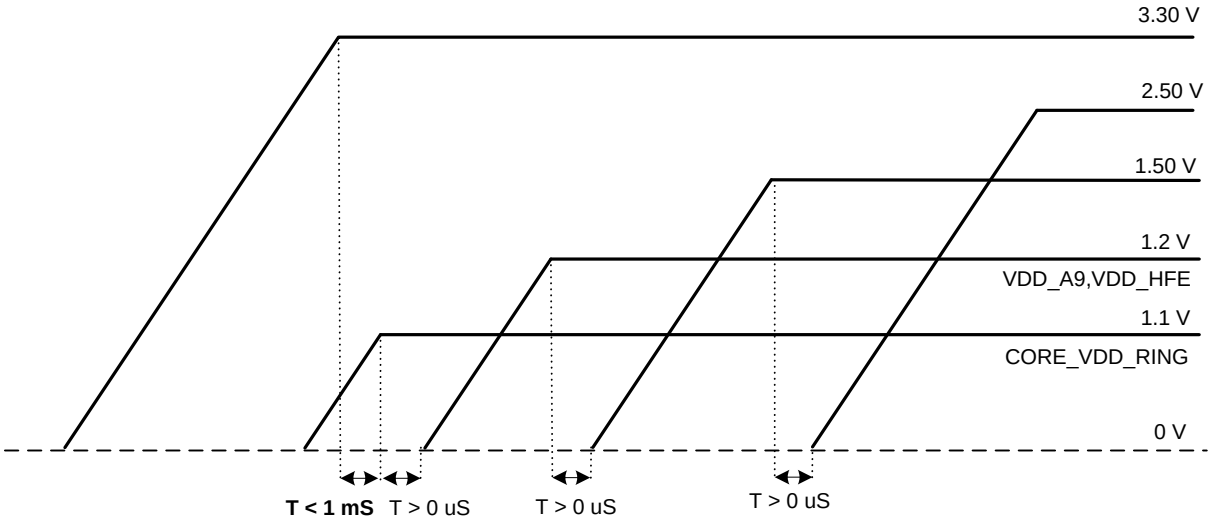
Power Up Sequence, 3.3V Before 1.5V

Figure 31-5 Power Up Sequence, 3.3 V before 2.5 V



Power Up Sequence, 3.3V Before 2.5V

Figure 31-6 Power Up Sequence, 3.3 V before 1.1 V



Power Up Sequence, 3.3V Before 1.1V

In case of USB 3.0 PHY, the power supplies can be brought up in any sequence provided they come up at relatively the same time. The 3.3 V may come up earlier than the 1.1 V but the maximum time the high supply (VDD330/vph) is applied before the low supply (DVDD/vp/vptx) is 10 mS.

31.2.2 Power Down Procedure

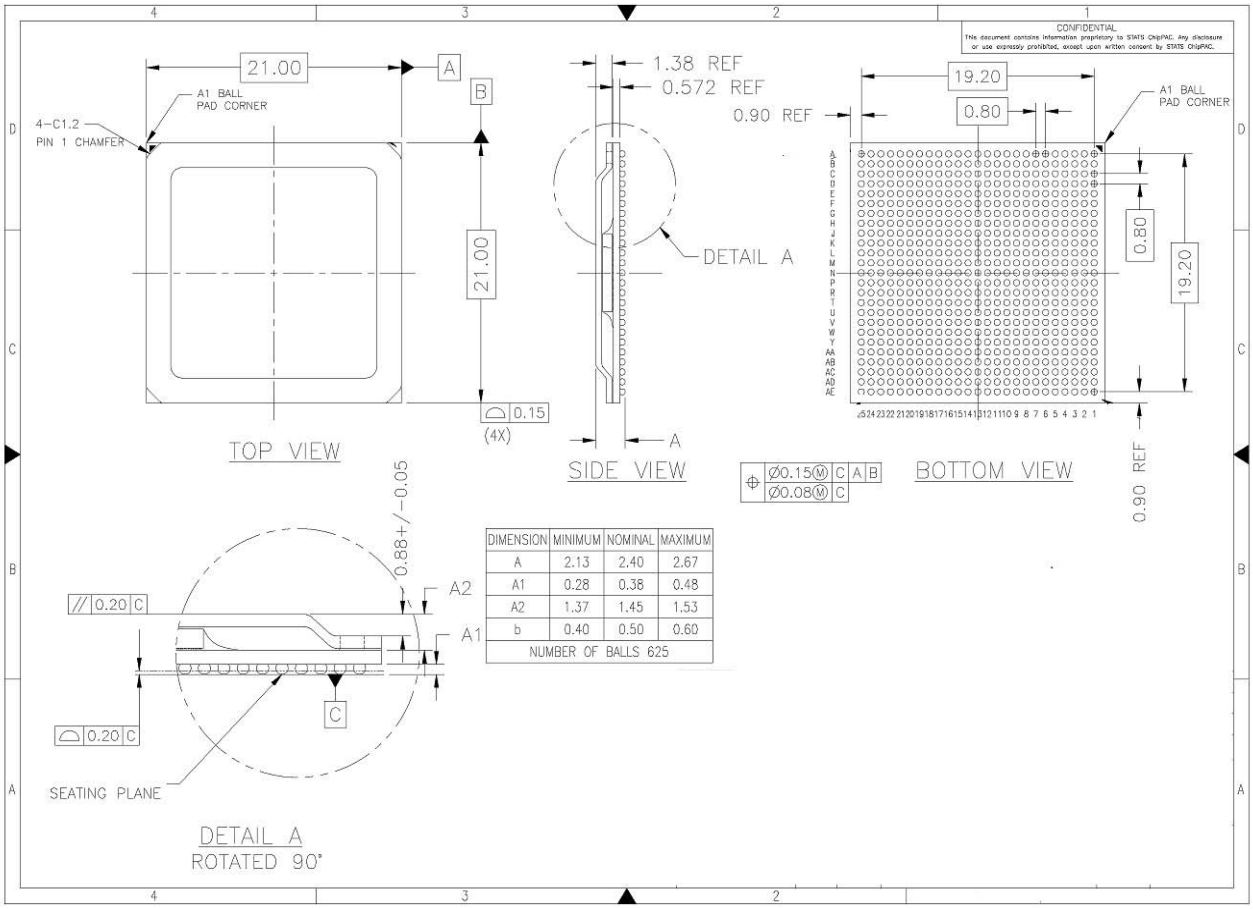
The power down sequence is the reverse of the power up sequence.

32 Package Dimensions

This section gives the LS1024A package dimensions, tray and reflow details.

The LS1024A device is housed in a 21 mm by 21 mm Flip Chip Ball Grid Array with Heat Slug (FCPBGAH) package. It consists of a 1-2-1 layers, 0.972 mm thick laminate substrate with an array of 625 BGA balls spaced at 0.8 mm (a 0.8 mm pitch). Package dimensions are shown in Figure 32-1.

Figure 32-1 Package Drawing



33 Ordering Information

This section gives the LS1024A ordering information.

Table 33-1 lists the legacy part numbers for existing designs. New designs should use LS1024A part numbers as listed in Table 33-2.

Table 33-1 Legacy M86XX Part Information

Version	VoIP Channels	DPI	DECT	Prototype Part Number	Production Part Number	IPSEC perf.	CPU freq
C2000 dual core 1.2 GHz							
M86207	16	Yes	No	M86208G12P	M86207G12	2 Gbps	1.2 GHz
M86206	16	No	Yes		M86206G12	2 Gbps	1.2 GHz
M86204	8	Yes	Yes		M86204G12	300 Mbps	1.2 GHz
M86203	8	Yes	No		M86203G12	300 Mbps	1.2 GHz
M86202	8	No	Yes		M86202G12	300 Mbps	1.2 GHz
M86201	8	No	No		M86201G12	300 Mbps	1.2 GHz
C2000 dual core 900 MHz							
M86297	16	Yes	No	M86298G12P	M86297G12	2 Gbps	900 MHz
M86296	16	No	Yes		M86296G12	2 Gbps	900 MHz
M86294	8	Yes	Yes		M86294G12	300 Mbps	900 MHz
M86293	8	Yes	No		M86293G12	300 Mbps	900 MHz
M86292	8	No	Yes		M86292G12	300 Mbps	900 MHz
M86291	8	No	No		M86291G12	300 Mbps	900 MHz
C2000 dual core 650 MHz							
M86268	16	Yes	Yes	M86268G12P	M86268G12	2 Gbps	650 MHz
M86267	16	Yes	No		M86267G12	2 Gbps	650 MHz
M86266	16	No	Yes		M86266G12	2 Gbps	650 MHz
M86265	16	No	No		M86265G12	2 Gbps	650 MHz
M86264	8	Yes	Yes		M86264G12	300 Mbps	650 MHz
M86263	8	Yes	No		M86263G12	300 Mbps	650 MHz

Table 33-2 LS1024A Family Ordering Information

Version	VoIP Channels	DPI	DECT	Legacy Part Number	Freescale QorIQ Part Number	IPSEC perf.	CPU freq
LS1024A dual core 1.2 GHz							
M86208	16	Yes	Yes	M86208G12	LS1024ASE7MLA	2 Gbps	1.2 GHz
M86205	16	No	No	M86205G12	LS1024ASN7MLA	2 Gbps	1.2 GHz
LS1024A dual core 900 MHz							
M86298	16	Yes	Yes	M86298G12	LS1024ASE7JLA	2 Gbps	900 MHz

Table 33-2 LS1024A Family Ordering Information

M86295	16	No	No	M86295G12	LS1024ASN7JLA	2 Gbps	900 MHz
LS1024A dual core 650 MHz							
M86262	8	No	Yes	M86262G12	LS1024ASE7ELA	300 Mbps	650 MHz
M86261	8	No	No	M86261G12	LS1024ASN7ELA	300 Mbps	650 MHz

How to Reach Us:

Home Page:
freescale.com

Web Support:
freescale.com/support

Document Number: LS1024A
Rev. 0, 09/2014

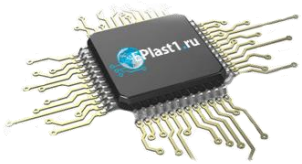
Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits,General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

Телефон: 8 (812) 309 58 32 (многоканальный)
Факс: 8 (812) 320-02-42
Электронная почта: org@eplast1.ru
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.