## GENERAL DESCRIPTION

The XRT85L61 is an integrated E1, T1, 64KHz Centralized Clock interface for T1 (1.544Mbps) 100Ω, E1 (2.048Mbps) 75Ω or 120Ω applications.

The XRT85L61 extracts either 2048kHz or 1544 kHz clock signals from an E1 (2.048 MHz), T1 (1.544 Mhz) inputs respectively or 64 KHz, 8kHz or 400 Hz clock signals from the 64kHz reference clock input.

The XRT85L61 includes an on-chip crystal-less jitter attenuator with 32 bit FIFO that can either be enabled or disabled.

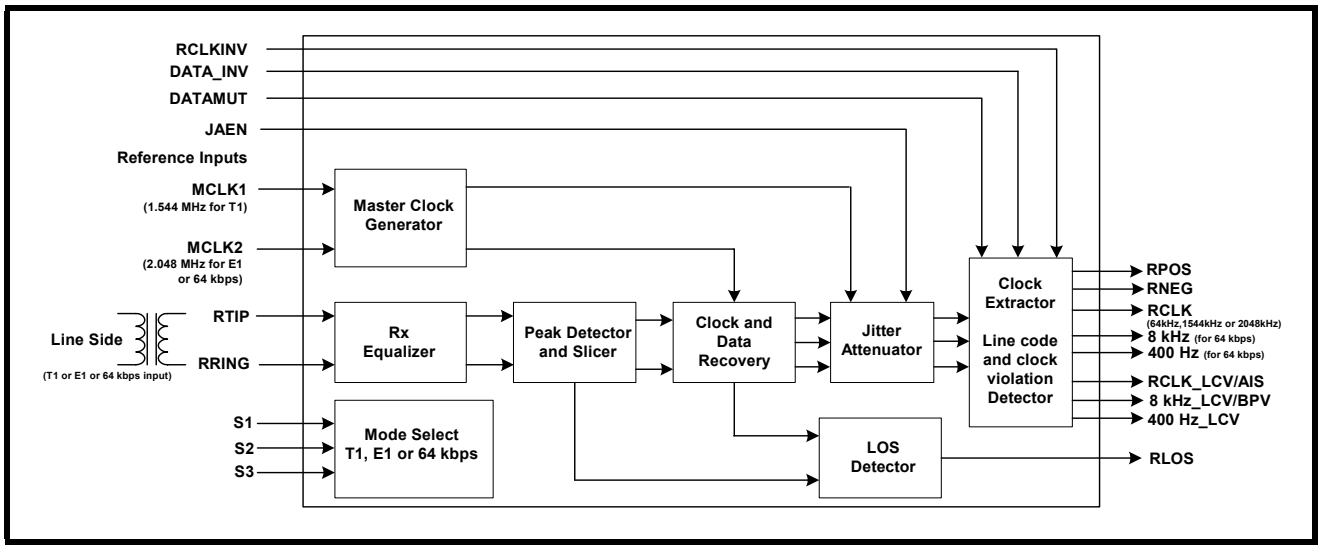
### FEATURES

- Fully integrated single chip solution for E1,T1 or 64 kHz clock synchronization applications.
- Extracts 2048 kHz, 1544 kHz clock and data components
- Extracts 64 KHz and 8 kHz, 400 Hz clock information
- Line Code Violation alarms
- On-chip digital clock recovery circuit
- Supports 75Ω and 120Ω (E1), 100Ω (T1) applications.
- Crystal-less digital jitter attenuator with 32-bit FIFO that can either be enabled or disabled
- Receive loss of signal (RLOS) output
- Meets Telcordia GR-1244-CORE Section 3.4.1 R3-27 specification
- Meets or exceeds T1 and E1 specifications in ITU G.703, G.775
- Single +3.3V Supply Operation
- Logic inputs accept either 3.3 V or 5 V levels
- 28 pin TSSOP package

### *APPLICATIONS*

- Universal Clock Synchronization for G.703 Telecom Formats
- T1/E1 Line Receiver with Clock and Data Recovery
- DSLAM

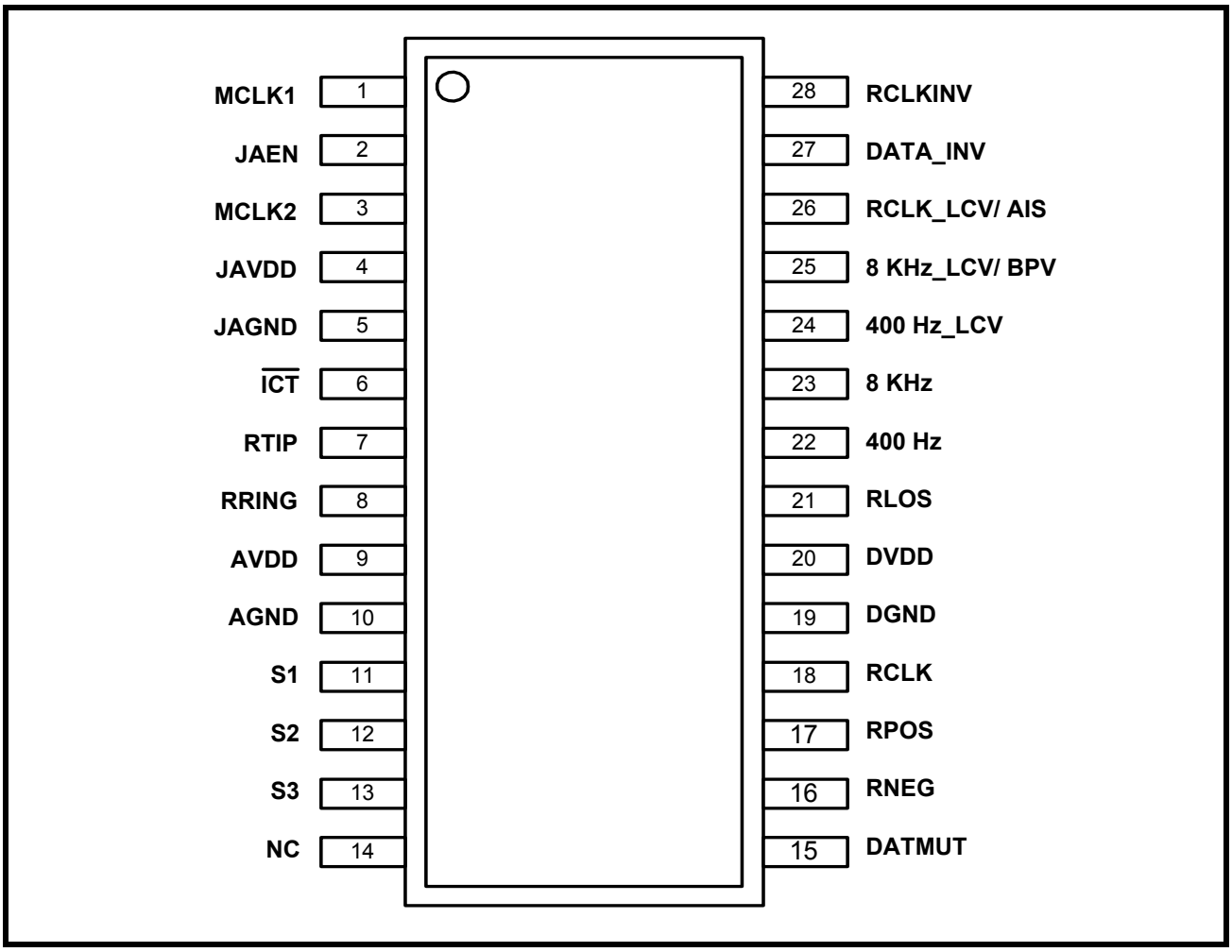
**FIGURE 1. BLOCK DIAGRAM OF THE XRT85L61**



## ORDERING INFORMATION

| PART NUMBER | PACKAGE | OPERATING TEMPERATURE RANGE |
|---|---|---|
| XRT85L61IG | 28 Lead TSSOP | -40°C to +85°C |

**FIGURE 2. PIN OUT OF THE XRT85L61**



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## PIN DESCRIPTIONS

<table>
<tr><th>PIN #</th><th>SYMBOL</th><th>TYPE</th><th>DESCRIPTION</th></tr>
<tr><td>1</td><td>MCLK1</td><td>I</td><td>Reference T1 Clock input:<br>This signal is an independent 1544 kHz clock with accuracy better than ± 32 ppm and duty cycle within 40% to 60%. This clock provides timing source for the PLL clock recovery circuit in T1 mode. This signal must be available for the device to operate.</td></tr>
<tr><td>2</td><td>JAEN</td><td>I</td><td>Jitter Attenuator Enable:<br>Tie this pin “High” to enable the Jitter Attenuator. When enabled, a 32 bit FIFO is included in the data path for all modes of operation.<br>NOTE: Internally Pulled down with 50 kΩ resistor</td></tr>
<tr><td>3</td><td>MCLK2</td><td>I</td><td>Reference E1 and 64 kHz Clock Input:<br>This signal is an independent 2048 kHz clock with accuracy better than ± 50 ppm and duty cycle within 40% to 60%. This clock provides timing source for the PLL clock recovery circuit in E1 and 64 kHz mode. This signal must be available for the device to operate.<br>NOTE: To reduce intrinsic jitter when JA is enabled, it is recommended to have reference clock with an accuracy of ± 25 ppm or better.</td></tr>
<tr><td>4</td><td>JAVDD</td><td>***</td><td>VDD for Jitter Attenuator (3.3V ± 5%)</td></tr>
<tr><td>5</td><td>JAGND</td><td>***</td><td>Jitter Attenuator Ground</td></tr>
<tr><td>6</td><td>$\overline{\text{ICT}}$</td><td>I</td><td>In circuit Testing<br>When this pin is grounded, all output pins are Tri-stated for testing purposes.<br>NOTE: Internally Pulled up with 50 kΩ resistor</td></tr>
<tr><td>7</td><td>RTIP</td><td>I</td><td>Receive Positive Input</td></tr>
<tr><td>8</td><td>RRING</td><td>I</td><td>Receive Negative Input</td></tr>
<tr><td>9</td><td>AVDD</td><td>***</td><td>Analog VDD (3.3V ± 5%)</td></tr>
<tr><td>10</td><td>AGND</td><td>***</td><td>Analog Ground</td></tr>
<tr><td>11</td><td>S1</td><td>I</td><td>Mode Select
<table>
<tr><th>S1</th><th>S2</th><th>S3</th><th>MODE</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>64 kHz + 8 kHz</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>64kHz+8kHz+400Hz</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>E1 RZ</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>E1 NRZ</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>T1</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>T1 (output full width data)</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>E1 (output full width data)</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Reserved</td></tr>
</table>
NOTE: T1 NRZ or E1 NRZ means the output data at RPOS and RNEG are 1 RCLK wide.</td></tr>
</table>

## PIN DESCRIPTIONS

| PIN # | SYMBOL | TYPE | DESCRIPTION |
|---|---|---|---|
| 12 | S2 | I | **Mode Select** |
| 13 | S3 | I | **Mode Select** |
| 14 | NC | *** | **This pin must be grounded for normal operation** |
| 15 | DATMUT | I | **Data Muting:**<br>Connect this pin "High" to mute data output to "Low" state at RPOS/RNEG. The RLOS pin can be connected to this pin to mute the output when RLOS occurs.<br>***NOTE:*** *Internally Pulled down with 50 kΩ resistor* |
| 16 | RNEG | O | **Receive Negative Data Output:**<br>The data is half clock cycle wide. |
| 17 | RPOS | O | **Receive Positive Data Output:**<br>The data is half clock cycle wide |
| 18 | RCLK | O | **Receive Clock Output**<br>Outputs either 1.544 MHz or 2.048 MHz or 64 kHz clock |
| 19 | DGND | *** | **Digital Supply Ground** |
| 20 | DVDD | *** | **Digital Supply Voltage (3.3V ± 5%)** |
| 21 | RLOS | O | **Receive Loss of Signal Output** |
| 22 | 400Hz | O | **400 Hz Clock output for 64 kHz Operation** |
| 23 | 8 kHz | O | **8 kHz clock output for 64 kHz Operation** |
| 24 | 400Hz_LCV | O | **Line Code Violation for 400 Hz**<br>This pin will stay "High" when 400 Hz is not in sync. |
| 25 | 8 kHz_LCV/ BPV | O | **Line Code Violation for 8 kHz in 64 kHz operation**<br>**Bipolar Violation:**<br>In E1RZ or T1 mode, every Bipolar violation valid or not valid is indicated at this pin.<br>This pin will stay "High" when 8 kHz is not in sync. |
| 26 | RCLK_LCV/AIS | O | **Receive Clock Violation.**<br>In 64 kbps operation, every missing pulse will cause this pin to go "High" for half the clock cycle<br>**AIS Indication**<br>In E1RZ or T1 mode, this output serves as an AIS indicator. AIS will stay "High" for 250 μs in E1 RZ mode, and in T1 mode, AIS will stay "High" for 3 ms. |
| 27 | DATA_INV | I | **Data Invert:**<br>Connect this pin "High" to output active "Low" data at RPOS/RNEG.<br>***NOTE:*** *Internally Pulled down with 50 kΩ resistor* |
| 28 | RCLK_INV | I | **Receive Clock Invert:**<br>Connect this pin "High" to align the data to change at the falling edge of RCLK.<br>***NOTE:*** *Internally Pulled down with 50 kΩ resistor* |

## ELECTRICAL CHARACTERISTICS

***ABSOLUTE MAXIMUM RATINGS***

| | |
|---|---|
| Storage Temperature | - 65°C to + 150°C |
| Operating Temperature | - 40°C to + 85°C |
| Supply Voltage Range | -0.5V to +6.0V |
| ESD | 2000 V |
| Theta-JA | 68°C/W |
| Theta-JC | 13°C/W |

**TABLE 1: DC Electrical Characteristics**

| **(TA = -40°C TO 85°C, VDD = 3.3 V ± 5%, unless otherwise specified)** | | | | | |
|---|---|---|---|---|---|
| **SYMBOL** | **PARAMETER** | **MIN.** | **TYP.** | **MAX.** | **UNITS** |
| $V_{DDD}$ | DC Supply Voltage (Digital) | 3.135 | 3.3 | 3.465 | V |
| $V_{DDA}$ | DC Supply Voltage (Analog) | 3.135 | 3.3 | 3.465 | V |
| - | Power Consumption | | 42 | 50 | mW |
| $V_{IL}$ | Input Low Voltage | | | 0.8 | V |
| $V_{IH}$ | Input High Voltage | 2.0 | | $V_{DD}$ | V |
| $V_{OL}$ | Output Low Voltage, IOUT = -4.0mA | 0 | | 0.4 | V |
| $V_{OH}$ | Output High Voltage, IOUT = 4.0mA | 2.4 | | $V_{DD}$ | V |
| $I_L$ | Input Leakage Current* | | | ±10 | µA |
| $C_I$ | Input Capacitance | | 5 | | pF |
| $C_L$ | Output Load Capacitance | | | 25 | pF |

***NOTE:*** ** Not applicable to pins with pull-down resistors.*

**TABLE 2: E1 RECEIVER SENSITIVITY**

| Vdd = 3.3V±5%, $T_A$ = -40°C to 85°C, Unless Otherwise Specified | | | | | |
|---|---|---|---|---|---|
| **PARAMETER** | **MIN CABLE LOSS** | **TYP** | **MAX** | **UNIT** | **TEST CONDITION** |
| Receiver Sensitivity with PBRS $2^{23}$-1 pattern | 9 | | | dB | 9dB Cable Loss |
| | 6 | | | dB | 6dB Cable Loss + 6dB Flat Loss |
| ***NOTE:*** *0dB = 2.37Vp* | 4 | | | dB | 4dB Cable Loss + 8dB Flat Loss |

**TABLE 3: T1 RECEIVER SENSITIVITY**

| Vdd = 3.3V±5%, $T_A$ = -40°C to 85°C, Unless Otherwise Specified | | | | | |
|---|---|---|---|---|---|
| **PARAMETER** | **MIN CABLE LOSS** | **TYP** | **MAX** | **UNIT** | **TEST CONDITION** |
| Receiver Sensitivity with PBRS $2^{15}$-1 pattern | 9 | | | dB | 9dB Cable Loss |
| | 6 | | | dB | 6dB Cable Loss + 6dB Flat Loss |
| ***NOTE:*** *0dB = 3.0Vp* | 4 | | | dB | 4dB Cable Loss + 8dB Flat Loss |

**TABLE 4: 64KBITS/SEC RECEIVER SENSITIVITY**

| Vdd = 3.3V±5%, $T_A$ = -40°C to 85°C, Unless Otherwise Specified | | | | | |
|---|---|---|---|---|---|
| **PARAMETER** | **MIN** | **TYP** | **MAX** | **UNIT** | **TEST CONDITION** |
| Receiver Sensitivity with Bipolar Violation Encoded "All 1's" Pattern | 9 | | | dB | 9dB Cable Loss |
| | 6 | | | dB | 6dB Cable Loss + 6dB Flat Loss |
| ***NOTE:*** *0dB = 1.0Vp* | 4 | | | dB | 4dB Cable Loss + 8dB Flat Loss |

**FIGURE 3. TIMING DIAGRAM FOR SYSTEM INTERFACE**

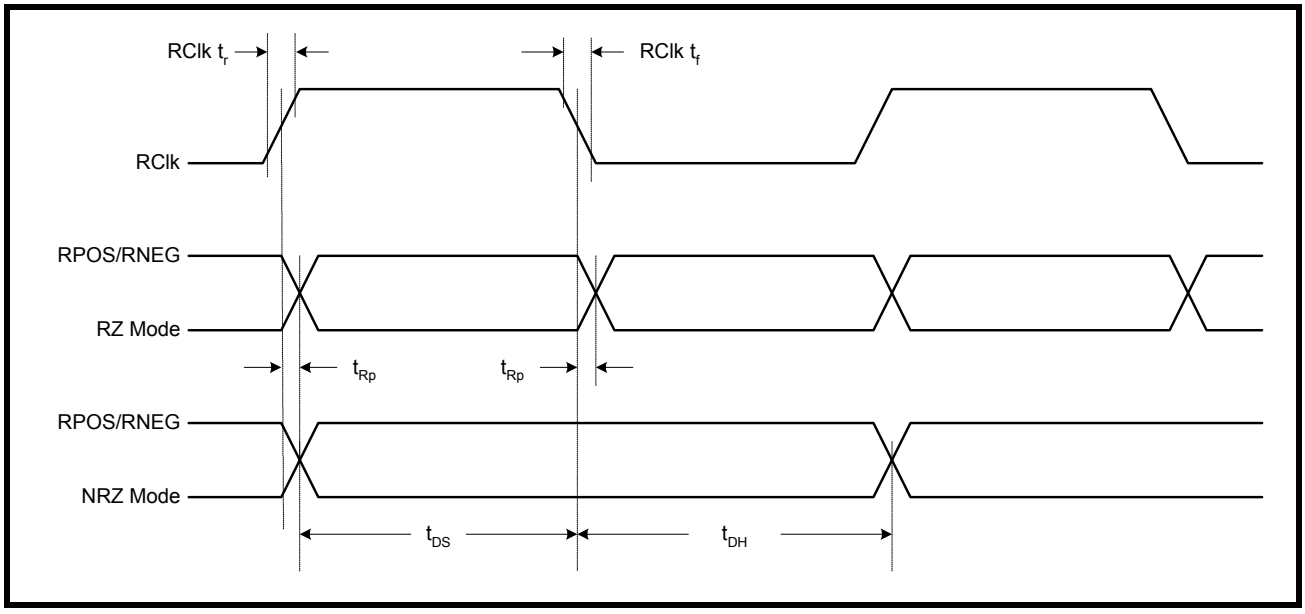


**TABLE 5: AC ELECTRICAL SPECIFICATIONS**

| Vdd = 3.3V±5%, $T_A$ = -40°C to 85°C, Unless Otherwise Specified | | | | | |
|---|---|---|---|---|---|
| **SYMBOL** | **PARAMETER** | **MIN** | **TYP** | **MAX** | **UNITS** |
| - | Receive Clock Duty Cycle | 45 | 50 | 55 | % |
| RClk $t_r$/RClk $t_f$ | Receive Clock Rise/Fall time (10 - 90%) | - | 3.0 | - | ns |
| $t_{Rp}$ | RClk to RPOS/RNEG Delay | 0 | - | 10 | ns |
| $t_{DS}$ | Receive Data Setup Time | 20 | - | - | ns |
| $t_{DH}$ | Receive Data Hold Time | 20 | - | - | ns |

## FUNCTIONAL DESCRIPTION

The XRT85L61 is an integrated BITS (Building Integrated Timing Supply) Clock Generator. Simplified block diagram of the chip is shown in Figure 1.

The XRT85L61 extracts the clock signals from the following synchronization lines:

- Balanced 100 Ω lines with 1544 kbps DS1 pattern.
- Balanced 120 Ω or unbalanced 75 Ω lines with 2048 kbps RZ pattern.
- Balanced 120 Ω or unbalanced 75 Ω line with 2048 kbps NRZ pattern.
- Balanced 110 Ω line with 64 kbps having 8 kHz violations; a “64 kHz + 8 kHz sync pattern.
- Balanced 110 Ω line with a 64 kbps pattern having both 8 kHz and 400 Hz violations; a “64 kHz + 8 kHz + 400 Hz” sync pattern.

### 1.0 OPERATING MODE:

The operating mode for the XRT85L61 is shown in Table 6.

**TABLE 6: OPERATING MODE SELECTION**

| S1 | S2 | S3 | MODE | DATA OUTPUT AT RPOS / RNEG |
|---|---|---|---|---|
| 0 | 0 | 0 | 64 kHz + 8 kHz | RZ |
| 0 | 0 | 1 | 64 kHz + 8 kHz + 400 Hz | RZ |
| 0 | 1 | 0 | E1RZ | RZ |
| 0 | 1 | 1 | E1NRZ | RZ |
| 1 | 0 | 0 | T1 | RZ |
| 1 | 0 | 1 | T1 (full width) | NRZ |
| 1 | 1 | 0 | E1 (full width) | NRZ |
| 1 | 1 | 1 | Reserved | |

### 1.1 64 kHz Clock Mode:

The XRT85L61 receives the 64 kbps ternary RZ signal. Two modes of 64 kHz operation is possible by selecting S1, S2 and S3 as shown in Table 1.

**TABLE 7: G.703 SPECIFICATION FOR THE 64 KHZ CLOCK SIGNAL AT INPUT PORT**

| FREQUENCY | (A) 64 KHZ + 8 KHZ OR (B) 64 KHZ + 8 KHZ + 400 HZ |
|---|---|
| Signal Format | (a) AMI with 8 kHz Bipolar Violation<br>(b) AMI with 8 kHz Bipolar Violation removed at every 400 Hz. |
| Alarm Condition | Alarm should not occur against the amplitude range from 0.63 V to 1.1 V |

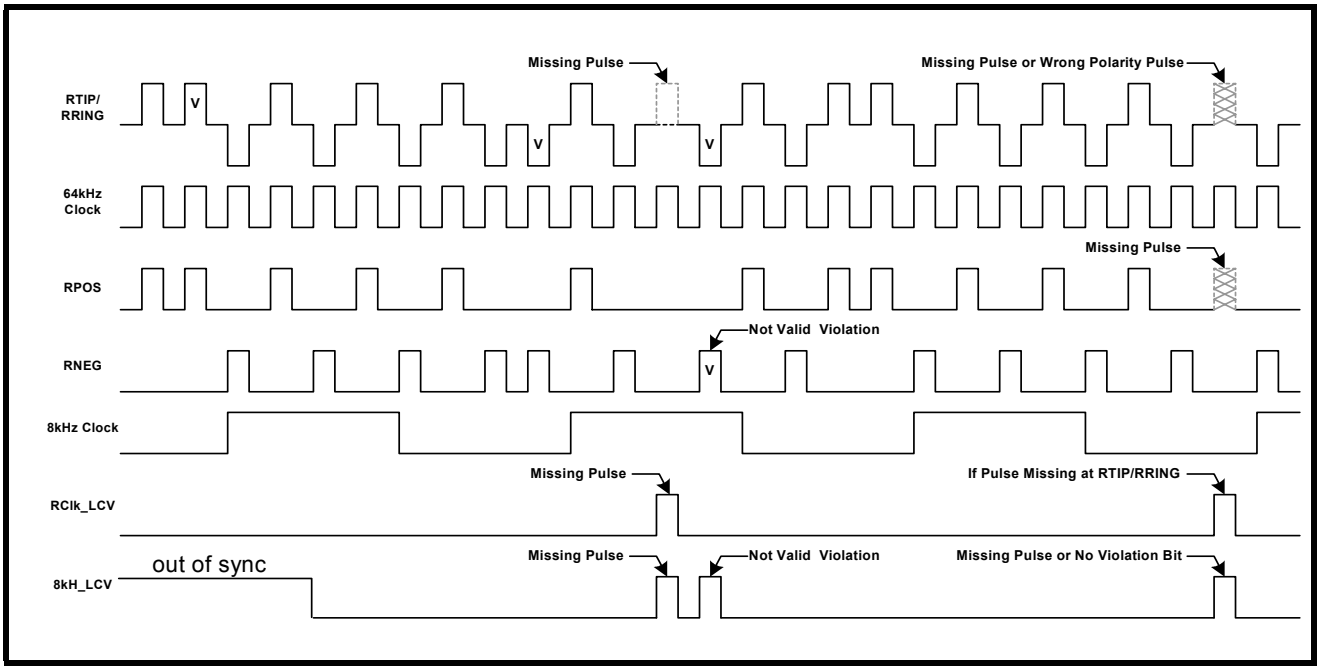
**TABLE 8: G.703 SPECIFICATION FOR THE 64 KHZ CLOCK SIGNAL AT OUTPUT PORT**

| FREQUENCY | (A) 64 KHZ + 8 KHZ OR (B) 64 KHZ + 8 KHZ + 400 HZ |
|---|---|
| Load Impedance | 110 Ω resistive |
| Transmission Media | Symmetric Pair Cable |
| Pulse Width (FWHM) | < 7.8 ± 0.78 μs |
| Amplitude | < 1 V ± 0.1 V |

### 1.1.1 64 kHz + 8 kHz Clock Extraction

The input data is shown in Figure 4. The 64 kHz clock signal consist of AMI code with 8 kHz Bipolar Violation. Both the 64 kHz and 8 kHz components are extracted from the composite received signal and presented at the 64 kHz and 8 kHz output pins.

**FIGURE 4. INPUT DATA 64 KHZ + 8 KHZ OPERATION (S1 = 0, S2 = 0, S3 = 0)**

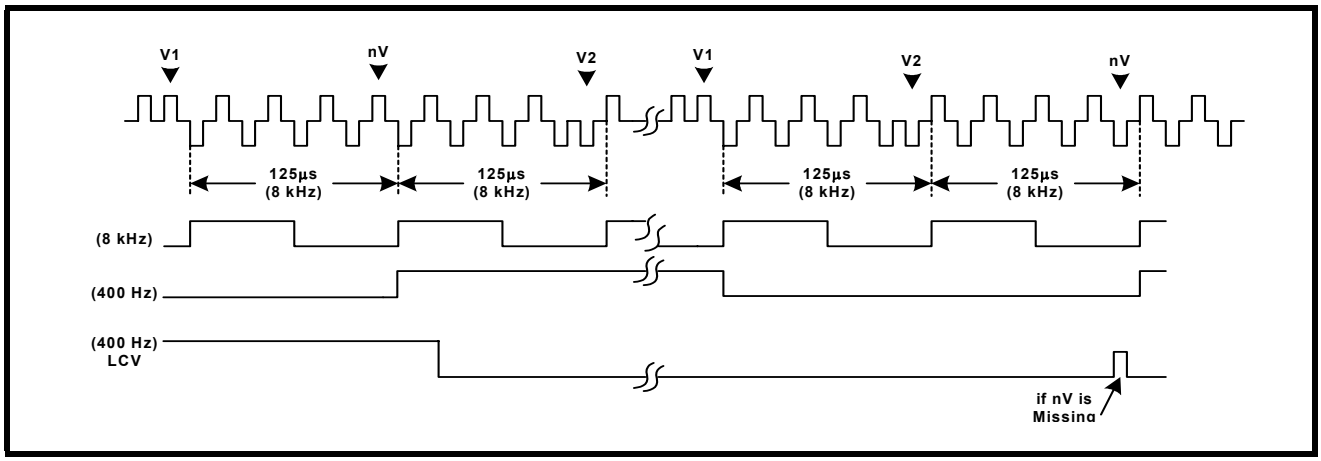



### 1.1.2 64 kHz + 8 kHz + 400 Hz Clock Extraction

Figure 4 shows the input data for this mode. The 64 kHz clock signal consist of AMI code with 8 kHz Bipolar Violation removed every 400 Hz. The 64 kHz, 8 kHz and 400 Hz components are extracted from the composite received signal and presented at the RClk, 8 kHz and 400 Hz output pins.

***NOTE:*** *The inputs are not aligned with all output signals. The above diagram is used to depict the output activity when the input signals have errors.*

**FIGURE 5. INPUT DATA 64 KHZ + 8 KHZ + 400 HZ OPERATION (S1 = 0, S2 = 0, S3 = 1)**



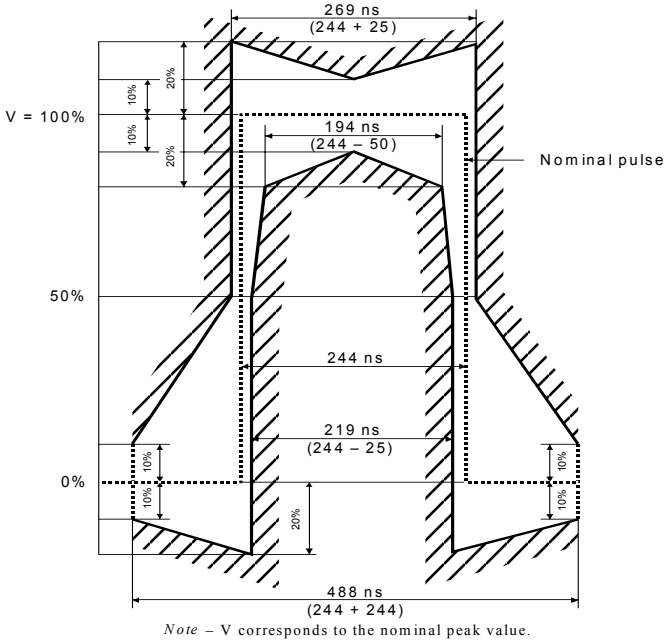

***NOTES:***

1. *V1 and V2 indicate AMI code-rule violations, and give the 8kHz timing.*
2. *V1 and V2 have different violation polarity with respect to each other.*
3. *nV indicates no violation (violation stealing) and gives the 400 Hz timing.*

### 1.2 2048 kHz RZ E1 Mode

In this mode, the XRT85L61 receives a standard E1 signal as shown in Figure 6. Table 4 gives the details of the E1 pulse.

**FIGURE 6. E1 PULSE MASK (G.703)**




*Note* – V corresponds to the nominal peak value.

**TABLE 9: G.703 SPECIFICATION E1**

| PULSE | INTERFACE | |
|---|---|---|
| Pulse Shape (nominally rectangular) | All Marks of a valid signal must conform with the mask irrespective of the sign. The value V corresponds to the nominal peak value. | |
| Pair(s) in each direction | One coaxial pair | One symmetrical pair |
| Test Load Impedance | 75 Ω Resistive | 120 Ω Resistive |
| Nominal peak voltage of a mark (pulse) | 2.37 V | 3 V |
| Peak voltage of a space (no pulse) | 0 ± 0.237 V | 0 ± 0.3 V |
| Nominal Pulse Width | 244 ns | |
| Ratio of the amplitudes of positive and negative pulses at the center of the pulse interval | 0.95 to 1.05 | |
| Ratio of the widths of positive and negative pulses at the nominal half amplitude | 0.95 to 1.05 | |
| Maximum peak to peak jitter at an output port | Refer to ITU-T G.823 specification | |

### 1.3 2048 kHz NRZ Mode

In this mode, XRT85L61 receives 2048 kbps synchronization signal as shown in Figure 7.

**FIGURE 7. E1 CLOCK SIGNAL WAVE SHAPE - G.703**

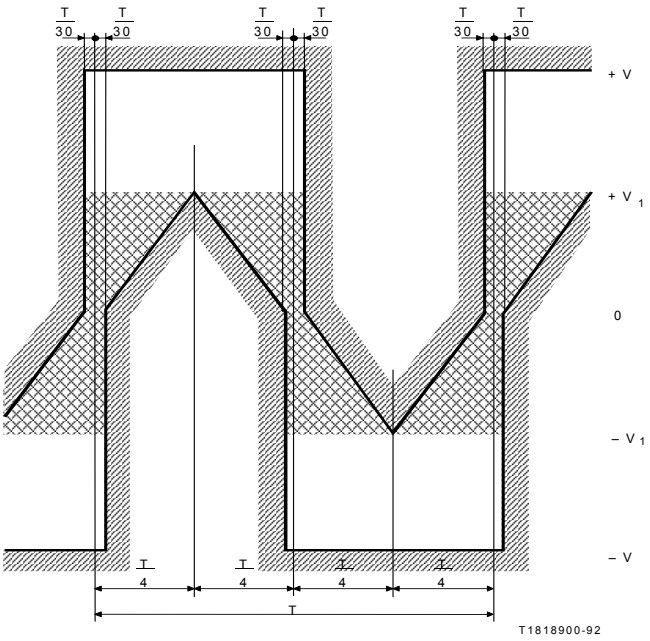



FIGURE 21/G.703
Wave shape at an output port

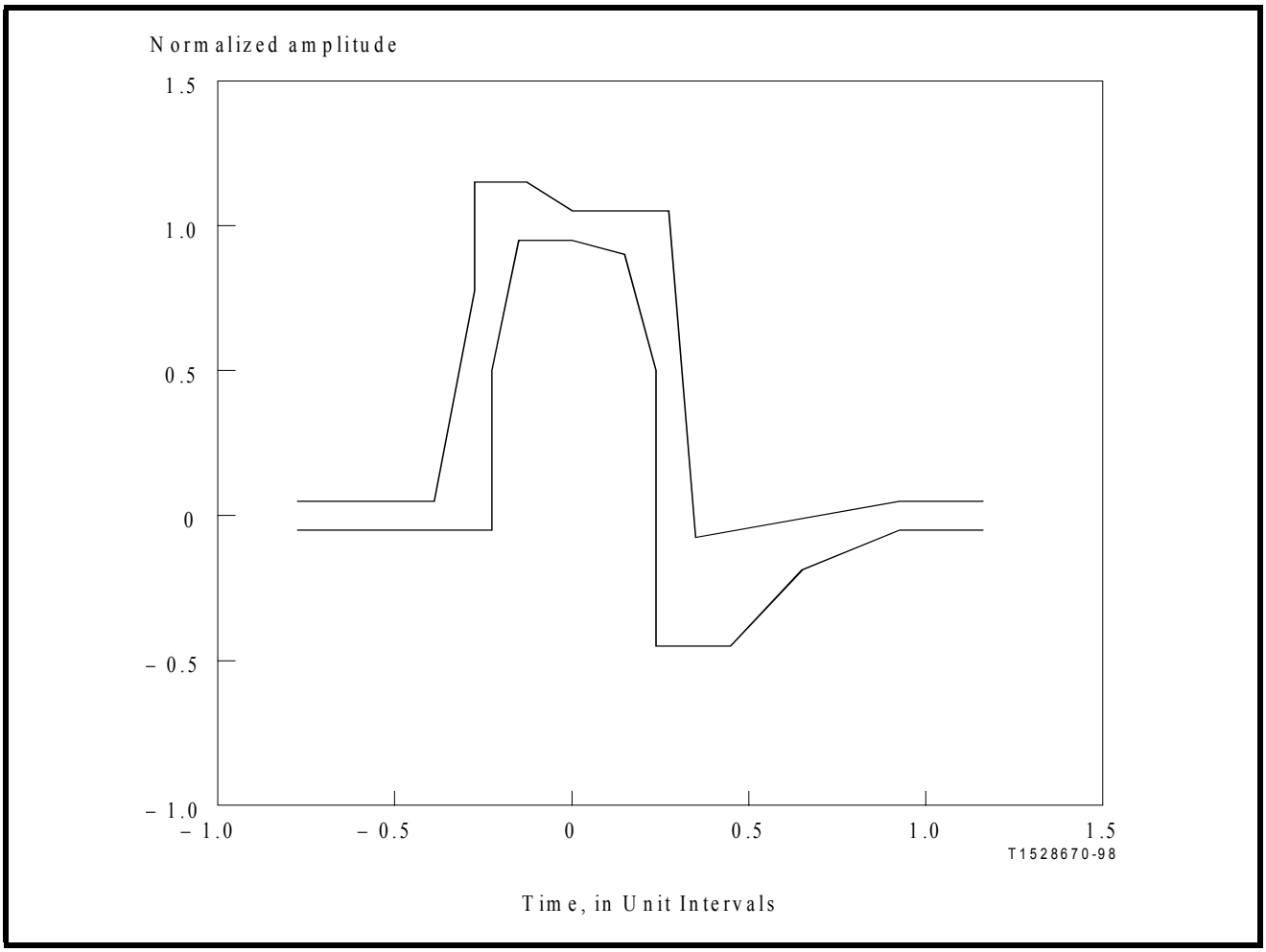
**TABLE 10: G.703 2048 KHZ CLOCK INTERFACE**

| PULSE | INTERFACE | |
|---|---|---|
| Frequency | 2048 kHz ± 50 ppm | |
| Pulse Shape | The signal must conform with the mask.<br>The value V corresponds to maximum peak value<br>The value $V_1$ corresponds to minimum peak value | |
| Pair(s) in each direction | Coaxial pair | Symmetrical pair |
| Test Load Impedance | 75 Ω Resistive | 120 Ω Resistive |
| Maximum peak value ($V_{op}$) | 1.5 | 1.9 |
| Minimum peak value ($V_{op}$) | 0.75 | 1.0 |
| Maximum jitter at an output port | 0.05 UI peak to peak measured within the frequency range $f_1$ = 20 Hz to $f_4$ = 100 kHz<br>***NOTE:*** *This value is valid for network timing distribution equipment. Other values may be specified for timing output ports of digital links carrying the network timing.* | |

### 1.4 1544 kHz T1 Mode

In this mode, the XRT85L61 receives a standard DS1 signal as shown in Figure 8.

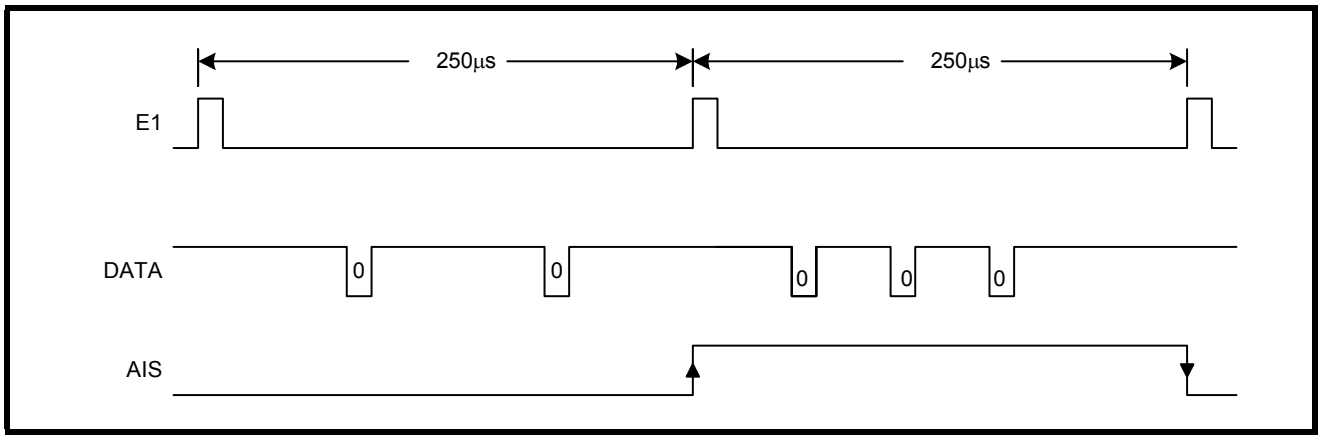
**FIGURE 8. G.703 DS1 WAVE FORM**



## 2.0 AIS DETECTION TIMING

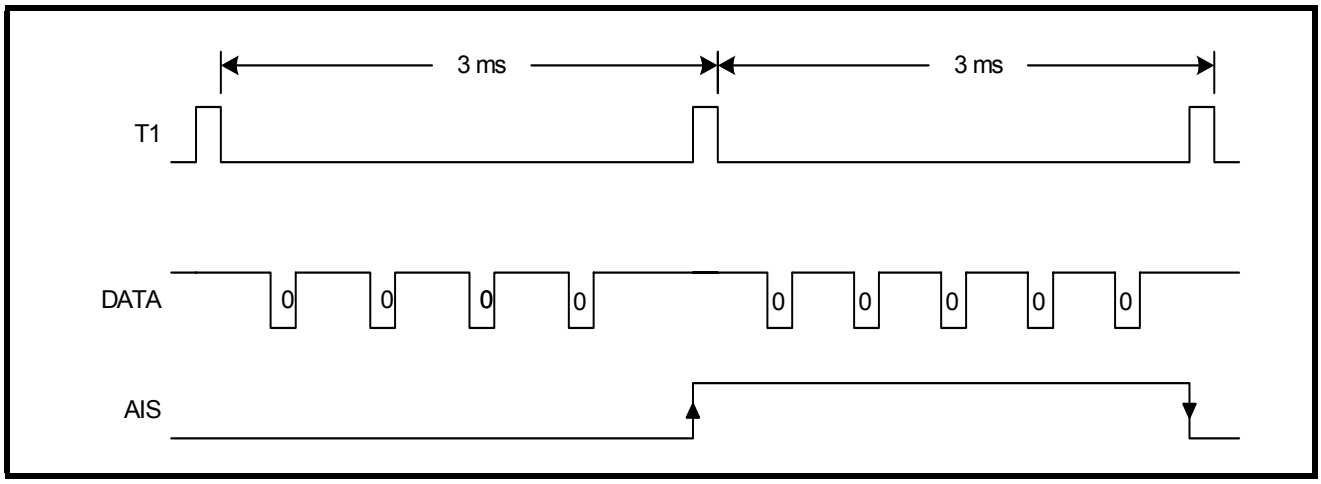
In E1 mode, AIS is set when the received incoming signal has 2 or less Zero's in a sequence of 512 bits. AIS will stay "High" for 250 μs and AIS is cleared upon receiving three or more Zero's in the subsequent 512 bits (250μs) time-frame. Figure 9 shows the AIS timing.

**FIGURE 9. AIS DETECTION FOR E1 MODE**




In T1 mode, AIS is detected if the received input signal has 4 or less Zero's in a sequence of 4632 bits (3ms) and AIS is cleared when 5 or more Zero's are detected in the subsequent 4632 bits (3 ms) time-frame. Figure 10 shows the AIS timing for T1 mode.

**FIGURE 10. AIS DETECTION FOR T1 MODE**




## 3.0 LOSS OF SIGNAL

The XRT85L61 Receive Loss of Signal (RLOS) monitoring circuits consist of both analog and digital schemes. Both E1 and T1 meet G.775 RLOS declare and clear criteria. In E1 and 64kb/s modes, RLOS will be set if the input pattern exceeds 32 bit consecutive zeros. In T1 mode, RLOS will go "High" if the number of consecutive zeros exceeds 175.

The XRT85L61 RLOS detection circuit also reports RLOS if the input signal level drops below 220mVp (typical) and RLOS is cleared when the input signal level returns to more than 380mVp (typical) when the input pattern meets 12.5% density over a 32 bit period.

## 4.0 APPLICATIONS

**FIGURE 11. CEPT APPLICATION FOR TWISTED PAIR INTERFACE**

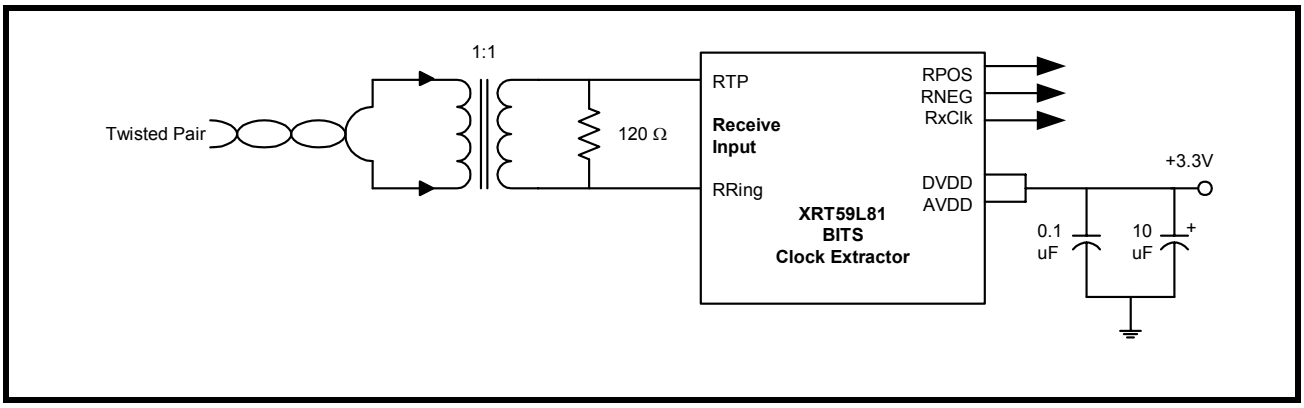



**FIGURE 12. CEPT APPLICATION FOR COAXIAL INTERFACE**

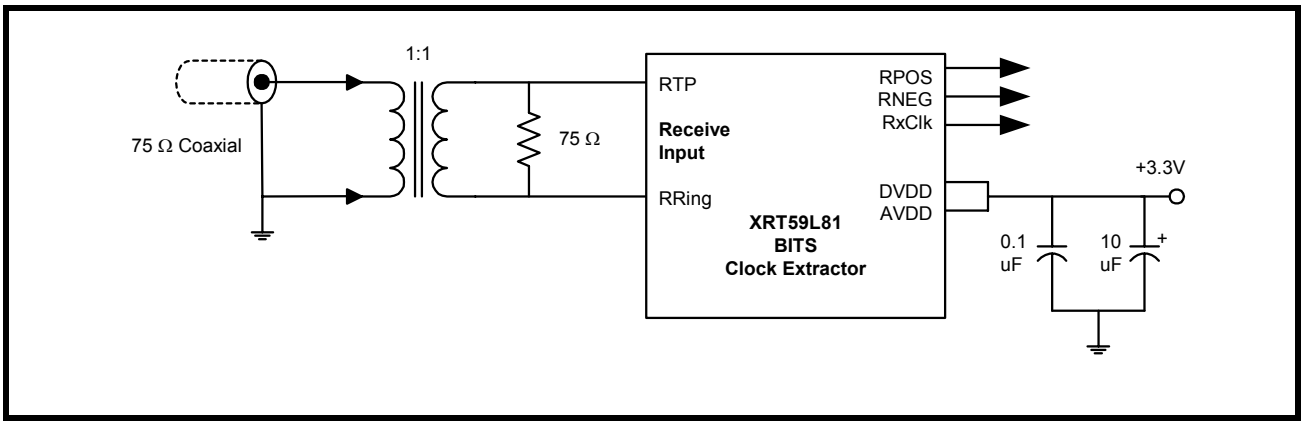



**FIGURE 13. T1 APPLICATION FOR TWISTED PAIR INTERFACE**

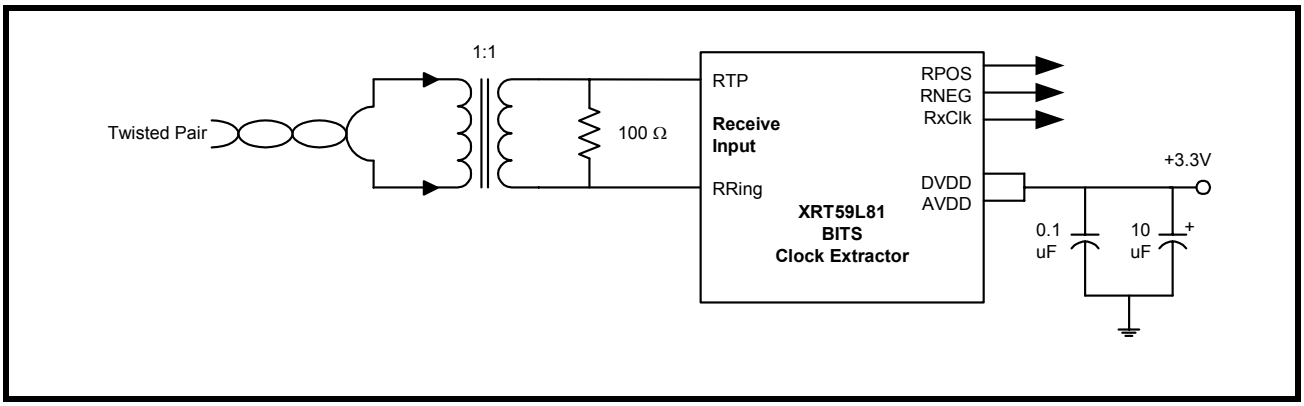
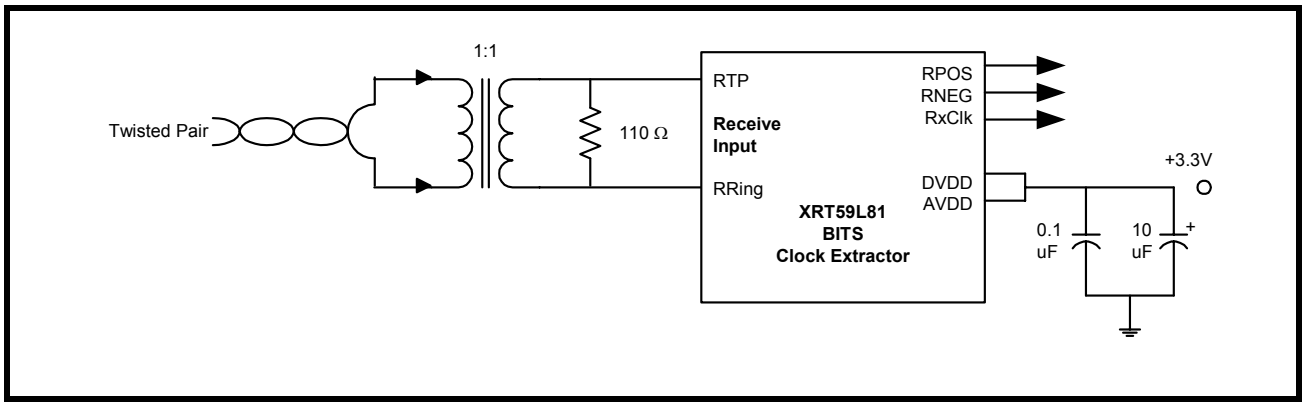


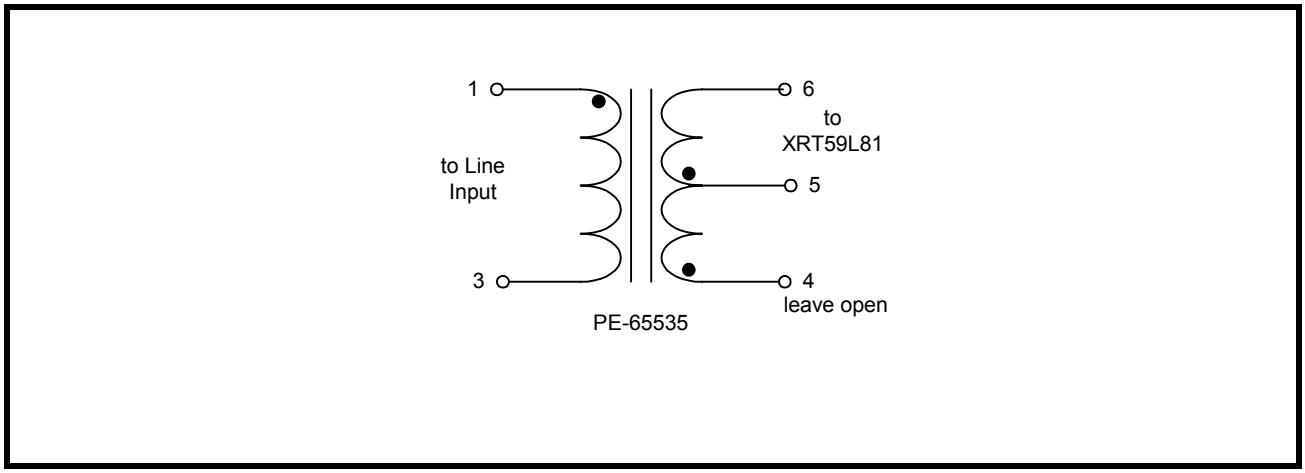
**FIGURE 14. 64KBPS APPLICATION FOR TWISTED PAIR**




***TRANSFORMER RECOMENDATION***

For all applications a 1:1 transformer ratio is required. 64kbps applications require a larger Inductance transformer. Although E1 and T1 can use lower inductance transformers, Exar reccomends the use of the PULSE ENGINEERING PE-65535 1:2CT transformer in a 1:1 mode by using pins 1 & 3 for the Line input and Pins 6 & 5 as the secondary input to the XRT85L61. See Figure 15 below. Smaller transformers will be evaluated in the future and recommendations will be published at that time.

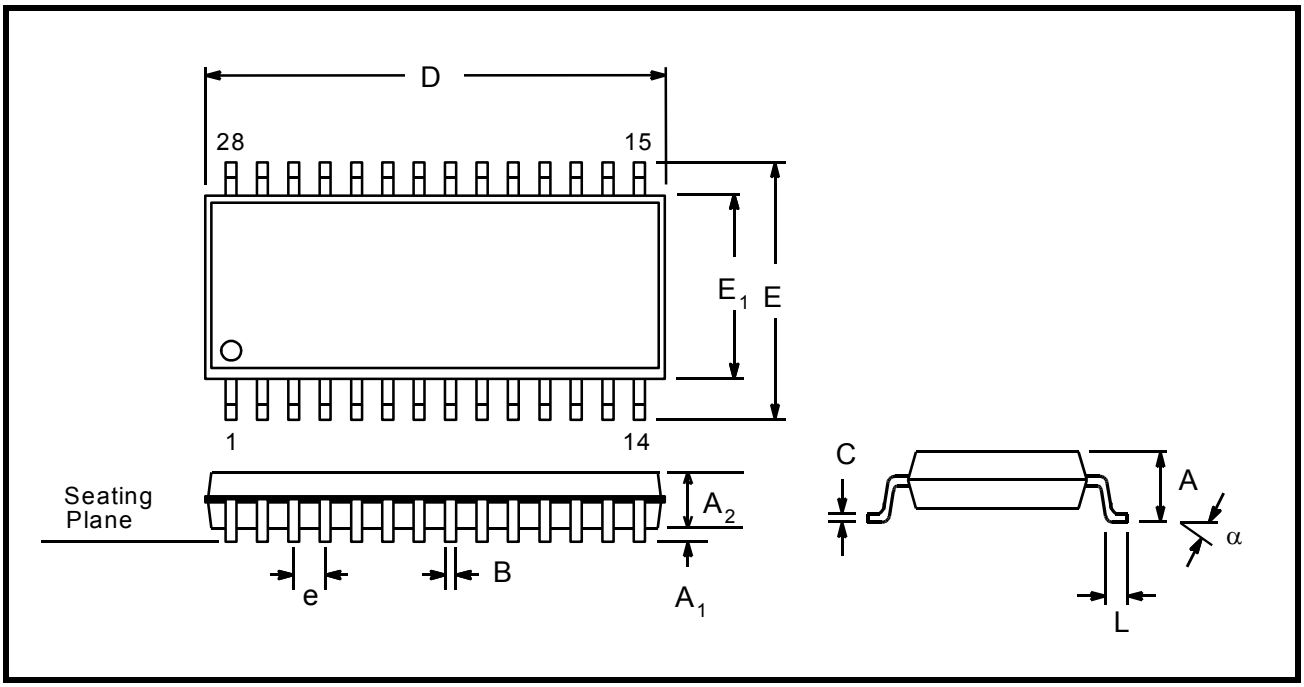
**FIGURE 15. CONNECTING THE PULSE ENGINEERING PE-65535 1:2CT TRANSFORMER TO THE XRT85L61**



## ORDERING INFORMATION

| PART NUMBER | PACKAGE | OPERATING TEMPERATURE RANGE |
|---|---|---|
| XRT85L61IG | 28 Lead TSSOP | -40°C to +85°C |

## PACKAGE OUTLINE DRAWING




*Note: The control dimension is in the millimeter column*

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| SYMBOL | MIN | MAX | MIN | MAX |
| A | 0.033 | 0.047 | 0.85 | 1.20 |
| A1 | 0.002 | 0.006 | 0.05 | 0.15 |
| A2 | 0.031 | 0.041 | 0.80 | 1.05 |
| B | 0.007 | 0.012 | 0.19 | 0.30 |
| C | 0.004 | 0.008 | 0.09 | 0.20 |
| D | 0.378 | 0.386 | 9.60 | 9.80 |
| E | 0.248 | 0.260 | 6.30 | 6.60 |
| E1 | 0.169 | 0.177 | 4.30 | 4.50 |
| e | 0.0256 BSC | | 0.65 BSC | |
| L | 0.018 | 0.030 | 0.45 | 0.75 |
| α | 0° | 8° | 0° | 8° |

## REVISION HISTORY

| REVISION # | DATE | CHANGES |
|---|---|---|
| 1.0.0 | January 2004 | Final Release |
| 1.0.1 | February 2004 | Added description for MCLK1 and MCLK2 |
| 1.0.2 | October 2004 | Modified applications drawings. Added RLOS description. Added AC Electrical characteristics. Added description for T1 AIS detection. |

## NOTICE

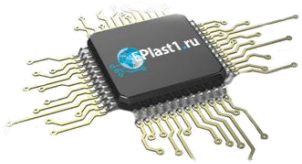
Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits,General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.




**Как с нами связаться**

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