

## 0.3 $\mu\text{A}$ $I_Q$ Ultra-low Quiescent Current 100 mA Buck DC/DC Converter

No. EA-502-190401

### OVERVIEW

RP511x is a DC/DC converter featuring 0.3  $\mu\text{A}$  ultra-low operating quiescent current. It is suitable for use in wearable and IoT devices that require miniaturization and long-lifetime of battery.

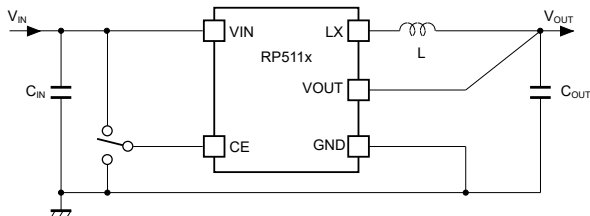
### KEY BENEFITS

- VFM ( $f_{\text{sw}}$  up to 1 MHz) control achieves 0.3  $\mu\text{A}$  ultra-low operating quiescent current.
- The wide range of  $V_{\text{IN}}$  from 2.0 V to 5.5 V allows operation from coin cell to USB port.
- Total mount area including  $C_{\text{IN}}$ ,  $C_{\text{OUT}}$ , and inductor is 8.0 mm<sup>2</sup>.
- Selectable packages including WLCSP, DFN, and SOT. 0.4 mm-thickness WLCSP package adaptable to IC cards.

### KEY SPECIFICATIONS

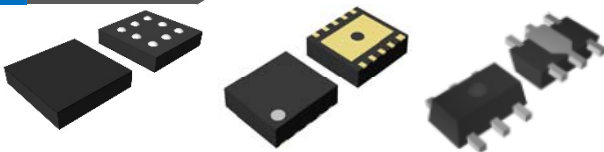
- Output Current: 100 mA
- Output Voltage Range: 1.0 V to 4.0 V (Settable in 0.1 V step)
- Output Voltage Accuracy:  $\pm 1.5\%$  ( $V_{\text{SET}} \geq 1.2$  V),  $\pm 18$  mV ( $V_{\text{SET}} < 1.2$  V)
- Built-in Driver On-resistance ( $V_{\text{IN}} = 3.6$  V): Typ. PMOS 0.15  $\Omega$ , NMOS 0.15  $\Omega$  (RP511Z)
- Standby Current: 0.01  $\mu\text{A}$

### TYPICAL APPLICATIONS



L: 2.2  $\mu\text{H}$ ,  $C_{\text{OUT}}$ : 22  $\mu\text{F}$

### PACKAGES



WLCSP-8-P1

1.45 mm x 1.48 mm,  
t=0.4mm (max.)

DFN(PLP)2527-10

2.7mm x 2.5 mm,  
t=0.6mm (max.)

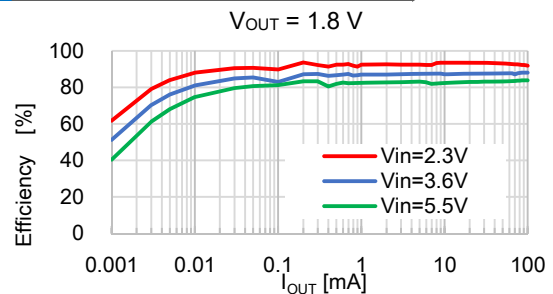
SOT-89-5

4.5mm x 4.35mm,  
t=1.6mm (max.)

### APPLICATIONS

- Wearable equipment such as SmartWatch, SmartBand, and health monitoring
- Li-ion battery-used equipment, Coin cell-used equipment
- Low power RF such as Bluetooth® Low Energy, Zigbee, WiSun, and ANT
- Low power CPU, memory, sensor devices, and energy harvesting

### TYPICAL CHARACTERISTICS



### SELECTION GUIDE

Product Name	Package	Q'ty per Reel
RP511Zxx1\$-TR-F	WLCSP-8-P1	5,000 pcs
RP511Kxx1\$-TR	DFN(PLP)2527-10	5,000 pcs
RP511Hxx1\$-T1-FE	SOT-89-5	1,000 pcs

xx: Set output voltage ( $V_{\text{SET}}$ )

Fixed Output Voltage Type:

1.0 V (10) to 4.0 V (40) in 0.1 V step.

\$: Version

Version	Auto-discharge Function	$V_{\text{SET}}$
A	No	1.0 V to 4.0 V
B	Yes	

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## RP511x

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### SELECTION GUIDE

The set output voltage, the output voltage type, the auto-discharge function<sup>(1)</sup>, and the package for the ICs are user-selectable options.

#### Selection Guide

Product Name	Package	Quantity per Reel	Pb Free	Halogen Free
RP511Zxx1\$-TR-F	WLCSP-8-P1	5,000 pcs	Yes	Yes
RP511Kxx1\$-TR	DFN(PLP)2527-10	5,000 pcs	Yes	Yes
RP511Hxx1\$-T1-FE	SOT-89-5	1,000 pcs	Yes	Yes

xx: Designation of the set output voltage ( $V_{SET}$ )

For Fixed Output Voltage Type<sup>(2)</sup>: 1.0 V (10) to 4.0 V (40) in 0.1 V step

\$: Designation of Version

Version	Auto-discharge Function	$V_{SET}$
A	Disable	1.0 V to 4.0 V
B	Auto-discharge	

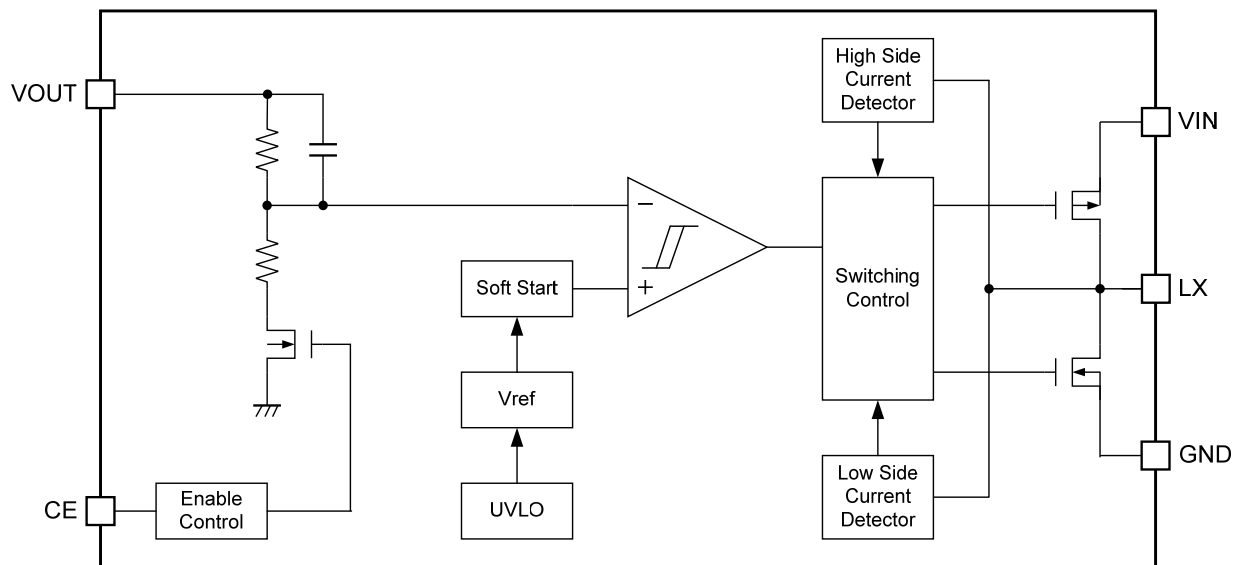
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<sup>(1)</sup> Auto-discharge function quickly lowers the output voltage to 0 V, when the chip enable signal is switched from the active mode to the standby mode, by releasing the electrical charge accumulated in the external capacitor.

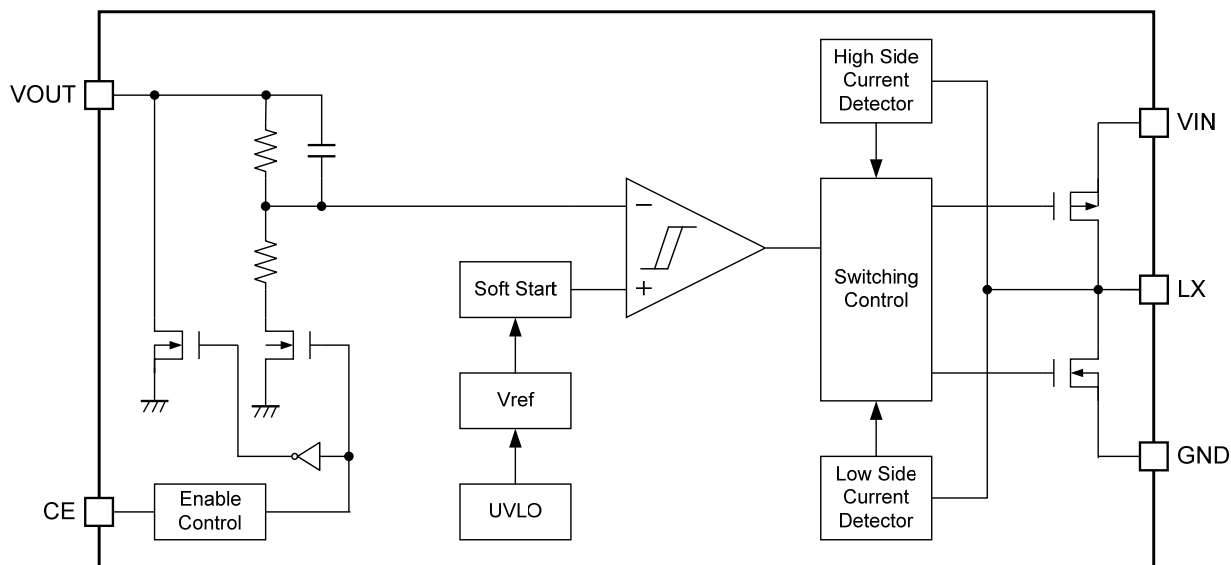
<sup>(2)</sup> The customization of specifying in 0.05 V step is available.

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### BLOCK DIAGRAM



RP511xxx1A Block Diagram

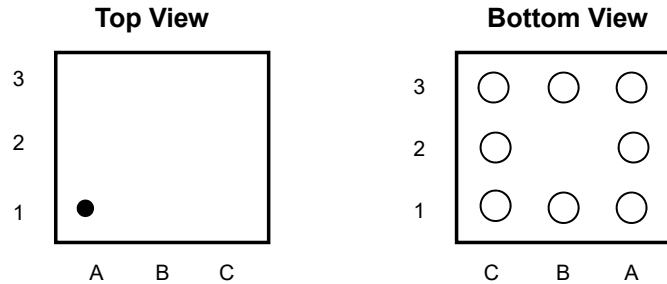


RP511xxx1B Block Diagram

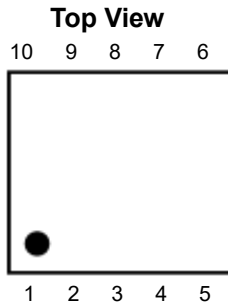
# RP511x

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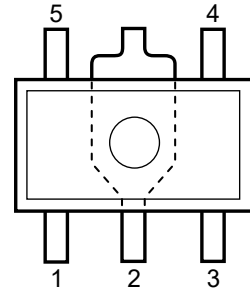
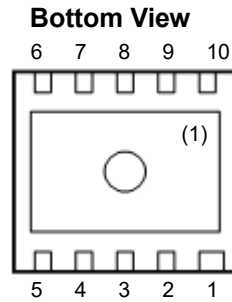
## PIN DESCRIPTION



**RP511Z (WLCSP-8-P1) Pin Configuration**



**RP511K [DFN(PLP)2527-10] Pin Configuration**



**RP511H (SOT-89-5)  
Pin Configuration**

### RP511Z Pin Description

Pin No.	Symbol	Description
A1	VIN	Input Pin
B1	VIN	Input Pin
C1	LX	Switching Pin
A2	VOUT	Output voltage Pin
C2	GND	Ground Pin
A3	CE	Chip Enable Pin (Active-high)
B3	GND	Ground Pin
C3	GND	Ground Pin

<sup>(1)</sup> The tab on the bottom of the package enhances thermal performance and is electrically connected to GND (substrate level). It is recommended that the tab be connected to the ground plane on the board, or otherwise be left floating.

**RP511K Pin Description**

<b>Pin No.</b>	<b>Symbol</b>	<b>Description</b>
1	VOUT	Output Pin
2	GND	Ground Pin
3	GND	Ground Pin
4	LX	Switching Pin
5	LX	Switching Pin
6	VIN	Input Pin
7	VIN	Input Pin
8	NC	No connection
9	CE	Chip Enable Pin (Active-high)
10	NC	No connection

**RP511H Pin Description**

<b>Pin No.</b>	<b>Symbol</b>	<b>Description</b>
1	VOUT	Output Pin
2	GND	Ground Pin
3	LX	Switching Pin
4	VIN	Input Pin
5	CE	Chip Enable Pin (Active-high)

## RP511x

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## ABSOLUTE MAXIMUM RATINGS

### Absolute Maximum Ratings

(GND = 0 V)

Symbol	Parameter	Rating	Unit	
$V_{IN}$	Input Voltage	-0.3 to 6.5	V	
$V_{LX}$	LX Pin Voltage	-0.3 to $V_{IN} + 0.3$	V	
$V_{CE}$	CE Pin Voltage	-0.3 to 6.5	V	
$V_{MODE}$	MODE Pin Voltage	-0.3 to 6.5	V	
$V_{OUT}$	VOOUT Pin Voltage	-0.3 to 6.5	V	
$I_{LX}$	LX Pin Output Current	650	mA	
$P_D$	Power Dissipation <sup>(1)</sup>	WLCSP-8-P1, JEDEC STD. 51-9	1140	mW
		DFN(PLP)2527-10, JEDEC STD. 51-7	2500	mW
		SOT-89-5, JEDEC STD. 51-7	2600	mW
$T_j$	Junction Temperature Range	-40 to 125	°C	
$T_{stg}$	Storage Temperature Range	-55 to 125	°C	

### ABSOLUTE MAXIMUM RATINGS

Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause the permanent damages and may degrade the lifetime and safety for both device and system using the device in the field. The functional operation at or over these absolute maximum ratings is not assured.

## RECOMMENDED OPERATING CONDITIONS

### Recommended Operating Conditions

Symbol	Parameter	Rating	Unit
$V_{IN}$	Input Voltage	2.0 to 5.5	V
$T_a$	Operating Temperature Range	-40 to 85	°C

### RECOMMENDED OPERATING CONDITIONS

All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if when they are used over such conditions by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

<sup>(1)</sup> Refer to *POWER DISSIPATION* for detailed information.

## ELECTRICAL CHARACTERISTICS

The specifications surrounded by   are guaranteed by design engineering at  $-40^{\circ}\text{C} \leq T_a \leq 85^{\circ}\text{C}$ .

### RP511x Electrical Characteristics

( $T_a = 25^{\circ}\text{C}$ )

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit	
V <sub>OUT</sub>	Output Voltage	V <sub>IN</sub> = V <sub>CE</sub> = 3.6 V (V <sub>SET</sub> ≤ 2.6 V), V <sub>IN</sub> = V <sub>CE</sub> = V <sub>SET</sub> + 1 V (V <sub>SET</sub> > 2.6 V)	V <sub>SET</sub> ≥ 1.2 V	x 0.985		x 1.015	V
		V <sub>SET</sub> < 1.2 V	-0.018		+0.018		
I <sub>Q</sub>	Operating Quiescent Current	V <sub>IN</sub> = V <sub>CE</sub> = V <sub>OUT</sub> = 3.6 V, V <sub>SET</sub> = 1.8 V, device not switching		0.3		μA	
I <sub>STANDBY</sub>	Standby Current	V <sub>IN</sub> = 5.5 V, V <sub>CE</sub> = 0 V		0.01	<span style="border: 1px solid black; padding: 0 2px;">0.5</span>	μA	
I <sub>CEH</sub>	CE Pin Input Current, high	V <sub>IN</sub> = V <sub>CE</sub> = 5.5 V	<span style="border: 1px solid black; padding: 0 2px;">-0.025</span>	0	<span style="border: 1px solid black; padding: 0 2px;">0.025</span>	μA	
I <sub>CEL</sub>	CE Pin Input Current, low	V <sub>IN</sub> = 5.5 V, V <sub>CE</sub> = 0 V	<span style="border: 1px solid black; padding: 0 2px;">-0.025</span>	0	<span style="border: 1px solid black; padding: 0 2px;">0.025</span>	μA	
I <sub>VOUTH</sub>	V <sub>OUT</sub> "High" Input Current	V <sub>IN</sub> = V <sub>OUT</sub> = 5.5 V, V <sub>CE</sub> = 0 V	<span style="border: 1px solid black; padding: 0 2px;">-0.025</span>	0	<span style="border: 1px solid black; padding: 0 2px;">0.025</span>	μA	
I <sub>VOUTL</sub>	V <sub>OUT</sub> "Low" Input Current	V <sub>IN</sub> = 5.5 V, V <sub>CE</sub> = V <sub>OUT</sub> = 0 V	<span style="border: 1px solid black; padding: 0 2px;">-0.025</span>	0	<span style="border: 1px solid black; padding: 0 2px;">0.025</span>	μA	
R <sub>DISN</sub>	Auto-discharge NMOS On-state Resistance <sup>(1)</sup>	V <sub>IN</sub> = 3.6 V, V <sub>CE</sub> = 0 V		60		Ω	
V <sub>CEH</sub>	CE Pin Input Voltage, high	V <sub>IN</sub> = 5.5 V	<span style="border: 1px solid black; padding: 0 2px;">1.0</span>			V	
V <sub>CEL</sub>	CE Pin Input Voltage, low	V <sub>IN</sub> = 2.0 V			<span style="border: 1px solid black; padding: 0 2px;">0.4</span>	V	
R <sub>ONP</sub>	PMOS On-state Resistance	RP511Z	V <sub>IN</sub> = 3.6 V, I <sub>LX</sub> = -100 mA		0.15		Ω
		RP511K	V <sub>IN</sub> = 3.6 V, I <sub>LX</sub> = -100 mA		0.19		Ω
		RP511H	V <sub>IN</sub> = 3.6 V, I <sub>LX</sub> = -100 mA		0.19		Ω
R <sub>ONN</sub>	NMOS On-state Resistance	RP511Z	V <sub>IN</sub> = 3.6 V, I <sub>LX</sub> = -100 mA		0.15		Ω
		RP511K	V <sub>IN</sub> = 3.6 V, I <sub>LX</sub> = -100 mA		0.19		Ω
		RP511H	V <sub>IN</sub> = 3.6 V, I <sub>LX</sub> = -100 mA		0.19		Ω
t <sub>START</sub>	Soft-start Time	V <sub>IN</sub> = V <sub>CE</sub> = 3.6 V (V <sub>SET</sub> ≤ 2.6 V), V <sub>IN</sub> = V <sub>CE</sub> = V <sub>SET</sub> + 1 V (V <sub>SET</sub> > 2.6 V)		10		ms	
I <sub>LXLIM</sub>	LX Current Limit	V <sub>IN</sub> = V <sub>CE</sub> = 3.6 V (V <sub>SET</sub> ≤ 2.6 V), V <sub>IN</sub> = V <sub>CE</sub> = V <sub>SET</sub> + 1 V (V <sub>SET</sub> > 2.6 V)	<span style="border: 1px solid black; padding: 0 2px;">210</span>	430		mA	
V <sub>UVLOF</sub>	Undervoltage Lockout (UVLO) Threshold	V <sub>IN</sub> = V <sub>CE</sub> , Falling	<span style="border: 1px solid black; padding: 0 2px;">1.40</span>	1.50	<span style="border: 1px solid black; padding: 0 2px;">1.65</span>	V	
V <sub>UVLOR</sub>		V <sub>IN</sub> = V <sub>CE</sub> , Rising	<span style="border: 1px solid black; padding: 0 2px;">1.55</span>	1.65	<span style="border: 1px solid black; padding: 0 2px;">1.80</span>	V	

All test items listed under Electrical Characteristics are done under the pulse load condition ( $T_j \approx T_a = 25^{\circ}\text{C}$ ).  
Test circuit is operated with "Open Loop Control" (GND = 0 V), unless otherwise specified.

<sup>(1)</sup> RP511xxx1B only

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**RP511x**

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**Product-specific Electrical Characteristics**

Product Name	V <sub>OUT</sub>		
	Min.	Typ.	Max.
RP511x101x	0.9820	1.00	1.0180
RP511x111x	1.0820	1.10	1.1180
RP511x121x	1.1820	1.20	1.2180
RP511x131x	1.2805	1.30	1.3195
RP511x141x	1.3790	1.40	1.4210
RP511x151x	1.4775	1.50	1.5225
RP511x161x	1.5760	1.60	1.6240
RP511x171x	1.6745	1.70	1.7255
RP511x181x	1.7730	1.80	1.8270
RP511x191x	1.8715	1.90	1.9285
RP511x201x	1.9700	2.00	2.0300
RP511x211x	2.0685	2.10	2.1315
RP511x221x	2.1670	2.20	2.2330
RP511x231x	2.2655	2.30	2.3345
RP511x241x	2.3640	2.40	2.4360
RP511x251x	2.4625	2.50	2.5375
RP511x261x	2.5610	2.60	2.6390
RP511x271x	2.6595	2.70	2.7405
RP511x281x	2.7580	2.80	2.8420
RP511x291x	2.8565	2.90	2.9435
RP511x301x	2.9550	3.00	3.0450
RP511x311x	3.0535	3.10	3.1465
RP511x321x	3.1520	3.20	3.2480
RP511x331x	3.2505	3.30	3.3495
RP511x341x	3.3490	3.40	3.4510
RP511x351x	3.4475	3.50	3.5525
RP511x361x	3.5460	3.60	3.6540
RP511x371x	3.6445	3.70	3.7555
RP511x381x	3.7430	3.80	3.8570
RP511x391x	3.8415	3.90	3.9585
RP511x401x	3.9400	4.00	4.0600



## THEORY OF OPERATION

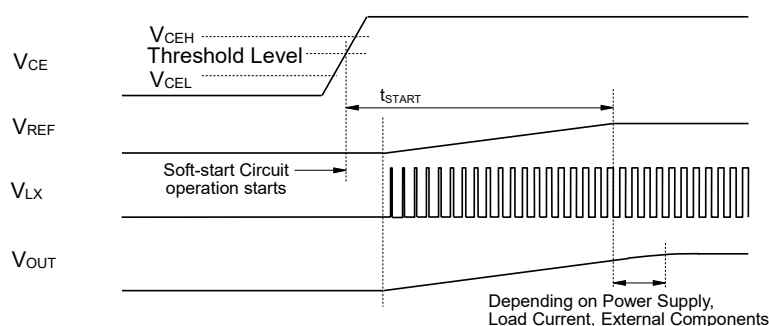
### Soft-start Time

#### Starting-up with CE Pin

The IC starts to operate when the CE pin voltage ( $V_{CE}$ ) exceeds the threshold voltage. The threshold voltage is preset between CE "H" input voltage ( $V_{CEH}$ ) and CE "Low" input voltage ( $V_{CEL}$ ).

After the start-of the start-up of the IC, soft-start circuit starts to operate. Then, after a certain period of time, the reference voltage ( $V_{REF}$ ) in the IC gradually increases up to the specified value.

Notes: Soft start time ( $t_{START}$ )<sup>(1)</sup> is not always equal to the turn-on speed of the step-down DC/DC converter. Please note that the turn-on speed could be affected by the power supply capacity, the output current, the inductance value and the  $C_{OUT}$  value.

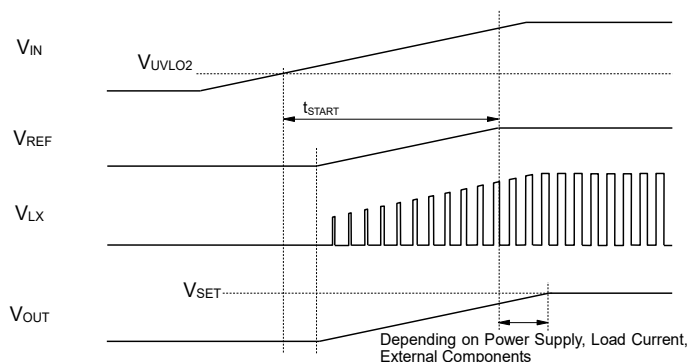


Timing Chart when Starting-up with CE Pin

#### Starting-up with Power Supply

After the power-on, when  $V_{IN}$  exceeds the UVLO released voltage ( $V_{UVLO2}$ ), the IC starts to operate. Then, soft-start circuit starts to operate and after a certain period of time,  $V_{REF}$  gradually increases up to the specified value.

Note: Please note that the turn-on speed of  $V_{OUT}$  could be affected by the power supply capacity, the output current, the inductance value, the  $C_{OUT}$  value and the turn-on speed of  $V_{IN}$  determined by  $C_{IN}$ .



Timing Chart when Starting-up with Power Supply

<sup>(1)</sup> Soft-start time ( $t_{START}$ ) indicates the duration until the reference voltage ( $V_{REF}$ ) reaches the specified voltage after soft-start circuit's activation.

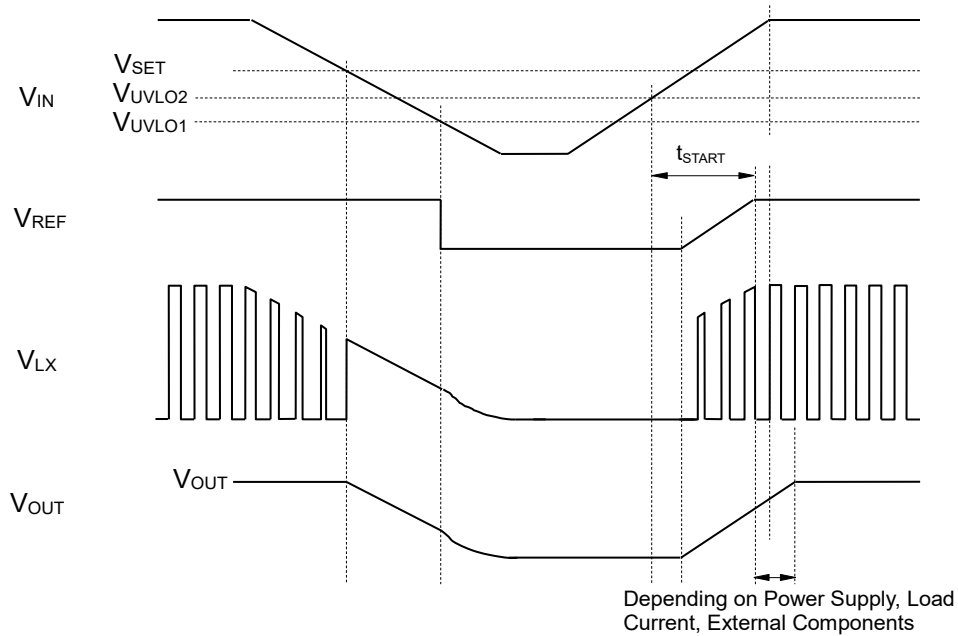
**Undervoltage Lockout (UVLO) Circuit**

If  $V_{IN}$  becomes lower than  $V_{SET}$ , the step-down DC/DC converter stops the switching operation and ON duty becomes 100%, and then  $V_{OUT}$  gradually drops according to  $V_{IN}$ . If the  $V_{IN}$  drops more and becomes lower than the UVLO detector threshold ( $V_{UVLO1}$ ), the UVLO circuit starts to operate,  $V_{REF}$  stops, and PMOS and NMOS built-in switch transistors turn "OFF". As a result,  $V_{OUT}$  drops according to the  $C_{OUT}$  capacitance value and  $I_{OUT}$ .

As for RP511xxx1B, the discharge transistor for  $C_{OUT}$  discharges after it turns on. To restart the operation,  $V_{IN}$  needs to be higher than  $V_{UVLO2}$ .

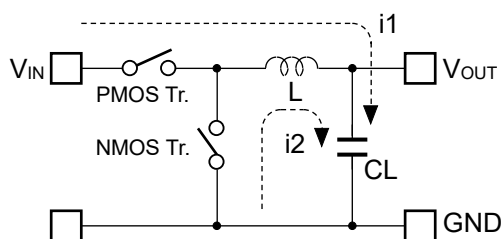
The timing chart below shows the voltage shifts of  $V_{REF}$ ,  $V_{LX}$  and  $V_{OUT}$  when  $V_{IN}$  value is varied.

Note: Falling edge (operating) and rising edge (releasing) waveforms of  $V_{OUT}$  could be affected by the initial voltage of  $C_{OUT}$  and the output current of  $V_{OUT}$ .

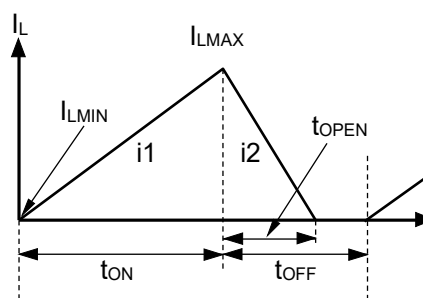
**Timing Chart with Variations in Input Voltage ( $V_{IN}$ )**

### Operation of Step-down DC/DC Converter and Output Current

The step-down DC/DC converter charges energy in the inductor when LX transistor turns “ON”, and discharges the energy from the inductor when LX transistor turns “OFF” and controls with less energy loss, so that a lower output voltage ( $V_{OUT}$ ) than the input voltage ( $V_{IN}$ ) can be obtained. The operation of the step-down DC/DC converter is explained in the following figures.



Basic Circuit



Inductor Current ( $I_L$ ) flowing through Inductor ( $L$ )

- Step1.** PMOS transistor turns “ON” and  $I_L$  ( $i1$ ) flows,  $L$  is charged with energy. At this moment,  $i1$  increases from the minimum inductor current ( $I_{LMIN}$ ), which is 0 A, and reaches the maximum inductor current ( $I_{LMAX}$ ) in proportion to the on-time period ( $t_{ON}$ ) of PMOS Transistor.
- Step2.** When PMOS transistor turns “OFF”,  $L$  tries to maintain  $I_L$  at  $I_{LMAX}$ , so  $L$  turns NMOS transistor “ON” and  $I_L$  ( $i2$ ) flows into  $L$ .
- Step3.**  $i2$  decreases gradually and reaches  $I_{LMIN}$  after the open-time period ( $t_{OPEN}$ ) of NMOS transistor, and then NMOS transistor turns “OFF”. This is called discontinuous current mode.  
As the output current ( $I_{OUT}$ ) increases, the off-time period ( $t_{OFF}$ ) of PMOS transistor runs out before  $I_L$  reaches  $I_{LMIN}$ . The next cycle starts, and PMOS transistor turns “ON” and NMOS transistor turns “OFF”, which means  $I_L$  starts increasing from  $I_{LMIN}$ . This is called continuous current mode.

When the step-down DC/DC operation is constant,  $I_{LMIN}$  and  $I_{LMAX}$  during  $t_{ON}$  of PMOS transistor would be same as during  $t_{OFF}$  of PMOS transistor. The current differential between  $I_{LMAX}$  and  $I_{LMIN}$  is described as  $\Delta I$ , as the following equation 1.

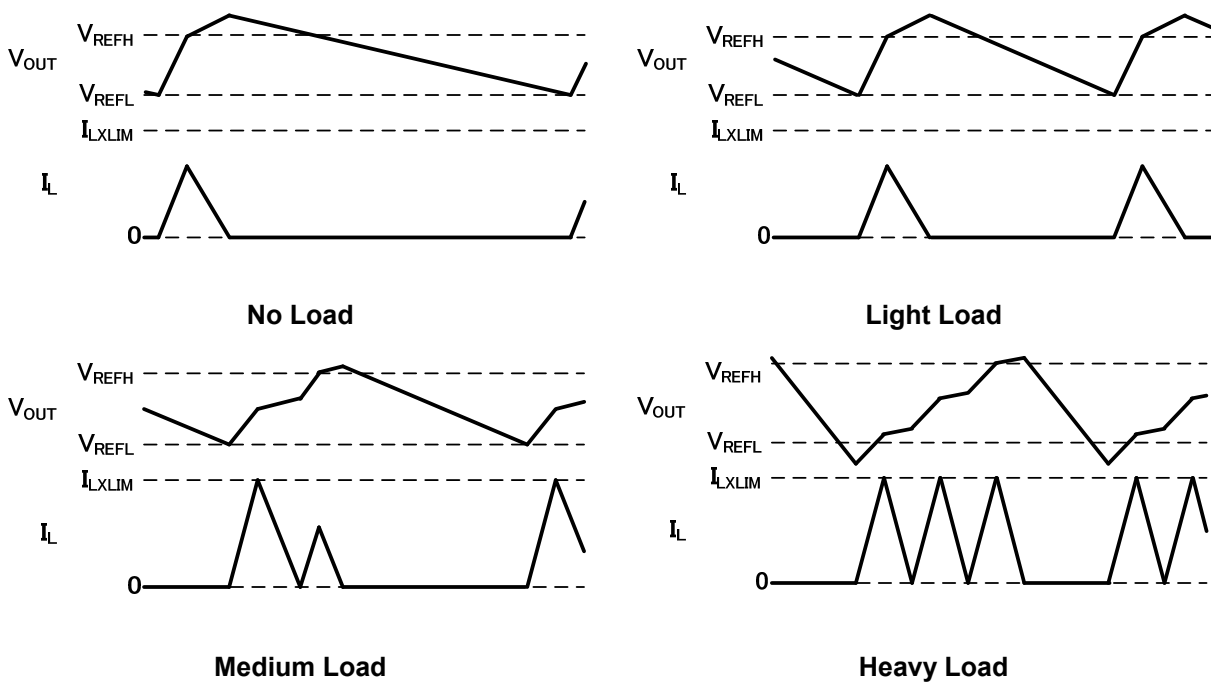
$$\Delta I = I_{LMAX} - I_{LMIN} = V_{OUT} \times t_{OPEN} / L = (V_{IN} - V_{OUT}) \times t_{ON} / L \dots \dots \dots (1)$$

**VFM Mode**

A switching method is a VFM (Variable Frequency Modulation) mode to achieve a high efficiency during light load conditions. A switching frequency varies depending on values of input voltage ( $V_{IN}$ ), output voltage ( $V_{OUT}$ ), and output current ( $I_{OUT}$ ). Check the actual characteristics for concerns regarding the switching noise.

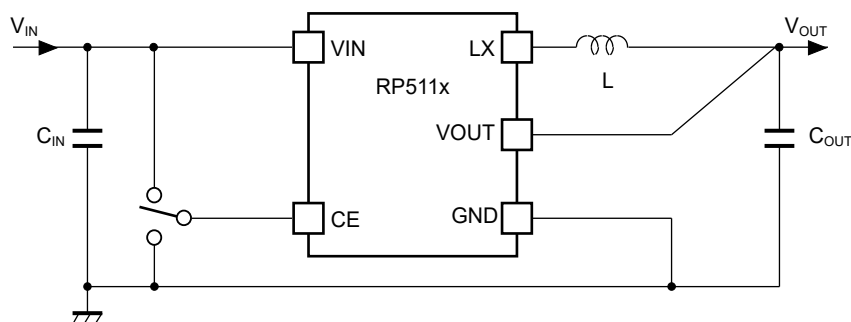
A switching starts when  $V_{OUT}$  drops below the lower-limit reference voltage ( $V_{REFL}$ ). When  $V_{OUT}$  exceeds the upper-limit reference voltage ( $V_{REFH}$ ), a constant voltage outputs by a hysteresis control which stops the switching.

In order not to exceed the rated current of inductor or to avoid using the deteriorated band frequency of DC superimposed characteristics, the operation shifts to off-cycle once when the inductor current ( $I_L$ ) exceeds LX current limit ( $I_{LXLIM}$ ), and then it shifts back to on-cycle again when  $I_L$  becomes 0 A.



## APPLICATION INFORMATION

### Typical Application



RP511x Typical Application

### Recommended External Components

Symbol	Descriptions
C <sub>IN</sub>	10 μF, GRM155R60J106ME44D, MURATA
C <sub>OUT</sub>	22 μF, JMK107BBJ226MA-T, TAIYO
L	2.2 μH, MBKK1608T2R2M, TAIYO 2.2 μH, MLP2012H2R2MT0S1, TDK

### ● Precautions for Selecting External Components

- Using ceramic capacitors with low ESR (Equivalent Series Resistance) are recommended. Select capacitors with considerations of bias characteristics and input/output voltages.
- When a built-in Lx switch is turned off, a spike-like high voltage may be generated due to an action of an inductor. Using 1.5 times or more of a set output voltage is recommended for the withstanding voltage of C<sub>OUT</sub>.
- Select an inductor that has small DC resistance, has sufficient allowable current and is hard to cause magnetic saturation.

## TECHNICAL NOTES

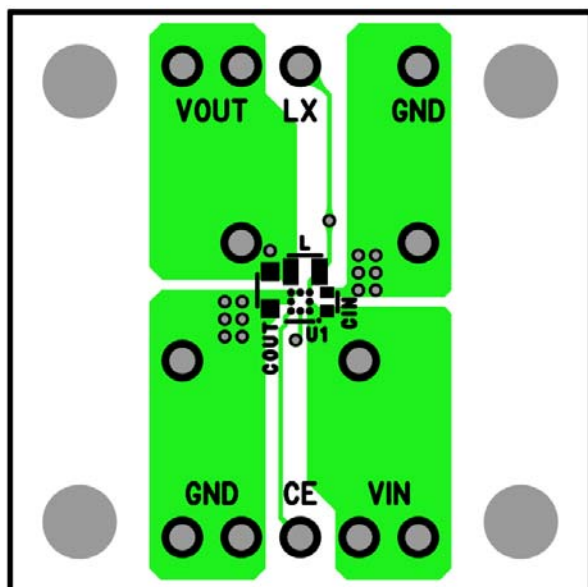
The performance of a power source circuit using this device is highly dependent on a peripheral circuit. A peripheral component or the device mounted on PCB should not exceed a rated voltage, a rated current or a rated power. When designing a peripheral circuit, please be fully aware of the following points. Refer to *PCB Layout* below.

- External components must be connected as close as possible to the ICs and make wiring as short as possible. Especially, the capacitor connected in between VIN pin and GND pin must be wiring the shortest.
- If the impedance of power supply lines and GND lines is high, the internal voltage of the IC may shift by the switching current, and the operating may be unstable. Make the power supply and GND lines sufficient.
- A sufficient consideration is required due to a large switching current flows through power supply lines, GND lines, an inductor, L<sub>X</sub>, and V<sub>OUT</sub> line.
- The wiring between V<sub>OUT</sub> pin and inductor should be separated from the wiring connected to the load.
- When an intermediate voltage other than V<sub>IN</sub> or GND is input to the CE pin, a supply current may be increased with a through current of a logic circuit in the IC. The CE pin is neither pulled up nor pulled down, therefore an operation is not stable at open.

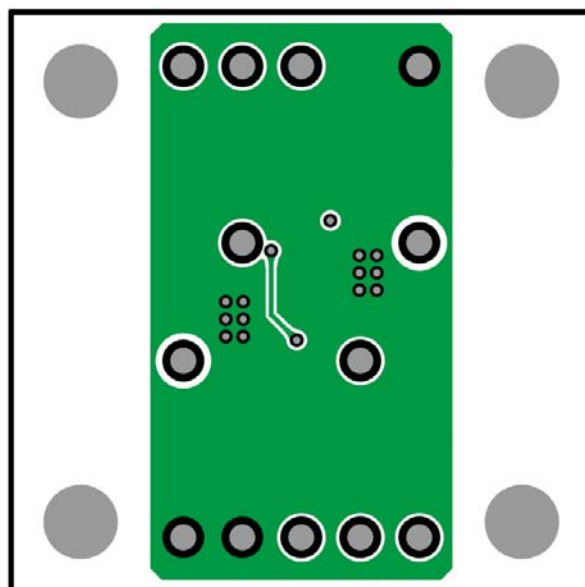
PCB Layout

RP511Zxx1x (WLCSP-8-P1)

Top Layer

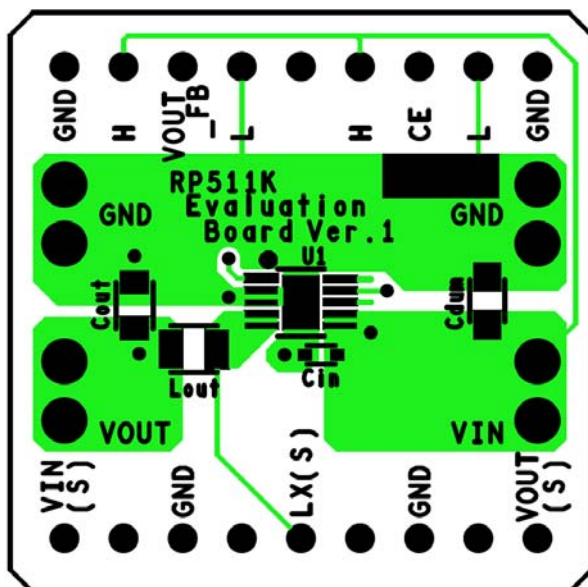


Bottom Layer

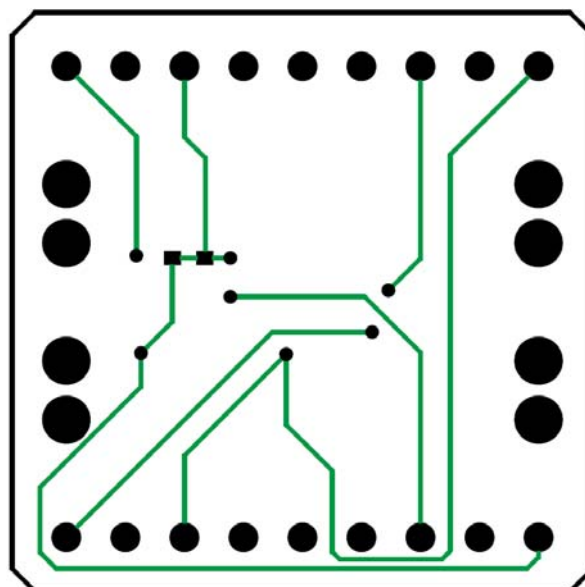


RP511Kxx1x [DFN(PLP)2527-10]

Top Layer



Bottom Layer



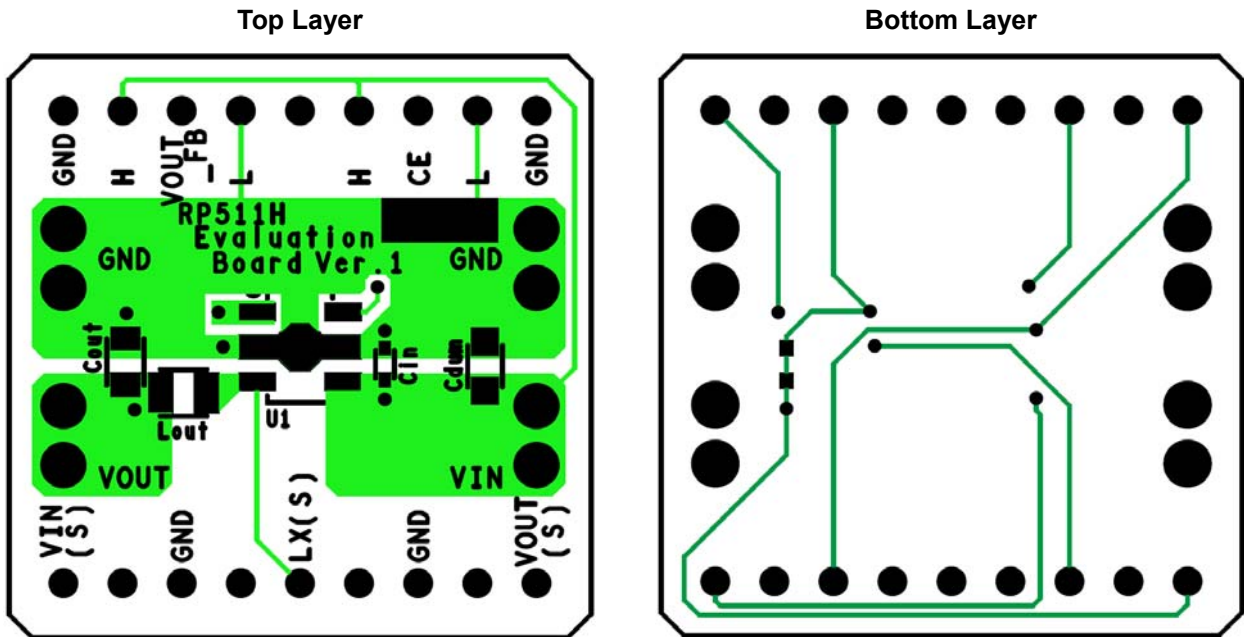
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## RP511x

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No. EA-502-190401

### RP511Hxx1x (SOT-89-5)

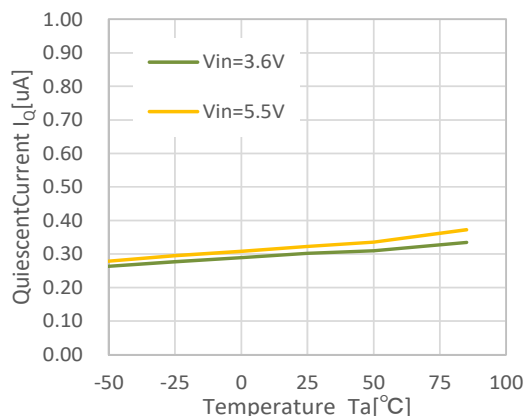




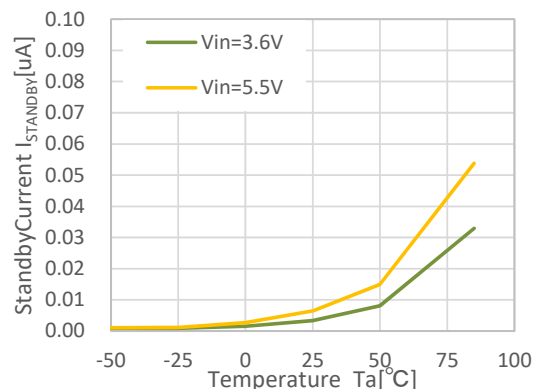
## TYPICAL CHARACTERISTICS

Typical Characteristics are intended to be used as reference data; they are not guaranteed.  
As for the inductor, MLP2012H2R2MT0S1 (TDK) is used.

### 1) Quiescent Current vs. Temperature

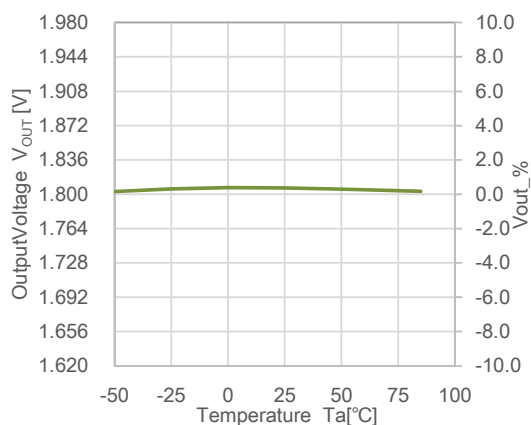


### 2) Standby Current vs. Temperature



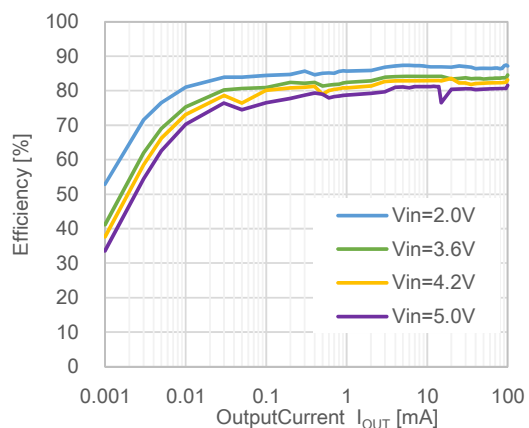
### 3) Output Voltage vs. Temperature

RP511x181x, V<sub>IN</sub> = 3.6 V

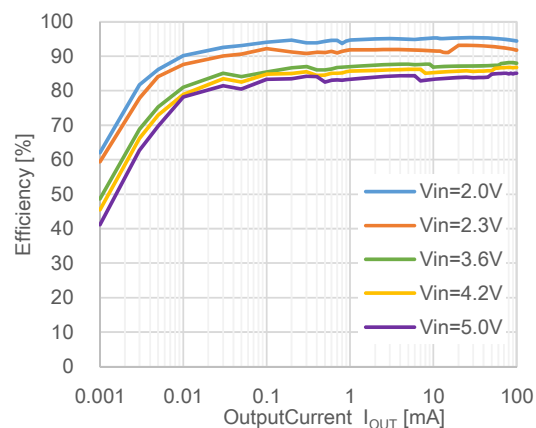


### 4) Efficiency vs. Output Current

RP511x121x, Ta = 25°C



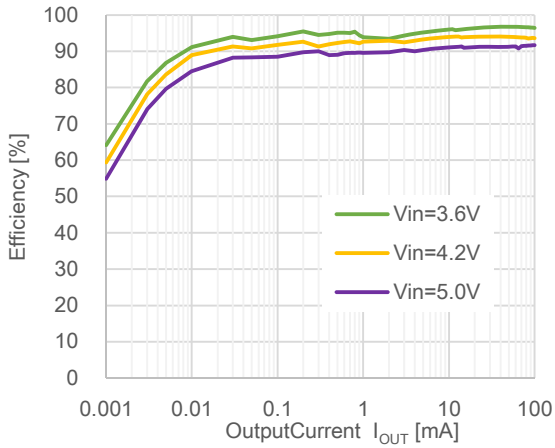
RP511x181x, Ta = 25°C



# RP511x

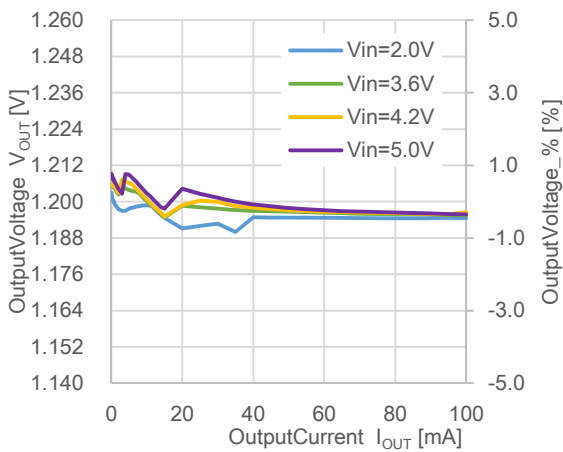
No. EA-502-190401

RP511x331x, Ta = 25°C

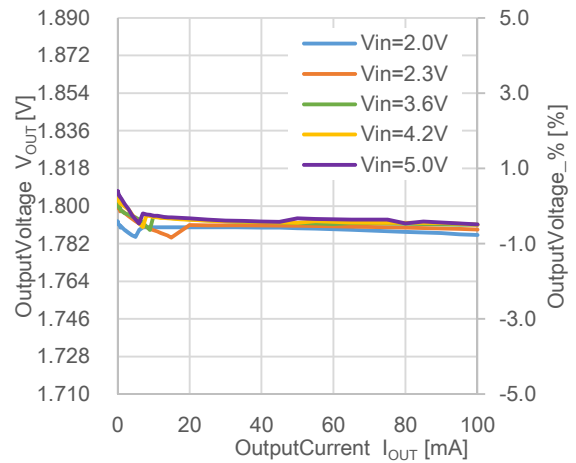


## 5) Output Voltage vs. Output Current

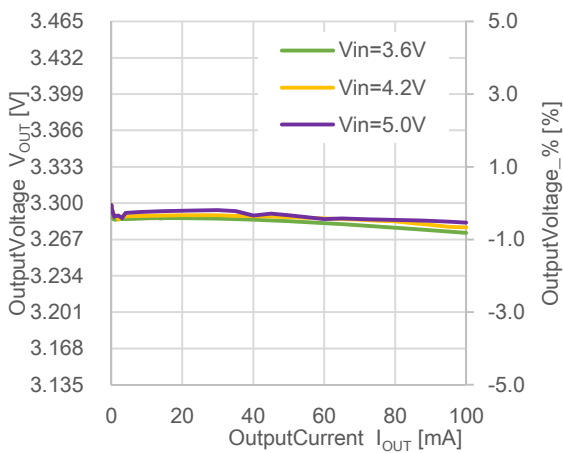
RP511x121x, Ta = 25°C



RP511x181x, Ta = 25°C

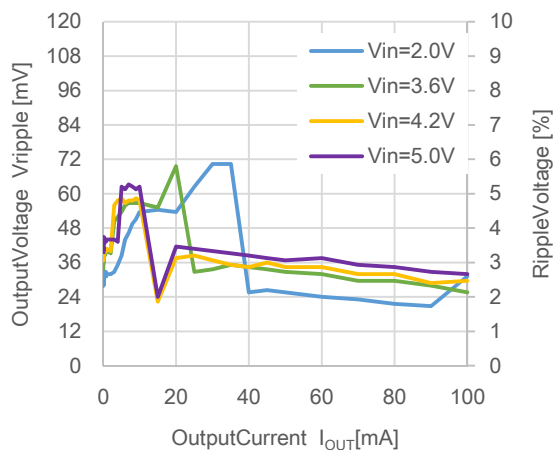


RP511x331x, Ta = 25°C

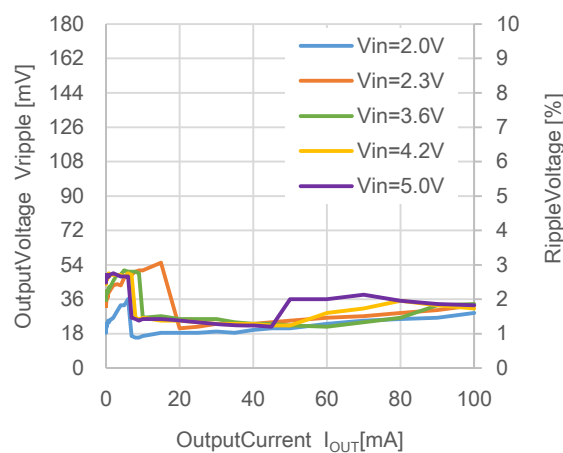


6) Ripple Voltage vs. Output Current

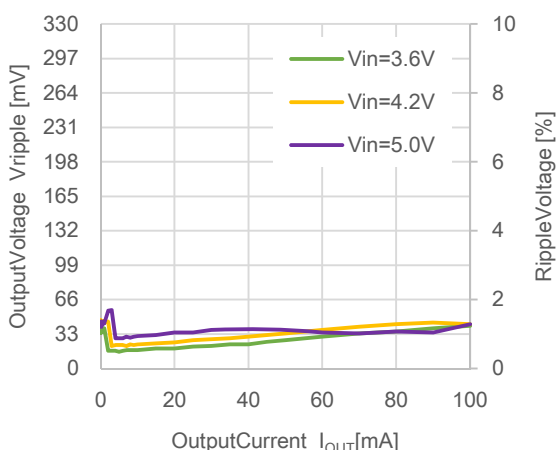
RP511x121x, Ta = 25°C



RP511x181x, Ta = 25°C

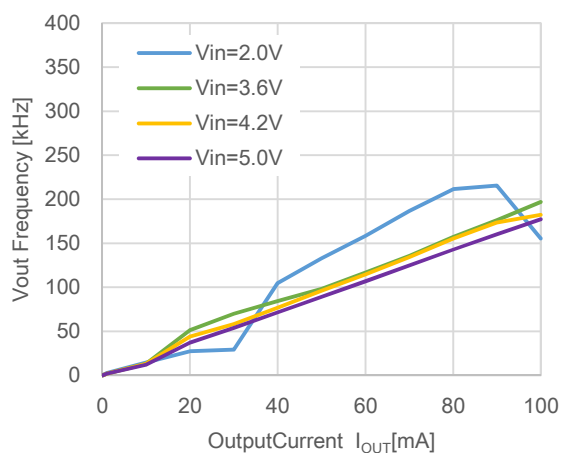


RP511x331x, Ta = 25°C

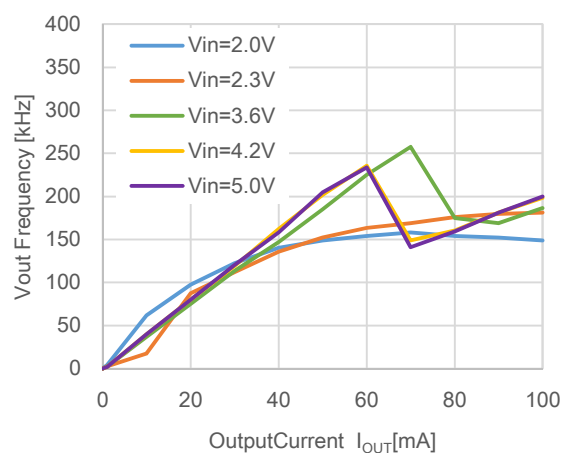


7) Switching Frequency vs. Output Current

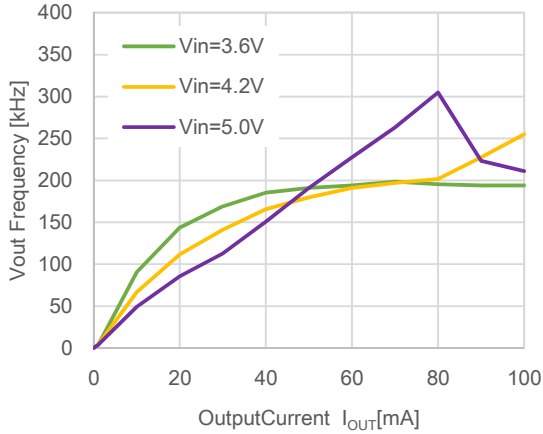
RP511x121x, Ta = 25°C



RP511x181x, Ta = 25°C

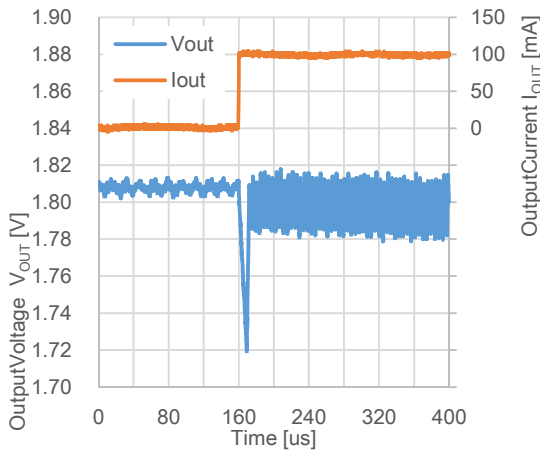


RP511x331x, Ta = 25°C

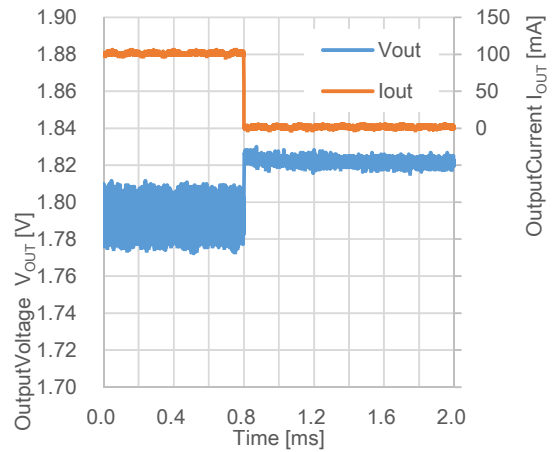


**8) Load Transient Response**

RP511x181x, Ta = 25°C, V<sub>IN</sub> = 3.6 V  
I<sub>OUT</sub> = 0.01 mA -> 50 mA



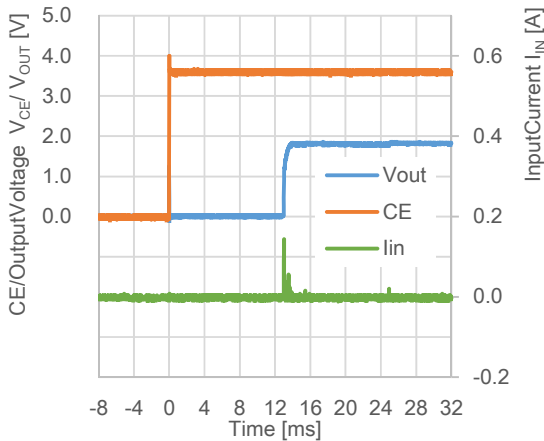
I<sub>OUT</sub> = 50 mA -> 0.01 mA



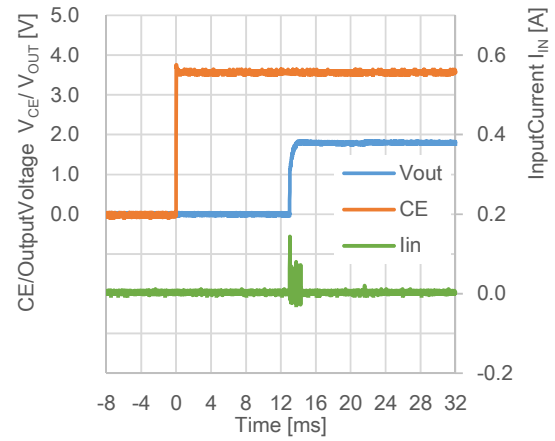
**9) Soft Start Time**

RP511x181x, Ta = 25°C

V<sub>IN</sub> = V<sub>CE</sub> = 0 V -> 3.6 V, Δt = 10 μs



V<sub>IN</sub> = 3.6 V, V<sub>CE</sub> = 0 V -> 3.6 V, Δt = 10 μs



The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following measurement conditions are based on JEDEC STD. 51-9.

**Measurement Conditions**

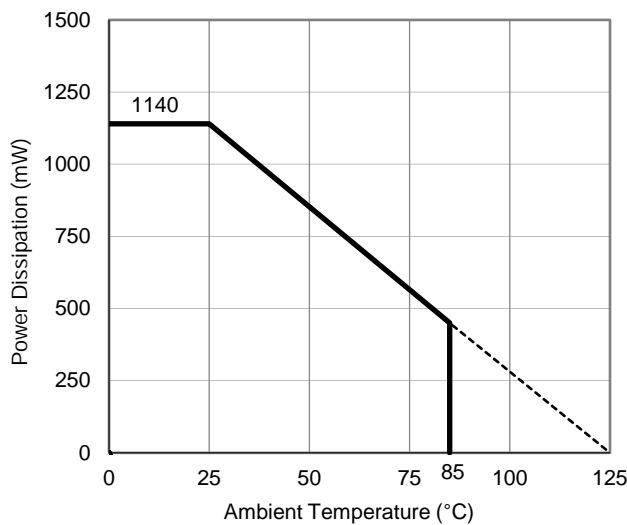
Item	Measurement Conditions
Environment	Mounting on Board (Wind Velocity = 0 m/s)
Board Material	Glass Cloth Epoxy Plastic (Four-Layer Board)
Board Dimensions	101.5 mm x 114.5 mm x 1.6 mm
Copper Ratio	Outer Layers (First and Fourth Layers): 60% Inner Layers (Second and Third Layers): 100%

**Measurement Result**

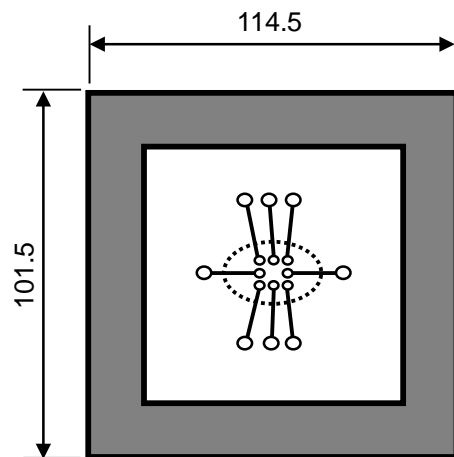
(Ta = 25°C, Tjmax = 125°C)

Item	Measurement Result
Power Dissipation	1140 mW
Thermal Resistance ( $\theta_{ja}$ )	$\theta_{ja} = 87^\circ\text{C/W}$

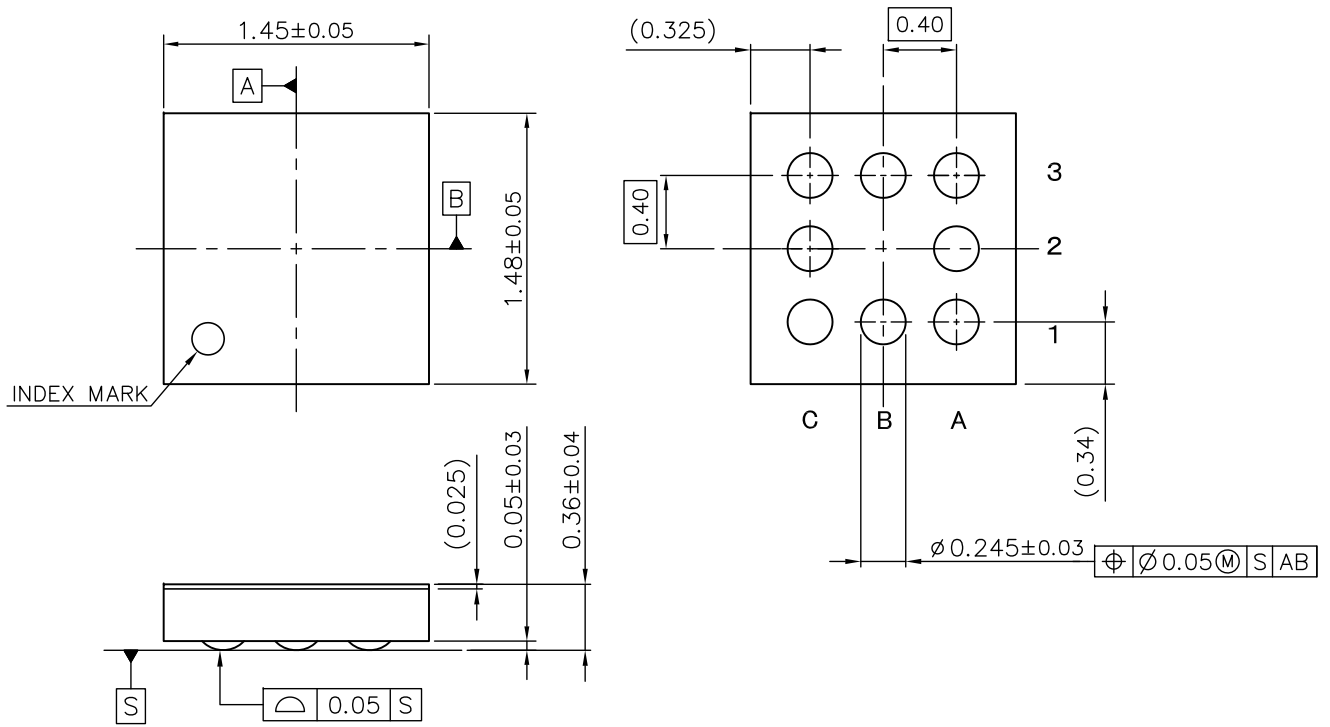
$\theta_{ja}$ : Junction-to-Ambient Thermal Resistance



**Power Dissipation vs. Ambient Temperature**



**Measurement Board Pattern**



WLCSP-8-P1 Package Dimensions (Unit: mm)

The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following measurement conditions are based on JEDEC STD. 51-7.

**Measurement Conditions**

Item	Measurement Conditions
Environment	Mounting on Board (Wind Velocity = 0 m/s)
Board Material	Glass Cloth Epoxy Plastic (Four-Layer Board)
Board Dimensions	76.2 mm × 114.3 mm × 0.8 mm
Copper Ratio	Outer Layer (First Layer): Less than 95% of 50 mm Square Inner Layers (Second and Third Layers): Approx. 100% of 50 mm Square Outer Layer (Fourth Layer): Approx. 100% of 50 mm Square
Through-holes	φ 0.3 mm × 30 pcs

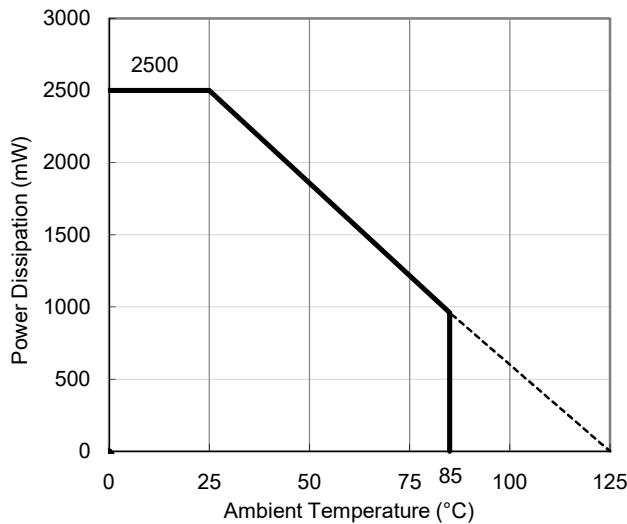
**Measurement Result**

(Ta = 25°C, Tjmax = 125°C)

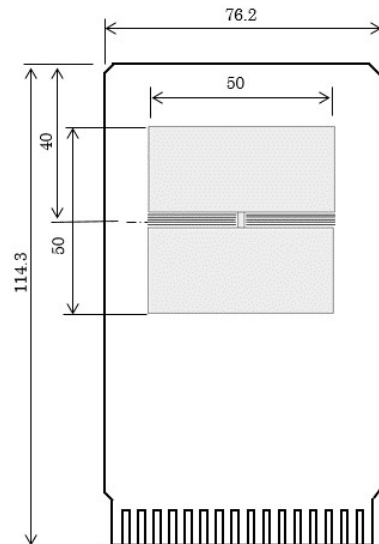
Item	Measurement Result
Power Dissipation	2500 mW
Thermal Resistance (θja)	θja = 39°C/W
Thermal Characterization Parameter (ψjt)	ψjt = 11°C/W

θja: Junction-to-Ambient Thermal Resistance

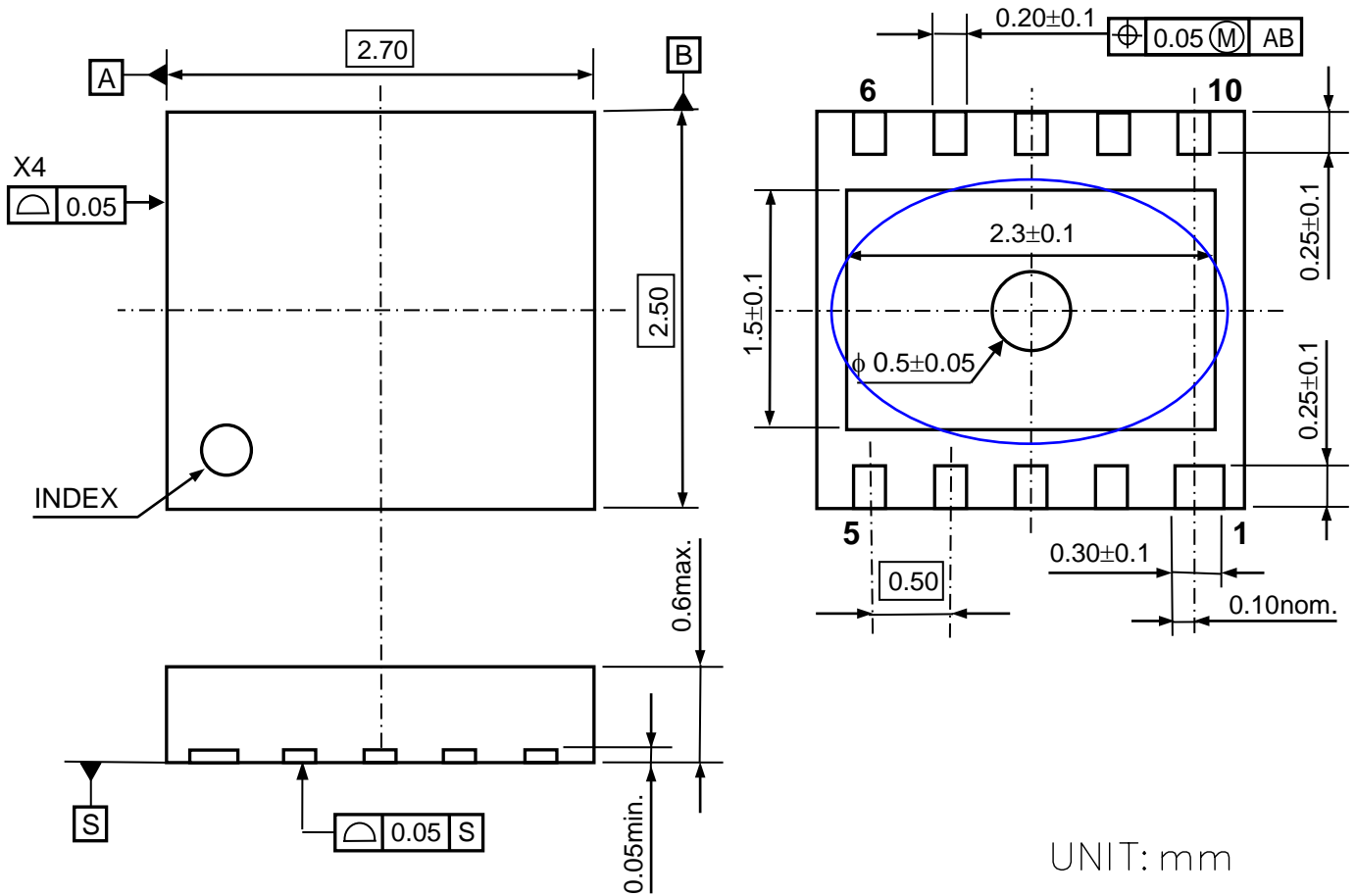
ψjt: Junction-to-Top Thermal Characterization Parameter



**Power Dissipation vs. Ambient Temperature**



**Measurement Board Pattern**



DFN(PLP)2527-10 Package Dimensions

\* The tab on the bottom of the package is substrate level (GND). It is recommended that the tab be connected to the ground plane on the board, or otherwise be left floating.



The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following measurement conditions are based on JEDEC STD. 51-7.

**Measurement Conditions**

Item	Measurement Conditions
Environment	Mounting on Board (Wind Velocity = 0 m/s)
Board Material	Glass Cloth Epoxy Plastic (Four-Layer Board)
Board Dimensions	76.2 mm × 114.3 mm × 0.8 mm
Copper Ratio	Outer Layer (First Layer): Less than 95% of 50 mm Square Inner Layers (Second and Third Layers): Approx. 100% of 50 mm Square Outer Layer (Fourth Layer): Approx. 100% of 50 mm Square
Through-holes	φ 0.3 mm × 13 pcs

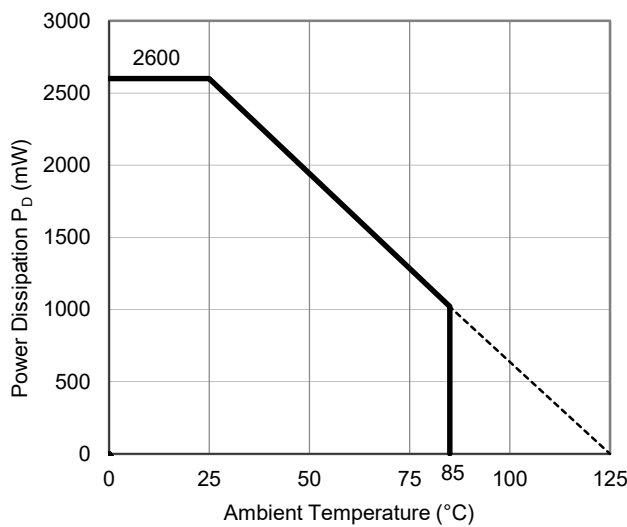
**Measurement Result**

(Ta = 25°C, Tjmax = 125°C)

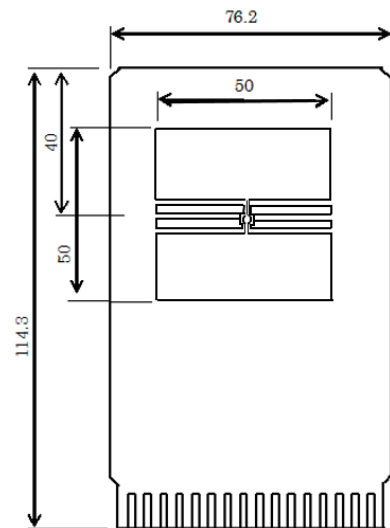
Item	Measurement Result
Power Dissipation	2600 mW
Thermal Resistance (θja)	θja = 38°C/W
Thermal Characterization Parameter (ψjt)	ψjt = 13°C/W

θja: Junction-to-Ambient Thermal Resistance

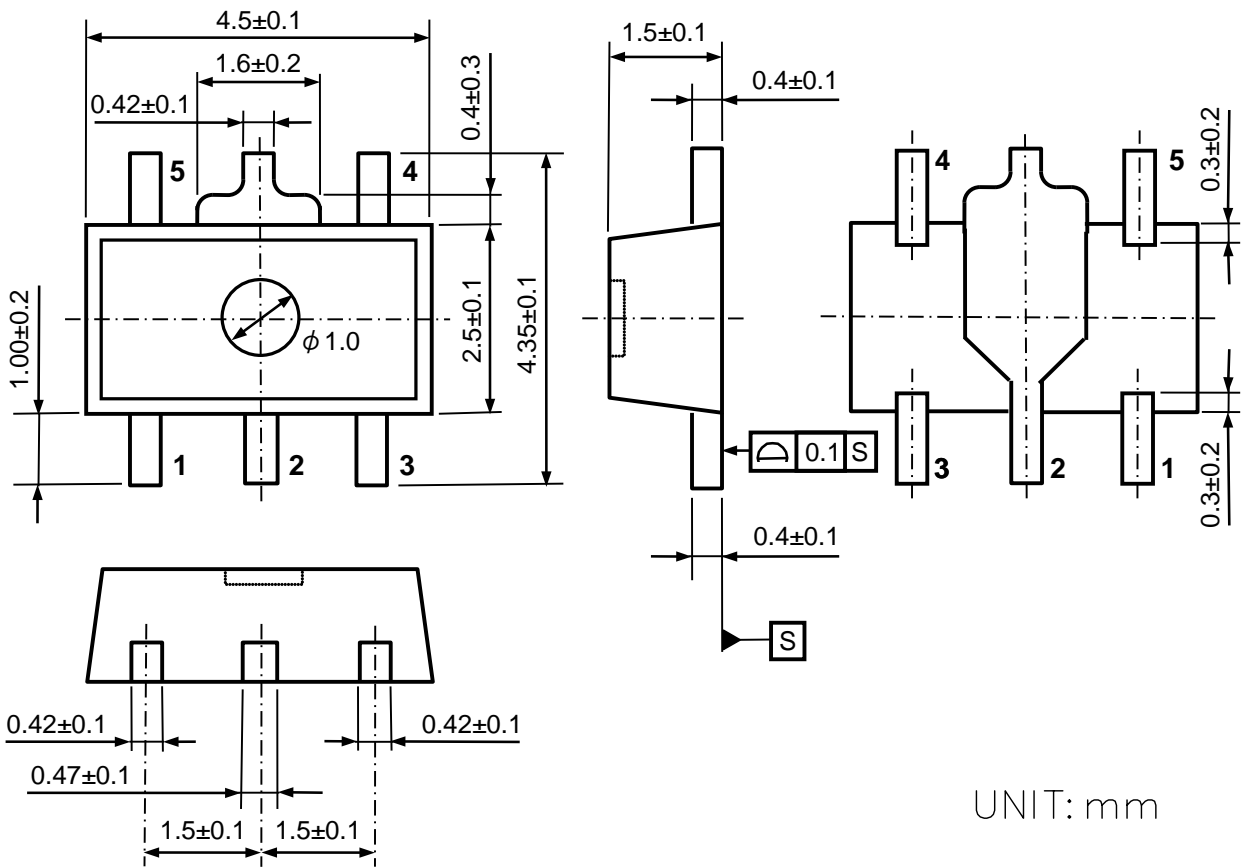
ψjt: Junction-to-Top Thermal Characterization Parameter



**Power Dissipation vs. Ambient Temperature**



**Measurement Board Pattern**



SOT-89-5 Package Dimensions



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