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February 2015

2N5550 NPN Epitaxial Silicon Transistor

Features

- Amplifier Transistor
- Collector-Emitter Voltage: V_{CEO} = 140 V



Ordering Information

Part Number	Top Mark	Package	Packing Method		
2N5550BU	2N5550	TO-92 3L	Bulk		
2N5550TA	2N5550	TO-92 3L	Ammo		
2N5550TAR	2N5550	TO-92 3L	Ammo		
2N5550TF	2N5550	TO-92 3L	Tape and Reel		
2N5550TFR	2N5550	2N5550 TO-92 3L Tape and R			

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Values are at $T_A = 25^{\circ}\text{C}$ unless otherwise noted.

Symbol	Parameter	Value	Unit
V _{CBO}	Collector-Base Voltage	160	V
V _{CEO}	Collector-Emitter Voltage	140	V
V _{EBO}	Emitter-Base Voltage	6	V
I _C	Collector Current	600	mA
TJ	Junction Temperature	150	°C
T _{STG}	Storage Temperature	-55 to 150	°C

Thermal Characteristics(1)

Values are at $T_A = 25$ °C unless otherwise noted.

Symbol	Parameter	Max.	Unit
В	Total Device Dissipation	625	mW
P _D	Derate Above 25°C	5.0	mW/°C
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	200	°C/W

Note:

1. PCB size: FR-4, 76 mm x 114 mm x 1.57 mm (3.0 inch x 4.5 inch x 0.062 inch) with minimum land pattern size.

Electrical Characteristics

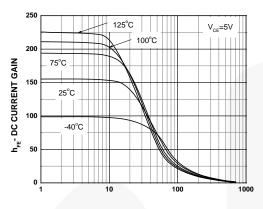
Values are at $T_A = 25$ °C unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit	
BV _{CBO}	Collector-Base Breakdown Voltage	$I_C = 100 \mu\text{A}, I_E = 0$	160			V	
BV _{CEO}	Collector-Emitter Breakdown Voltage ⁽²⁾	$I_C = 1 \text{ mA}, I_B = 0$	140			V	
BV _{EBO}	Emitter-Base Breakdown Voltage	$I_E = 10 \mu A, I_C = 0$	6			V	
I _{CBO}	Collector Cut-Off Current	V _{CB} = 100 V, I _E = 0			100	nA	
I _{EBO}	Emitter Cut-Off Current	$V_{EB} = 4 \text{ V}, I_{C} = 0$			50	nA	
		$I_C = 1 \text{ mA}, V_{CE} = 5 \text{ V}$	60				
h _{FE}	DC Current Gain ⁽²⁾	I _C = 10 mA, V _{CE} = 5 V	60		250		
		$I_C = 50 \text{ mA}, V_{CE} = 5 \text{ V}$	20				
\/ (cot)	Collector-Emitter Saturation Voltage ⁽²⁾	$I_C = 10 \text{ mA}, I_B = 1 \text{ mA}$			0.15	V	
V _{CE} (sat)	Collector-Emitter Saturation voltage	$I_C = 50 \text{ mA}, I_B = 5 \text{ mA}$			0.25	V	
V _{BE} (sat)	Base-Emitter Saturation Voltage ⁽²⁾	$I_C = 10 \text{ mA}, I_B = 1 \text{ mA}$			1.0	V	
v _{BE} (sai)	Base-Emilier Saluration Voltage	$I_C = 50 \text{ mA}, I_B = 5 \text{ mA}$			1.2	V	
f _T	Current Gain Bandwidth Product	I _C = 10 mA, V _{CE} = 10 V f = 100 MHz	100		300	MHz	
C _{ob}	Output Capacitance	V _{CB} = 10 V, I _E = 0, f = 1 MHz			6	pF	
NF	Noise Figure	I_C = 250 μA, V_{CE} = 5 V, R_S = 1 kΩ,f = 10 Hz to 15.7 kHz			10	dB	

Note:

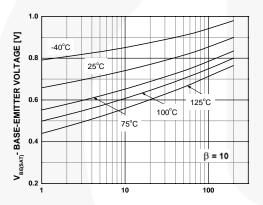
2. Pulse test: pulse width $\leq 300~\mu s,$ duty cycle $\leq 2\%$

Typical Performance Characteristics



I_- COLLECTOR CURRENT [mA]

Figure 1. Typical Pulsed Current Gain vs. Collector Current



I_c- COLLECTOR CURRENT [mA]
Figure 3. Base-Emitter Saturation Voltage vs.
Collector Current

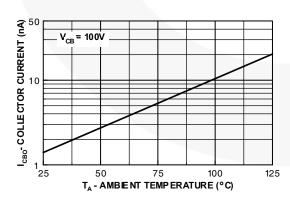
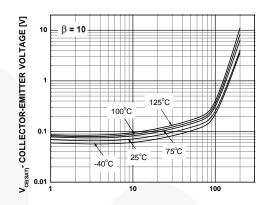
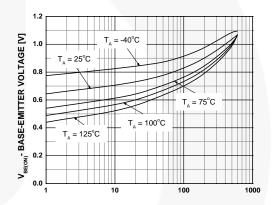


Figure 5. Collector Cut-Off Current vs.
Ambient Temperature



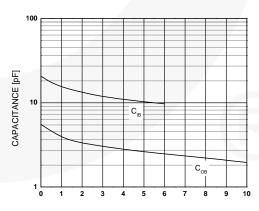
I_- COLLECTOR CURRENT [mA]

Figure 2. Collector-Emitter Saturation Voltage vs. Collector Current



I_c- COLLECTOR CURRENT [mA]

Figure 4. Base-Emitter On Voltage vs. Collector Current



REVERSE BIAS VOLTAGE [V]

Figure 6. Input and Output Capacitance vs. Reverse Voltage

Typical Performance Characteristics (Continued)

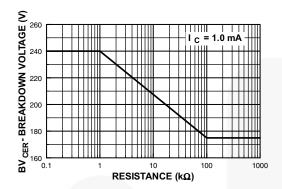


Figure 7. Collector- Emitter Breakdown Voltage with Resistance between Emitter-Base

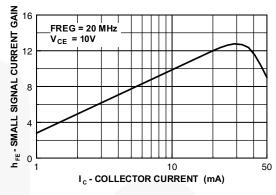


Figure 8. Small Signal Current Gain vs. Collector Current

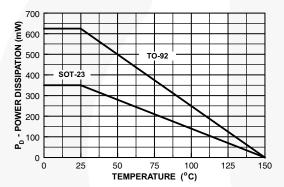
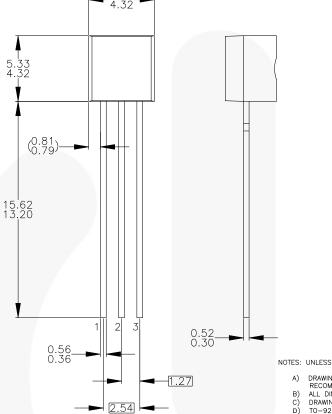


Figure 9. Power Dissipation vs. Ambient Temperature

Physical Dimensions



_4.19 3.05

2 3 NOTES: UNLESS OTHERWISE SPECIFIED

- DRAWING WITH REFERENCE TO JEDEC TO-92 RECOMMENDATIONS. ALL DIMENSIONS ARE IN MILLIMETERS. DRAWING CONFORMS TO ASME Y14.5M-1994. TO-92 (92,94,96,97,98) PIN CONFIGURATION:

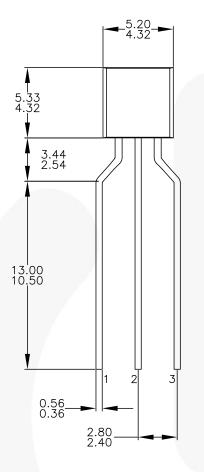
를		92		94		96			97		98				
ā	Ρ	F	М	Ρ	F	М	В	F	М	Ρ	F	М	Р	F	М
1	Ε	S	S	Ε	S	S	В	D	G	О	G	D	С	G	О
2	В	D	G	С	G	D	Ε	S	S	В	D	G	Ε	S	S
3	С	G	D	В	D	G	С	G	D	Ε	S	S	В	D	O
LEGEND: P - BIPOLAR E - EMITTER D - DRAIN F - JFET B - BASE S - SOURCE M - DMCS C - COLLECTOR G - CATF															

E) FOR PACKAGE 92, 94, 96, 97 AND 98:
PIN CONFIGURATION DRAIN "D" AND SOURCE "S"
ARE INTERCHANGEAGLE AT JFET "F" OPTION.
F) DRAWING FILENAME: MKT-ZAJ3DREV3.

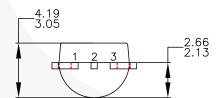
Figure 10. 3-Lead, TO-92, JEDEC TO-92 Compliant Straight Lead Configuration, Bulk Type

_2.66 2.13

Physical Dimensions (Continued)







NOTES: UNLESS OTHERWISE SPECIFIED

- DRAWING CONFORMS TO JEDEC MS-013, VARIATION AC. ALL DIMENSIONS ARE IN MILLIMETERS. DRAWING CONFORMS TO ASME Y14.5M-2009. DRAWING FILENAME: MKT-ZAO3FREV3. FAIRCHILD SEMICONDUCTOR.

Figure 11. 3-Lead, TO-92, Molded, 0.2 In Line Spacing Lead Form, Ammo, Tape and Reel Type





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