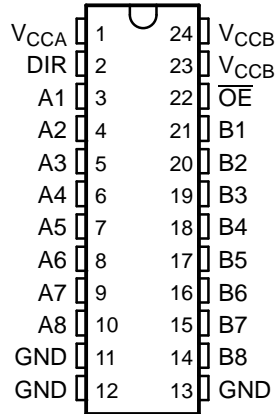


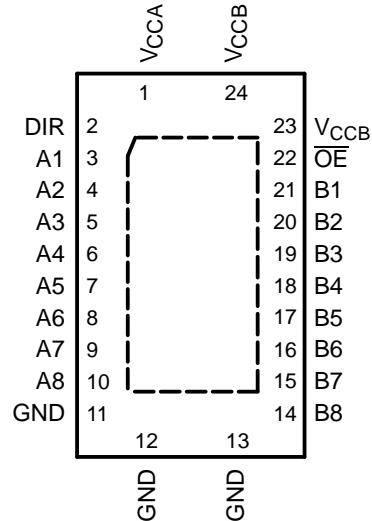
FEATURES

- Control Inputs V_{IH}/V_{IL} Levels Are Referenced to V_{CCA} Voltage
- V_{CC} Isolation Feature – If Either V_{CC} Input Is at GND, All Are in the High-Impedance State
- Fully Configurable Dual-Rail Design Allows Each Port to Operate Over the Full 1.65-V to 5.5-V Power-Supply Range
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 4000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

DB, DBQ, DGV, OR PW PACKAGE
(TOP VIEW)



RHL PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

This 8-bit noninverting bus transceiver uses two separate configurable power-supply rails. The SN74LVC8T245 is optimized to operate with V_{CCA} and V_{CCB} set at 1.65 V to 5.5 V. The A port is designed to track V_{CCA} . V_{CCA} accepts any supply voltage from 1.65 V to 5.5 V. The B port is designed to track V_{CCB} . V_{CCB} accepts any supply voltage from 1.65 V to 5.5 V. This allows for universal low-voltage bidirectional translation between any of the 1.8-V, 2.5-V, 3.3-V, and 5.5-V voltage nodes.

ORDERING INFORMATION

| T_A | PACKAGE ⁽¹⁾ | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---------------|------------------------|---------------|-----------------------|------------------|
| –40°C to 85°C | QFN – RHL | Tape and reel | SN74LVC8T245RHLR | NH245 |
| | SSOP – DBR | Tape and reel | SN74LVC8T245DBR | NH245 |
| | SSOP (QSOP) – DBQ | Tape and reel | SN74LVC8T245DBQR | NH245 |
| | TSSOP – PW | Tube | SN74LVC8T245PW | NH245 |
| | | Tape and reel | SN74LVC8T245PWR | |
| | TVSOP – DGV | Tape and reel | SN74LVC8T245DGVR | NH245 |

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

SN74LVC8T245

8-BIT DUAL-SUPPLY BUS TRANSCEIVER

WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

SCES584A–JUNE 2005–REVISED AUGUST 2005

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

The SN74LVC8T245 is designed for asynchronous communication between two data buses. The logic levels of the direction-control (DIR) input and the output-enable (\overline{OE}) input activate either the B-port outputs or the A-port outputs or place both output ports into the high-impedance mode. The device transmits data from the A bus to the B bus when the B-port outputs are activated, and from the B bus to the A bus when the A-port outputs are activated. The input circuitry on both A and B ports is always active and must have a logic HIGH or LOW level applied to prevent excess I_{CC} and I_{CCZ} .

The SN74LVC8T245 is designed so that the control pins (DIR and \overline{OE}) are supplied by V_{CCA} .

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The V_{CC} isolation feature ensures that if either V_{CC} input is at GND, all outputs are in the high-impedance state.

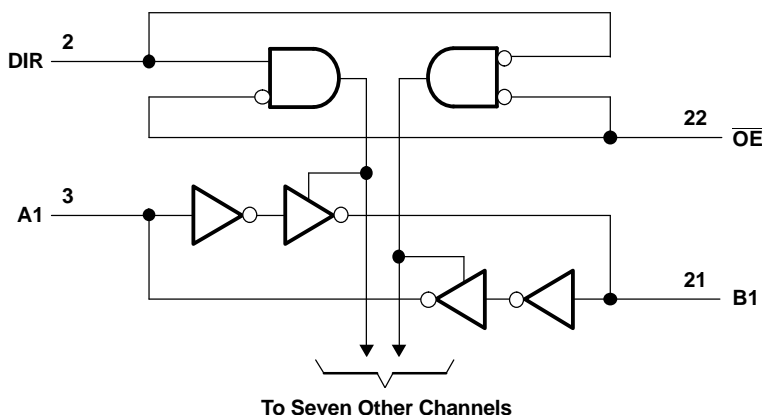
To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

FUNCTION TABLE⁽¹⁾
(EACH 8-BIT SECTION)

| CONTROL INPUTS | | OUTPUT CIRCUITS | | OPERATION |
|-----------------|-----|-----------------|---------|-----------------|
| \overline{OE} | DIR | A PORT | B PORT | |
| L | L | Enabled | Hi-Z | B data to A bus |
| L | H | Hi-Z | Enabled | A data to B bus |
| H | X | Hi-Z | Hi-Z | Isolation |

(1) Input circuits of the data I/Os are always active.

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|------------------------|---|--------------------|------|-----------------|------|
| V_{CCA} V_{CCB} | Supply voltage range | | –0.5 | 6.5 | V |
| V_I | Input voltage range ⁽²⁾ | I/O ports (A port) | –0.5 | 6.5 | V |
| | | I/O ports (B port) | –0.5 | 6.5 | |
| | | Control inputs | –0.5 | 6.5 | |
| V_O | Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾ | A port | –0.5 | 6.5 | V |
| | | B port | –0.5 | 6.5 | |
| V_O | Voltage range applied to any output in the high or low state ⁽²⁾⁽³⁾ | A port | –0.5 | $V_{CCA} + 0.5$ | V |
| | | B port | –0.5 | $V_{CCB} + 0.5$ | |
| I_{IK} | Input clamp current | $V_I < 0$ | | –50 | mA |
| I_{OK} | Output clamp current | $V_O < 0$ | | –50 | mA |
| I_O | Continuous output current | | | ±50 | mA |
| | Continuous current through each V_{CCA} , V_{CCB} , and GND | | | ±100 | mA |
| θ_{JA} | Package thermal impedance ⁽⁴⁾ | DB package | | 63 | °C/W |
| | | DBQ package | | 61 | |
| | | DGV package | | 86 | |
| | | PW package | | 88 | |
| | | RHL package | | 43 | |
| T_{stg} | Storage temperature range | | –65 | 150 | °C |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The output positive-voltage rating may be exceeded up to 6.5 V maximum if the output current rating is observed.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

SN74LVC8T245

8-BIT DUAL-SUPPLY BUS TRANSCEIVER

WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

SCES584A–JUNE 2005–REVISED AUGUST 2005

Recommended Operating Conditions⁽¹⁾⁽²⁾⁽³⁾⁽⁴⁾

| | | | V _{CCI} | V _{CCO} | MIN | MAX | UNIT |
|------------------|------------------------------------|--|------------------|------------------|-------------------------|------------------|------|
| V _{CCA} | Supply voltage | | | | 1.65 | 5.5 | V |
| V _{CCB} | | | | | 1.65 | 5.5 | |
| V _{IH} | High-level input voltage | Data inputs ⁽⁵⁾ | 1.65 V to 1.95 V | | V _{CCI} × 0.65 | | V |
| | | | 2.3 V to 2.7 V | | 1.7 | | |
| | | | 3 V to 3.6 V | | 2 | | |
| | | | 4.5 V to 5.5 V | | V _{CCI} × 0.7 | | |
| V _{IL} | Low-level input voltage | Data inputs ⁽⁵⁾ | 1.65 V to 1.95 V | | V _{CCI} × 0.35 | | V |
| | | | 2.3 V to 2.7 V | | 0.7 | | |
| | | | 3 V to 3.6 V | | 0.8 | | |
| | | | 4.5 V to 5.5 V | | V _{CCI} × 0.3 | | |
| V _{IH} | High-level input voltage | Control inputs (referenced to V _{CCA}) ⁽⁶⁾ | 1.65 V to 1.95 V | | V _{CCA} × 0.65 | | V |
| | | | 2.3 V to 2.7 V | | 1.7 | | |
| | | | 3 V to 3.6 V | | 2 | | |
| | | | 4.5 V to 5.5 V | | V _{CCA} × 0.7 | | |
| V _{IL} | Low-level input voltage | Control inputs (referenced to V _{CCA}) ⁽⁶⁾ | 1.65 V to 1.95 V | | V _{CCA} × 0.35 | | V |
| | | | 2.3 V to 2.7 V | | 0.7 | | |
| | | | 3 V to 3.6 V | | 0.8 | | |
| | | | 4.5 V to 5.5 V | | V _{CCA} × 0.3 | | |
| V _I | Input voltage | Control inputs | | | 0 | 5.5 | V |
| V _{I/O} | Input/output voltage | Active state | | | 0 | V _{CCO} | V |
| | | 3-State | | | 0 | 5.5 | V |
| I _{OH} | High-level output current | | | 1.65 V to 1.95 V | −4 | | mA |
| | | | | 2.3 V to 2.7 V | −8 | | |
| | | | | 3 V to 3.6 V | −24 | | |
| | | | | 4.5 V to 5.5 V | −32 | | |
| I _{OL} | Low-level output current | | | 1.65 V to 1.95 V | 4 | | mA |
| | | | | 2.3 V to 2.7 V | 8 | | |
| | | | | 3 V to 3.6 V | 24 | | |
| | | | | 4.5 V to 5.5 V | 32 | | |
| Δt/Δv | Input transition rise or fall rate | Data inputs | 1.65 V to 1.95 V | | 20 | | ns/V |
| | | | 2.3 V to 2.7 V | | 20 | | |
| | | | 3 V to 3.6 V | | 10 | | |
| | | | 4.5 V to 5.5 V | | 5 | | |
| T _A | Operating free-air temperature | | | | −40 | 85 | °C |

(1) V_{CCI} is the V_{CC} associated with the data input port.

(2) V_{CCO} is the V_{CC} associated with the output port.

(3) All unused or driven (floating) data inputs (I/Os) of the device must be held at logic HIGH or LOW (preferably V_{CCI} or GND) to ensure proper device operation and minimize power. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

(4) All unused control inputs must be held at V_{CCA} or GND to ensure proper device operation and minimize power consumption.

(5) For V_{CCI} values not specified in the data sheet, V_{IH} min = V_{CCI} × 0.7 V, V_{IL} max = V_{CCI} × 0.3 V.

(6) For V_{CCA} values not specified in the data sheet, V_{IH} min = V_{CCA} × 0.7 V, V_{IL} max = V_{CCA} × 0.3 V.

Electrical Characteristics⁽¹⁾⁽²⁾

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CCA} | V _{CCB} | MIN | TYP | MAX | MIN | MAX | UNIT |
|-------------------------------------|----------------|---|------------------|------------------|-----|-----|-----|------------------------|-----|------|
| V _{OH} | | I _{OH} = –100 µA, V _I = V _{IH} | 1.65 V to 4.5 V | 1.65 V to 4.5 V | | | | V _{CCO} – 0.1 | | V |
| | | I _{OH} = –4 mA, V _I = V _{IH} | 1.65 V | 1.65 V | | | | 1.2 | | |
| | | I _{OH} = –8 mA, V _I = V _{IH} | 2.3 V | 2.3 V | | | | 1.9 | | |
| | | I _{OH} = –24 mA, V _I = V _{IH} | 3 V | 3 V | | | | 2.4 | | |
| | | I _{OH} = –32 mA, V _I = V _{IH} | 4.5 V | 4.5 V | | | | 3.8 | | |
| V _{OL} | | I _{OL} = 100 µA, V _I = V _{IL} | 1.65 V to 4.5 V | 1.65 V to 4.5 V | | | | 0.1 | | V |
| | | I _{OL} = 4 mA, V _I = V _{IL} | 1.65 V | 1.65 V | | | | 0.45 | | |
| | | I _{OL} = 8 mA, V _I = V _{IL} | 2.3 V | 2.3 V | | | | 0.3 | | |
| | | I _{OL} = 24 mA, V _I = V _{IL} | 3 V | 3 V | | | | 0.55 | | |
| | | I _{OL} = 32 mA, V _I = V _{IL} | 4.5 V | 4.5 V | | | | 0.55 | | |
| I _I | DIR | V _I = V _{CCA} or GND | 1.65 V to 5.5 V | 1.65 V to 5.5 V | | | ±1 | | ±2 | µA |
| I _{off} | A or B port | V _I or V _O = 0 to 5.5 V | 0 V | 0 to 5.5 V | | | ±1 | | ±2 | µA |
| | | | 0 to 5.5 V | 0 V | | | ±1 | | ±2 | |
| I _{OZ} | A or B port | V _O = V _{CCO} or GND, OE = V _{IH} | 1.65 V to 5.5 V | 1.65 V to 5.5 V | | | ±1 | | ±2 | µA |
| I _{CCA} | | V _I = V _{CCI} or GND, I _O = 0 | 1.65 V to 5.5 V | 1.65 V to 5.5 V | | | | | 15 | µA |
| | | | 5 V | 0 V | | | | | 15 | |
| | | | 0 V | 5 V | | | | | –2 | |
| I _{CCB} | | V _I = V _{CCI} or GND, I _O = 0 | 1.65 V to 5.5 V | 1.65 V to 5.5 V | | | | | 15 | µA |
| | | | 5 V | 0 V | | | | | –2 | |
| | | | 0 V | 5 V | | | | | 15 | |
| I _{CCA} + I _{CCB} | | V _I = V _{CCI} or GND, I _O = 0 | 1.65 V to 5.5 V | 1.65 V to 5.5 V | | | | | 25 | µA |
| ΔI _{CCA} | A port | One A port at V _{CCA} – 0.6 V, DIR at V _{CCA} , B port = open | 3 V to 5.5 V | 3 V to 5.5 V | | | | | 50 | µA |
| | DIR | DIR at V _{CCA} – 0.6 V, B port = open, A port at V _{CCA} or GND | | | | | | | 50 | |
| ΔI _{CCB} | B port | One B port at V _{CCB} – 0.6 V, DIR at GND, A port = open | 3 V to 5.5 V | 3 V to 5.5 V | | | | | 50 | µA |
| C _i | Control inputs | V _I = V _{CCA} or GND | 3.3 V | 3.3 V | | | 4 | | 5 | pF |
| C _{io} | A or B port | V _O = V _{CCA/B} or GND | 3.3 V | 3.3 V | | | 8.5 | | 10 | pF |

(1) V_{CCO} is the V_{CC} associated with the output port.

(2) V_{CCI} is the V_{CC} associated with the input port.

SN74LVC8T245
8-BIT DUAL-SUPPLY BUS TRANSCEIVER
WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

SCES584A–JUNE 2005–REVISED AUGUST 2005

Switching Characteristics

over recommended operating free-air temperature range, $V_{CCA} = 1.8\text{ V} \pm 0.15\text{ V}$ (unless otherwise noted) (see [Figure 1](#))

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$ | | $V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$ | | $V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$ | | $V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$ | | UNIT |
|-----------|-----------------|----------------|--|------|---|------|---|------|---|------|------|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| t_{PLH} | A | B | 1.7 | 21.9 | 1.3 | 9.2 | 1 | 7.4 | 0.8 | 7.1 | ns |
| t_{PHL} | | | | | | | | | | | |
| t_{PLH} | B | A | 0.9 | 23.8 | 0.8 | 23.6 | 0.7 | 23.4 | 0.7 | 23.4 | ns |
| t_{PHL} | | | | | | | | | | | |
| t_{PHZ} | \overline{OE} | A | 1.5 | 29.6 | 1.5 | 29.4 | 1.5 | 29.3 | 1.4 | 29.2 | ns |
| t_{PLZ} | | | | | | | | | | | |
| t_{PHZ} | \overline{OE} | B | 2.4 | 32.2 | 1.9 | 13.1 | 1.7 | 12 | 1.3 | 10.3 | ns |
| t_{PLZ} | | | | | | | | | | | |
| t_{PZH} | \overline{OE} | A | 0.4 | 24 | 0.4 | 23.8 | 0.4 | 23.7 | 0.4 | 23.7 | ns |
| t_{PZL} | | | | | | | | | | | |
| t_{PZH} | \overline{OE} | B | 1.8 | 32 | 1.5 | 16 | 1.2 | 12.6 | 0.9 | 10.8 | ns |
| t_{PZL} | | | | | | | | | | | |

Switching Characteristics

over recommended operating free-air temperature range, $V_{CCA} = 2.5\text{ V} \pm 0.2\text{ V}$ (unless otherwise noted) (see [Figure 1](#))

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$ | | $V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$ | | $V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$ | | $V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$ | | UNIT |
|-----------|-----------------|----------------|--|------|---|------|---|------|---|------|------|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| t_{PLH} | A | B | 1.5 | 21.4 | 1.2 | 9 | 0.8 | 6.2 | 0.6 | 4.8 | ns |
| t_{PHL} | | | | | | | | | | | |
| t_{PLH} | B | A | 1.2 | 9.3 | 1 | 9.1 | 1 | 8.9 | 0.9 | 8.8 | ns |
| t_{PHL} | | | | | | | | | | | |
| t_{PHZ} | \overline{OE} | A | 1.4 | 9 | 1.4 | 9 | 1.4 | 9 | 1.4 | 9 | ns |
| t_{PLZ} | | | | | | | | | | | |
| t_{PHZ} | \overline{OE} | B | 2.3 | 29.6 | 1.8 | 11 | 1.7 | 9.3 | 0.9 | 6.9 | ns |
| t_{PLZ} | | | | | | | | | | | |
| t_{PZH} | \overline{OE} | A | 1 | 10.9 | 1 | 10.9 | 1 | 10.9 | 1 | 10.9 | ns |
| t_{PZL} | | | | | | | | | | | |
| t_{PZH} | \overline{OE} | B | 1.7 | 28.2 | 1.5 | 12.9 | 1.2 | 9.4 | 1 | 6.9 | ns |
| t_{PZL} | | | | | | | | | | | |

Switching Characteristics

over recommended operating free-air temperature range, $V_{CCA} = 3.3 \text{ V} \pm 0.3 \text{ V}$ (unless otherwise noted) (see [Figure 1](#))

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$ | | $V_{CCB} = 2.5 \text{ V} \pm 0.2 \text{ V}$ | | $V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$ | | $V_{CCB} = 5 \text{ V} \pm 0.5 \text{ V}$ | | UNIT |
|-----------|-----------------|----------------|--|------|---|------|---|-----|---|-----|------|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| t_{PLH} | A | B | 1.5 | 21.2 | 1.1 | 8.8 | 0.8 | 6.3 | 0.5 | 4.4 | ns |
| t_{PHL} | | | | | | | | | | | |
| t_{PLH} | B | A | 0.8 | 7.2 | 0.8 | 6.2 | 0.7 | 6.1 | 0.6 | 6 | ns |
| t_{PHL} | | | | | | | | | | | |
| t_{PHZ} | \overline{OE} | A | 1.6 | 8.2 | 1.6 | 8.2 | 1.6 | 8.2 | 1.6 | 8.2 | ns |
| t_{PLZ} | | | | | | | | | | | |
| t_{PHZ} | \overline{OE} | B | 2.1 | 29 | 1.7 | 10.3 | 1.5 | 8.6 | 0.8 | 6.3 | ns |
| t_{PLZ} | | | | | | | | | | | |
| t_{PZH} | \overline{OE} | A | 0.8 | 8.1 | 0.8 | 8.1 | 0.8 | 8.1 | 0.8 | 8.1 | ns |
| t_{PZL} | | | | | | | | | | | |
| t_{PZH} | \overline{OE} | B | 1.8 | 27.7 | 1.4 | 12.4 | 1.1 | 8.5 | 0.9 | 6.4 | ns |
| t_{PZL} | | | | | | | | | | | |

Switching Characteristics

over recommended operating free-air temperature range, $V_{CCA} = 5 \text{ V} \pm 0.5 \text{ V}$ (unless otherwise noted) (see [Figure 1](#))

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$ | | $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$ | | $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ | | $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$ | | UNIT |
|-----------|-----------------|----------------|---|------|--|------|--|-----|--|-----|------|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| t_{PLH} | A | B | 1.5 | 21.4 | 1 | 8.8 | 0.7 | 6 | 0.4 | 4.2 | ns |
| t_{PHL} | | | | | | | | | | | |
| t_{PLH} | B | A | 0.7 | 7 | 0.4 | 4.8 | 0.3 | 4.5 | 0.3 | 4.3 | ns |
| t_{PHL} | | | | | | | | | | | |
| t_{PHZ} | \overline{OE} | A | 0.3 | 5.4 | 0.3 | 5.4 | 0.3 | 5.4 | 0.3 | 5.4 | ns |
| t_{PLZ} | | | | | | | | | | | |
| t_{PHZ} | \overline{OE} | B | 2 | 28.7 | 1.6 | 9.7 | 1.4 | 8 | 0.7 | 5.7 | ns |
| t_{PLZ} | | | | | | | | | | | |
| t_{PZH} | \overline{OE} | A | 0.7 | 6.4 | 0.7 | 6.4 | 0.7 | 6.4 | 0.7 | 6.4 | ns |
| t_{PZL} | | | | | | | | | | | |
| t_{PZH} | \overline{OE} | B | 1.5 | 27.6 | 1.3 | 11.4 | 1 | 8.1 | 0.9 | 6 | ns |
| t_{PZL} | | | | | | | | | | | |

Operating Characteristics

$T_A = 25^\circ\text{C}$

| PARAMETER | | TEST CONDITIONS | $V_{CCA} =$ $V_{CCB} = 1.8 \text{ V}$ | $V_{CCA} =$ $V_{CCB} = 2.5 \text{ V}$ | $V_{CCA} =$ $V_{CCB} = 3.3 \text{ V}$ | $V_{CCA} =$ $V_{CCB} = 5 \text{ V}$ | UNIT |
|-----------------|-----------------------------|---|--|--|--|--|------|
| | | | TYP | TYP | TYP | TYP | |
| $C_{pdA}^{(1)}$ | A-port input, B-port output | $C_L = 0,$ $f = 10 \text{ MHz},$ $t_r = t_f = 1 \text{ ns}$ | 2 | 2 | 2 | 3 | pF |
| | B-port input, A-port output | | 12 | 13 | 13 | 16 | |
| $C_{pdB}^{(1)}$ | A-port input, B-port output | | 13 | 13 | 14 | 16 | |
| | B-port input, A-port output | | 2 | 2 | 2 | 3 | |

(1) Power dissipation capacitance per transceiver

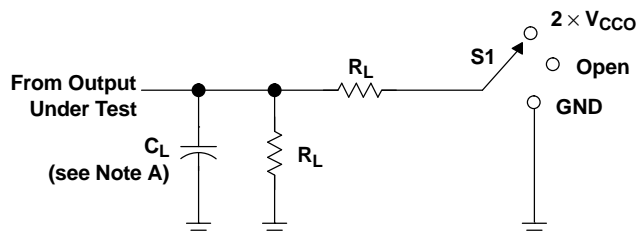
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8-BIT DUAL-SUPPLY BUS TRANSCEIVER

WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

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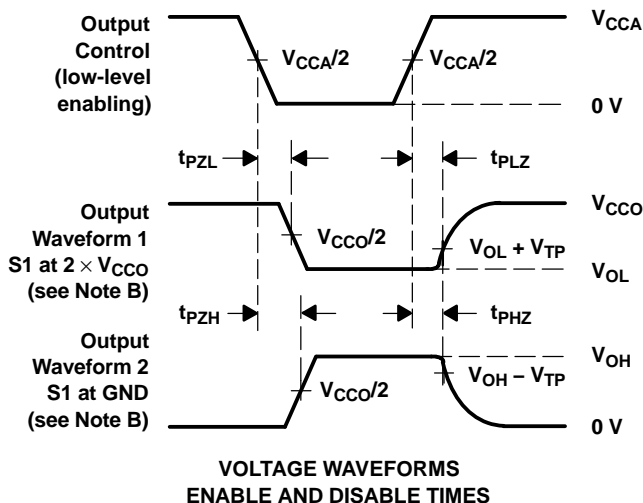
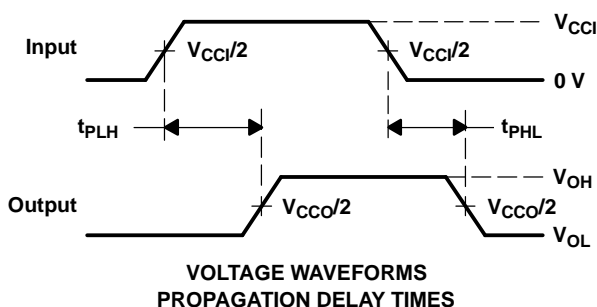
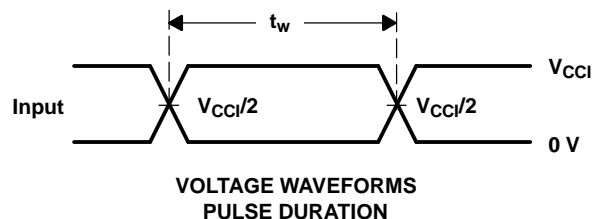
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

| V_{CCO} | C_L | R_L | V_{TP} |
|----------------------------------|-------|--------------|----------|
| $1.8\text{ V} \pm 0.15\text{ V}$ | 15 pF | 2 k Ω | 0.15 V |
| $2.5\text{ V} \pm 0.2\text{ V}$ | 15 pF | 2 k Ω | 0.15 V |
| $3.3\text{ V} \pm 0.3\text{ V}$ | 15 pF | 2 k Ω | 0.3 V |
| $5\text{ V} \pm 0.5\text{ V}$ | 15 pF | 2 k Ω | 0.3 V |

| TEST | S1 |
|-------------------|--------------------|
| t_{pd} | Open |
| t_{PLZ}/t_{PZL} | $2 \times V_{CCO}$ |
| t_{PHZ}/t_{PZH} | GND |



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\text{ }\Omega$, $dv/dt \geq 1\text{ V/ns}$.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .
 - V_{CCI} is the V_{CC} associated with the input port.
 - V_{CCO} is the V_{CC} associated with the output port.
 - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|--------------------|---------------|--------------|--------------------|------|-------------|----------------------------|------------------|----------------------|--------------|--------------------------|-------------------------|
| 74LVC8T245DBQRG4 | ACTIVE | SSOP | DBQ | 24 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | LVC8T245 | Samples |
| 74LVC8T245RHLRG4 | ACTIVE | QFN | RHL | 24 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | NH245 | Samples |
| SN74LVC8T245DBQR | ACTIVE | SSOP | DBQ | 24 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | LVC8T245 | Samples |
| SN74LVC8T245DBR | ACTIVE | SSOP | DB | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | NH245 | Samples |
| SN74LVC8T245DBRE4 | ACTIVE | SSOP | DB | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | NH245 | Samples |
| SN74LVC8T245DBRG4 | ACTIVE | SSOP | DB | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | NH245 | Samples |
| SN74LVC8T245DGVR | ACTIVE | TVSOP | DGV | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | NH245 | Samples |
| SN74LVC8T245DGVRG4 | ACTIVE | TVSOP | DGV | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | NH245 | Samples |
| SN74LVC8T245DWR | ACTIVE | SOIC | DW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LVC8T245 | Samples |
| SN74LVC8T245DWRG4 | ACTIVE | SOIC | DW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LVC8T245 | Samples |
| SN74LVC8T245NSR | ACTIVE | SO | NS | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LVC8T245 | Samples |
| SN74LVC8T245NSRG4 | ACTIVE | SO | NS | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LVC8T245 | Samples |
| SN74LVC8T245PW | ACTIVE | TSSOP | PW | 24 | 60 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | NH245 | Samples |
| SN74LVC8T245PWE4 | ACTIVE | TSSOP | PW | 24 | 60 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | NH245 | Samples |
| SN74LVC8T245PWG4 | ACTIVE | TSSOP | PW | 24 | 60 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | NH245 | Samples |
| SN74LVC8T245PWR | ACTIVE | TSSOP | PW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | NH245 | Samples |
| SN74LVC8T245PWRE4 | ACTIVE | TSSOP | PW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | NH245 | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|-------------------|---------------|--------------|--------------------|------|-------------|----------------------------|------------------|----------------------|--------------|--------------------------|-------------------------|
| SN74LVC8T245PWRG4 | ACTIVE | TSSOP | PW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | NH245 | Samples |
| SN74LVC8T245RHRLR | ACTIVE | QFN | RHL | 24 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | NH245 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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OTHER QUALIFIED VERSIONS OF SN74LVC8T245 :

● Automotive: [SN74LVC8T245-Q1](#)

● Enhanced Product: [SN74LVC8T245-EP](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LVC8T245DBQR | SSOP | DBQ | 24 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74LVC8T245DBR | SSOP | DB | 24 | 2000 | 330.0 | 16.4 | 8.2 | 8.8 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74LVC8T245DGVR | TVSOP | DGV | 24 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LVC8T245DWR | SOIC | DW | 24 | 2000 | 330.0 | 24.4 | 10.75 | 15.7 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74LVC8T245NSR | SO | NS | 24 | 2000 | 330.0 | 24.4 | 8.2 | 15.4 | 2.5 | 12.0 | 24.0 | Q1 |
| SN74LVC8T245PWR | TSSOP | PW | 24 | 2000 | 330.0 | 16.4 | 6.95 | 8.3 | 1.6 | 8.0 | 16.0 | Q1 |
| SN74LVC8T245RHRLR | QFN | RHL | 24 | 1000 | 180.0 | 12.4 | 3.8 | 5.8 | 1.2 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LVC8T245DBQR | SSOP | DBQ | 24 | 2500 | 367.0 | 367.0 | 38.0 |
| SN74LVC8T245DBR | SSOP | DB | 24 | 2000 | 367.0 | 367.0 | 38.0 |
| SN74LVC8T245DGVR | TVSOP | DGV | 24 | 2000 | 367.0 | 367.0 | 35.0 |
| SN74LVC8T245DWR | SOIC | DW | 24 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74LVC8T245NSR | SO | NS | 24 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74LVC8T245PWR | TSSOP | PW | 24 | 2000 | 367.0 | 367.0 | 38.0 |
| SN74LVC8T245RHLR | QFN | RHL | 24 | 1000 | 210.0 | 185.0 | 35.0 |

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

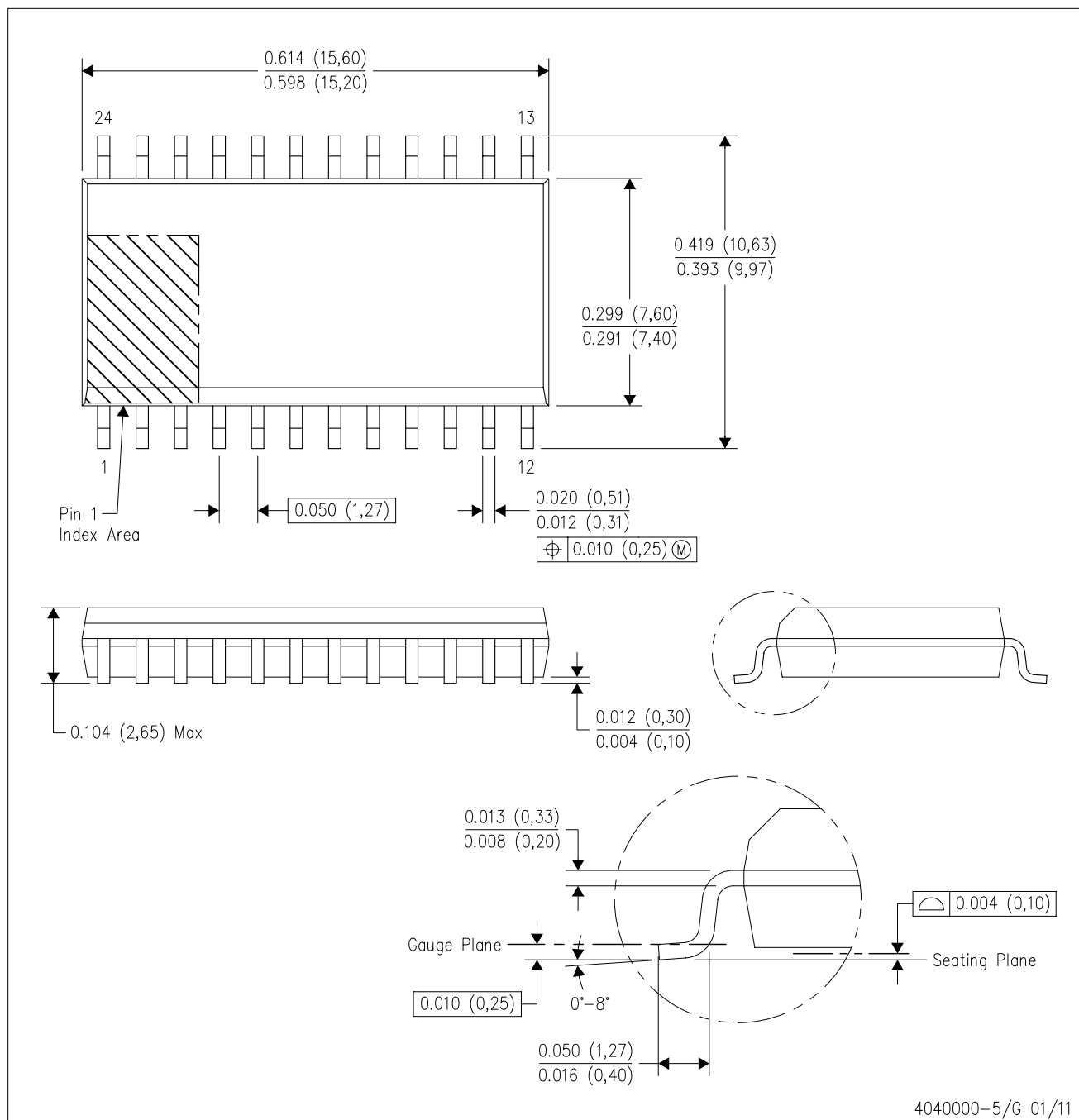
24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

DW (R-PDSO-G24)

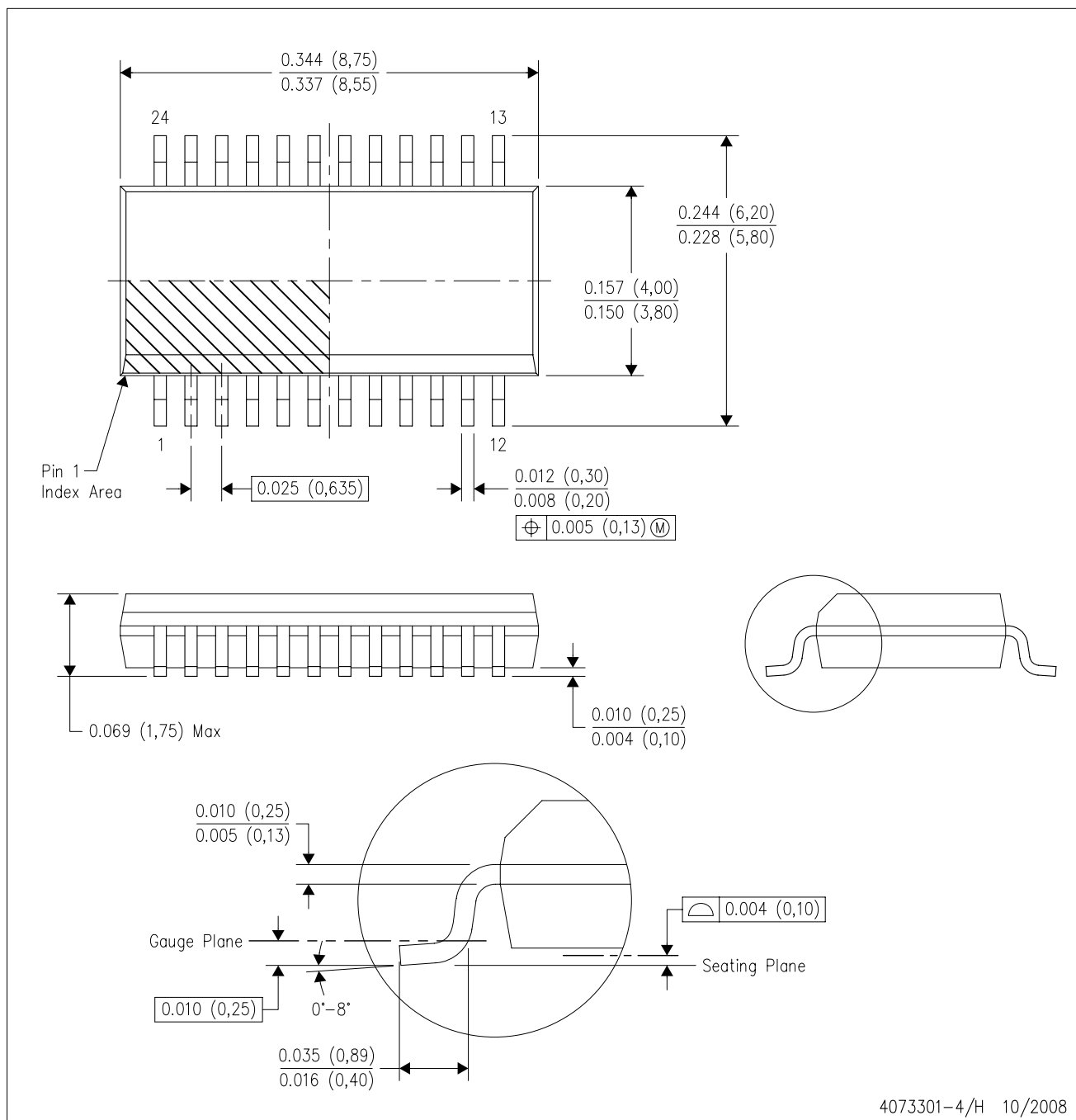
PLASTIC SMALL OUTLINE



- NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-013 variation AD.

DBQ (R-PDSO-G24)

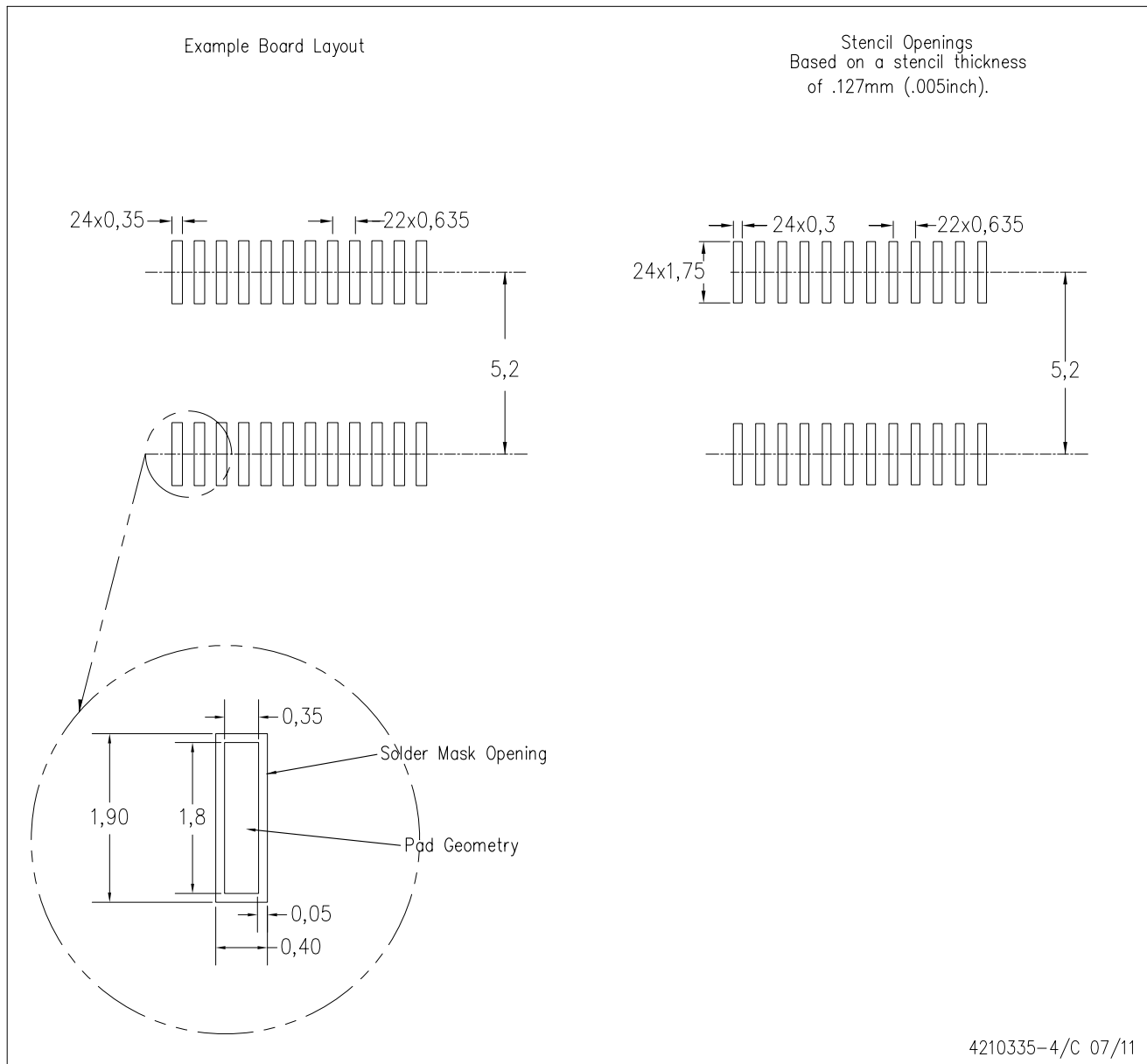
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
 - D. Falls within JEDEC MO-137 variation AE.

DBQ (R-PDSO-G24)

PLASTIC SMALL OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

PW (R-PDSO-G24)

PLASTIC SMALL OUTLINE

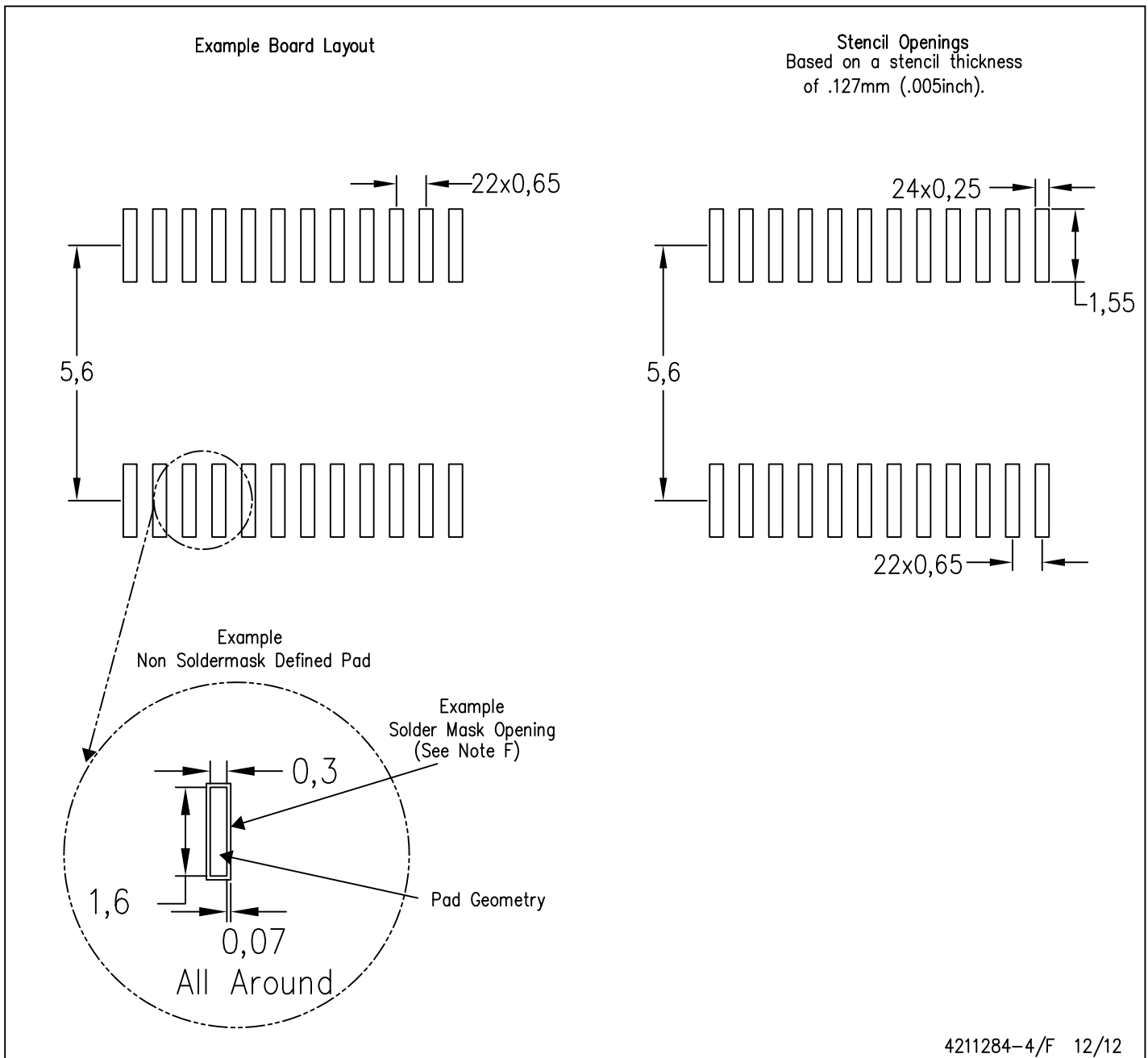


4040064-6/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G24)

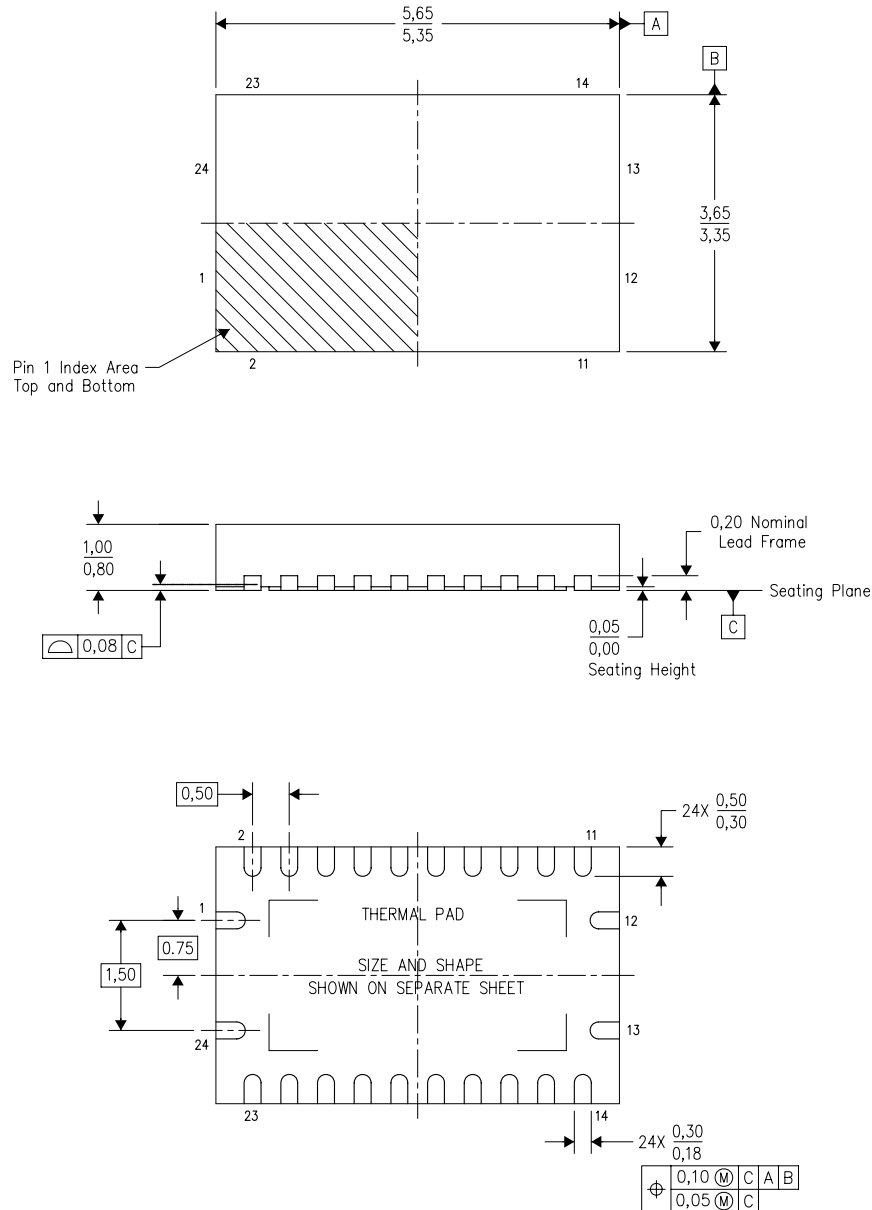
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RHL (R-PVQFN-N24)

PLASTIC QUAD FLATPACK NO-LEAD



Bottom View

4205346-4/J 12/11

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - QFN (Quad Flatpack No-Lead) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - JEDEC MO-241 package registration pending.

RHL (S-PVQFN-N24)

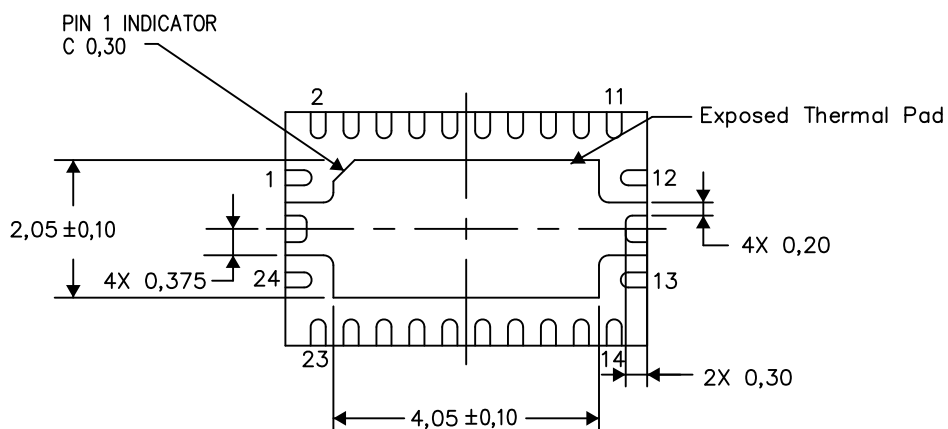
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

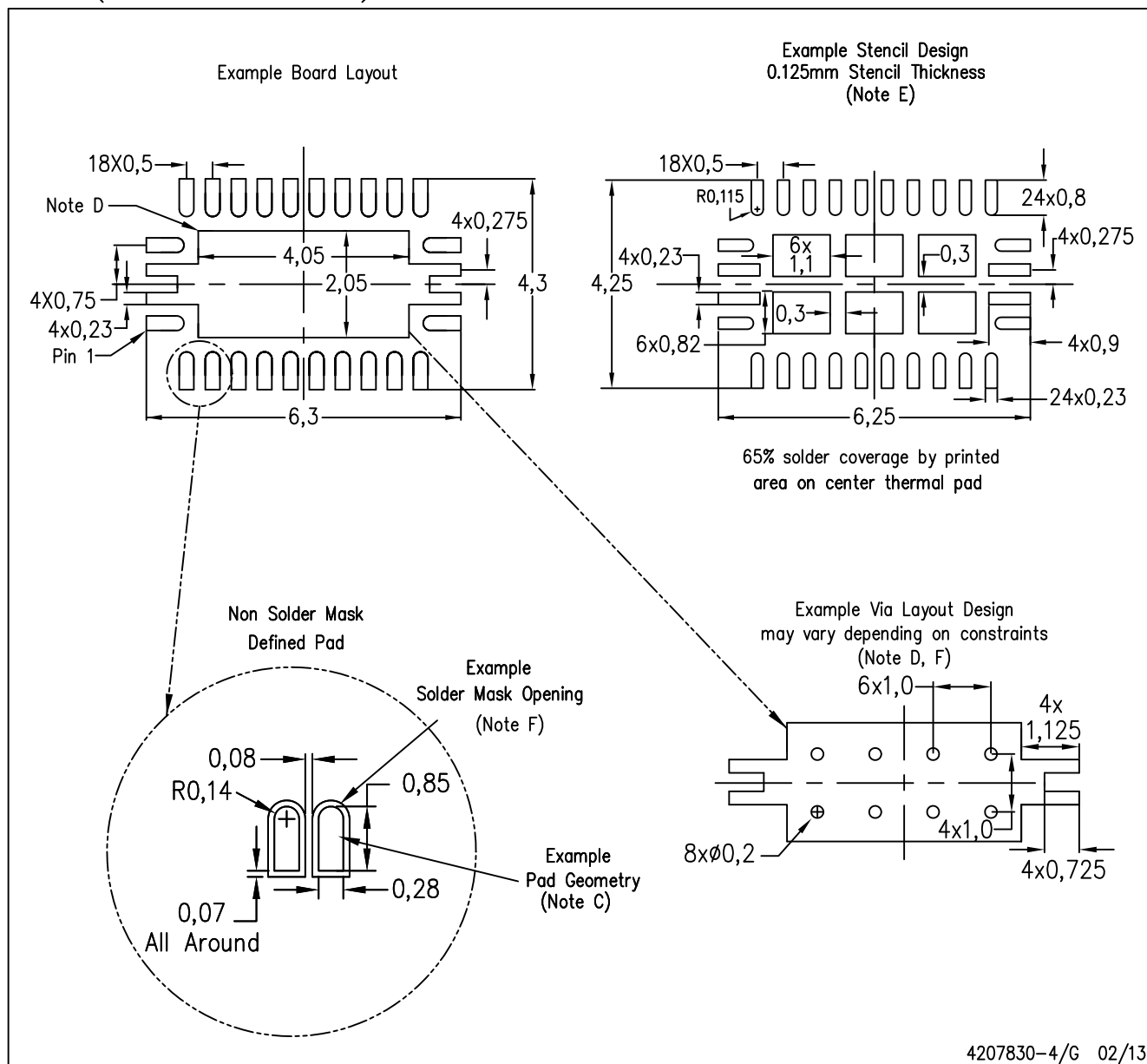
Exposed Thermal Pad Dimensions

4206363-4/M 08/12

NOTE: All linear dimensions are in millimeters

RHL (R-PVQFN-N24)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

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