

LMH6654/LMH6655 Single/Dual Low Power, 250 MHz, Low Noise Amplifiers

Check for Samples: [LMH6654](#), [LMH6655](#)

FEATURES

- ($V_S = \pm 5V$, $T_J = 25^\circ C$, Typical Values Unless Specified).
- Voltage Feedback Architecture
- Unity Gain Bandwidth 250 MHz
- Supply Voltage Range $\pm 2.5V$ to $\pm 6V$
- Slew Rate 200 V/ μ sec
- Supply Current 4.5 mA/channel
- Input Common Mode Voltage $-5.15V$ to $+3.7V$
- Output Voltage Swing ($R_L = 100\Omega$) $-3.6V$ to $3.4V$
- Input Voltage Noise 4.5 nV/ $\sqrt{Hz}$
- Input Current Noise 1.7 pA/ $\sqrt{Hz}$
- Settling Time to 0.01% 25 ns

APPLICATIONS

- ADC Drivers
- Consumer Video
- Active Filters
- Pulse Delay Circuits
- xDSL Receiver
- Pre-amps

DESCRIPTION

The LMH6654/LMH6655 single and dual high speed, voltage feedback amplifiers are designed to have unity-gain stable operation with a bandwidth of 250 MHz. They operate from $\pm 2.5V$ to $\pm 6V$ and each channel consumes only 4.5 mA. The amplifiers feature very low voltage noise and wide output swing to maximize signal-to-noise ratio.

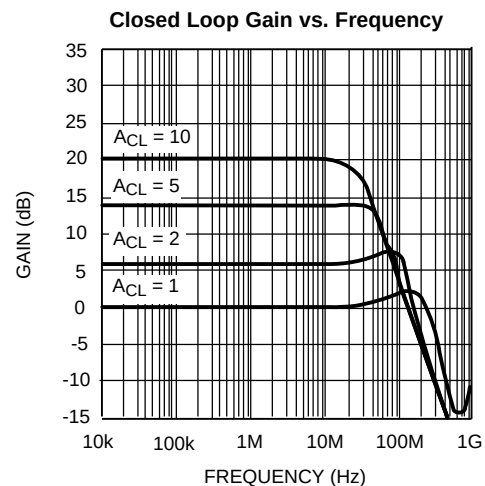
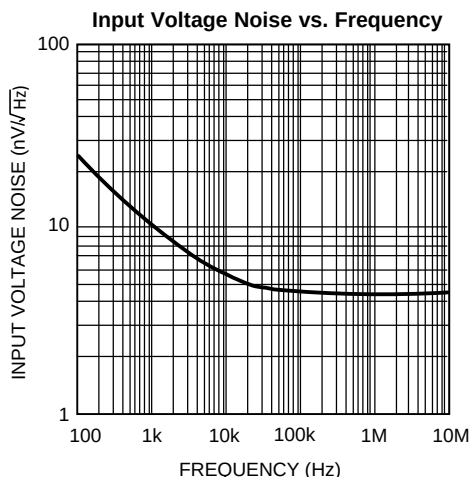
The LMH6654/LMH6655 have a true single supply capability with input common mode voltage range extending 150 mV below negative rail and within 1.3V of the positive rail.

LMH6654/LMH6655 high speed and low power combination make these products an ideal choice for many portable, high speed application where power is at a premium.

The LMH6654 is packaged in 5-Pin SOT-23 and 8-Pin SOIC. The LMH6655 is packaged in 8-Pin VSSOP (DGK) and 8-Pin SOIC.

The LMH6654/LMH6655 are built on TI's Advance VIP10™ (Vertically Integrated PNP) complementary bipolar process.

Typical Performance Characteristics



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings ⁽¹⁾

ESD Tolerance ⁽²⁾	
Human Body Model	2 kV
Machine Model	200V
V _{IN} Differential	±1.2V
Output Short Circuit Duration	⁽³⁾
Supply Voltage (V ⁺ - V ⁻)	13.2V
Voltage at Input pins	V ⁺ +0.5V, V ⁻ -0.5V
Storage Temperature Range	-65°C to +150°C
Junction Temperature ⁽⁴⁾	+150°C
Soldering Information	
Infrared or Convection (20 sec.)	235°C
Wave Soldering (10 sec.)	260°C

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics Table.
- (2) Human body model, 1.5 kΩ in series with 100 pF. Machine model: 0Ω in series with 100 pF.
- (3) Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature at 150°C.
- (4) The maximum power dissipation is a function of T_{J(MAX)}, θ_{JA} and T_A. The maximum allowable power dissipation at any ambient temperature is P_D = (T_{J(MAX)} - T_A)/θ_{JA}. All numbers apply for packages soldered directly onto a PC board.

Operating Ratings ⁽¹⁾

Supply Voltage (V ⁺ - V ⁻)	±2.5V to ±6.0V
Junction Temperature Range	-40°C to +85°C
Thermal Resistance (θ _{JA})	
8-Pin SOIC	172°C/W
8-Pin VSSOP (DGK)	235°C/W
5-Pin SOT-23	265°C/W

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics Table.

±5V Electrical Characteristics

Unless otherwise specified, all limits ensured for $T_J = 25^\circ\text{C}$, $V^+ = +5\text{V}$, $V^- = -5\text{V}$, $V_{CM} = 0\text{V}$, $A_V = +1$, $R_F = 25\Omega$ for gain = +1, $R_F = 402\Omega$ for gain = $\geq +2$, and $R_L = 100\Omega$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
Dynamic Performance						
f _{CL}	Close Loop Bandwidth	A _V = +1		250		MHz
		A _V = +2		130		
		A _V = +5		52		
		A _V = +10		26		
GBWP	Gain Bandwidth Product	A _V ≥ +5		260		MHz
	Bandwidth for 0.1 dB Flatness	A _V +1		18		MHz
φ _m	Phase Margin			50		deg
SR	Slew Rate ⁽³⁾	A _V = +1, V _{IN} = 2 V _{PP}		200		V/μs
t _S	Settling Time 0.01%	A _V = +1, 2V Step		25		ns
	0.1%			15		ns
t _r	Rise Time	A _V = +1, 0.2V Step		1.4		ns
t _f	Fall Time	A _V = +1, 0.2V Step		1.2		ns
Distortion and Noise Response						
e _n	Input Referred Voltage Noise	f ≥ 0.1 MHz		4.5		nV/√Hz
i _n	Input-Referred Current Noise	f ≥ 0.1 MHz		1.7		pA/√Hz
	Second Harmonic Distortion	A _V = +1, f = 5 MHz		-80		dBc
	Third Harmonic Distortion	V _O = 2 V _{PP} , R _L = 100Ω		-85		
X _t	Crosstalk (for LMH6655 only)	Input Referred, 5 MHz, Channel-to-Channel		-80		dB
DG	Differential Gain	A _V = +2, NTSC, R _L = 150Ω		0.01		%
DP	Differential Phase	A _V = +2, NTSC, R _L = 150Ω		0.025		deg
Input Characteristics						
V _{OS}	Input Offset Voltage	V _{CM} = 0V	-3 -4	±1	3 4	mV
TC V _{OS}	Input Offset Average Drift	V _{CM} = 0V ⁽⁴⁾		6		μV/°C
I _B	Input Bias Current	V _{CM} = 0V		5	12 18	μA
I _{OS}	Input Offset Current	V _{CM} = 0V	-1 -2	0.3	1 2	μA
R _{IN}	Input Resistance	Common Mode		4		MΩ
		Differential Mode		20		kΩ
C _{IN}	Input Capacitance	Common Mode		1.8		pF
		Differential Mode		1		
CMRR	Common Mode Rejection Ration	Input Referred, V _{CM} = 0V to -5V	70 68	90		dB
CMVR	Input Common- Mode Voltage Range	CMRR ≥ 50 dB		-5.15	-5.0	V
			3.5	3.7		
Transfer Characteristics						
A _{VOL}	Large Signal Voltage Gain	V _O = 4 V _{PP} , R _L = 100Ω	60 58	67		dB

(1) All limits are specified by testing or statistical analysis.

(2) Typical Values represent the most likely parametric norm.

(3) Slew rate is the slower of the rising and falling slew rates. Slew rate is rate of change from 10% to 90% of output voltage step.

(4) Offset voltage average drift is determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.

±5V Electrical Characteristics (continued)

Unless otherwise specified, all limits ensured for $T_J = 25^\circ\text{C}$, $V^+ = +5\text{V}$, $V^- = -5\text{V}$, $V_{CM} = 0\text{V}$, $A_V = +1$, $R_F = 25\Omega$ for gain = +1, $R_F = 402\Omega$ for gain = $\geq +2$, and $R_L = 100\Omega$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
Output Characteristics						
V_O	Output Swing High	No Load	3.4 3.2	3.6		V
	Output Swing Low	No Load		-3.9	-3.7 -3.5	
	Output Swing High	$R_L = 100\Omega$	3.2 3.0	3.4		
	Output Swing Low	$R_L = 100\Omega$		-3.6	-3.4 -3.2	
I_{SC}	Short Circuit Current ⁽⁵⁾	Sourcing, $V_O = 0\text{V}$ $\Delta V_{IN} = 200\text{ mV}$	145 130	280		mA
		Sinking, $V_O = 0\text{V}$ $\Delta V_{IN} = 200\text{ mV}$	100 80	185		
I_{OUT}	Output Current	Sourcing, $V_O = +3\text{V}$		80		mA
		Sinking, $V_O = -3\text{V}$		120		
R_O	Output Resistance	$A_V = +1$, $f < 100\text{ kHz}$		0.08		Ω
Power Supply						
PSRR	Power Supply Rejection Ratio	Input Referred, $V_S = \pm 5\text{V}$ to $\pm 6\text{V}$	60	76		dB
I_S	Supply Current (per channel)			4.5	6 7	mA

(5) Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature at 150°C .

5V Electrical Characteristics

Unless otherwise specified, all limits ensured for $T_J = 25^\circ\text{C}$, $V^+ = +5\text{V}$, $V^- = -0\text{V}$, $V_{CM} = 2.5\text{V}$, $A_V = +1$, $R_F = 25\Omega$ for gain = +1, $R_F = 402\Omega$ for gain = $\geq +2$, and $R_L = 100\Omega$ to $V^+/2$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
Dynamic Performance						
f _{CL}	Close Loop Bandwidth	A _V = +1		230		MHz
		A _V = +2		120		
		A _V = +5		50		
		A _V = +10		25		
GBWP	Gain Bandwidth Product	A _V ≥ +5		250		MHz
	Bandwidth for 0.1 dB Flatness	A _V = +1		17		MHz
φ _m	Phase Margin			48		deg
SR	Slew Rate ⁽³⁾	A _V = +1, V _{IN} = 2 V _{PP}		190		V/μs
t _S	Settling Time 0.01%	A _V = +1, 2V Step		30		ns
	0.1%			20		ns
t _r	Rise Time	A _V = +1, 0.2V Step		1.5		ns
t _f	Fall Time	A _V = +1, 0.2V Step		1.35		ns
Distortion and Noise Response						
e _n	Input Referred Voltage Noise	f ≥ 0.1 MHz		4.5		nV/√Hz
i _n	Input Referred Current Noise	f ≥ 0.1 MHz		1.7		pA/√Hz
	Second Harmonic Distortion	A _V = +1, f = 5 MHz		-65		dBc
	Third Harmonic Distortion	V _O = 2 V _{PP} , R _L = 100Ω		-70		
X _t	Crosstalk (for LMH6655 only)	Input Referred, 5 MHz		-78		dB
Input Characteristics						
V _{OS}	Input Offset Voltage	V _{CM} = 2.5V	-5 -6.5	±2	5 6.5	mV
TC V _{OS}	Input Offset Average Drift	V _{CM} = 2.5V ⁽⁴⁾		6		μV/°C
I _B	Input Bias Current	V _{CM} = 2.5V		6	12 18	μA
I _{OS}	Input Offset Current	V _{CM} = 2.5V	-2 -3	0.5	2 3	μA
R _{IN}	Input Resistance	Common Mode		4		MΩ
		Differential Mode		20		kΩ
C _{IN}	Input Capacitance	Common Mode		1.8		pF
		Differential Mode		1		
CMRR	Common Mode Rejection Ration	Input Referred, V _{CM} = 0V to -2.5V	70 68	90		dB
CMVR	Input Common Mode Voltage Range	CMRR ≥ 50 dB		-0.15	0	V
			3.5	3.7		
Transfer Characteristics						
A _{VOL}	Large Signal Voltage Gain	V _O = 1.6 V _{PP} , R _L = 100Ω	58 55	64		dB

- (1) All limits are specified by testing or statistical analysis.
- (2) Typical Values represent the most likely parametric norm.
- (3) Slew rate is the slower of the rising and falling slew rates. Slew rate is rate of change from 10% to 90% of output voltage step.
- (4) Offset voltage average drift is determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.

5V Electrical Characteristics (continued)

Unless otherwise specified, all limits ensured for $T_J = 25^\circ\text{C}$, $V^+ = +5\text{V}$, $V^- = -0\text{V}$, $V_{CM} = 2.5\text{V}$, $A_V = +1$, $R_F = 25\Omega$ for gain = +1, $R_F = 402\Omega$ for gain = $\geq +2$, and $R_L = 100\Omega$ to $V^+/2$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
Output Characteristics						
V_O	Output Swing High	No Load	3.6 3.4	3.75		V
	Output Swing Low	No Load		0.9	1.1 1.3	
	Output Swing High	$R_L = 100\Omega$	3.5 3.35	3.70		
	Output Swing Low	$R_L = 100\Omega$		1	1.3 1.45	
I_{SC}	Short Circuit Current ⁽⁵⁾	Sourcing, $V_O = 2.5\text{V}$ $\Delta V_{IN} = 200\text{ mV}$	90 80	170		mA
		Sinking, $V_O = 2.5\text{V}$ $\Delta V_{IN} = 200\text{ mV}$	70 60	140		
I_{OUT}	Output Current	Sourcing, $V_O = +3.5\text{V}$		30		mA
		Sinking, $V_O = 1.5\text{V}$		60		
R_O	Output Resistance	$A_V = +1$, $f < 100\text{ kHz}$		.08		Ω
Power Supply						
PSRR	Power Supply Rejection Ratio	Input Referred , $V_S = \pm 2.5\text{V}$ to $\pm 3\text{V}$	60	75		dB
I_S	Supply Current (per channel)			4.5	6 7	mA

(5) Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature at 150°C .

Connection Diagram

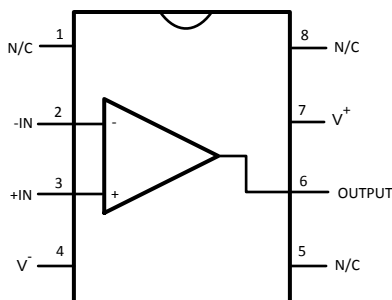


Figure 1. 8-Pin SOIC (LMH6654)
Top View

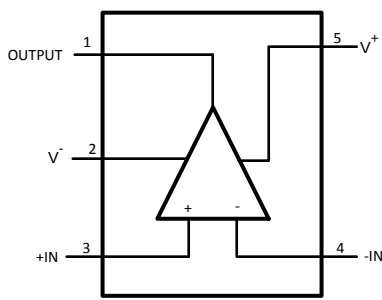


Figure 2. 5-Pin SOT-23
(LMH6654) Top View

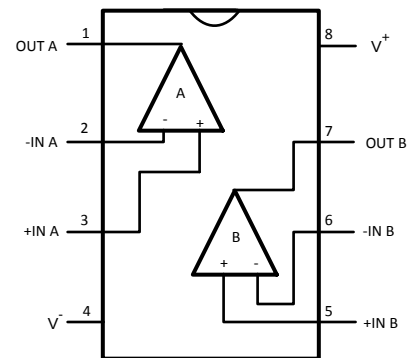


Figure 3. 8-Pin SOIC and VSSOP
(DGK) (LMH6655) Top View

Typical Performance Characteristics

$T_J = 25^\circ\text{C}$, $V^+ = \pm 5\text{V}$, $V^- = -5$, $R_F = 25\Omega$ for gain = +1, $R_F = 402\Omega$ and for gain $\geq +2$, and $R_L = 100\Omega$, unless otherwise specified.

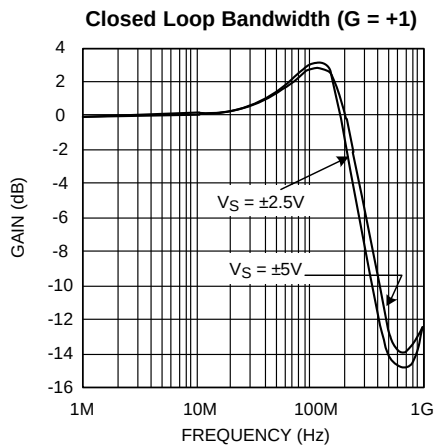


Figure 4.

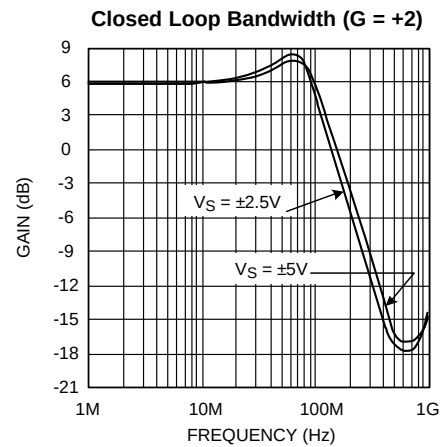


Figure 5.

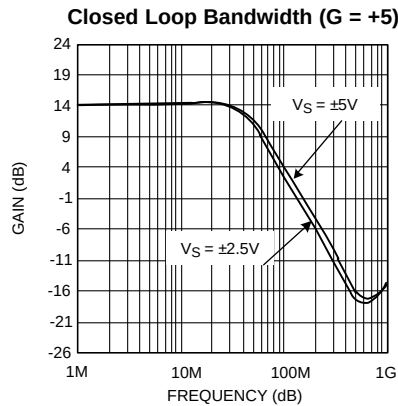


Figure 6.

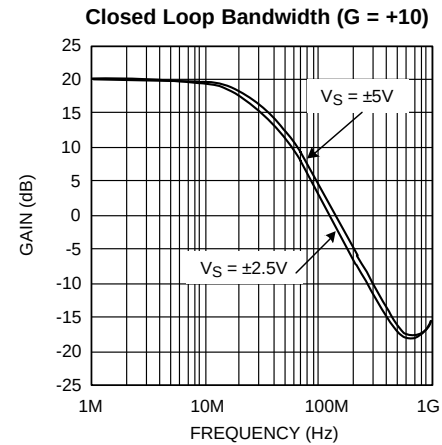


Figure 7.

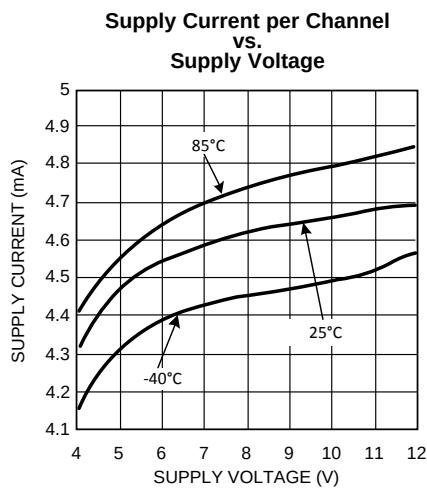


Figure 8.

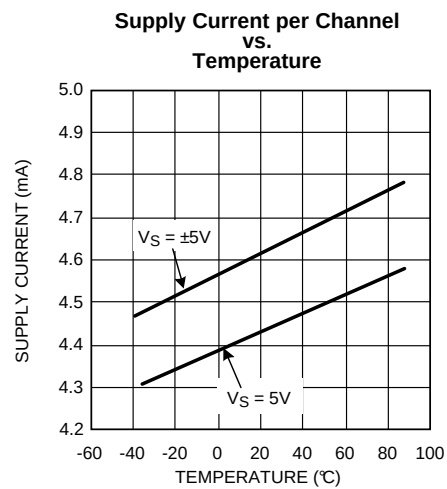


Figure 9.

Typical Performance Characteristics (continued)

$T_J = 25^\circ\text{C}$, $V^+ = \pm 5\text{V}$, $V^- = -5$, $R_F = 25\Omega$ for gain = +1, $R_F = 402\Omega$ and for gain $\geq +2$, and $R_L = 100\Omega$, unless otherwise specified.

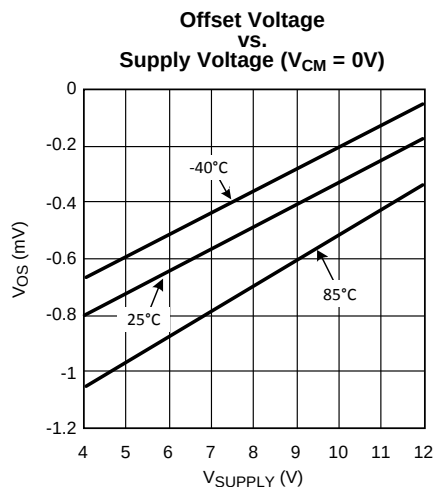


Figure 10.

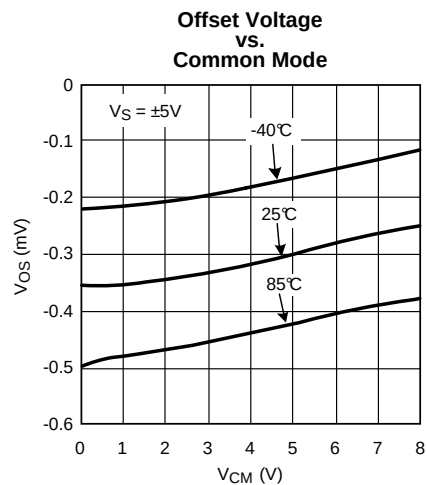


Figure 11.

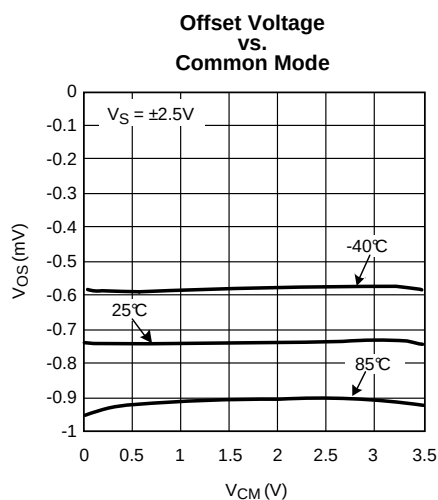


Figure 12.

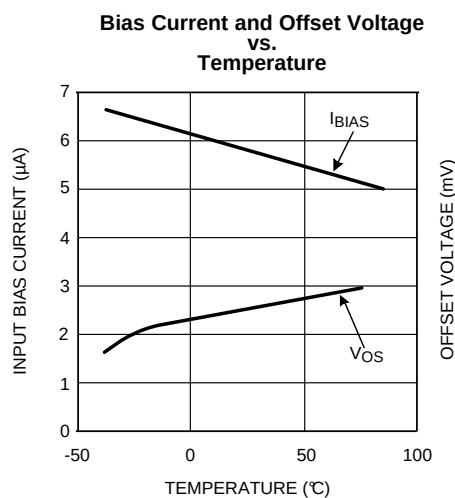


Figure 13.

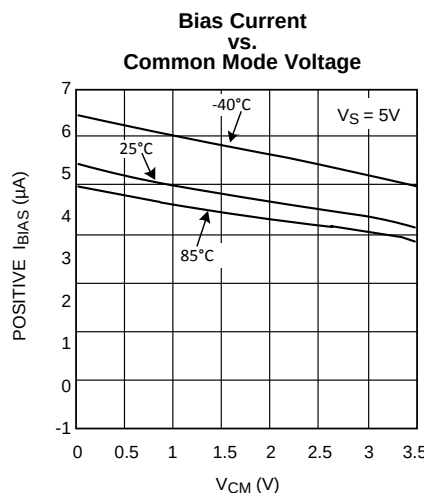


Figure 14.

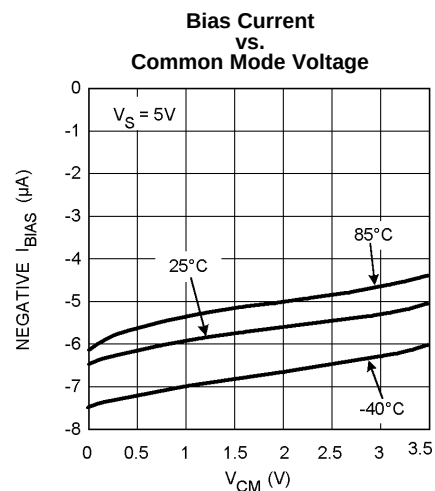


Figure 15.

Typical Performance Characteristics (continued)

$T_J = 25^\circ\text{C}$, $V^+ = \pm 5\text{V}$, $V^- = -5$, $R_F = 25\Omega$ for gain = +1, $R_F = 402\Omega$ and for gain $\geq +2$, and $R_L = 100\Omega$, unless otherwise specified.

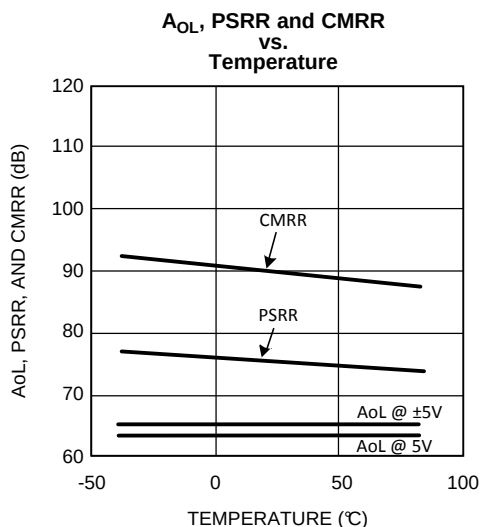
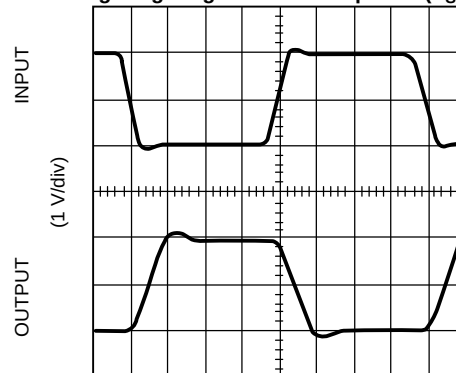


Figure 16.

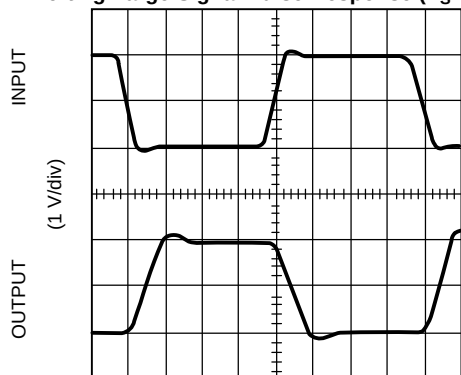
Inverting Large Signal Pulse Response ($V_S = 5\text{V}$)



TIME (12.5 ns/div)

Figure 17.

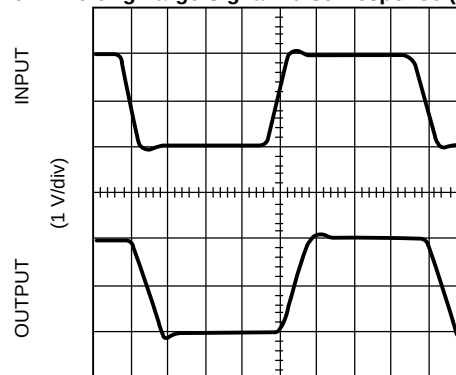
Inverting Large Signal Pulse Response ($V_S = \pm 5\text{V}$)



TIME (12.5 ns/div)

Figure 18.

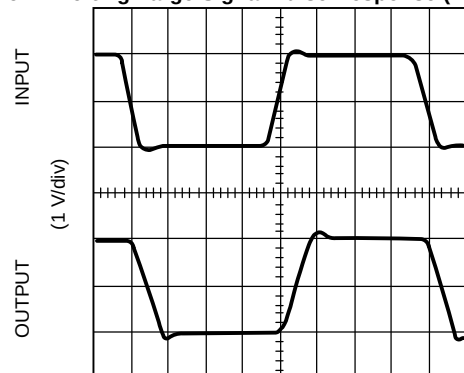
Non-Inverting Large Signal Pulse Response ($V_S = 5\text{V}$)



TIME (12.5 ns/div)

Figure 19.

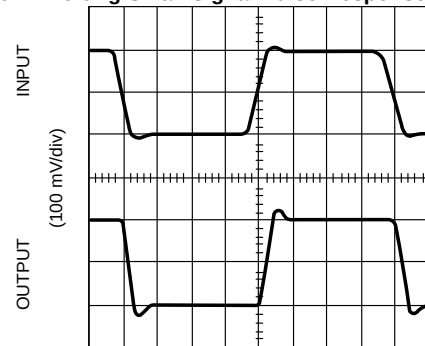
Non-Inverting Large Signal Pulse Response ($V_S = \pm 5\text{V}$)



TIME (12.5 ns/div)

Figure 20.

Non-Inverting Small Signal Pulse Response ($V_S = 5\text{V}$)



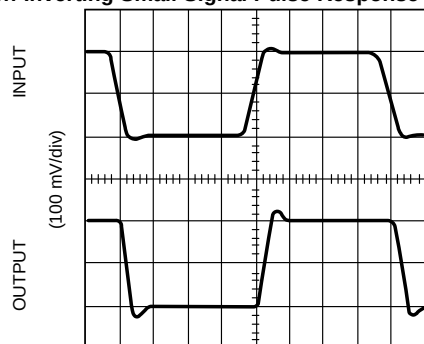
TIME (12.5 ns/div)

Figure 21.

Typical Performance Characteristics (continued)

$T_J = 25^\circ\text{C}$, $V^+ = \pm 5\text{V}$, $V^- = -5$, $R_F = 25\Omega$ for gain = +1, $R_F = 402\Omega$ and for gain $\geq +2$, and $R_L = 100\Omega$, unless otherwise specified.

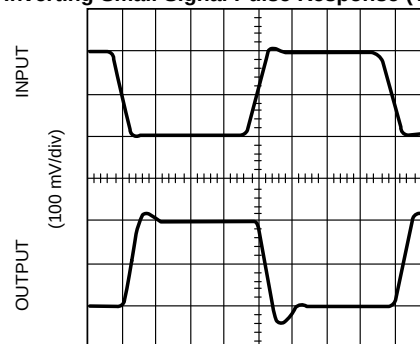
Non-Inverting Small Signal Pulse Response ($V_S = \pm 5\text{V}$)



TIME (12.5 ns/div)

Figure 22.

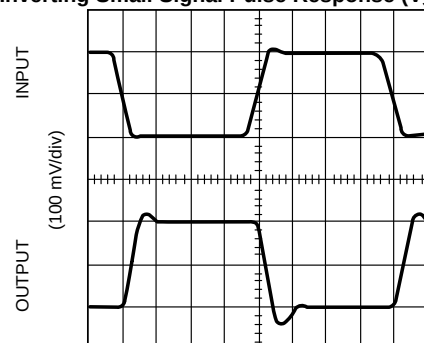
Inverting Small Signal Pulse Response ($V_S = 5\text{V}$)



TIME (12.5 ns/div)

Figure 23.

Inverting Small Signal Pulse Response ($V_S = \pm 5\text{V}$)



TIME (12.5 ns/div)

Figure 24.

Input Voltage and Current Noise
vs.
Frequency ($V_S = 5\text{V}$)

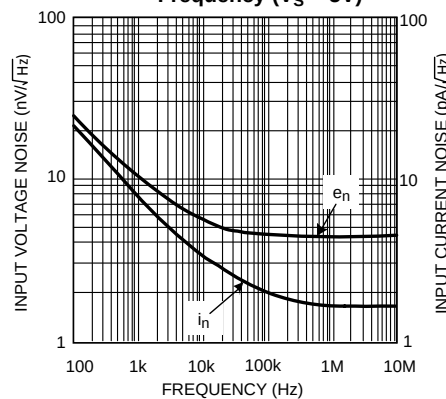


Figure 25.

Input Voltage and Current Noise
vs.
Frequency
($V_S = \pm 5\text{V}$)

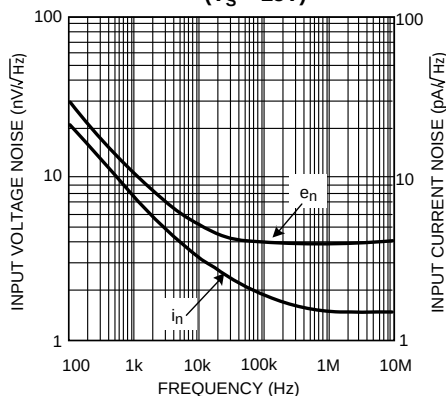


Figure 26.

Harmonic Distortion
vs.
Frequency
 $G = +1$, $V_O = 2 V_{PP}$, $V_S = 5\text{V}$

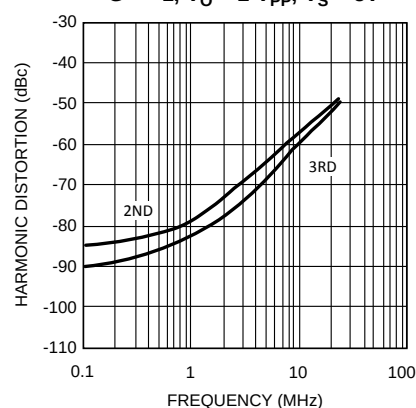


Figure 27.

Typical Performance Characteristics (continued)

$T_J = 25^\circ\text{C}$, $V^+ = \pm 5\text{V}$, $V^- = -5$, $R_F = 25\Omega$ for gain = +1, $R_F = 402\Omega$ and for gain $\geq +2$, and $R_L = 100\Omega$, unless otherwise specified.

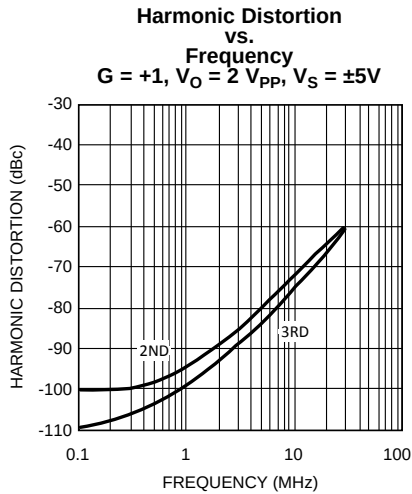


Figure 28.

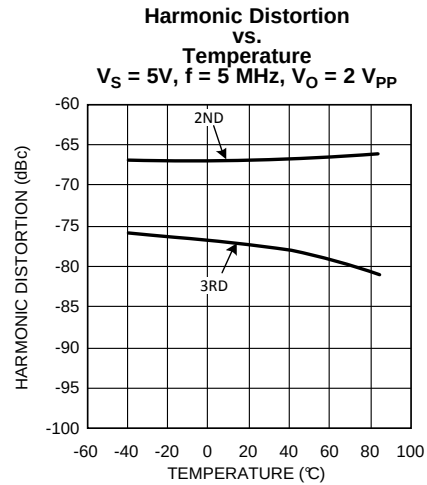


Figure 29.

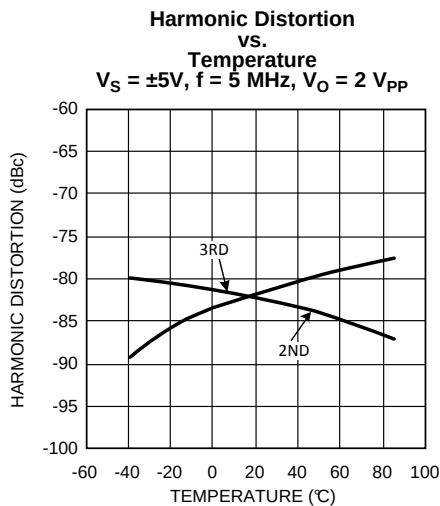


Figure 30.

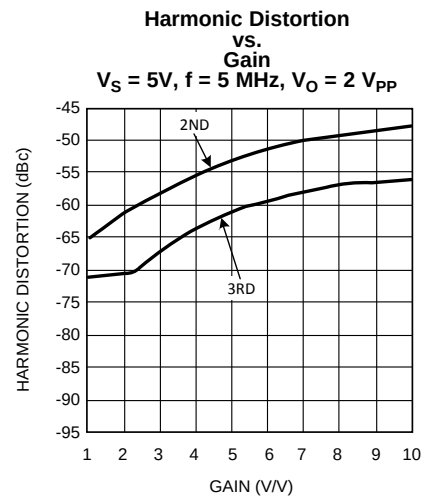


Figure 31.

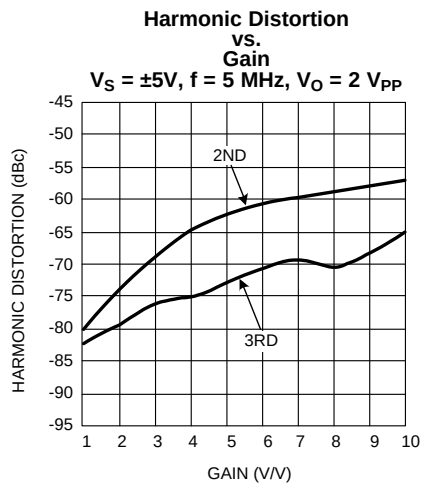


Figure 32.

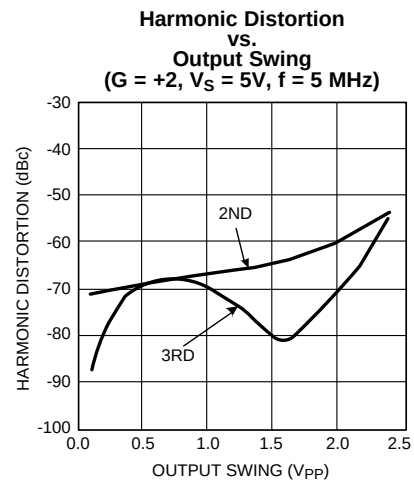


Figure 33.

Typical Performance Characteristics (continued)

$T_J = 25^\circ\text{C}$, $V^+ = \pm 5\text{V}$, $V^- = -5$, $R_F = 25\Omega$ for gain = +1, $R_F = 402\Omega$ and for gain $\geq +2$, and $R_L = 100\Omega$, unless otherwise specified.

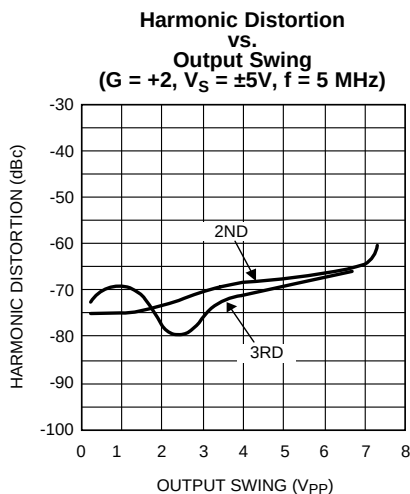


Figure 34.

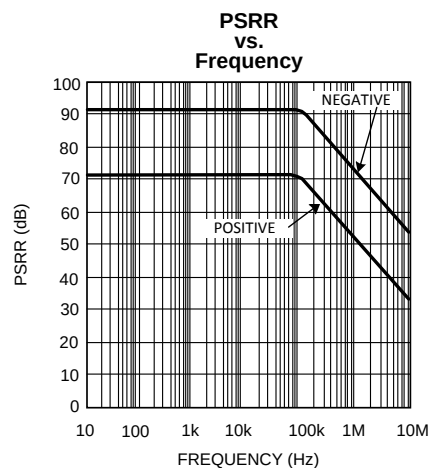


Figure 35.

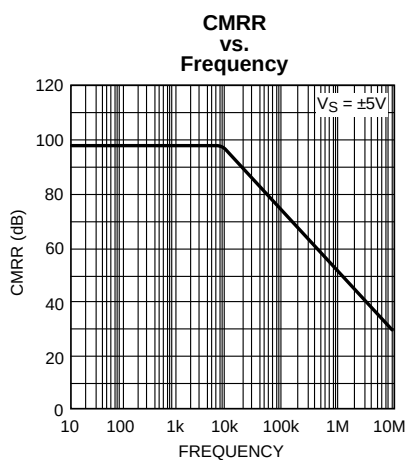


Figure 36.

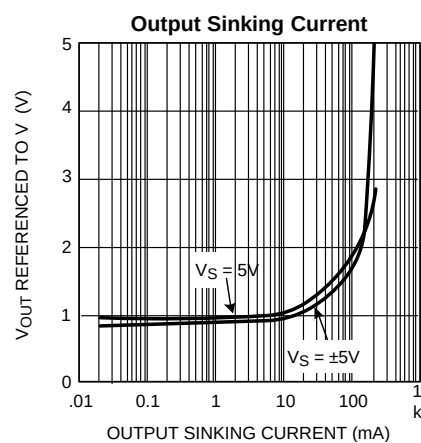


Figure 37.

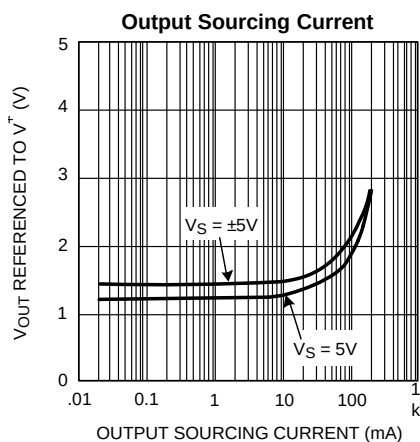


Figure 38.

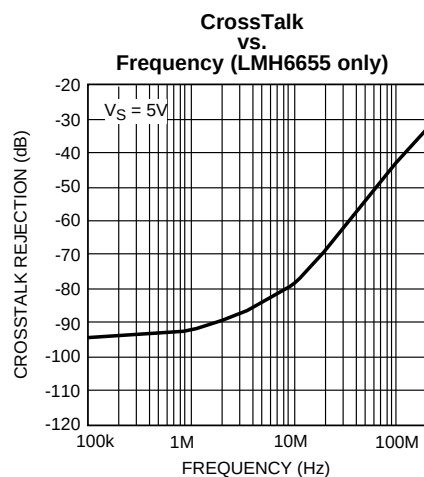


Figure 39.

Typical Performance Characteristics (continued)

$T_J = 25^\circ\text{C}$, $V^+ = \pm 5\text{V}$, $V^- = -5$, $R_F = 25\Omega$ for gain = +1, $R_F = 402\Omega$ and for gain $\geq +2$, and $R_L = 100\Omega$, unless otherwise specified.

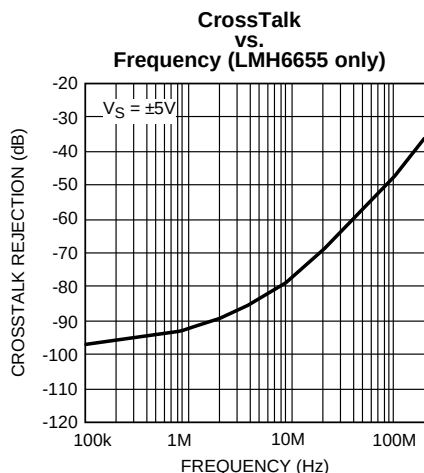


Figure 40.

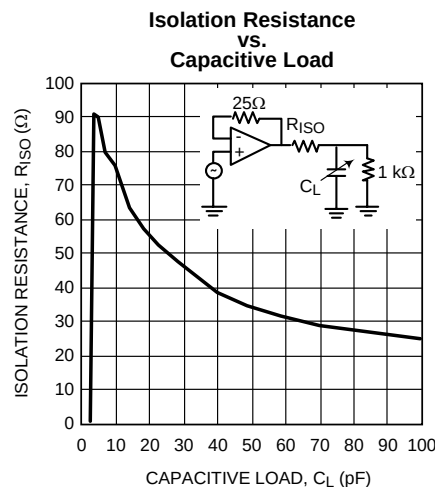


Figure 41.

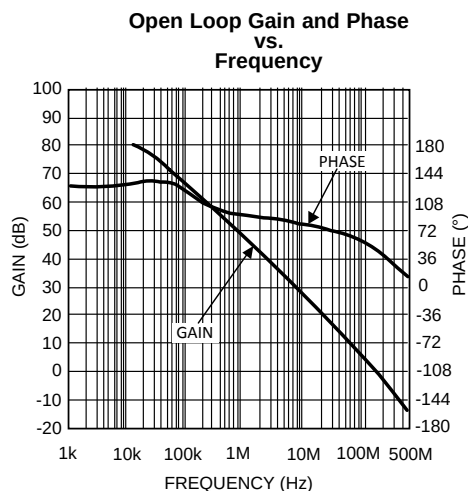


Figure 42.

APPLICATION INFORMATION

GENERAL INFORMATION

The LMH6654 single and LMH6655 dual high speed, voltage feedback amplifiers are manufactured on TI's new VIP10™ (Vertically Integrated PNP) complementary bipolar process. These amplifiers can operate from $\pm 2.5\text{V}$ to $\pm 6\text{V}$ power supply. They offer low supply current, wide bandwidth, very low voltage noise and large output swing. Many of the typical performance plots found in the datasheet can be reproduced if 50Ω coax and 50Ω $R_{IN/ROUT}$ resistors are used.

CIRCUIT LAYOUT CONSIDERATION

With all high frequency devices, board layouts with stray capacitance have a strong influence on the AC performance. The LMH6654/LMH6655 are not exception and the inverting input and output pins are particularly sensitive to the coupling of parasitic capacitance to AC ground. Parasitic capacitances on the inverting input and output nodes to ground could cause frequency response peaking and possible circuit oscillation. Therefore, the power supply, ground traces and ground plan should be placed away from the inverting input and output pins. Also, it is very important to keep the parasitic capacitance across the feedback to an absolute minimum.

The PCB should have a ground plane covering all unused portion of the component side of the board to provide a low impedance path. All trace lengths should be minimized to reduce series inductance.

Supply bypassing is required for the amplifiers performance. The bypass capacitors provide a low impedance return current path at the supply pins. They also provide high frequency filtering on the power supply traces. It is recommended that a ceramic decoupling capacitor 0.1 μF chip should be placed with one end connected to the ground plane and the other side as close as possible to the power pins. An additional 10 μF tantalum electrolytic capacitor should be connected in parallel, to supply current for fast large signal changes at the output.

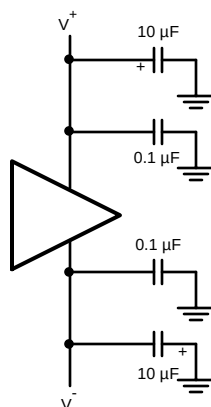


Figure 43. Supply Bypass Capacitors

EVALUATION BOARDS

TI provides the following evaluation boards as a guide for high frequency layout and as an aid in device testing and characterization.

Device	Package	Evaluation Board PN
LMH6654MF	5-Pin SOT-23	LMH730216
LMH6654MA	8-Pin SOIC	LMH730227
LMH6655MA	8-Pin SOIC	LMH730036
LMH6655MM	8-Pin VSSOP (DGK)	LMH730123

Components Needed to Evaluate the LMH6654 on the LMH730227 Evaluation Board:

- $R_f R_g$ use the datasheet to select values.
- R_{IN} , R_{OUT} typically 50 Ω (Refer to the Basic Operation section of the evaluation board datasheet for details)
- R_f is an optional resistor for inverting again configurations (select R_f to yield desired input impedance = $R_g || R_f$)
- C_1 , C_2 use 0.1 μF ceramic capacitors
- C_3 , C_4 use 10 μF tantalum capacitors

Components not used:

1. C_5 , C_6 , C_7 , C_8
2. R_1 thru R_8

The evaluation boards are designed to accommodate dual supplies. The board can be modified to provide single operation. For best performance;

- 1) do not connect the unused supply.
- 2) ground the unused supply pin.

POWER DISSIPATION

The package power dissipation should be taken into account when operating at high ambient temperature and/or high power dissipative conditions. In determining maximum operable temperature of the device, make sure the total power dissipation of the device is considered; this power dissipated in the device with a load connected to the output as well as the nominal dissipation of the op amp.

DRIVING CAPACITIVE LOADS

Capacitive loads decrease the phase margin of all op amps. The output impedance of a feedback amplifier becomes inductive at high frequencies, creating a resonant circuit when the load is capacitive. This can lead to overshoot, ringing and oscillation. To eliminate oscillation or reduce ringing, an isolation resistor can be placed as shown in [Figure 44](#) below. At frequencies above

$$F = \frac{1}{2 \pi R_{ISO} C_{LOAD}} \quad (1)$$

the load impedance of the Amplifier approaches R_{ISO} . The desired performance depends on the value of the isolation resistor. The isolation resistance vs. capacitance load graph in the typical performance characteristics provides the means for selection of the value of R_S that provides ≤ 3 dB peaking in closed loop $A_V = 1$ response. In general, the bigger the isolation resistor, the more damped the pulse response becomes. For initial evaluation, a 50Ω isolation resistor is recommended.

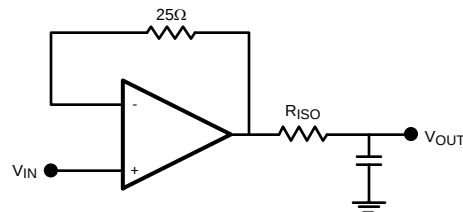


Figure 44. Isolation Resistor Placement

COMPONENTS SELECTION AND FEEDBACK RESISTOR

It is important in high-speed applications to keep all component leads short since wires are inductive at high frequency. For discrete components, choose carbon composition axially leaded resistors and micro type capacitors. Surface mount components are preferred over discrete components for minimum inductive effect. Never use wire wound type resistors in high frequency applications.

Large values of feedback resistors can couple with parasitic capacitance and cause undesired effects such as ringing or oscillation in high-speed amplifiers. Keep resistors as low as possible consistent with output loading consideration. For a gain of 2 and higher, 402Ω feedback resistor used for the typical performance plots gives optimal performance. For unity gain follower, a 25Ω feedback resistor is recommended rather than a direct short. This effectively reduces the Q of what would otherwise be a parasitic inductance (the feedback wire) into the parasitic capacitance at the inverting input.

BIAS CURRENT CANCELLATION

In order to cancel the bias current errors of the non-inverting configuration, the parallel combination of the gain setting R_g and feedback R_f resistors should equal the equivalent source resistance R_{seq} as defined in [Figure 45](#). Combining this constraint with the non-inverting gain equation, allows both R_f and R_g to be determined explicitly from the following equations:

$$R_f = A_V R_{seq} \text{ and } R_g = R_f / (A_V - 1) \quad (2)$$

For inverting configuration, bias current cancellation is accomplished by placing a resistor R_b on the non-inverting input equal in value to the resistance seen by the inverting input ($R_f / (R_g + R_s)$). The additional noise contribution of R_b can be minimized through the use of a shunt capacitor.

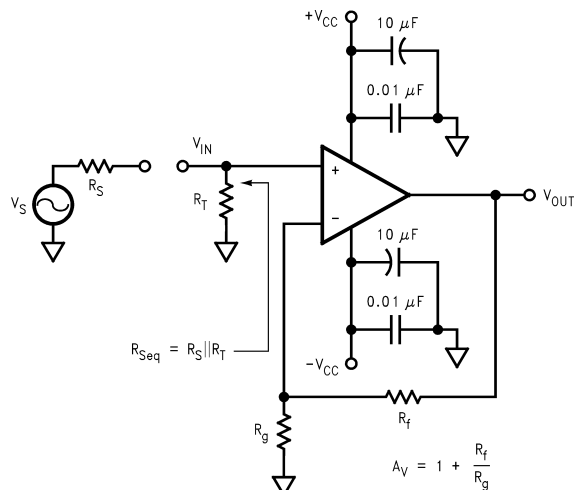


Figure 45. Non-Inverting Amplifier Configuration

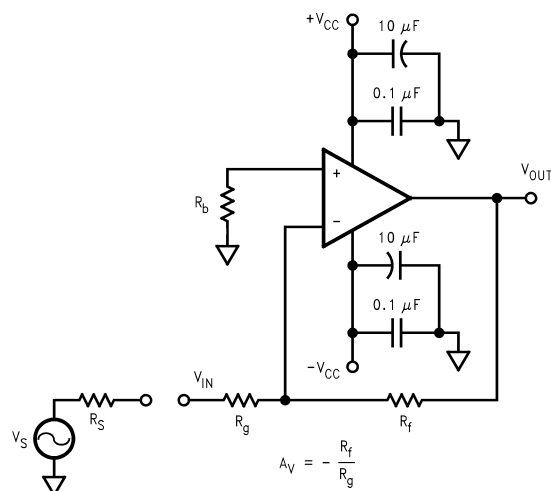


Figure 46. Inverting Amplifier Configuration

TOTAL INPUT NOISE VS. SOURCE RESISTANCE

The noise model for the non-inverting amplifier configuration showing all noise sources is described in [Figure 47](#). In addition to the intrinsic input voltage noise (e_n) and current noise ($i_n = i_{n+} = i_{n-}$) sources, there also exists thermal voltage noise $e_r = \sqrt{4kTR}$ associated with each of the external resistors. [Equation 3](#) provides the general form for total equivalent input voltage noise density (e_{ni}). [Equation 4](#) is a simplification of [Equation 3](#) that assumes $R_f || R_g = R_{seq}$ for bias current cancellation. [Figure 48](#) illustrates the equivalent noise model using this assumption. The total equivalent output voltage noise (e_{no}) is $e_{ni} * A_V$.

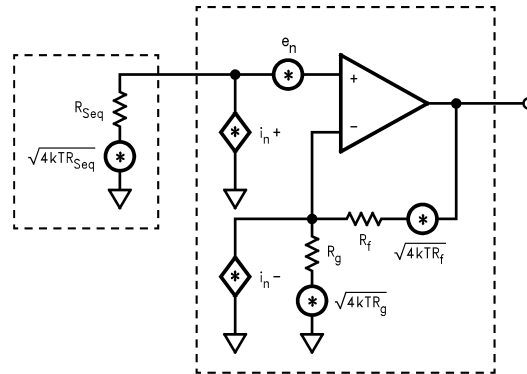


Figure 47. Non-Inverting Amplifier Noise Model

$$e_{ni} = \sqrt{e_n^2 + (i_{n+} \cdot R_{Seq})^2 + 4kTR_{Seq} + (i_{n-} \cdot (R_f \parallel R_g))^2 + 4kT(R_f \parallel R_g)} \quad (3)$$

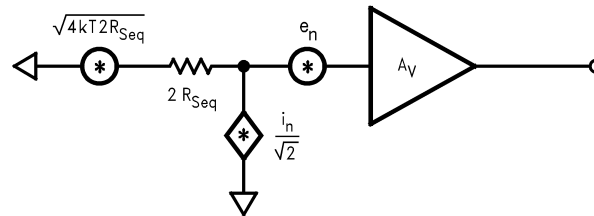


Figure 48. Noise Model with $R_f \parallel R_g = R_{Seq}$

$$e_{ni} = \sqrt{e_n^2 + 2(i_n \cdot R_{Seq})^2 + 4kT(2R_{Seq})} \quad (4)$$

If bias current cancellation is not a requirement, then $R_f \parallel R_g$ does not need to equal R_{Seq} . In this case, according to Equation 3, R_f and R_g should be as low as possible in order to minimize noise. Results similar to Equation 3 are obtained for the inverting configuration on Figure 46 if R_{Seq} is replaced by $R_b \parallel R_g$ if R_g is replaced by $R_g + R_s$. With these substitutions, Equation 3 will yield an e_{ni} referred to the non-inverting input. Referring e_{ni} to the inverting input is easily accomplished by multiplying e_{ni} by the ratio of non-inverting to inverting gains.

Noise Figure

Noise Figure (NF) is a measure of the noise degradation caused by an amplifier.

$$NF = 10 \log \left[\frac{S_i/N_i}{S_o/N_o} \right] = 10 \log \left[\frac{e_{ni}^2}{e_t^2} \right] \quad (5)$$

The noise figure formula is shown in Equation 5. The addition of a terminating resistor R_T , reduces the external thermal noise but increases the resulting NF.

The NF is increased because the R_T reduces the input signal amplitude thus reducing the input SNR.

$$\left[\frac{e_n^2 + i_n^2 (R_{Seq} + (R_f \parallel R_g))^2 + 4kTR_{Seq} + 4kT(R_f \parallel R_g)}{4kTR_{Seq}} \right] \quad (6)$$

The noise figure is related to the equivalent source resistance (R_{Seq}) and the parallel combination of R_f and R_g . To minimize noise figure, the following steps are recommended:

1. Minimize $R_f \parallel R_g$
2. Choose the Optimum R_s (R_{OPT})

R_{OPT} is the point at which the NF curve reaches a minimum and is approximated by:

$$R_{OPT} \approx (e_n/i_n)$$

REVISION HISTORY

Changes from Revision C (March 2013) to Revision D

Page

- Changed layout of National Data Sheet to TI format [17](#)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LMH6654MA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMH66 54MA	Samples
LMH6654MAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMH66 54MA	Samples
LMH6654MF	ACTIVE	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 85	A66A	Samples
LMH6654MF/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A66A	Samples
LMH6654MFX	ACTIVE	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 85	A66A	Samples
LMH6654MFX/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A66A	Samples
LMH6655MA	ACTIVE	SOIC	D	8	95	TBD	Call TI	Call TI	-40 to 85	LMH66 55MA	Samples
LMH6655MA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMH66 55MA	Samples
LMH6655MAX	ACTIVE	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 85	LMH66 55MA	Samples
LMH6655MAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMH66 55MA	Samples
LMH6655MM	ACTIVE	VSSOP	DGK	8	1000	TBD	Call TI	Call TI	-40 to 85	A67A	Samples
LMH6655MM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A67A	Samples
LMH6655MMX	ACTIVE	VSSOP	DGK	8	3500	TBD	Call TI	Call TI	-40 to 85	A67A	Samples
LMH6655MMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A67A	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

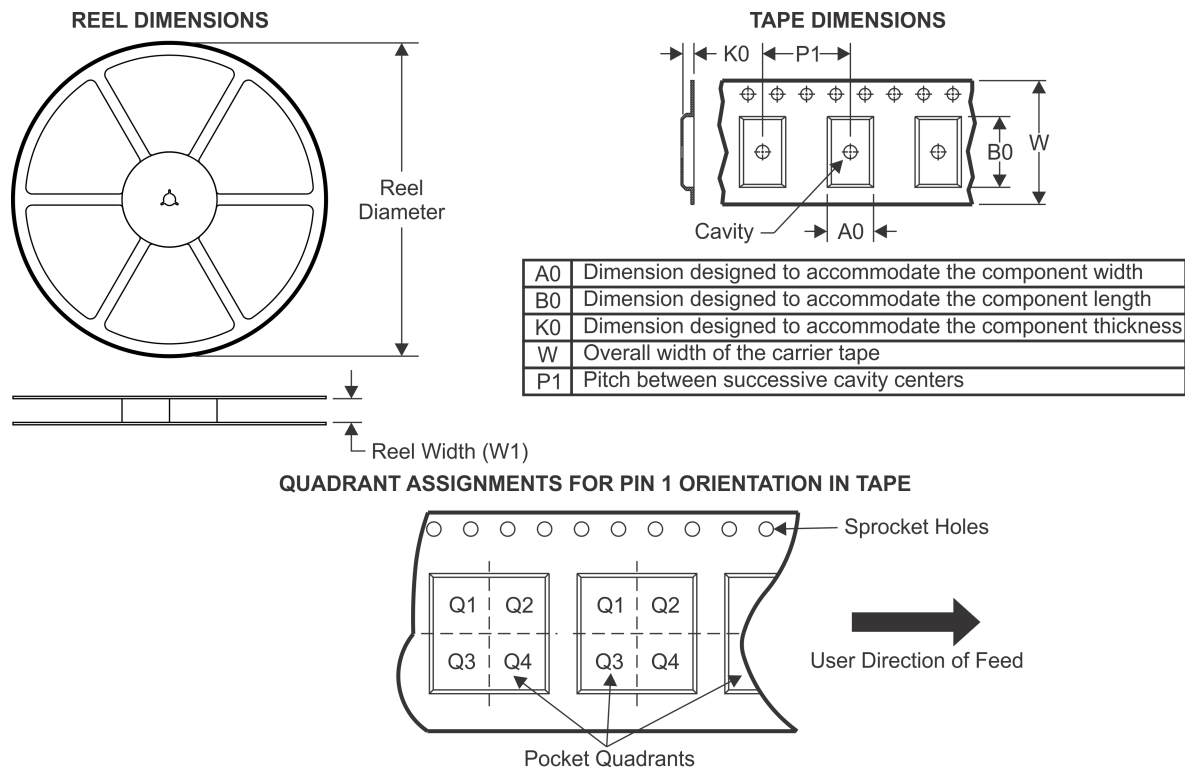
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ Only one of markings shown within the brackets will appear on the physical device.

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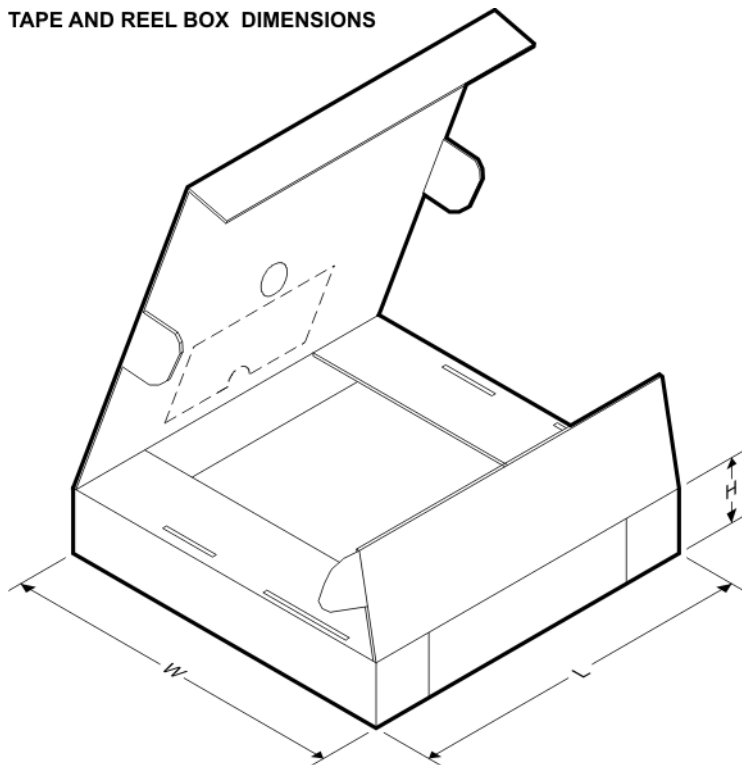
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TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH6654MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMH6654MF	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMH6654MF/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMH6654MFX	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMH6654MFX/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMH6655MAX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMH6655MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMH6655MM	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMH6655MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMH6655MMX	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMH6655MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

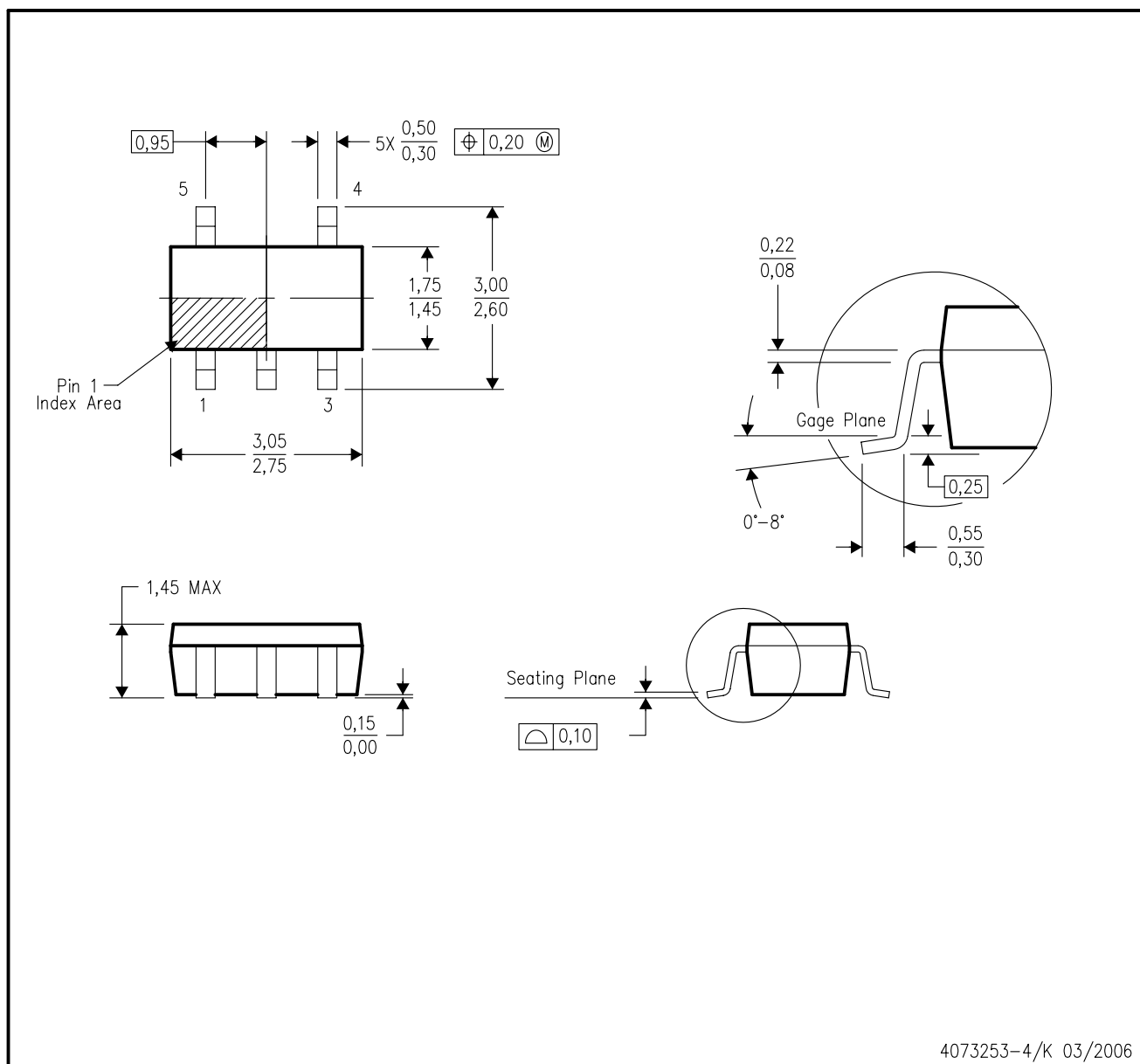


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH6654MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMH6654MF	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMH6654MF/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMH6654MFX	SOT-23	DBV	5	3000	210.0	185.0	35.0
LMH6654MFX/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LMH6655MAX	SOIC	D	8	2500	367.0	367.0	35.0
LMH6655MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMH6655MM	VSSOP	DGK	8	1000	210.0	185.0	35.0
LMH6655MM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LMH6655MMX	VSSOP	DGK	8	3500	367.0	367.0	35.0
LMH6655MMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0

DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE

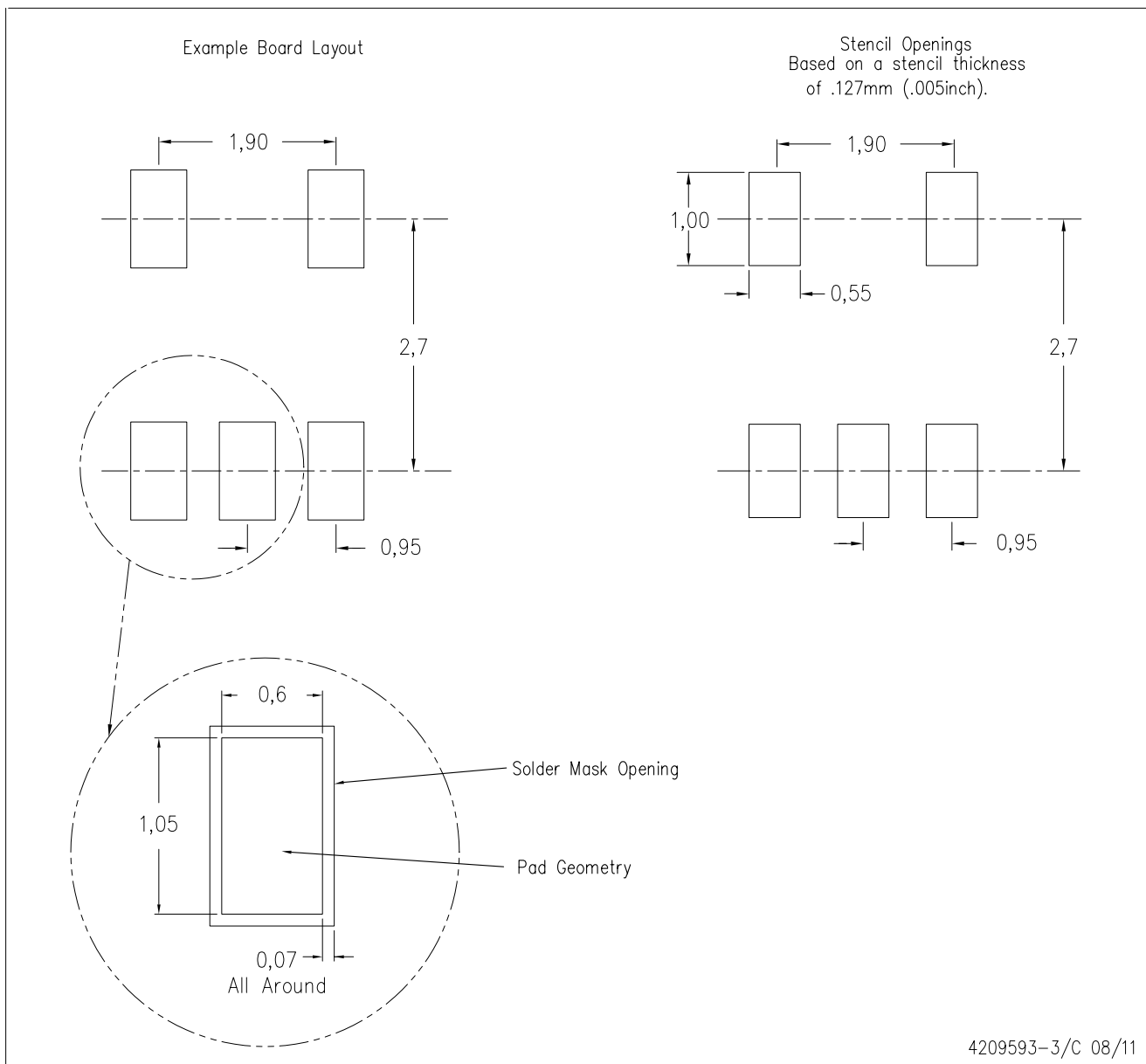


4073253-4/K 03/2006

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - Falls within JEDEC MO-178 Variation AA.

DBV (R-PDSO-G5)

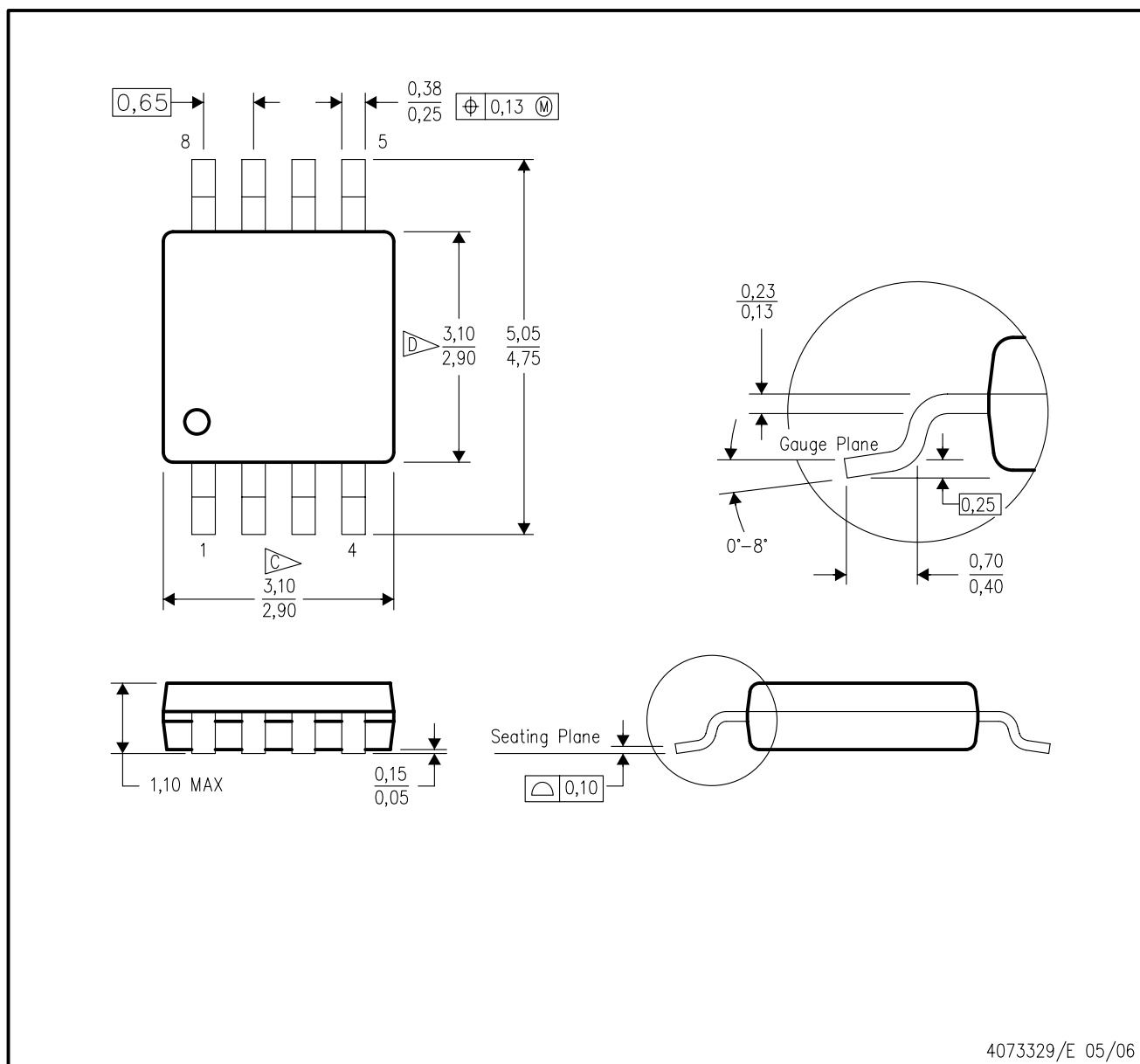
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE

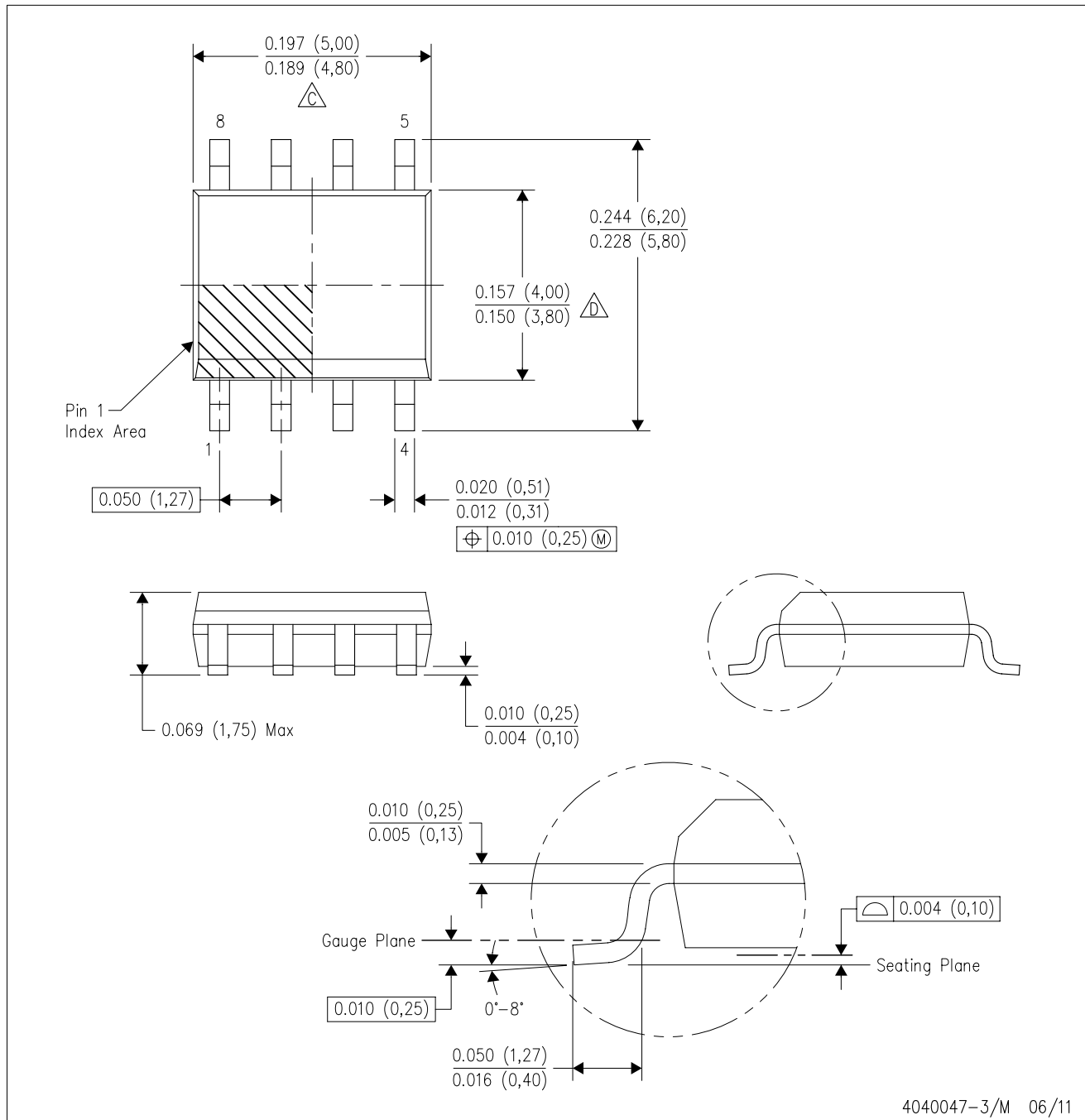


NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
- E. Falls within JEDEC MO-187 variation AA, except interlead flash.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AA.

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Как с нами связаться

Телефон: 8 (812) 309 58 32 (многоканальный)

Факс: 8 (812) 320-02-42

Электронная почта: org@eplast1.ru

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.