

## N-channel 600 V, 85 mΩ typ., 30 A MDmesh™ M6 Power MOSFET in a D<sup>2</sup>PAK package

Datasheet - production data

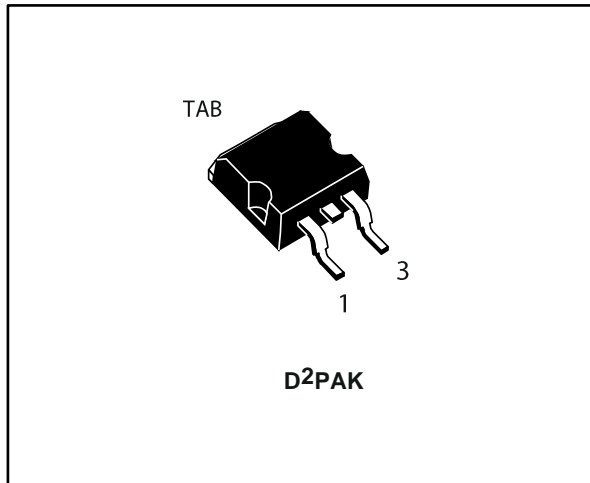
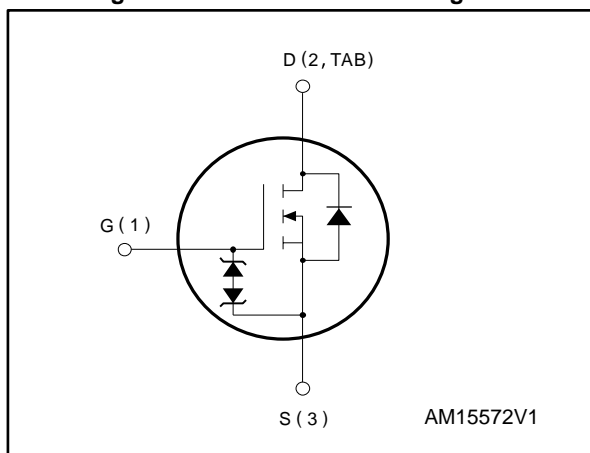


Figure 1: Internal schematic diagram



### Features

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>
STB36N60M6	600 V	99 mΩ	30 A

- Reduced switching losses
- Lower R<sub>DS(on)</sub> x area vs previous generation
- Low gate input resistance
- 100% avalanche tested
- Zener-protected

### Applications

- Switching applications

### Description

The new MDmesh™ M6 technology incorporates the most recent advancements to the well-known and consolidated MDmesh family of SJ MOSFETs. STMicroelectronics builds on the previous generation of MDmesh devices through its new M6 technology, which combines excellent R<sub>DS(on)</sub> \* area improvement with one of the most effective switching behaviors available, as well as a user-friendly experience for maximum end-application efficiency.

Table 1: Device summary

Order code	Marking	Package	Packing
STB36N60M6	36N60M6	D <sup>2</sup> PAK	Tape and reel

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# 1 Electrical ratings

**Table 2: Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{GS}$	Gate-source voltage	$\pm 25$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ °C}$	30	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ °C}$	19	A
$I_D^{(1)}$	Drain current (pulsed)	102	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ °C}$	208	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
$dv/dt^{(3)}$	MOSFET $dv/dt$ ruggedness	50	
$T_J$	Operating junction temperature range	-55 to 150	°C
$T_{stg}$	Storage temperature range		

**Notes:**

(1)Pulse width limited by safe operating area.

(2) $I_{SD} \leq 30\text{ A}$ ,  $di/dt = 400\text{ A}/\mu\text{s}$ ;  $V_{DS\text{ peak}} < V_{(BR)DSS}$ ,  $V_{DD} = 400\text{ V}$

(3) $V_{DS} \leq 480\text{ V}$

**Table 3: Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj\text{-case}}$	Thermal resistance junction-case	0.6	°C/W
$R_{thj\text{-pcb}}$	Thermal resistance junction-pcb <sup>(1)</sup>	30	

**Notes:**

(1)When mounted on 1 inch<sup>2</sup> FR-4, 2 Oz copper board.

**Table 4: Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AR}$	Avalanche current, repetitive or not repetitive (pulse width limited by $T_{jmax}$ )	5	A
$E_{AS}$	Single pulse avalanche energy (starting $T_j = 25\text{ °C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ )	750	mJ

## 2 Electrical characteristics

$T_C = 25\text{ °C}$  unless otherwise specified

**Table 5: On/off-state**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$ , $I_D = 1\text{ mA}$	600			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$ , $V_{DS} = 600\text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}$ , $V_{DS} = 600\text{ V}$ ; $T_C = 125\text{ °C}$ <sup>(1)</sup>			100	$\mu\text{A}$
$I_{GSS}$	Gate body leakage current	$V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 25\text{ V}$			$\pm 5$	$\mu\text{A}$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	3.25	4	4.75	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 15\text{ A}$		85	99	m $\Omega$

**Notes:**

<sup>(1)</sup>Defined by design, not subject to production test.

**Table 6: Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 100\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0\text{ V}$	-	1960	-	pF
$C_{oss}$	Output capacitance		-	93	-	pF
$C_{rss}$	Reverse transfer capacitance		-	6	-	pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0\text{ to }480\text{ V}$ , $V_{GS} = 0\text{ V}$	-	332	-	pF
$R_G$	Intrinsic gate resistance	$f = 1\text{ MHz}$ open drain	-	1.6	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 480\text{ V}$ , $I_D = 30\text{ A}$ , $V_{GS} = 0\text{ to }10\text{ V}$ , (See <a href="#">Figure 15: "Test circuit for gate charge behavior"</a> )	-	44.3	-	nC
$Q_{gs}$	Gate-source charge		-	10.1	-	nC
$Q_{gd}$	Gate-drain charge		-	25	-	nC

**Notes:**

<sup>(1)</sup> $C_{oss\text{ eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$ .

**Table 7: Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$ , $I_D = 15\text{ A}$ , $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$ (See <a href="#">Figure 14: "Test circuit for resistive load switching times"</a> and <a href="#">Figure 19: "Switching time waveform"</a> )	-	15.2	-	ns
$t_r$	Rise time		-	5.3	-	ns
$t_{d(off)}$	Turn-off delay time		-	50.2	-	ns
$t_f$	Fall time		-	7.3	-	ns

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		30	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		102	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 30\text{ A}$ , $V_{GS} = 0\text{ V}$	-		1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 30\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 60\text{ V}$ , (see <a href="#">Figure 16</a> : "Test circuit for inductive load switching and diode recovery times")	-	340		ns
$Q_{rr}$	Reverse recovery charge		-	5.3		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	31		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 30\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 60\text{ V}$ , $T_j = 150\text{ }^\circ\text{C}$ (see <a href="#">Figure 16</a> : "Test circuit for inductive load switching and diode recovery times")	-	430		ns
$Q_{rr}$	Reverse recovery charge		-	7.7		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	36		A

**Notes:**

(1)Pulse width limited by safe operating area.

(2)Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

## 2.1 Electrical characteristics (curves)

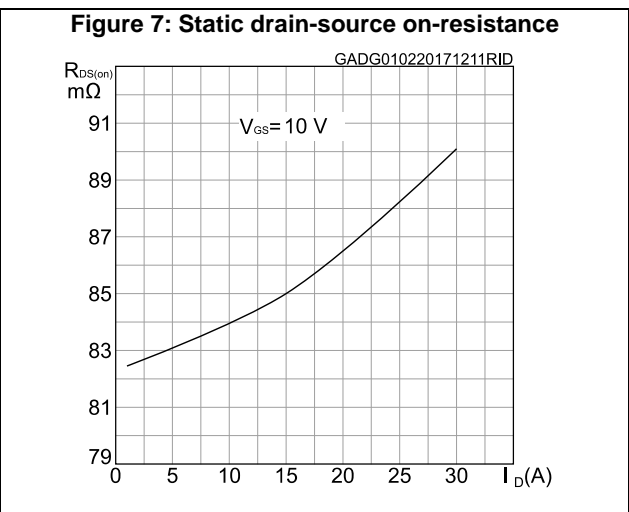
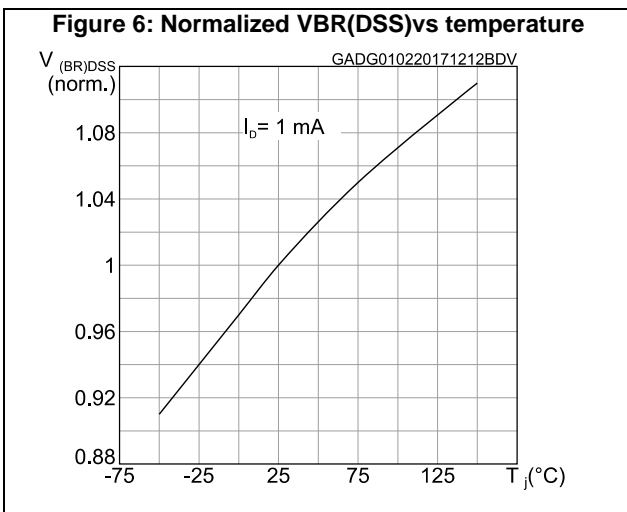
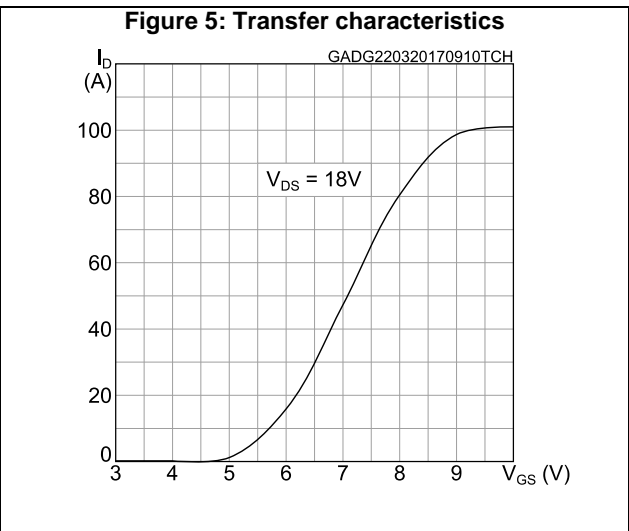
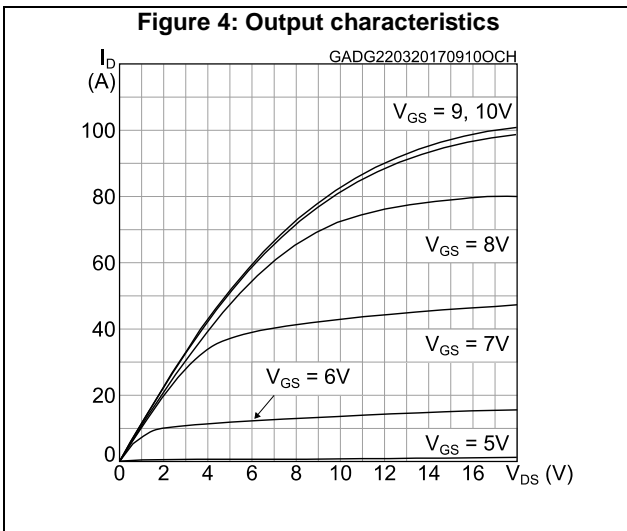
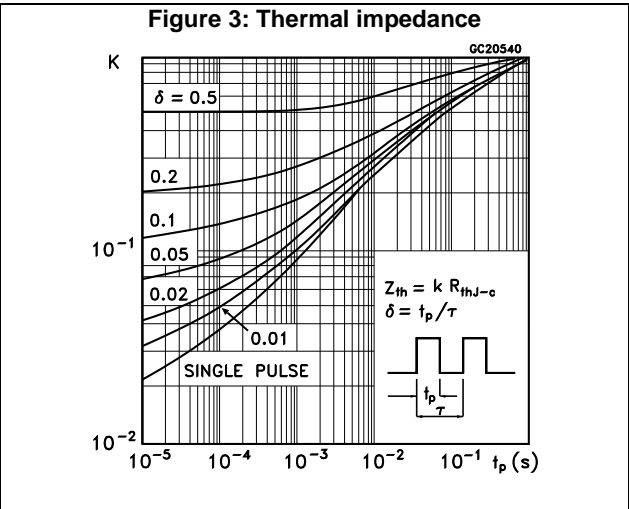
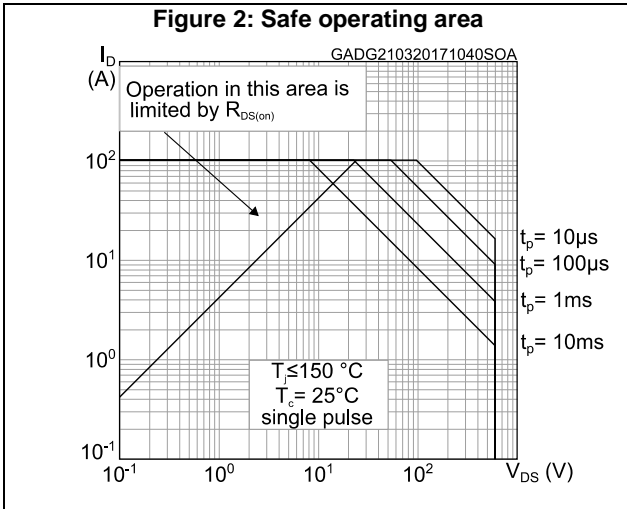


Figure 8: Gate charge vs gate-source voltage

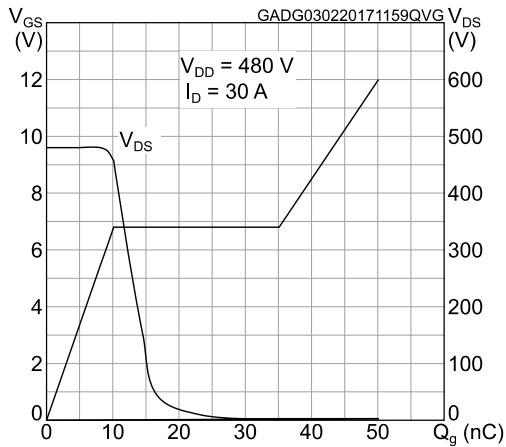


Figure 9: Capacitance variations

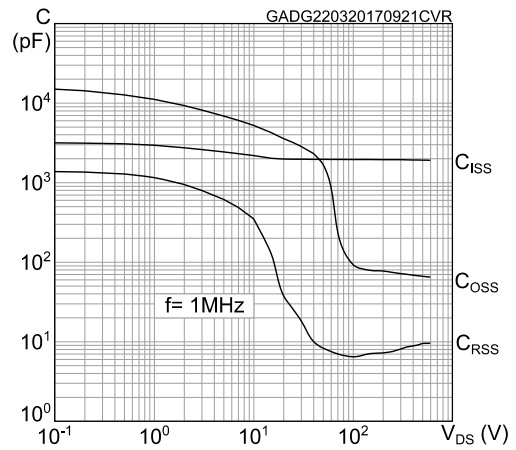


Figure 10: Normalized gate threshold voltage vs temperature

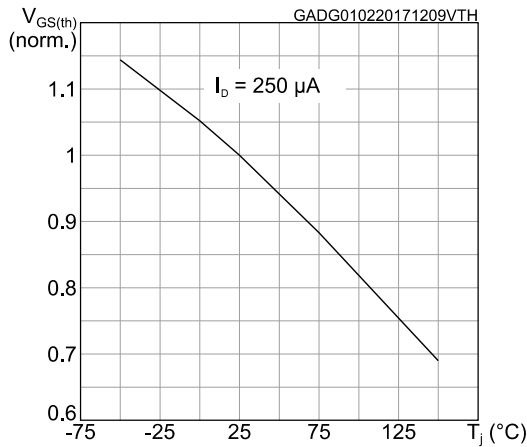


Figure 11: Normalized on-resistance vs temperature

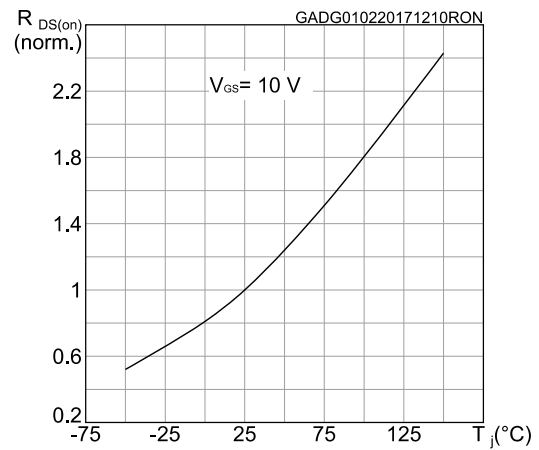


Figure 12: Source-drain diode forward characteristics

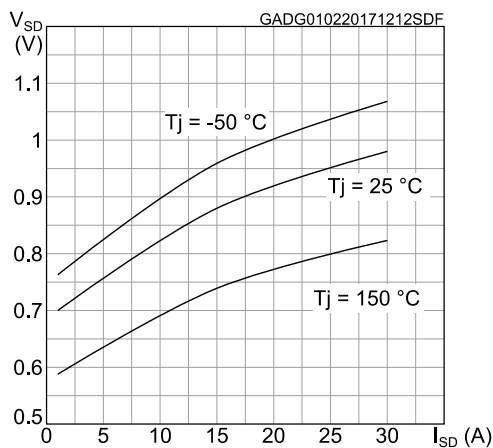
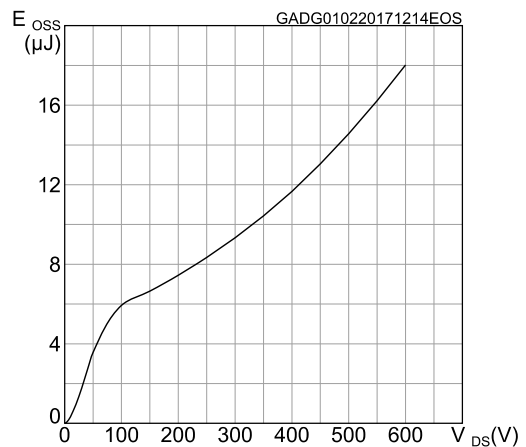


Figure 13: Output capacitance stored energy



### 3 Test circuits

**Figure 14: Test circuit for resistive load switching times**



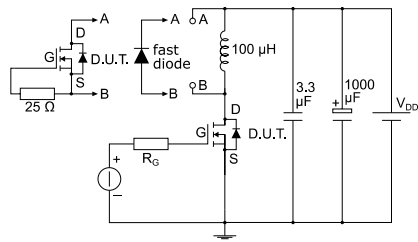
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**Figure 15: Test circuit for gate charge behavior**



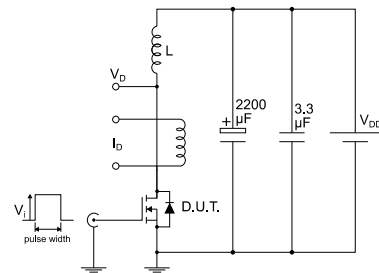
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**Figure 16: Test circuit for inductive load switching and diode recovery times**



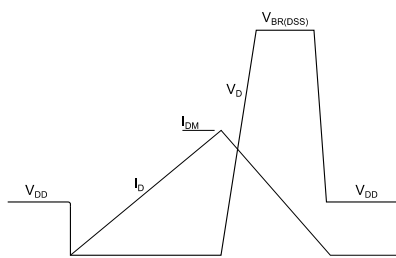
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**Figure 17: Unclamped inductive load test circuit**



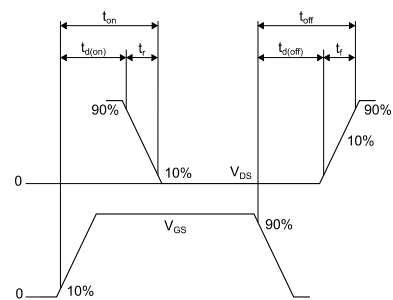
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**Figure 18: Unclamped inductive waveform**



AM01472v1

**Figure 19: Switching time waveform**



AM01473v1



## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 4.1 D2PAK type A package information

Figure 20: D<sup>2</sup>PAK (TO-263) type A package outline

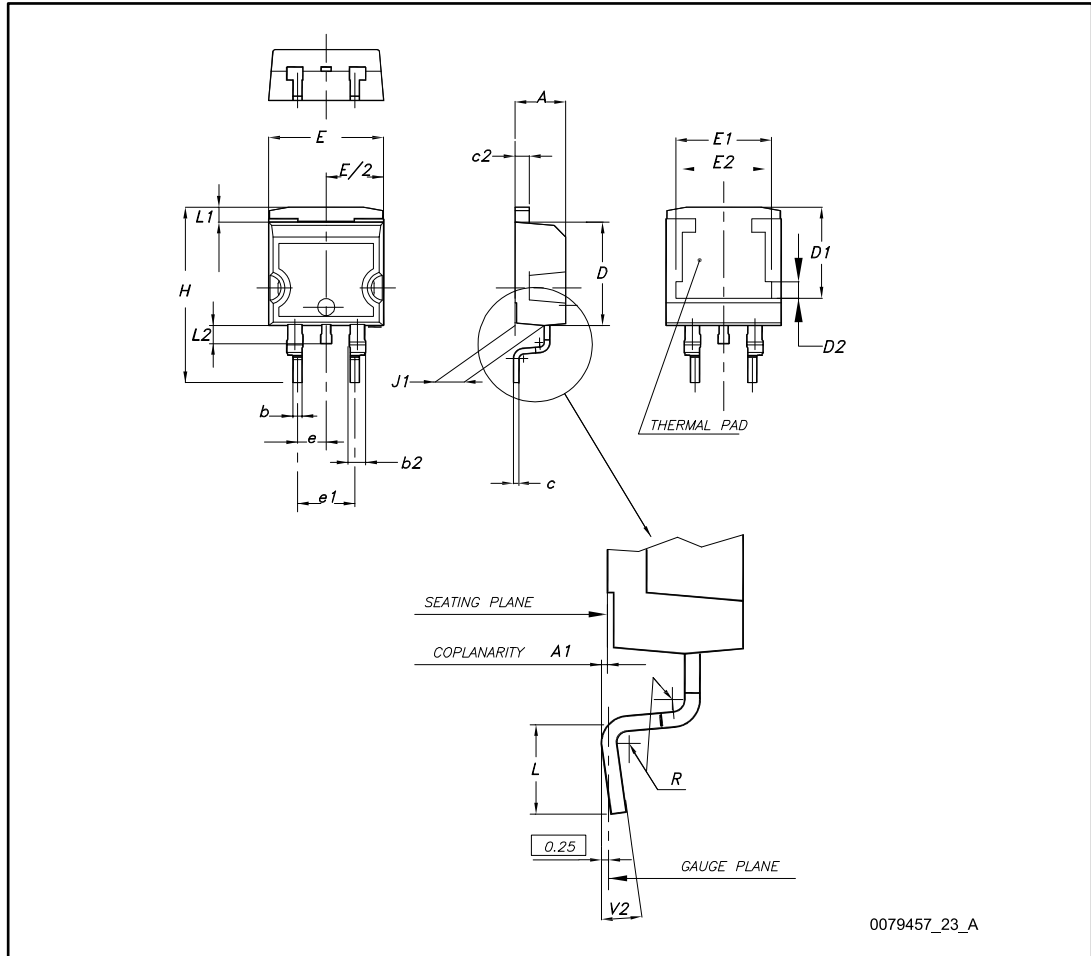
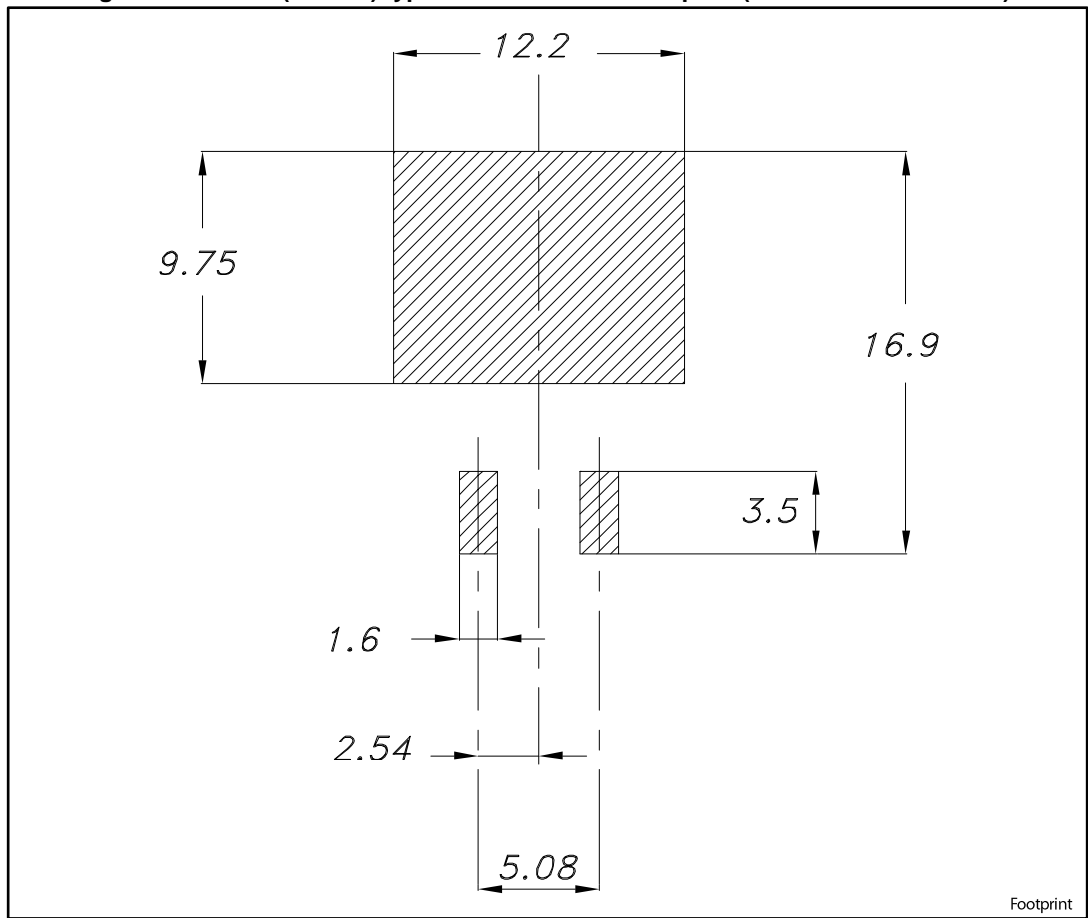


Table 9: D<sup>2</sup>PAK (TO-263) type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10.00		10.40
E1	8.50	8.70	8.90
E2	6.85	7.05	7.25
e		2.54	
e1	4.88		5.28
H	15.00		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.40	
V2	0°		8°

Figure 21: D<sup>2</sup>PAK (TO-263) type A recommended footprint (dimensions are in mm)



### 4.2 D<sup>2</sup>PAK (TO-263) type B package information

Figure 22: D<sup>2</sup>PAK (TO-263) type B package outline

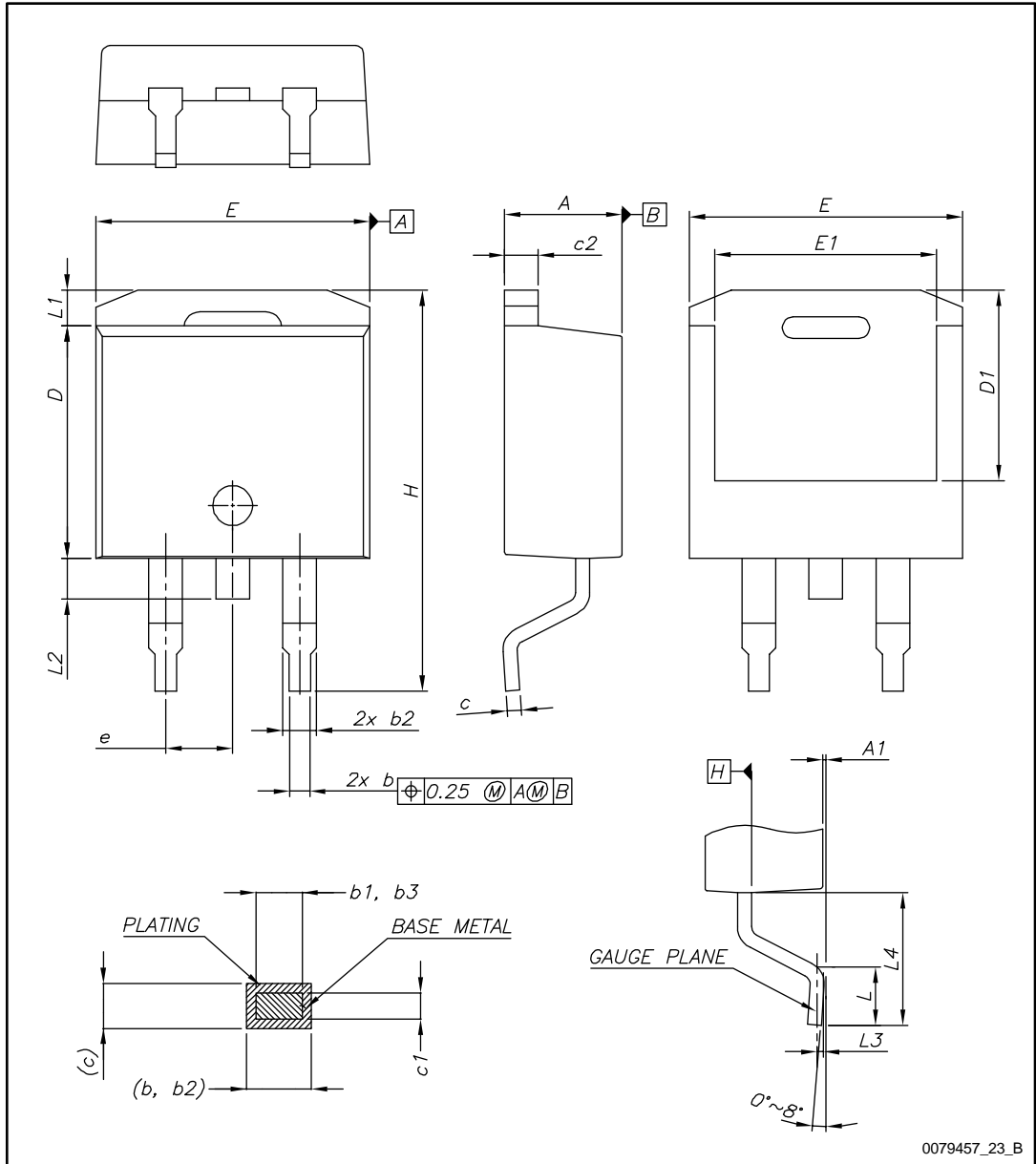
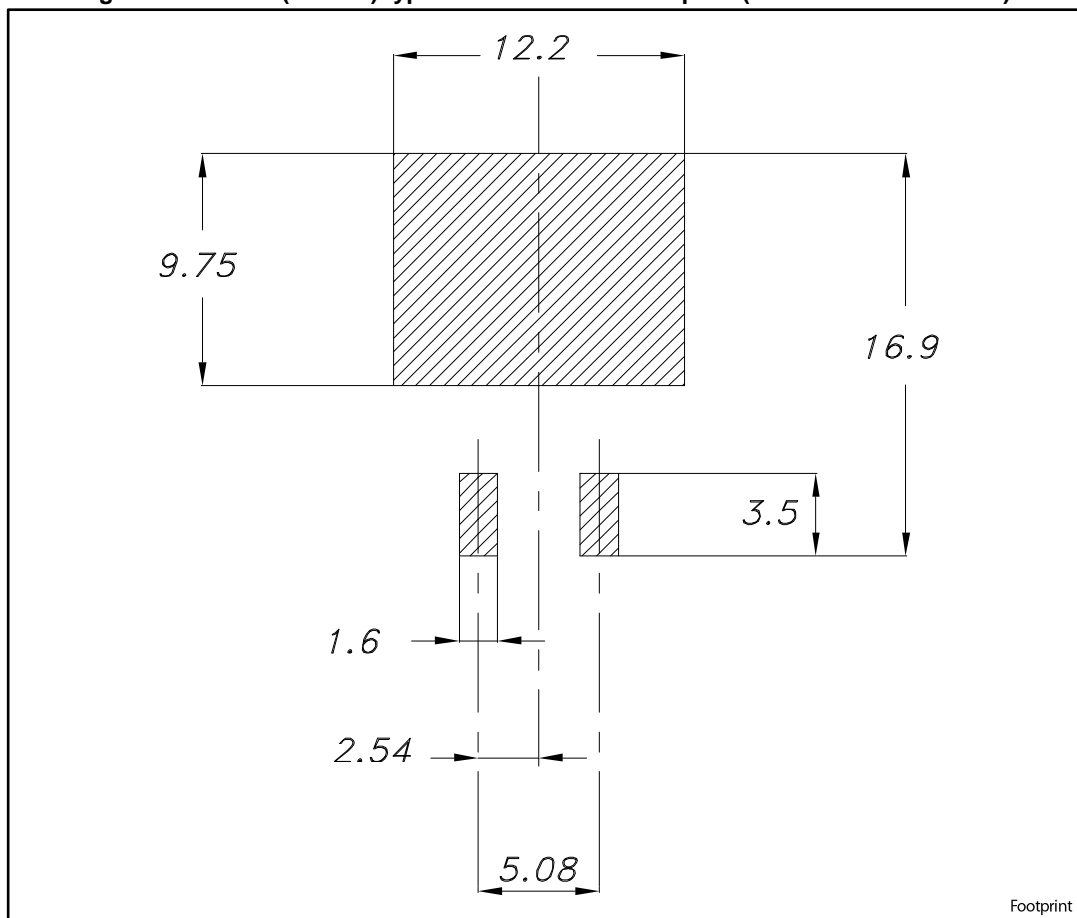


Table 10: D<sup>2</sup>PAK (TO-263) type B mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.36		4.56
A1	0		0.25
b	0.70		0.90
b1	0.51		0.89
b2	1.17		1.37
b3	1.36		1.46
c	0.38		0.694
c1	0.38		0.534
c2	1.19		1.34
D	8.60		9.00
D1	6.90		7.50
E	10.15		10.55
E1	8.10		8.70
e	2.54 BSC		
H	15.00		15.60
L	1.90		2.50
L1			1.65
L2			1.78
L3		0.25	
L4	4.78		5.28

Figure 23: D<sup>2</sup>PAK (TO-263) type B recommended footprint (dimensions are in mm)



### 4.3 D2PAK type A packing information

Figure 24: D2PAK type A tape outline

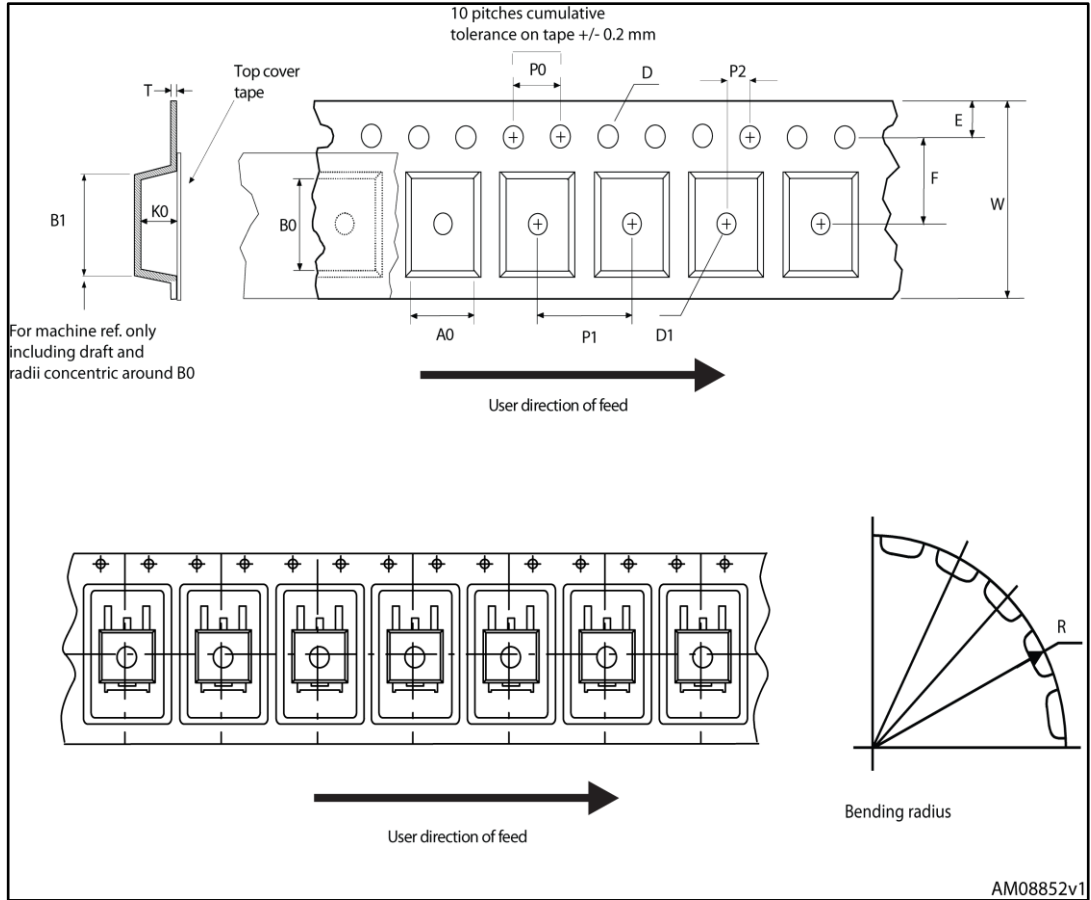


Figure 25: D2PAK type A reel outline

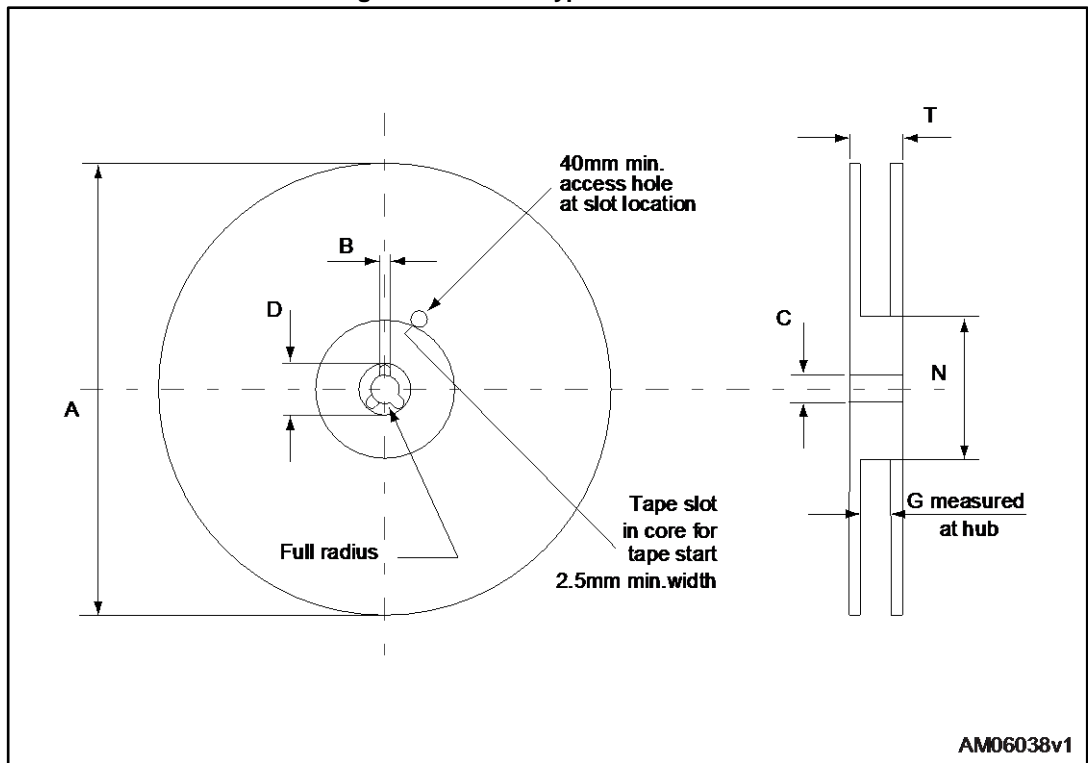


Table 11: D<sup>2</sup>PAK type A tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base quantity		1000
P2	1.9	2.1	Bulk quantity		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			



### 4.4 D<sup>2</sup>PAK type B packing information

Figure 26: D2PAK type B tape outline

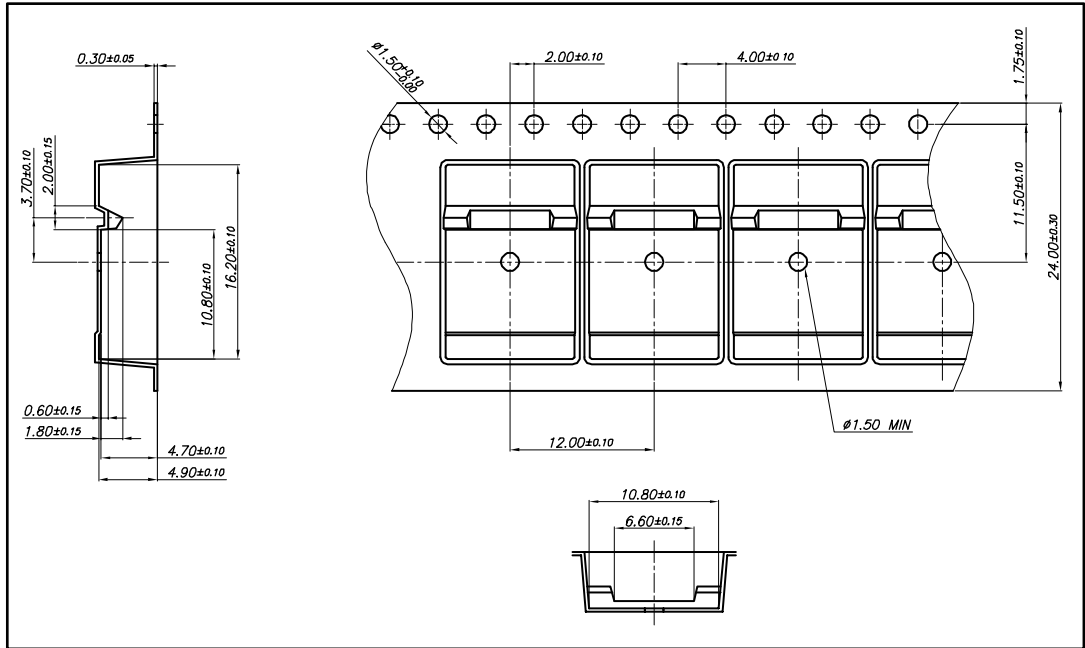


Figure 27: D2PAK type B reel outline

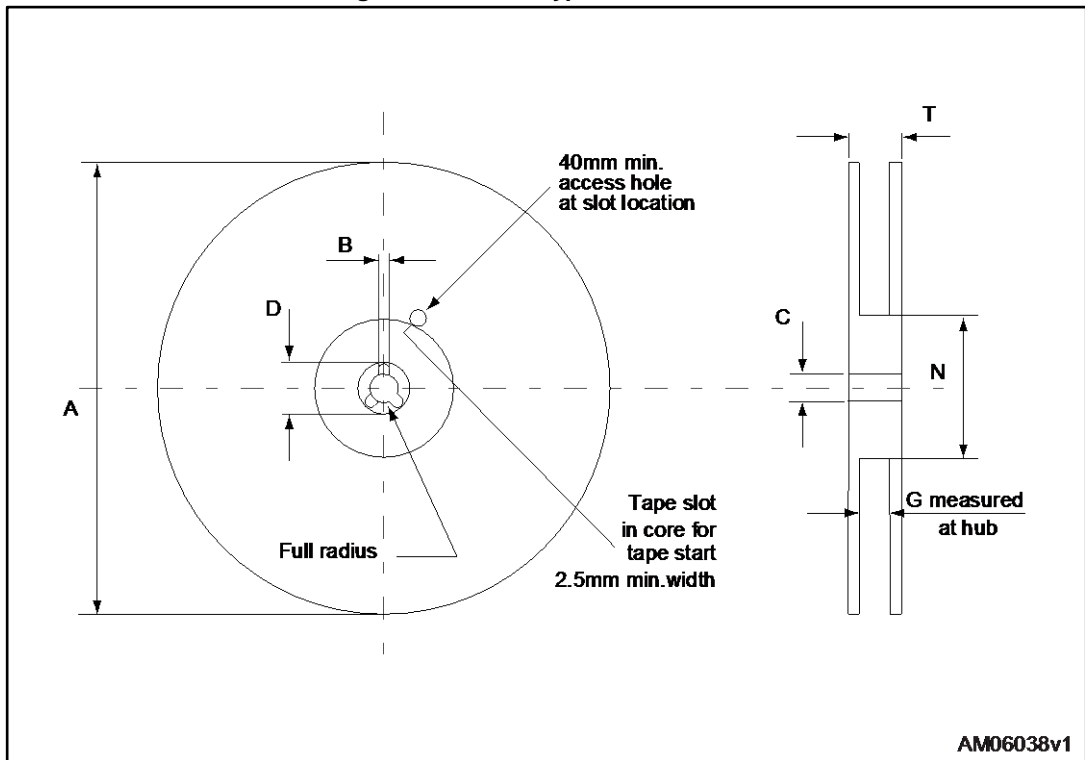


Table 12: D<sup>2</sup>PAK type B reel mechanical data

Dim.	mm	
	Min.	Max.
A		330
B	1.5	
C	12.8	13.2
D	20.2	
G	24.4	26.4
N	100	
T		30.4

## 5 Revision history

**Table 13: Document revision history**

Date	Revision	Changes
08-Jan-2015	1	Initial release.
07-Apr-2016	2	Updated <i>Table 2: "Absolute maximum ratings"</i> , <i>Table 6: "Dynamic"</i> , <i>Table 7: "Switching times"</i> and <i>Table 8: "Source-drain diode"</i> .
06-Feb-2017	3	Updated title, the table of features in cover page, <i>Section 1: "Electrical ratings"</i> and <i>Section 2: "Electrical characteristics"</i> . Added <i>Section 2.1: "Electrical characteristics (curves)"</i> . Added <i>Section 4.2: "D<sup>2</sup>PAK (TO-263) type B package information"</i> and <i>Section 4.4: "D<sup>2</sup>PAK type B packing information"</i> . Minor text changes.
21-Mar-2017	4	Updated document status from preliminary to production data. Updated <i>Table 2: "Absolute maximum ratings"</i> , <i>Table 6: "Dynamic"</i> and <i>Table 8: "Source-drain diode"</i> . Updated <i>Figure 2: "Safe operating area"</i> , <i>Figure 4: "Output characteristics"</i> , <i>Figure 5: "Transfer characteristics"</i> and <i>Figure 9: "Capacitance variations"</i> .

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