

FEATURES

- Controls supply voltages from 4 V to 60 V
- Gate drive for low voltage drop reverse supply protection
- Gate drive for P-channel FETs
- Inrush current limiting control
- Adjustable current limit
- Foldback current limiting
- Automatic retry or latch-off on current fault
- Programmable current-limit timer for safe operating area (SOA)
- Power-good and fault outputs
- Analog undervoltage (UV) and overvoltage (OV) protection
- 16-lead, 3 mm × 3 mm LFCSP
- 16-lead QSOP

APPLICATIONS

- Industrial modules
- Battery-powered/portable instrumentation

GENERAL DESCRIPTION

The [ADM1270](#) is a current-limiting controller that provides inrush current limiting and overcurrent protection for modular or battery-powered systems. When circuit boards are inserted into a live backplane, discharged supply bypass capacitors draw large transient currents from the backplane power bus as they charge. These transient currents can cause permanent damage to connector pins, as well as dips on the backplane supply that can reset other boards in the system.

The [ADM1270](#) is designed to control the inrush current, when powering on the system, via an external P-channel field effect transistor (FET).

To protect the system from a reverse polarity input supply, there is a provision made to control an additional external P-channel FET. This feature prevents reverse current flow in case of a reverse polarity connection, which can damage the load or the [ADM1270](#).

The [ADM1270](#) is available in a 3 mm × 3 mm, 16-lead LFCSP and a 16-lead QSOP.

SIMPLIFIED FUNCTIONAL BLOCK DIAGRAM

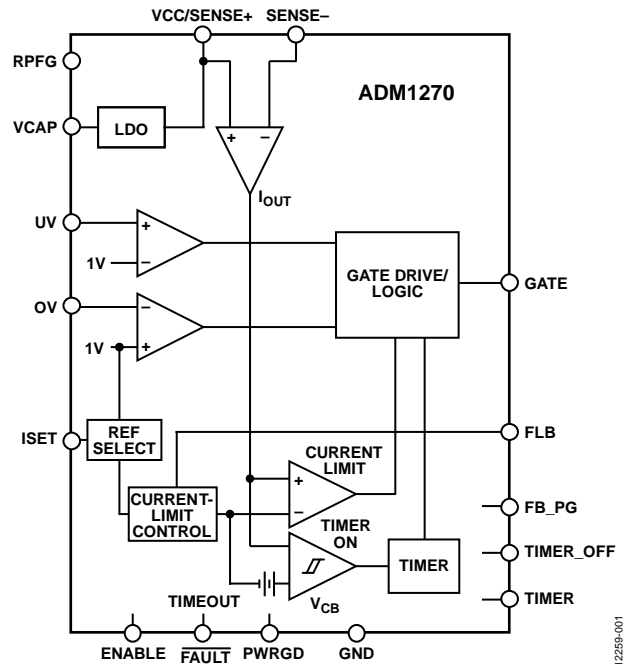


Figure 1.

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REVISION HISTORY

4/16—Rev. 0 to Rev. A
 Change to Setting the Current Limit (ISET) Section..... 17

12/14—Revision 0: Initial Version

SPECIFICATIONS

$V_{CC}/V_{SENSE+} = 4\text{ V to }60\text{ V}$, $V_{SENSE} = (V_{SENSE+} - V_{SENSE-}) = 0\text{ V}$, $T_A = -40^{\circ}\text{C to }+125^{\circ}\text{C}$, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
POWER SUPPLY						
Operating Voltage Range	V_{CC}	4		60	V	
Quiescent Current	I_{CC}		360	500	μA	GATE on
UV PIN						
Input Current	I_{UV}		0.005	0.2	μA	$UV \leq 5.5\text{ V}$, $T_A = -40^{\circ}\text{C to }+85^{\circ}\text{C}$
			0.005	1	μA	$UV \leq 5.5\text{ V}$, $T_A = -40^{\circ}\text{C to }+125^{\circ}\text{C}$
UV Threshold	UV_{TH}	0.985	1.0	1.015	V	UV falling
UV Threshold Hysteresis	UV_{HYST}	55	60	65	mV	
UV Glitch Filter	UV_{GF}	4		7	μs	50 mV overdrive
UV Propagation Delay	UV_{PD}		6	8	μs	UV low to GATE pull-down circuit active
OV PIN						
Input Current	I_{OV}		0.005	0.2	μA	$OV \leq 5.5\text{ V}$, $T_A = -40^{\circ}\text{C to }+85^{\circ}\text{C}$
			0.005	1	μA	$OV \leq 5.5\text{ V}$, $T_A = -40^{\circ}\text{C to }+125^{\circ}\text{C}$
OV Threshold	OV_{TH}	0.985	1.0	1.015	V	OV rising
OV Threshold Hysteresis	OV_{HYST}	25	30	35	mV	
OV Glitch Filter	OV_{GF}	0.5		2.0	μs	50 mV overdrive
OV Propagation Delay	OV_{PD}		1.5	2.5	μs	OV high to GATE pull-up circuit active
SENSE-						
Input Current	I_{SENSE-}	20	40	70	μA	$SENSE- = 60\text{ V}$
V_{CAP} PIN						
Internally Regulated Voltage	V_{VCAP}	3.546	3.6	3.636	V	$0\text{ }\mu\text{A} \leq I_{VCAP} \leq 1\text{ mA}$, $C_{VCAP} = 1\text{ }\mu\text{F}$
Undervoltage Lockout	$UVLO$					
Rising	$UVLO_{RISE}$			3.4	V	V_{CC} rising
Falling	$UVLO_{FALL}$	3.0			V	V_{CC} falling
Hysteresis	$UVLO_{HYST}$		230		mV	
ISET PIN						
Input Current	I_{SET}		0.005	0.2	μA	$V_{SET} \leq V_{VCAP}$, $T_A = -40^{\circ}\text{C to }+85^{\circ}\text{C}$
			0.005	1	μA	$V_{SET} \leq V_{VCAP}$, $T_A = -40^{\circ}\text{C to }+125^{\circ}\text{C}$
Reference Select Threshold	$V_{ISETRSTH}$	2.55	2.6	2.65	V	If $V_{ISET} > V_{ISETRSTH}$, an internal reference (V_{CLREF}) is used
Internal Reference	V_{CLREF}		2		V	Accuracies included in total sense voltage accuracies
Gain of Current Sense Amplifier	AV_{CSAMP}		40		V/V	Accuracies included in total sense voltage accuracies
RPF_G PIN						
Reverse Protection FET Gate Drive Voltage	V_{RPFG}		0		V	$V_{CC} \leq 10\text{ V}$
Reverse Protection FET Gate Drive Voltage Offset	ΔV_{RPFG}	10	12	14	V	$\Delta V_{RPFG} = V_{CC} - V_{RPFG}$, $60\text{ V} \geq V_{CC} \geq 14\text{ V}$, $I_{RPFG} \leq 5\text{ }\mu\text{A}$
RPF _G Pull-Down (On) Current	I_{RPFGND}	7	9	12	μA	$V_{RPFG} = V_{CC}$
GATE PIN						
GATE Drive Voltage	ΔV_{GATE}	10	12	14	V	$\Delta V_{GATE} = V_{CC} - V_{GATE}$, $60\text{ V} \geq V_{CC} \geq 14\text{ V}$, $I_{GATE} \leq 5\text{ }\mu\text{A}$
GATE Pull-Down (On) Current	I_{GATEDN}	20	25	30	μA	$V_{GATE} = V_{CC}$
GATE Pull-Up (Off) Current	I_{GATEUP}					
Regulation	I_{GATEUP_REG}	-50	-65	-80	μA	$\Delta V_{GATE} \geq 2\text{ V}$, $(V_{SENSE+} - V_{SENSE-}) = 70\text{ mV}$
Fault	I_{GATEUP_FLT}	-7	-13	-20	mA	$\Delta V_{GATE} = 2\text{ V}$

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
CURRENT SENSE VOLTAGE						
Sense Voltage Current Limit ($V_{SENSE+} - V_{SENSE-}$)	$V_{SENSECL}$	47	50	53	mV	$V_{ISET} > 2.65\text{ V}$, $V_{FLB} > 1.1\text{ V}$, $\Delta V_{GATE} = 3\text{ V}$, $I_{GATE} = 0\text{ }\mu\text{A}$
Foldback Inactive			62.5		mV	$V_{ISET} = 2.5\text{ V}$, $V_{FLB} > 1.35\text{ V}$, $\Delta V_{GATE} = 3\text{ V}$, $I_{GATE} = 0\text{ }\mu\text{A}$
		47	50	53	mV	$V_{ISET} = 2\text{ V}$, $V_{FLB} > 1.1\text{ V}$, $\Delta V_{GATE} = 3\text{ V}$, $I_{GATE} = 0\text{ }\mu\text{A}$
		22.5	25.0	27.5	mV	$V_{ISET} = 1\text{ V}$, $V_{FLB} > 0.57\text{ V}$, $\Delta V_{GATE} = 3\text{ V}$, $I_{GATE} = 0\text{ }\mu\text{A}$
Foldback Active		10.0	12.5	15.0	mV	$V_{ISET} = 0.5\text{ V}$, $V_{FLB} > 0.3\text{ V}$, $\Delta V_{GATE} = 3\text{ V}$, $I_{GATE} = 0\text{ }\mu\text{A}$
		7	10	13	mV	$V_{FLB} = 0\text{ V}$, $\Delta V_{GATE} = 3\text{ V}$, $I_{GATE} = 0\text{ }\mu\text{A}$
		22	25	28	mV	$V_{ISET} > 2\text{ V}$, $V_{FLB} = 0.5\text{ V}$, $\Delta V_{GATE} = 3\text{ V}$, $I_{GATE} = 0\text{ }\mu\text{A}$
Circuit Breaker Offset	V_{CBOS}	0.5	1	1.5	mV	Circuit breaker trip voltage, $V_{CB} = V_{SENSECL} - V_{CBOS}$
SEVERE OVERCURRENT						
Voltage Threshold	$V_{SENSEOC}$	90	100	110	mV	$V_{ISET} > 2.65\text{ V}$
		20	25	30	mV	$V_{ISET} = 0.5\text{ V}$
Glitch Filter Duration		0.4		1.6	μs	
Response Time			2.0	3.5	μs	
TIMER PIN						
TIMER Pull-Up Current	$I_{TIMERUP}$	-18	-20	-22	μA	Overcurrent fault, $0.2\text{ V} \leq V_{TIMER} \leq 2\text{ V}$
TIMER High Threshold	V_{TIMERH}	1.96	2.0	2.04	V	
TIMER Low Threshold	V_{TIMERL}	0.075	0.10	0.12	V	
TIMER Pull-Down Current	$I_{TIMERPD}$	0.85		1.15	μA	Timer pin voltage = 0.2 V
		75		105	μA	Timer pin voltage = 0.05 V
TIMER_OFF PIN						
Power-On Reset Pull-Up Current	I_{POR}	-18	-20	-22	μA	Initial power-on reset, $V_{TIMER_OFF} = 1\text{ V}$
Retry Pull-Up Current	I_{TMROFF}	-0.85	-1	-1.15	μA	After fault when GATE is off, $V_{TIMER_OFF} = 1\text{ V}$
TIMER_OFF High Threshold	$V_{TMROFFH}$	1.96	2.0	2.04	V	
FOLDBACK (FLB PIN)						
Input Current	I_{FLB}		0.005	0.2	μA	$V_{FLB} \leq 5.5\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$
			0.005	1	μA	$V_{FLB} \leq 5.5\text{ V}$, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$
PWRGD FEEDBACK INPUT (FB_PG PIN)						
Input Current	I_{FBPG}		0.005	0.2	μA	$V_{FB_PG} \leq 5.5\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$
			0.005	1	μA	$V_{FB_PG} \leq 5.5\text{ V}$, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$
PWRGD Rising Threshold	V_{PGTH}	0.985	1.0	1.015	V	FB_PG rising
PWRGD Threshold Hysteresis	PG_{HYST}	25	30	35	mV	
Power-Good Glitch Filter	PG_{GF}	0.5		1.5	μs	50 mV overdrive
FAULT PIN						
Output Low Voltage	V_{OL_FAULT}			0.1	V	$I_{FAULT} = 100\text{ }\mu\text{A}$
				0.4	V	$I_{FAULT} = 1\text{ mA}$
Leakage Current	I_{FAULT}		0.005	1	μA	$V_{FAULT} = 5.5\text{ V}$, FAULT output high-Z
ENABLE PIN						
Input High Voltage	V_{IH}	1.2			V	
Input Low Voltage	V_{IL}			0.4	V	
Leakage Current	I_{EN}		0.005	1	μA	$V_{EN} = 5.5\text{ V}$
PWRGD PIN						
Output Low Voltage	V_{OL_PWRGD}			0.1	V	$I_{PWRGD} = 100\text{ }\mu\text{A}$
				0.4	V	$I_{PWRGD} = 1\text{ mA}$
Output Low Voltage	V_{OL_PWRGD}			0.4	V	$V_{CC} = 1.7\text{ V}$, $I_{SINK} = 100\text{ }\mu\text{A}$,
Leakage Current	I_{PWRGD}		0.005	1	μA	$V_{PWRGD} = 60\text{ V}$, PWRGD output high-Z

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
VCC/SENSE+	-0.3 V to +66 V
VCAP	-0.3 V to +6 V
UV	-0.3 V to +6 V
OV	-0.3 V to +6 V
ISET	-0.3 V to VCAP + 0.3 V
FLB	-0.3 V to +6 V
FB_PG	-0.3 V to +6 V
TIMER_OFF	-0.3 V to VCAP + 0.3 V
TIMER	-0.3 V to VCAP + 0.3 V
FAULT	-0.3 V to +6 V
ENABLE	-0.3 V to +6 V
PWRGD	-0.3 V to +66 V
GATE	-0.3 V to V _{CC} + 0.3 V
GATE to VCC/SENSE+	-22 V to +0.3 V
SENSE-	-0.3 V to V _{CC} + 0.3 V
RPFPG	-0.3 V to V _{CC} + 0.3 V
RPFPG to VCC/SENSE+	-22 V to +0.3 V
V _{SENSE} (V _{SENSE+} - V _{SENSE-})	±0.3 V
Continuous Current into Any Pin	±10 mA
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	-40°C to +125°C
Lead Temperature, Soldering (10 sec)	300°C
Junction Temperature	150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL CHARACTERISTICS

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. Thermal Resistance

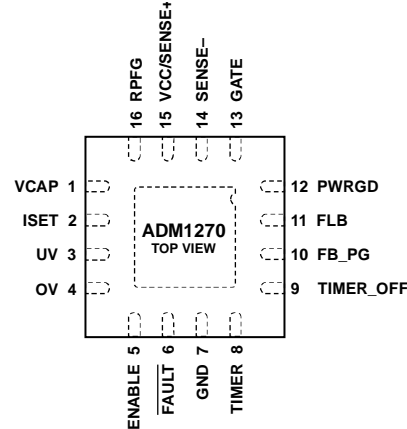
Package Type	θ_{JA}	θ_{JC}	Ψ_{JB}	Unit
16-Lead, 3 mm × 3 mm LFCSP	49.5	35.2	29.6	°C/W
16-Lead QSOP	106.03	28.31	43.22	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



NOTES
 1. THE EXPOSED PAD IS LOCATED ON THE UNDERSIDE OF THE LFCSP PACKAGE. SOLDER THE EXPOSED PAD TO THE PRINTED CIRCUIT BOARD (PCB) TO IMPROVE THERMAL DISSIPATION. THE EXPOSED PAD CAN BE CONNECTED TO GROUND.

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Figure 2. 16-Lead LFCSP Pin Configuration

Table 4. 16-Lead LFCSP Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VCAP	Internal Regulated Supply. Place a capacitor with a 1 μ F or greater value on this pin to maintain good accuracy. This pin can be used as a reference to program the ISET pin voltage.
2	ISET	Current Limit. This pin allows the current-limit threshold to be programmed. The default limit is set when this pin is connected directly to VCAP. To achieve a user defined sense voltage, the current limit can be adjusted using a resistor divider from VCAP. An external reference can also be used.
3	UV	Undervoltage Input Pin. An external resistor divider is connected from the supply to this pin to allow an internal comparator to detect whether the supply is under the UV limit.
4	OV	Overvoltage Input Pin. An external resistor divider is connected from the supply to this pin to allow an internal comparator to detect whether the supply is above the OV limit.
5	ENABLE	Enable Pin. This pin is a digital logic input. This input must be high to allow the ADM1270 controller to begin a power-up sequence. If this pin is held low, the ADM1270 is prevented from powering up. There is no internal pull-up on this pin.
6	FAULT	Fault Output. This pin indicates that the device has shut down due to an overcurrent fault condition. The device can be configured for automatic retry after shutdown by connecting this pin directly to the ENABLE pin.
7	GND	Ground Pin.
8	TIMER	Timer Pin. An external capacitor, C_{TIMER} , sets an SOA overcurrent fault delay. The GATE pin is pulled off when the voltage on the TIMER pin exceeds the upper threshold.
9	TIMER_OFF	Timer Off Pin. An external capacitor, $C_{\text{TIMER_OFF}}$, sets an initial timing cycle delay and the SOA off time delay. After an SOA overcurrent fault has occurred, the GATE pin is pulled off until the voltage on the TIMER_OFF pin exceeds the threshold.
10	FB_PG	PWRGD Feedback Input Pin. An external resistor divider is connected from the output voltage to this pin to allow an internal comparator to detect when the output voltage is above the PWRGD threshold.
11	FLB	Foldback Pin. A foldback resistor divider is placed from the source of the FET to this pin. Foldback reduces the current limit when the source voltage drops. The foldback feature ensures that the power through the FET is not increased beyond the SOA limits.
12	PWRGD	Power-Good Signal. This signal indicates that the supply is within tolerance. This signal is based on the voltage present on the FB_PG pin.
13	GATE	Gate Output Pin. This pin is the gate drive of an external P-channel FET. This pin is driven by the FET drive controller, which provides a pull-down current to charge the FET gate pin. The FET drive controller regulates to a maximum load current by regulating the GATE pin. GATE is held off when the supply is below the undervoltage lockout (UVLO).
14	SENSE-	Negative Current Sense Input Pin. A sense resistor between the VCC/SENSE+ pin and the SENSE- pin sets the analog current limit. The hot swap operation of the ADM1270 controls the external FET gate to maintain the sense voltage ($V_{\text{SENSE+}} - V_{\text{SENSE-}}$). This pin also connects to the FET drain pin.

Pin No.	Mnemonic	Description
15	VCC/SENSE+	Positive Supply Input Pin (VCC). A UVLO circuit resets the device when a low supply voltage is detected. GATE is held off when the supply is below UVLO. No sequencing is required. Positive Current Sense Input Pin (SENSE+). This pin connects to the main supply input. A sense resistor between the VCC/SENSE+ pin and the SENSE- pin sets the analog current limit. The hot swap operation of the ADM1270 controls the external FET gate to maintain the sense voltage ($V_{\text{SENSE+}} - V_{\text{SENSE-}}$).
16	RPFG	Reverse Protection FET Gate Driver Output. Connect this pin to the gate of the external reverse polarity protection P-channel FET for low voltage drop operation.
N/A ¹	EP	Exposed Pad. The exposed pad is located on the underside of the LFCSP package. Solder the exposed pad to the printed circuit board (PCB) to improve thermal dissipation. The exposed pad can be connected to ground.

¹ N/A = not applicable.

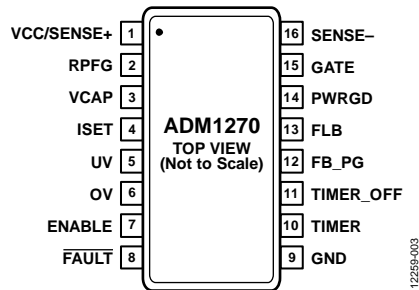


Figure 3. 16-Lead QSOP Pin Configuration

Table 5. 16-Lead QSOP Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VCC/SENSE+	Positive Supply Input Pin (VCC). A UVLO circuit resets the device when a low supply voltage is detected. GATE is held off when the supply is below UVLO. No sequencing is required. Positive Current Sense Input Pin (SENSE+). This pin connects to the main supply input. A sense resistor between the VCC/SENSE+ pin and the SENSE– pin sets the analog current limit. The hot swap operation of the ADM1270 controls the external FET gate to maintain the sense voltage ($V_{SENSE+} - V_{SENSE-}$).
2	RPFG	Reverse Protection FET Gate Driver Output. Connect this pin to the gate of the external reverse polarity protection P-channel FET for low voltage drop operation.
3	VCAP	Internal Regulated Supply. Place a capacitor with a 1 μ F or greater value on this pin to maintain good accuracy. This pin can be used as a reference to program the ISET pin voltage.
4	ISET	Current Limit. This pin allows the current-limit threshold to be programmed. The default limit is set when this pin is connected directly to VCAP. To achieve a user defined sense voltage, the current limit can be adjusted using a resistor divider from VCAP. An external reference can also be used.
5	UV	Undervoltage Input Pin. An external resistor divider is connected from the supply to this pin to allow an internal comparator to detect whether the supply is under the UV limit.
6	OV	Overvoltage Input Pin. An external resistor divider is connected from the supply to this pin to allow an internal comparator to detect whether the supply is above the OV limit.
7	ENABLE	Enable Pin. This pin is a digital logic input. This input must be high to allow the ADM1270 controller to begin a power-up sequence. If this pin is held low, the ADM1270 is prevented from powering up. There is no internal pull-up on this pin.
8	FAULT	Fault Output. This pin indicates that the device has shut down due to an overcurrent fault condition. The device can be configured for automatic retry after shutdown by connecting this pin directly to the ENABLE pin.
9	GND	Ground Pin.
10	TIMER	Timer Pin. An external capacitor, C_{TIMER} , sets an SOA overcurrent fault delay. The GATE pin is pulled off when the voltage on the TIMER pin exceeds the upper threshold.
11	TIMER_OFF	Timer Off Pin. An external capacitor, C_{TIMER_OFF} , sets an initial timing cycle delay and the SOA off time delay. After an SOA overcurrent fault has occurred, the GATE pin is pulled off until the voltage on the TIMER_OFF pin exceeds the threshold.
12	FB_PG	PWRGD Feedback Input Pin. An external resistor divider is connected from the output voltage to this pin to allow an internal comparator to detect when the output voltage is above the PWRGD threshold.
13	FLB	Foldback Pin. A foldback resistor divider is placed from the source of the FET to this pin. Foldback reduces the current limit when the source voltage drops. The foldback feature ensures that the power through the FET is not increased beyond the SOA limits.
14	PWRGD	Power-Good Signal. This signal indicates that the supply is within tolerance. This signal is based on the voltage present on the FB_PG pin.
15	GATE	Gate Output Pin. This pin is the gate drive of an external P-channel FET. This pin is driven by the FET drive controller, which provides a pull-down current to charge the FET gate pin. The FET drive controller regulates to a maximum load current by regulating the GATE pin. GATE is held off when the supply is below UVLO.
16	SENSE–	Negative Current Sense Input Pin. A sense resistor between the VCC/SENSE+ pin and the SENSE– pin sets the analog current limit. The hot swap operation of the ADM1270 controls the external FET gate to maintain the sense voltage ($V_{SENSE+} - V_{SENSE-}$). This pin also connects to the FET drain pin.

TYPICAL PERFORMANCE CHARACTERISTICS



Figure 4. $V_{V_{CAP}}$ vs. Junction Temperature (T_J), Different Loads

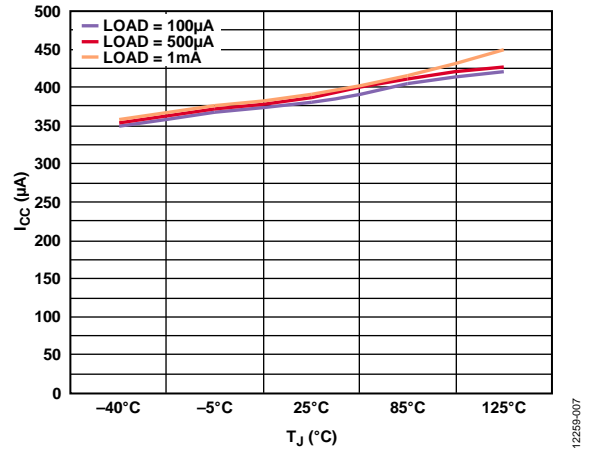


Figure 7. Supply Current (I_{CC}) vs. Junction Temperature (T_J), Different Loads



Figure 5. $V_{V_{CAP}}$ vs. Load Current (I_{LOAD})



Figure 8. Supply Current (I_{CC}) vs. Load Current (I_{LOAD})



Figure 6. $V_{V_{CAP}}$ vs. Input Voltage (V_{IN}), Different Loads

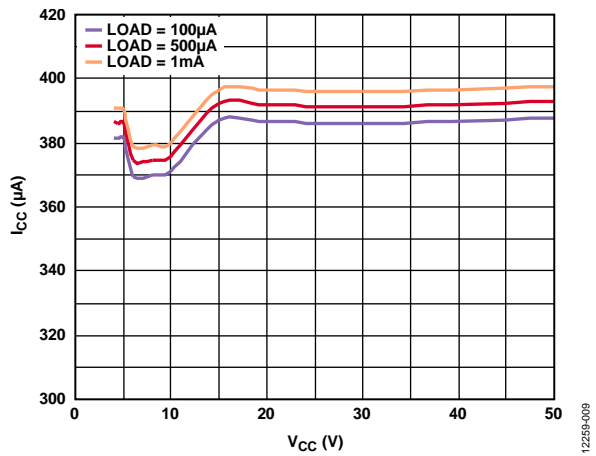


Figure 9. Supply Current (I_{CC}) vs. Supply Voltage (V_{CC}), Different Loads

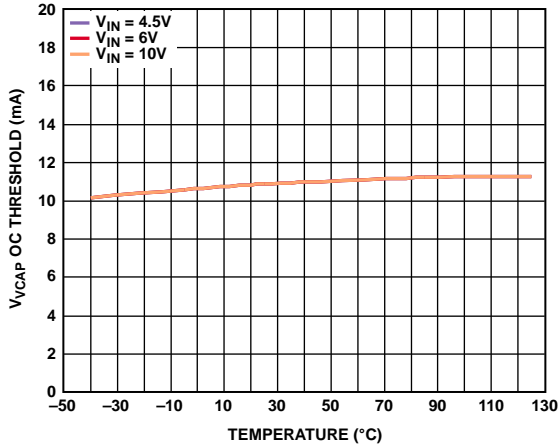


Figure 10. V_{VCAP} Overcurrent (OC) Threshold vs. Temperature, Different Input Voltages

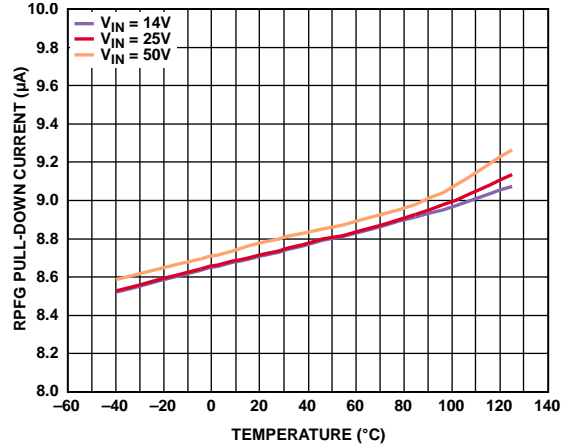


Figure 13. RPFG Pull-Down Current (I_{RPFGND}) vs. Temperature, Different Input Voltages

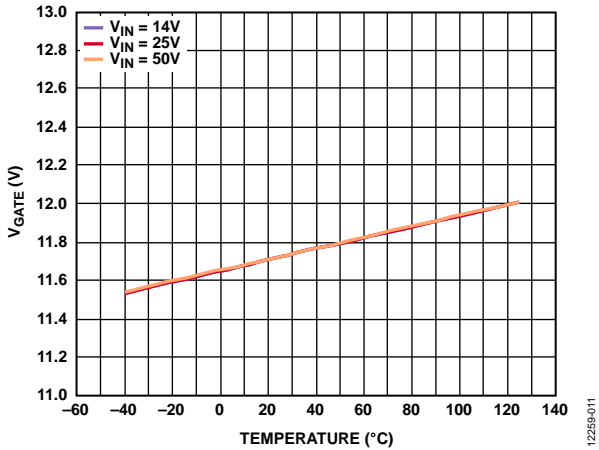


Figure 11. GATE Voltage (V_{GATE}) vs. Temperature, Different Input Voltages

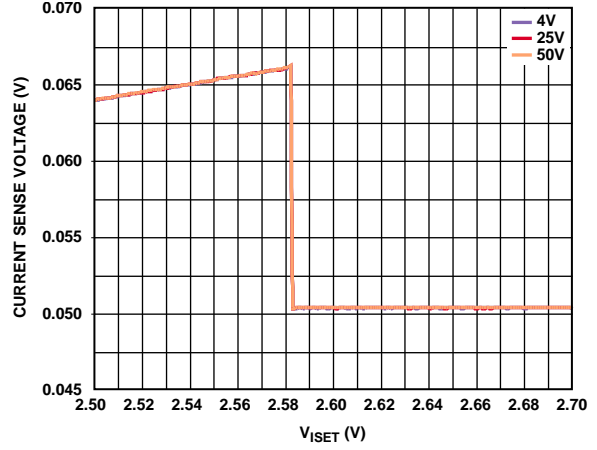


Figure 14. Current Sense Voltage vs. ISET Voltage (V_{ISET}), Different Input Voltages

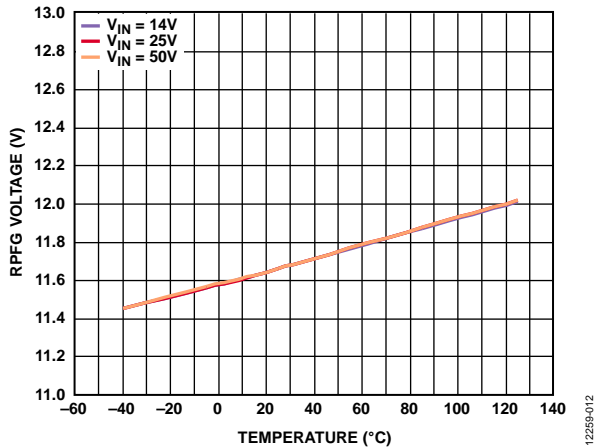


Figure 12. RPFG Voltage (V_{RPFG}) vs. Temperature, Different Input Voltages

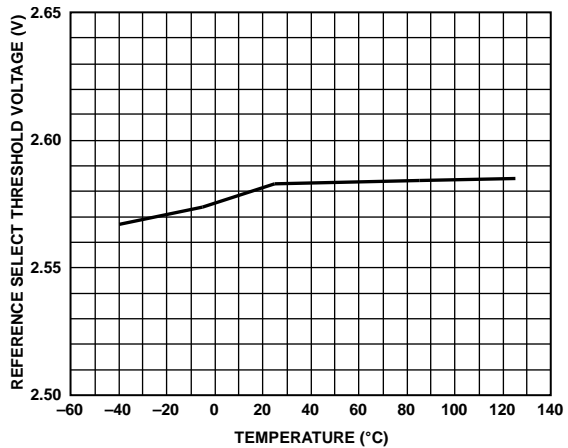


Figure 15. Reference Select Threshold Voltage (V_{ISETRSTH}) vs. Temperature, V_{IN} = 4V

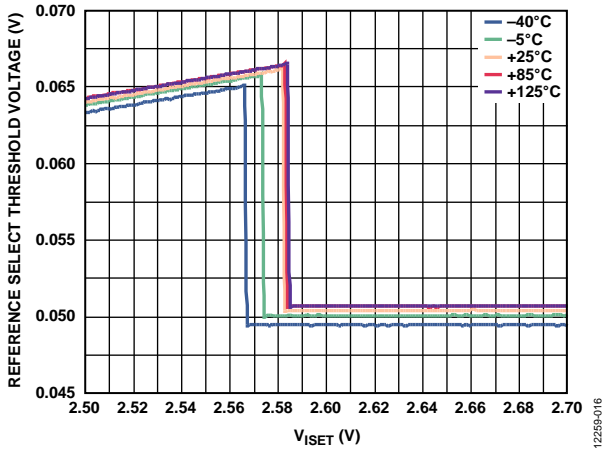


Figure 16. Reference Select Threshold Voltage ($V_{ISETRSTH}$) vs. $ISET$ Voltage (V_{ISET}), Different Temperatures

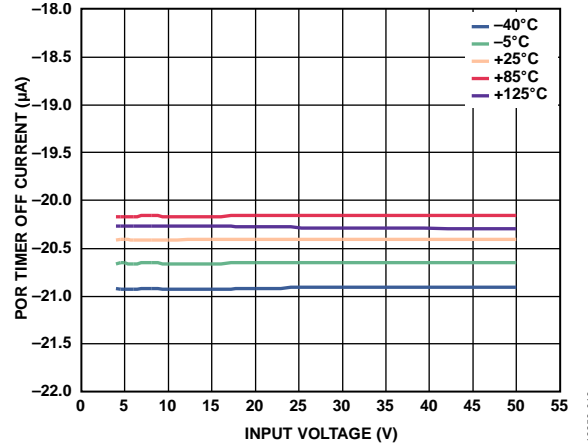


Figure 19. POR Timer Off Current (I_{POR}) vs. Input Voltage (V_{IN}), Different Temperatures

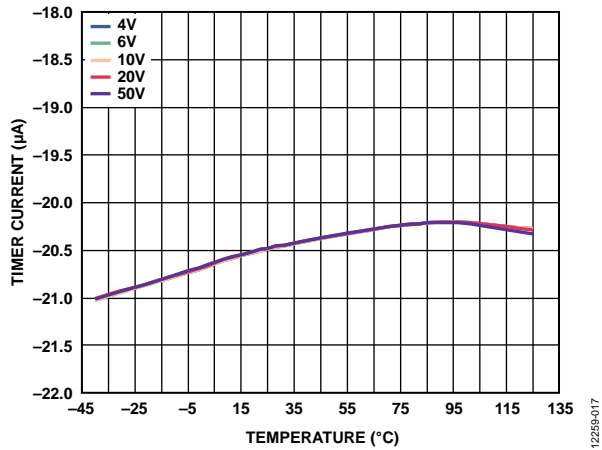


Figure 17. Timer Current vs. Temperature, Different Input Voltages

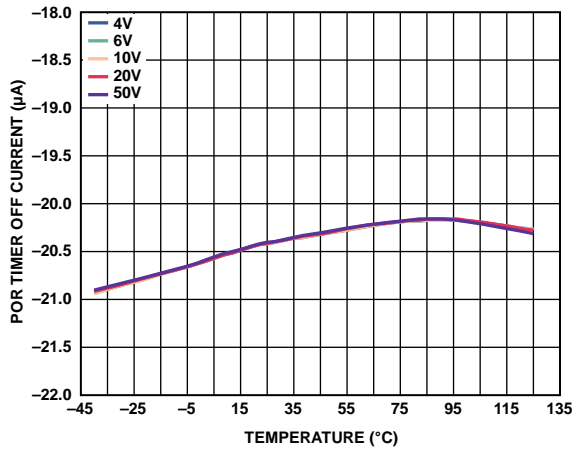


Figure 20. POR Timer Off Current (I_{POR}) vs. Temperature, Different Input Voltages

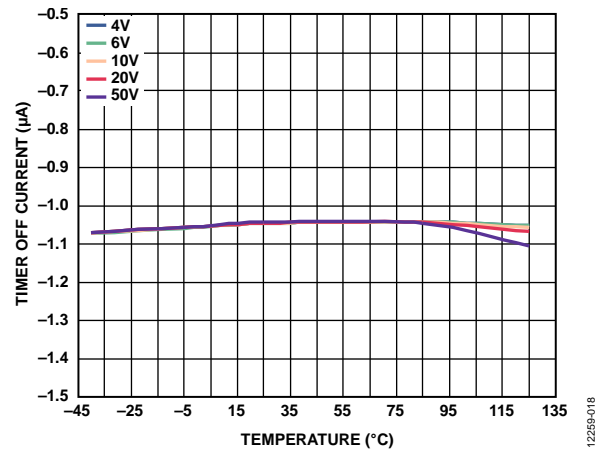


Figure 18. Timer Off Current ($I_{TMR OFF}$) vs. Temperature, Different Input Voltages

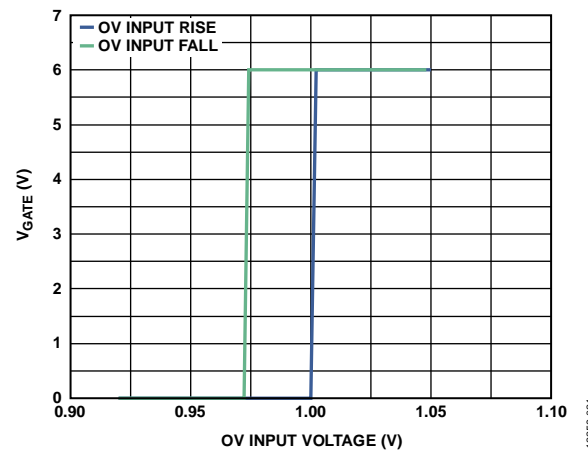


Figure 21. V_{GATE} vs. OV Input Voltage



Figure 22. UV Threshold Voltage vs. Temperature



Figure 25. Power-Good Falling Threshold vs. Temperature, Different Input Voltages



Figure 23. OV Threshold vs. Temperature



Figure 26. Severe Overcurrent (OC) Threshold vs. Temperature, Different Input Voltages



Figure 24. Power-Good Rising Threshold vs. Temperature, Different Input Voltages



Figure 27. Sense Voltage (V_{SENSE}) vs. FLB, Different Temperatures

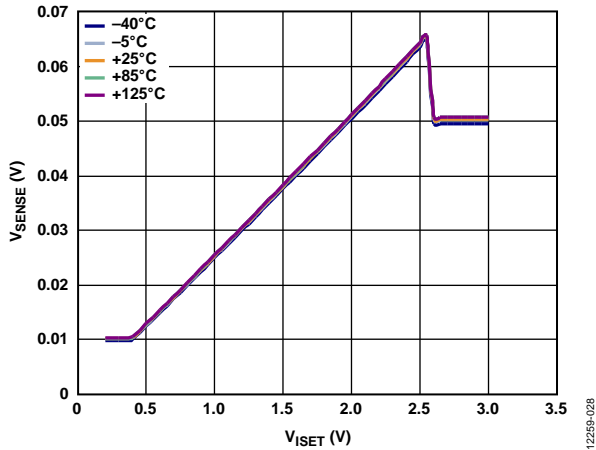


Figure 28. Sense Voltage (V_{SENSE}) vs. ISET Voltage (V_{ISET}), Different Temperatures

12259-028



Figure 31. OC TIMER Threshold vs. Temperature, Different Input Voltages

12259-031

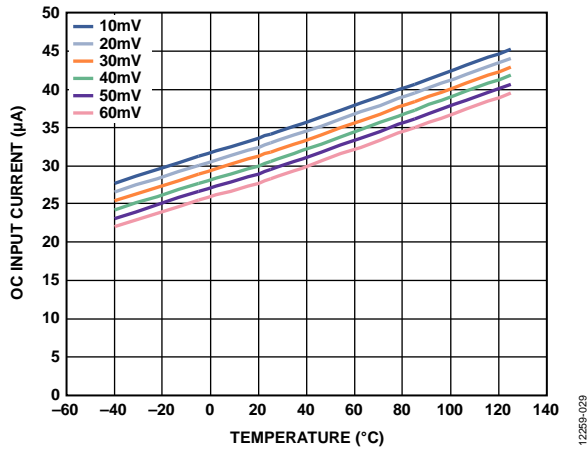


Figure 29. OC Input Current vs. Temperature, Different Sense Voltages (V_{SENSE})

12259-029

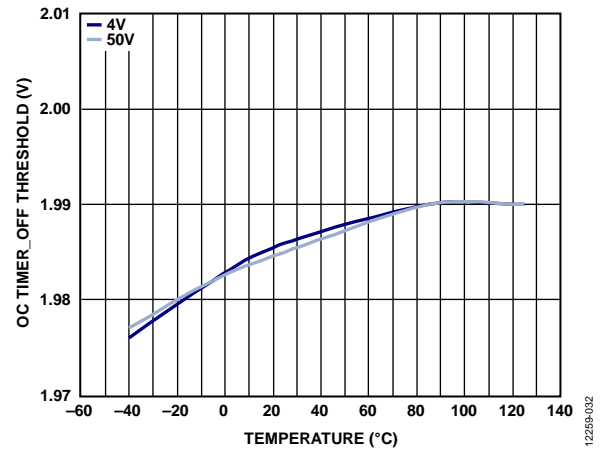


Figure 32. OC TIMER_OFF Threshold vs. Temperature, Different Input Voltages

12259-032

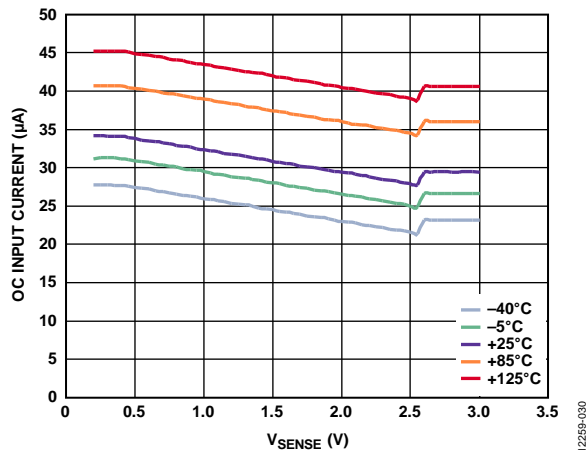


Figure 30. OC Input Current vs. Sense Voltage (V_{SENSE}), Different Temperatures

12259-030

TYPICAL APPLICATION CIRCUIT



Figure 33. Typical Application Circuit

12259-033

POWERING THE ADM1270

A supply voltage from 4 V to 60 V is required to power the ADM1270 via the VCC/SENSE+ pin. The VCC/SENSE+ pin provides the majority of the bias current for the device; the remainder of the current needed to control the gate drive and to best regulate the gate to source voltage (V_{GS}) is supplied by the SENSE- pin.

CURRENT SENSE INPUTS

The load current is monitored by measuring the voltage drop across an external current sense resistor, R_{SENSE} (see Figure 35). An internal current sense amplifier provides a gain of 40 to the voltage drop detected across R_{SENSE-} . The result is compared to an internal reference and is used by the hot swap control logic to detect an overcurrent condition.



Figure 35. Hot Swap Current Sense Amplifier

CURRENT-LIMIT REFERENCE

The current-limit reference voltage determines the load current at which the ADM1270 limits the current during an overcurrent event. This reference voltage is compared to the amplified current sense voltage to determine when the current-limit threshold is reached.

An internal current-limit reference selector block continuously compares the ISET and FLB voltages to determine which voltage is the lowest at any given time; the lowest voltage is used as the current-limit reference. This behavior ensures that the programmed current limit, ISET, is used in normal operation, and that the foldback feature reduces the current limit when required during startup and/or fault conditions.

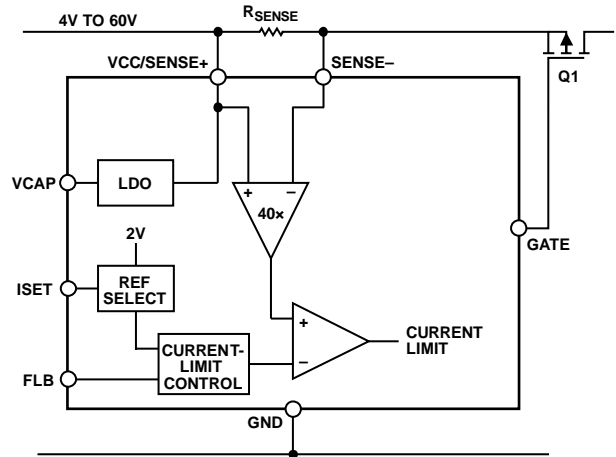


Figure 36. Current-Limit Reference Selection

The FLB voltage varies during different modes of operation and, therefore, is clamped to a minimum level of 200 mV. This behavior prevents zero current flow due to the current limit being set too low. Figure 37 provides an example of how the FLB and ISET voltages interact during startup as the ADM1270 turns on the FET and charges the load capacitance. Depending on how the foldback feature is configured, the transition point varies to ensure that the FET operates within the correct limits.

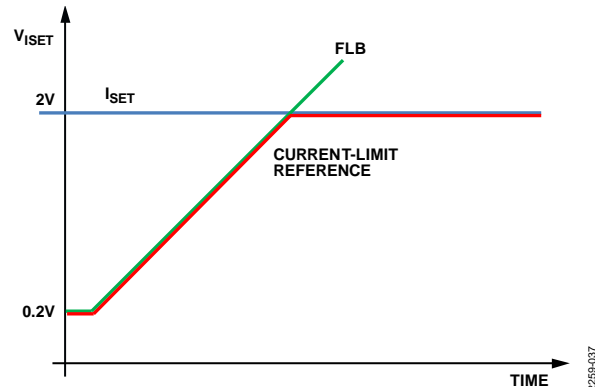


Figure 37. Interaction of Foldback (FLB) and ISET Current Limits

SETTING THE CURRENT LIMIT (ISET)

The maximum current limit is partially determined by selecting a sense resistor to match the current sense voltage limit on the controller for the desired load current. However, as currents become larger, the sense resistor value decreases for a given current sense voltage. Choosing an appropriate current sense resistor can be difficult due to the limited selection of low value resistors. The ADM1270 provides an adjustable current sense voltage limit to handle this issue. The device allows the user to program the required current sense voltage limit from 12.5 mV to 62.5 mV.

When the voltage across the sense resistor reaches the circuit breaker trip voltage, V_{CB} , the 20 μA TIMER pull-up current is activated. The ADM1270 begins to regulate the load current at the current limit, initiating a rising voltage ramp on the TIMER pin. If the sense voltage falls below this circuit breaker trip voltage before the TIMER pin reaches V_{TIMERH} , the 20 μA pull-up current is disabled, and the 1 μA pull-down current is enabled. If the voltage on the TIMER pin falls below V_{TIMERL} , the TIMER pin is discharged to GND using a strong pull-down current on the TIMER pin.

However, if the overcurrent condition is continuous and the sense voltage remains above the circuit breaker trip voltage, the 20 μA pull-up current remains active, and the FET remains in regulation. This condition allows the TIMER pin to reach V_{TIMERH} and to initiate the GATE shutdown, and the FAULT pin is pulled low immediately.

The circuit breaker trip voltage is not the same as the hot swap sense voltage current limit. There is a small circuit breaker offset, V_{CBOS} , which causes the timer to start shortly before the current reaches the defined current limit.

In latch-off mode, the TIMER pin is discharged to GND when it reaches the V_{TIMERH} threshold. The TIMER_OFF pin begins to charge up. While the TIMER_OFF pin is ramping up, the hot swap controller remains off and cannot be turned back on, and the FAULT pin remains low. When the voltage on the TIMER_OFF pin rises above the $V_{TMROFFH}$ threshold, the hot swap controller can be reenabled by toggling the ENABLE pin from high to low and then high again.

TIMER_OFF

The TIMER_OFF pin handles two timing functions with an external capacitor, C_{TIMER_OFF} . There is one TIMER_OFF pin comparator threshold at $V_{TMROFFH}$ (2.0 V). There are two timing current sources, a 20 μA pull-up current and a 1 μA pull-up current.

These current and voltage levels, in combination with the user chosen value of C_{TIMER_OFF} , determine the initial power-on reset time and also set the fault current-limit off time.

When VCC is connected to the input supply, the internal supply (VCAP) of the ADM1270 must charge up. VCAP starts up and settles in a very short time. When the UVLO threshold voltage is exceeded at VCAP, the device emerges from reset. During this first brief reset period, the GATE and TIMER pins are both held low.

The ADM1270 then proceeds through an initial timing cycle. The TIMER_OFF pin is pulled high with 20 μA . When the TIMER_OFF pin reaches the $V_{TMROFFH}$ threshold (2.0 V), the initial timing cycle is complete. This initial power-on reset duration is determined by the following equation:

$$t_{INITIAL} = V_{TMROFFH} \times (C_{TIMER_OFF}/20 \mu\text{A})$$

For example, a 100 nF capacitor results in a delay of approximately 10 ms. If the UV and OV inputs indicate that VCC is within the

defined window of operation when the initial timing cycle terminates, the device is ready to start a hot swap operation.

At the completion of this initial power-on reset cycle, the TIMER_OFF pin is ready to perform a second function. When the voltage at the TIMER pin exceeds the fault current-limit time threshold voltage of V_{TIMERH} (2.0 V), the 1 μA pull-up current is activated on TIMER_OFF, and C_{TIMER_OFF} begins to charge initiating a voltage ramp on the TIMER_OFF pin. When the TIMER_OFF pin reaches $V_{TMROFFH}$, the TIMER_OFF fault current-limit off time is complete.

This fault current-limit off time is determined by the following equation:

$$t_{TIMER_OFF} = V_{TMROFFH} \times (C_{TIMER_OFF}/1 \mu\text{A})$$

For example, a 100 nF capacitor results in an off time of approximately 200 ms from the time that TIMER exceeds V_{TIMERH} to the time that TIMER_OFF reaches $V_{TMROFFH}$.

HOT SWAP RETRY DUTY CYCLE

The ADM1270 turns off the FET after an overcurrent fault and then uses the capacitor on the TIMER_OFF pin to generate a delay before automatically retrying the hot swap operation. To configure the ADM1270 for automatic retry mode, tie the FAULT pin to the ENABLE pin. Note that a pull-up resistor to VCAP is required on the FAULT pin.

When an overcurrent fault occurs, the capacitor on the TIMER pin charges with a 20 μA pull-up current. When the TIMER pin reaches V_{TIMERH} (2.0 V), the GATE pin is pulled high, turning off the FET. When the FAULT pin is tied to the ENABLE pin for automatic retry mode, the TIMER_OFF pin begins to charge with a 1 μA current source. When the TIMER_OFF pin reaches $V_{TMROFFH}$ (2.0 V), the ADM1270 automatically restarts the hot swap operation.

The automatic retry duty cycle is set by the ratio of 1 $\mu\text{A}/20 \mu\text{A}$ and the ratio of C_{TIMER}/C_{TIMER_OFF} . The retry duty cycle is set by the following equation:

$$Duty_Cycle = (C_{TIMER} \times 1 \mu\text{A}) / (C_{TIMER_OFF} \times 20 \mu\text{A})$$

The value of the C_{TIMER} and C_{TIMER_OFF} capacitors determine the on and off time of this cycle, which are calculated as follows:

$$t_{ON} = V_{TIMERH} \times (C_{TIMER}/20 \mu\text{A})$$

$$t_{OFF} = V_{TMROFFH} \times (C_{TIMER_OFF}/1 \mu\text{A})$$

A 100 nF capacitor on the TIMER pin gives an on time of 10 ms. A 100 nF capacitor on the TIMER_OFF pin gives an off time of 200 ms. The device retries continuously in this manner and can be disabled manually by holding the ENABLE pin low, or by disconnecting the FAULT pin. To prevent thermal stress in the FET, a capacitor on the TIMER_OFF pin can be used to extend the retry time to any desired level.

POWER GOOD

The power-good (PWRGD) output can be used to indicate whether the output voltage exceeds a user defined threshold and can, therefore, be considered good. The PWRGD output is set by a resistor divider connected to the FB_PG pin (see Figure 42).



Figure 42. Generation of PWRGD Signal

When the voltage at the FB_PG pin exceeds the 1 V threshold (indicating that the output voltage has risen), the open-drain pull-down current is disabled, allowing PWRGD to be pulled high. The PWRGD pin is an open-drain output that pulls low when the voltage at the FB_PG pin is lower than the 1 V threshold minus the hysteresis (power bad). Hysteresis on the FB_PG pin is fixed at 30 mV. PWRGD is guaranteed to be in a valid state for $V_{CC} \geq 1.7$ V.

Calculate the power-good threshold using the following equation:

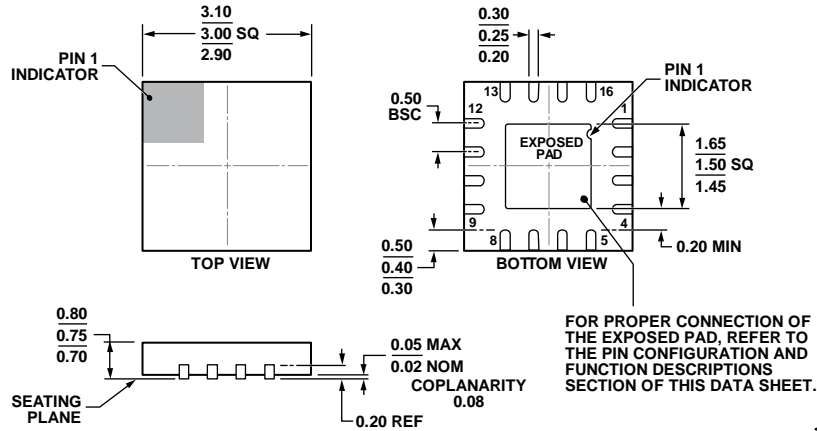
$$V_{PWRGD} = 1\text{ V} \times (1 + RPG1/RPG2)$$

where:

RPG1 is the resistance from V_{OUT} to FB_PG.

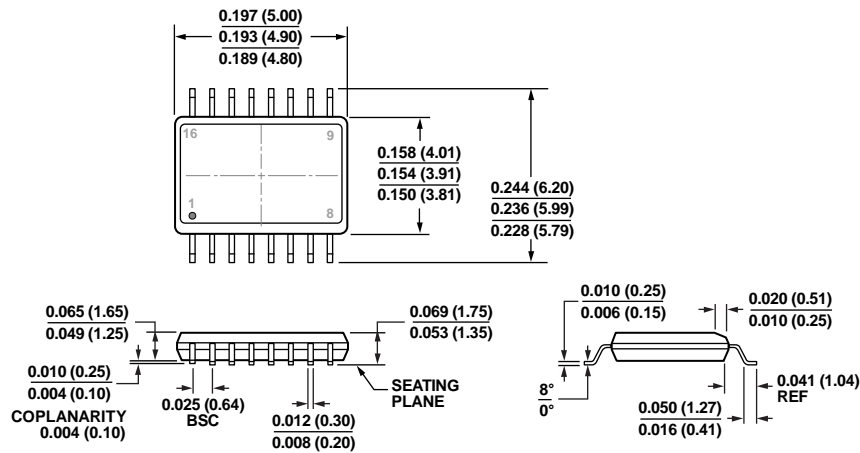
RPG2 is the resistance from FB_PG to GND.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WEED-6.

Figure 43. 16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
3 mm x 3 mm Body, Very, Very Thin Quad
(CP-16-27)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-137-AB

CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 44. 16-Lead Body, Shrink Small Outline Package [QSOP]
(RQ-16)
Dimensions shown in inches (and millimeters)

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option	Brand Code
ADM1270ACPZ-R2	-40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-16-27	LNQ
ADM1270ACPZ-R7	-40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-16-27	LNQ
ADM1270ARQZ	-40°C to +125°C	16-Lead Body, Shrink Small Outline Package [QSOP]	RQ-16	
ADM1270ARQZ-R7	-40°C to +125°C	16-Lead Body, Shrink Small Outline Package [QSOP]	RQ-16	
ADM1270CP-EVALZ		Evaluation Board for 16-Lead LFCSP_WQ		
ADM1270RQ-EVALZ		Evaluation Board for 16-Lead QSOP		

¹ Z = RoHS Compliant Part.



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- Поставка сложных, дефицитных, либо снятых с производства позиций;
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- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
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- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



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