



CPH5541 — PNP/NPN Epitaxial Planar Silicon Transistors

Push-Pull Circuit Applications

Applications

- MOSFET gate drivers, relay drivers, lamp drivers, motor drivers

Features

- Composite type with a PNP transistor and an NPN transistor contained in one package, facilitating high-density mounting
- Ultrasmall package facilitate miniaturization in end products. (0.9mm mounting height)

Specifications () : PNP

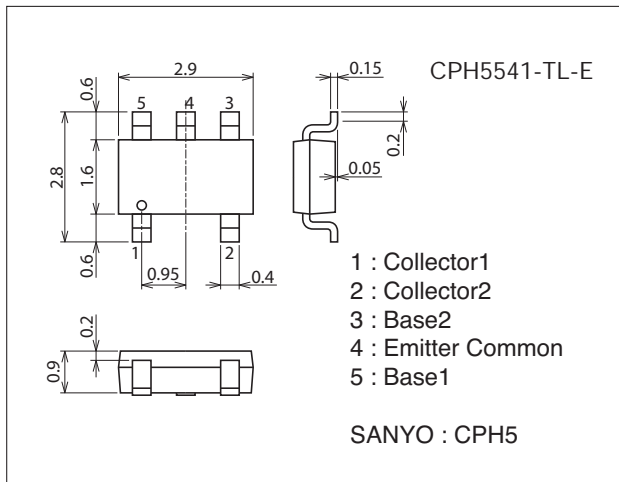
Absolute Maximum Ratings at Ta=25°C

Parameter	Symbol	Conditions	Ratings	Unit
Collector-to-Base Voltage	V _{CB0}		(-30)40	V
Collector-to-Emitter Voltage	V _{CEO}		(-30)	V
Emitter-to-Base Voltage	V _{EB0}		(-5)	V
Collector Current	I _C		(-)700	mA
Collector Current (Pulse)	I _{CP}	PW≤10μs	(-)3	A
Collector Dissipation	P _C	Mounted on a ceramic board (600mm ² ×0.8mm)	0.6	W
Junction Temperature	T _J		150	°C
Storage Temperature	T _{stg}		-55 to +150	°C

Package Dimensions

unit : mm (typ)

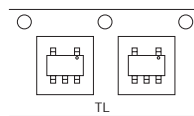
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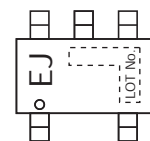
Product & Package Information

- Package : CPH5
- JEITA, JEDEC : SC-74A, SOT-25
- Minimum Packing Quantity : 3,000 pcs./reel

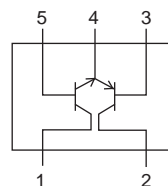
Packing Type : TL



Marking



Electrical Connection

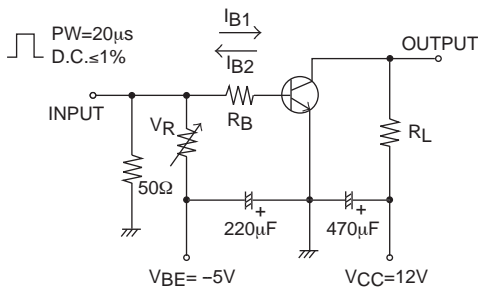


CPH5541

Electrical Characteristics at Ta=25°C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Collector Cutoff Current	I_{CBO}	$V_{CB} = (-)30V, I_E = 0A$			(-)100	nA
Emitter Cutoff Current	I_{EBO}	$V_{EB} = (-)4V, I_C = 0A$			(-)100	nA
DC Current Gain	h_{FE}	$V_{CE} = (-)2V, I_C = (-)50mA$	(200)300		(500)800	
Gain-Bandwidth Product	f_T	$V_{CE} = (-)2V, I_C = (-)50mA$		(520)540		MHz
Output Capacitance	C_{ob}	$V_{CB} = (-)10V, f = 1MHz$		(4.7)3.3		pF
Collector-to-Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C = (-)200mA, I_B = (-)10mA$		(-110)85	(-220)190	mV
Base-to-Emitter Saturation Voltage	$V_{BE(sat)}$	$I_C = (-)200mA, I_B = (-)10mA$		(-)0.9	(-)1.2	V
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = (-)10\mu A, I_E = 0A$	(-30)40			V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = (-)1mA, R_{BE} = \infty$	(-)30			V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = (-)10\mu A, I_C = 0A$	(-)5			V
Turn-On Time	t_{on}	See specified Test Circuit.		35		ns
Storage Time	t_{stg}			(125)255		ns
Fall Time	t_f			(25)40		ns

Switching Time Test Circuit

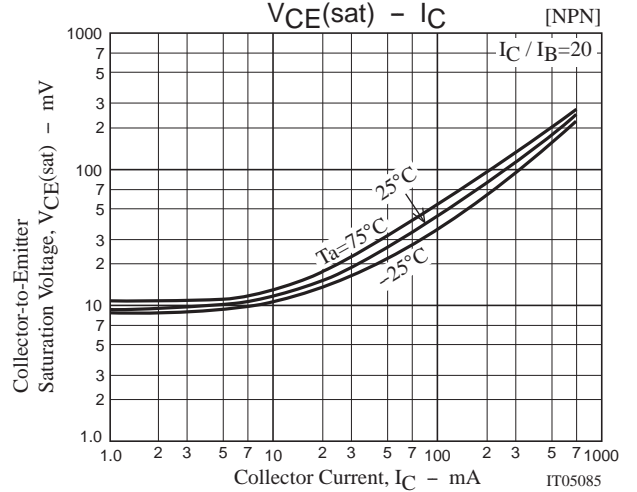
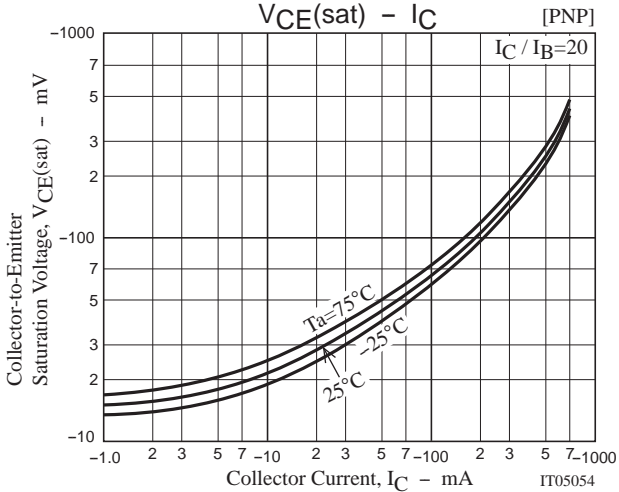
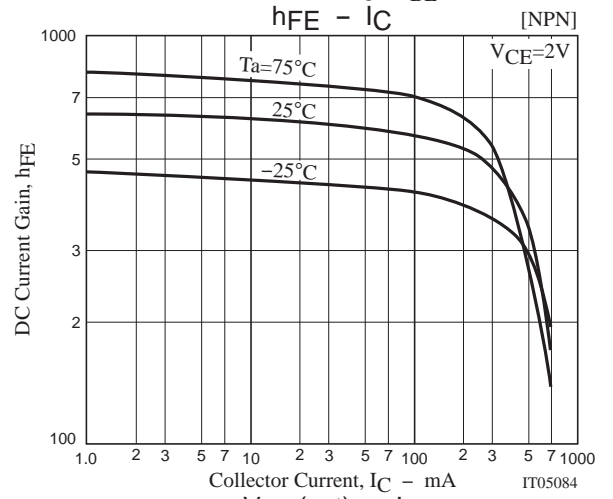
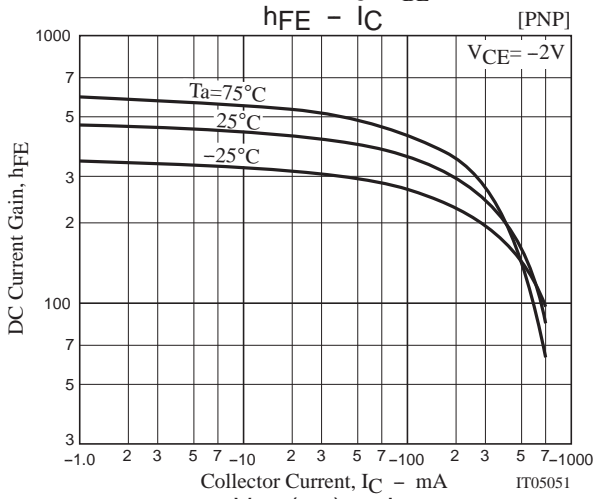
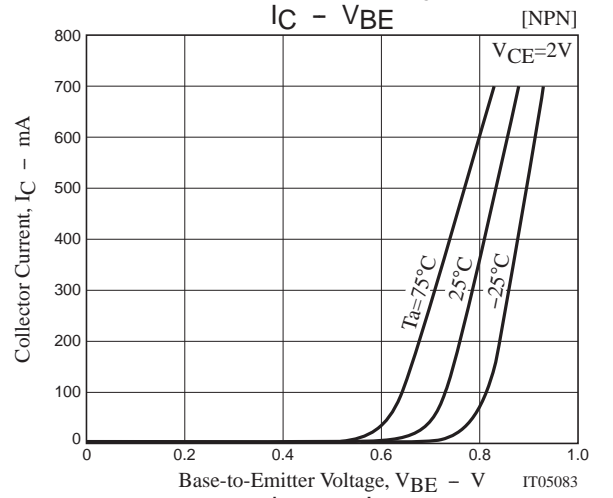
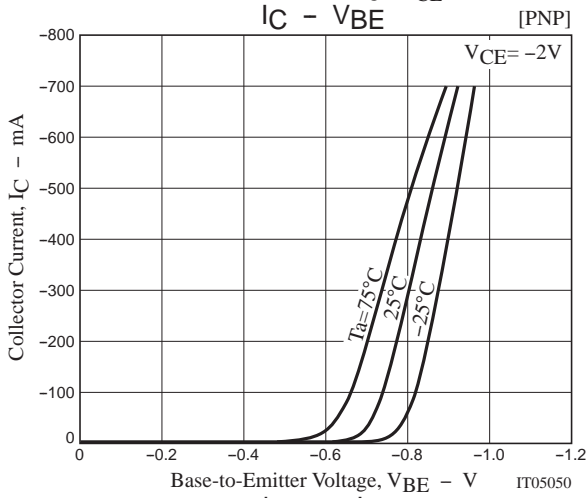
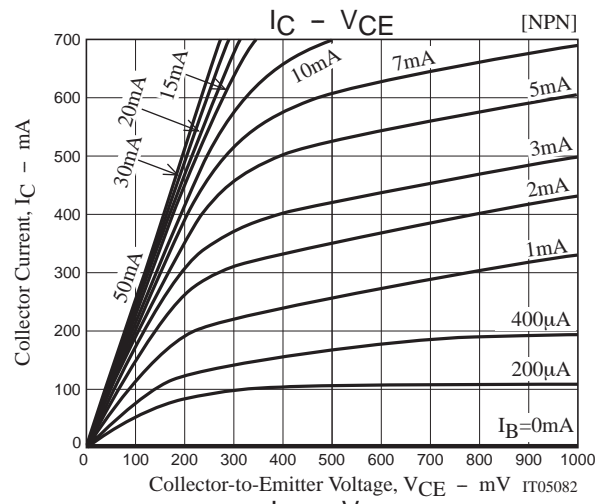
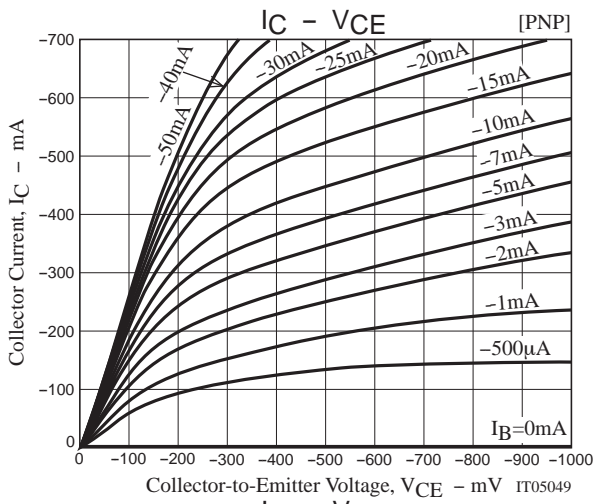


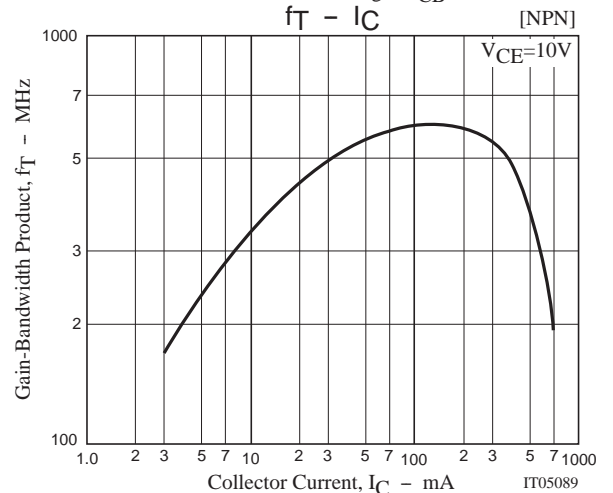
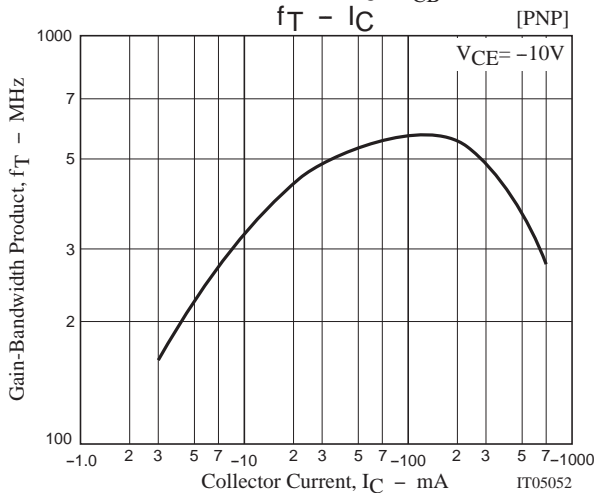
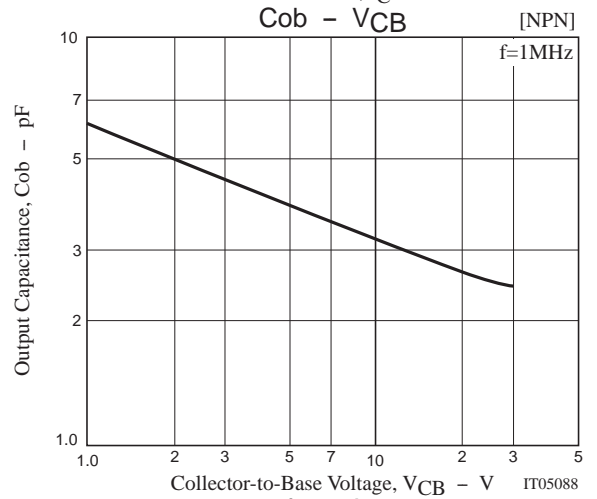
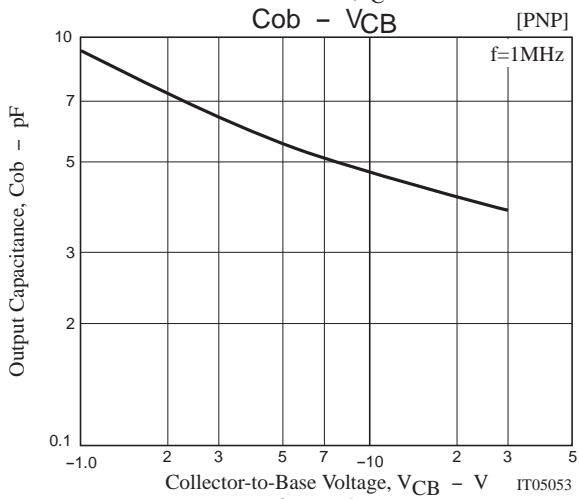
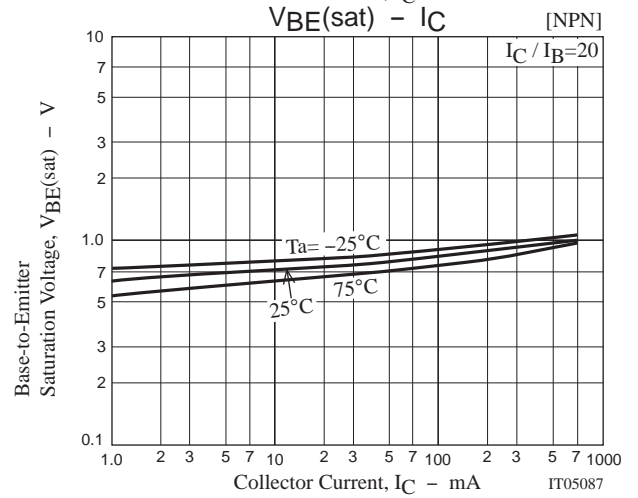
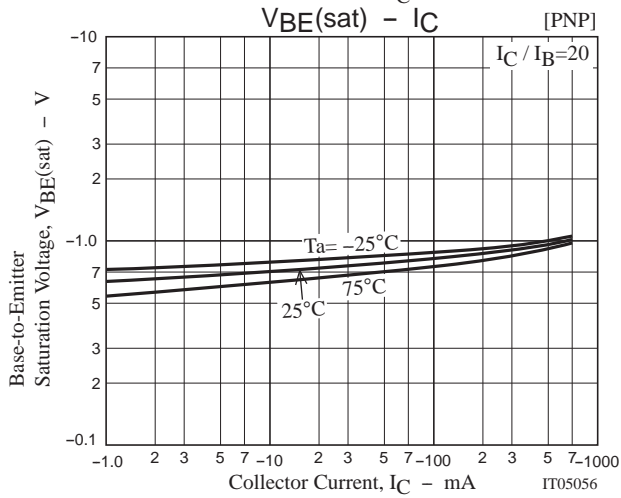
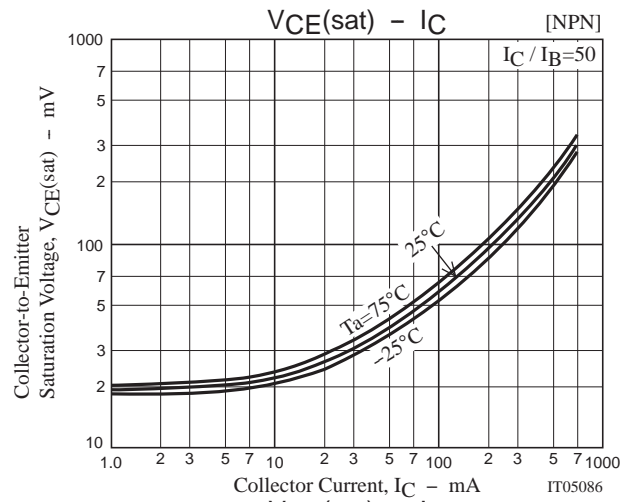
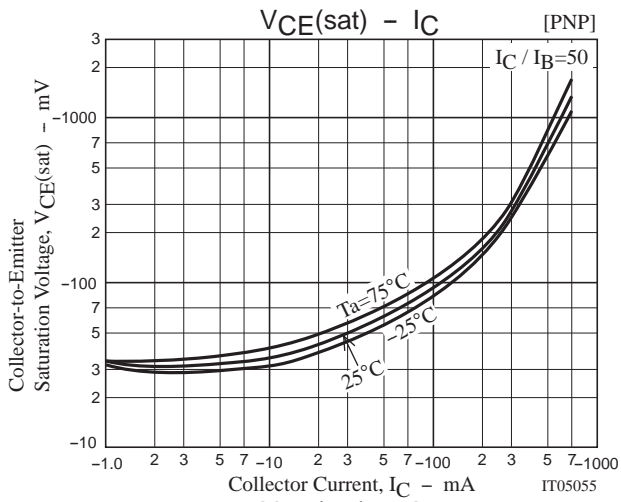
$$20I_{B1} = -20I_{B2} = I_C = 300mA$$

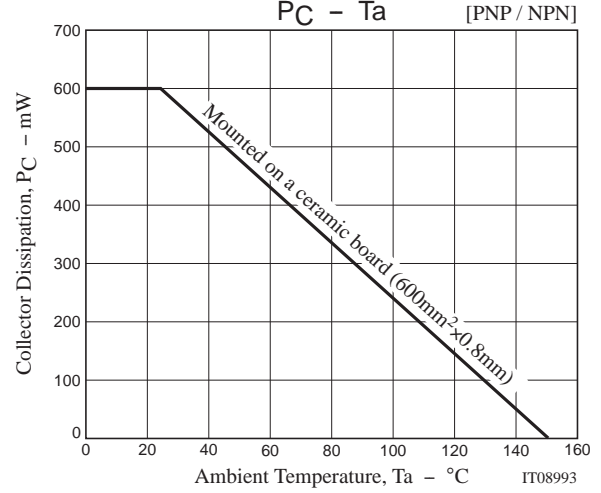
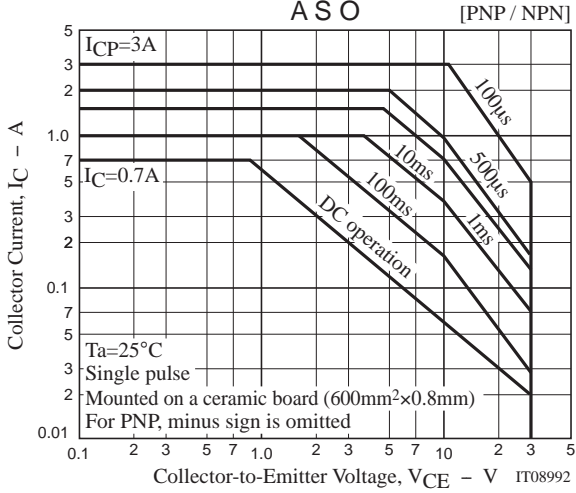
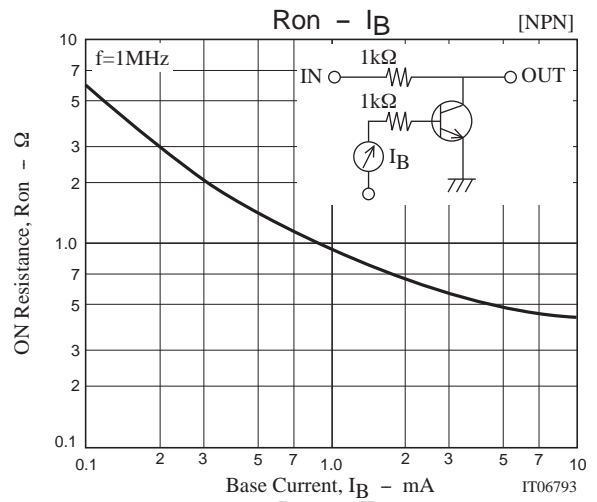
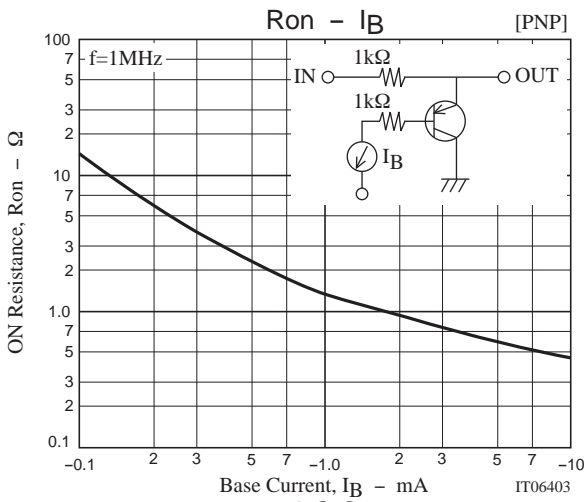
For PNP, minus sign is omitted.

Ordering Information

Device	Package	Shipping	memo
CPH5541-TL-E	CPH5	3,000pcs./reel	Pb Free







Embossed Taping Specification

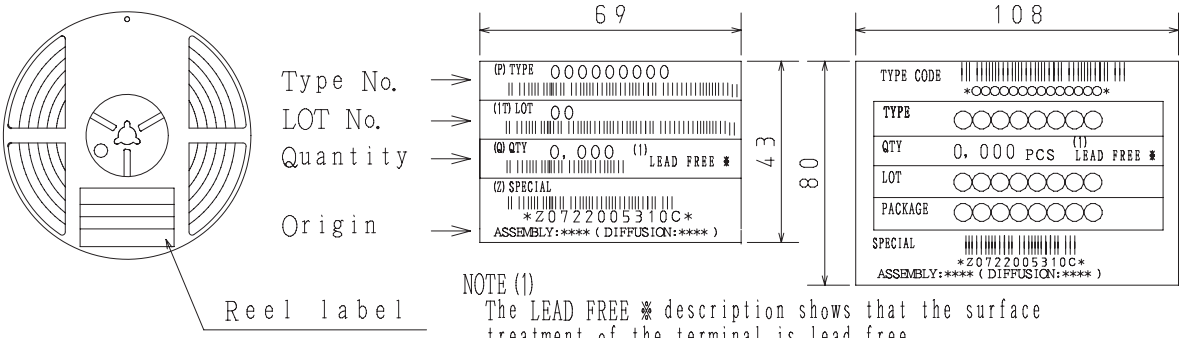
CPH5541-TL-E

1. Packing Format

Package Name	Carrier Tape Type	Maximum Number of devices contained (pcs)			Packing format	
		Reel	Inner box	Outer box	Inner BOX (C-1)	Outer BOX (A-7)
CPH5	CPH6	3,000	15,000	90,000	5 reels contained Dimensions:mm (external) 183×72×185	6 inner boxes contained Dimensions:mm (external) 440×195×210

Reel label, Inner box label (unit:mm) Outer box label
 [It is a label at the time of factory shipments. The form of a label may change in physical distribution process.]

Packing method

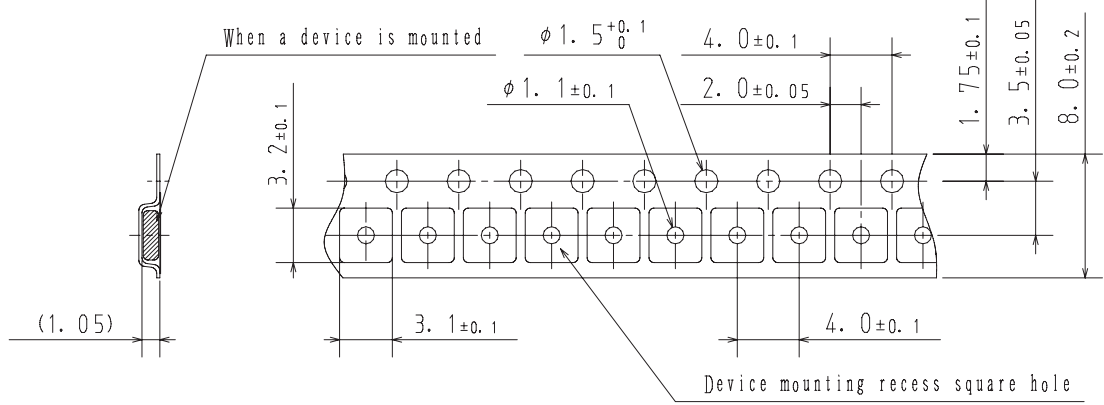


NOTE (1)
 The LEAD FREE * description shows that the surface treatment of the terminal is lead free.

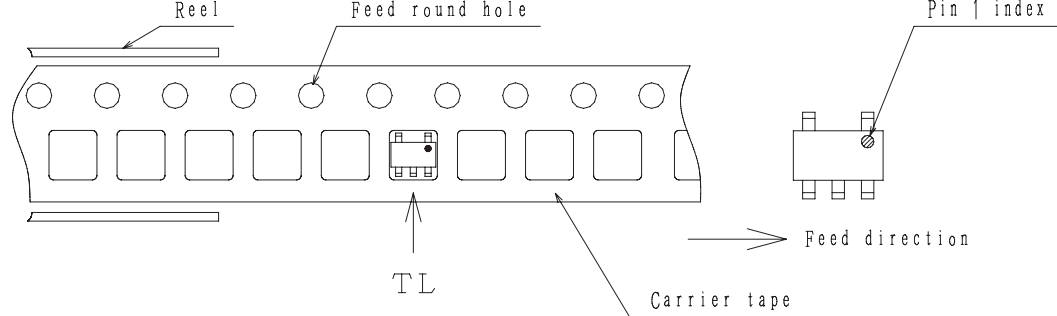
Label	JEITA Phase
LEAD FREE 3	JEITA Phase 3A
LEAD FREE 4	JEITA Phase 3

2. Taping configuration

2-1. Carrier tape size (unit:mm)



2-2. Device placement direction



Those with pin 1 index on the feed hole side.....TL

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