TPS65130EVM-063 User's Guide

This user's guide describes the characteristics, operation, and use of the TPS65130EVM evaluation module (EVM). This EVM contains Texas Instruments TPS65130 positive and negative output supply IC. This user's guide includes EVM specifications, recommended test setup, test results, bill of materials (BOM), and a schematic diagram.

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1 Introduction

The Texas Instruments TPS65130EVM evaluation module uses a TPS65130 multichannel output IC to provide both a positive and negative power rail. The goal of the EVM is to facilitate evaluation of the TPS65130.

1.1 Performance Specification Summary

Table 1 provides a summary of the TPS65130EVM performance specifications. All specifications are given for an ambient temperature of 25°C.

Table 1. Typical Performance Specification Summary

	CONDITION	VOLTAGE RANGE (V)			CURRENT RANGE (mA)		
		MIN	TYPE	MAX	MIN	TYP	MAX
VIN		2.7	3.3	5.5			2000
VPOS	V_I = 3.3 V	7.76	8	8.24			250
	V_I = 5 V						400
VNEG	V_I = 3.3 V	-5.15	-5	-4.85			190
	V_I = 5 V						260

1.2 Modifications

To aid user customization of the EVM, the board was designed with devices having 0603 or larger footprints. A real implementation would likely occupy less total board space.

Changing components can improve or degrade EVM performance. For example, using inductors with larger dc resistance lowers efficiency of the solution. Resistors R10 and R11 are for test purposes only. They can be replaced by a 51.1 - 100 ohm resistor and used to measure the loop gain with a loop gain analyzer. They are not required in a real application.

2 Input/Output Connector Descriptions

J1−VIN This is the positive connection to the input power supply. The leads to the input supply should be twisted and kept as short as possible.

J2−GND This is the return connection to the input power supply.

J3−VPOS This is the positive output of the device.

J4−GND This is the return connection for the load on the positive converter of the device.

J5−VNEG This is the negative output of the device.

J6−GND This is the return connection for the load on the negative converter of the device.

JP1−ENP This is the enable pin for the positive converter (VPOS). Placing a jumper across pins 2−3 of JP1 shorts the enable pin to GND, thereby disabling the device. Placing a jumper across pins 1−2 of JP1 connects the enable pin to Vin and enables the device.

JP2−PSP This is the control pin for the power-save mode of the positive converter. Placing a jumper across pins 2−3 of JP2 shorts the pin to GND, thereby disabling the power-save mode. Placing a jumper across pins 1−2 of JP2 connects the pin to VI, thereby enabling the power-save mode.

JP3−ENN This is the enable pin for the negative converter (VNEG). Placing a jumper across pins 2−3 of JP3 shorts the enable pin to GND, thereby disabling the device. Placing a jumper across pins 1−2 of JP3 connects the enable pin to Vin and enables the device.

JP4−PSN This is the control pin for the power-save mode of the negative converter. Placing a jumper across pins 2−3 of JP4 shorts the pin to GND, thereby disabling the power-save mode. Placing a jumper across pins 1−2 of JP4 connects the pin to V_I, thereby enabling the power-save mode.

2.1 Test Setup

The absolute maximum input voltage is 6 V. The TPS65130 is designed to operate with a maximum input voltage of 5.5 V. Connect a power supply set between 2.7 V and 5.5 V output voltage and current limit set to at least 3 A. Short pins 1−2 on jumpers JP1 and JP2 to enable both rails.

2.2 Test Results

Below are the efficiency results using this EVM:

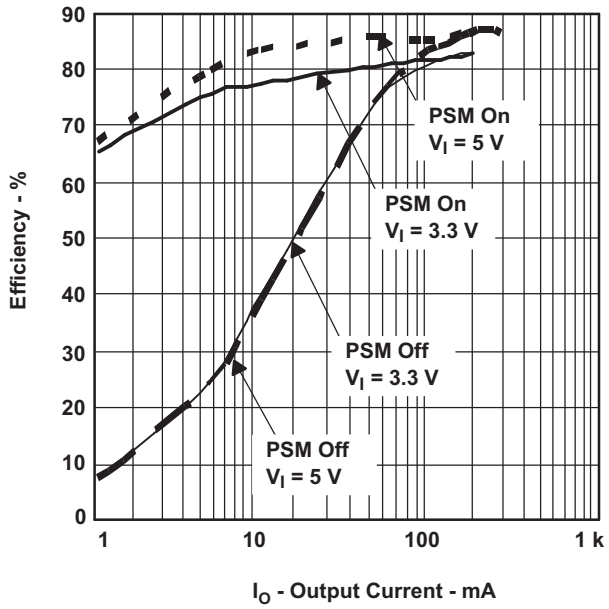

Figure 1. TPS65130 VPOS Efficiency Using the Wuerth 744031004, 4.7-μH Inductor

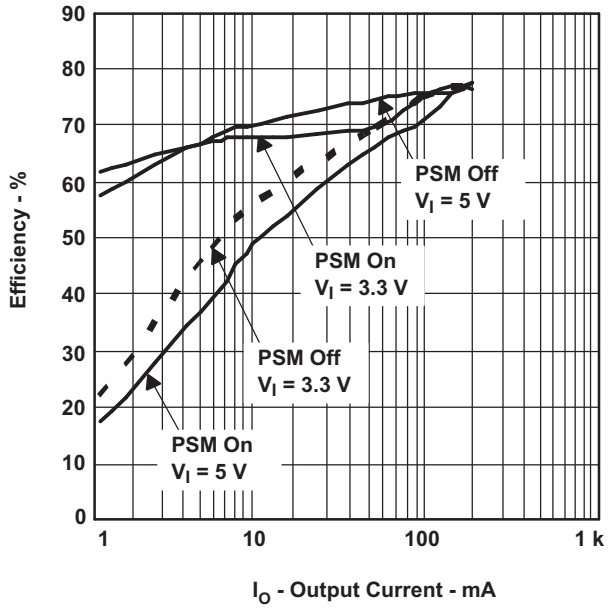

Figure 2. TPS65130 VNEG Efficiency Using Wuerth 744031004, 4.7-μH Inductor

3 Board Layout

Board layout is critical for all switch mode power supplies. Figure 3, Figure 4, and Figure 5 show the board layout for the HPA063 PWB. The switching nodes with high-frequency noise are isolated from the noise-sensitive feedback circuitry, and careful attention has been given to the routing of high-frequency current loops. See the data sheet for more specific layout guidelines.

To ensure that the IC provides its maximum designed output power, it is highly recommended that users follow the EVM board layout when laying out their boards, especially the separate analog and power ground paths and the small footprint, closely spaced feedback components.

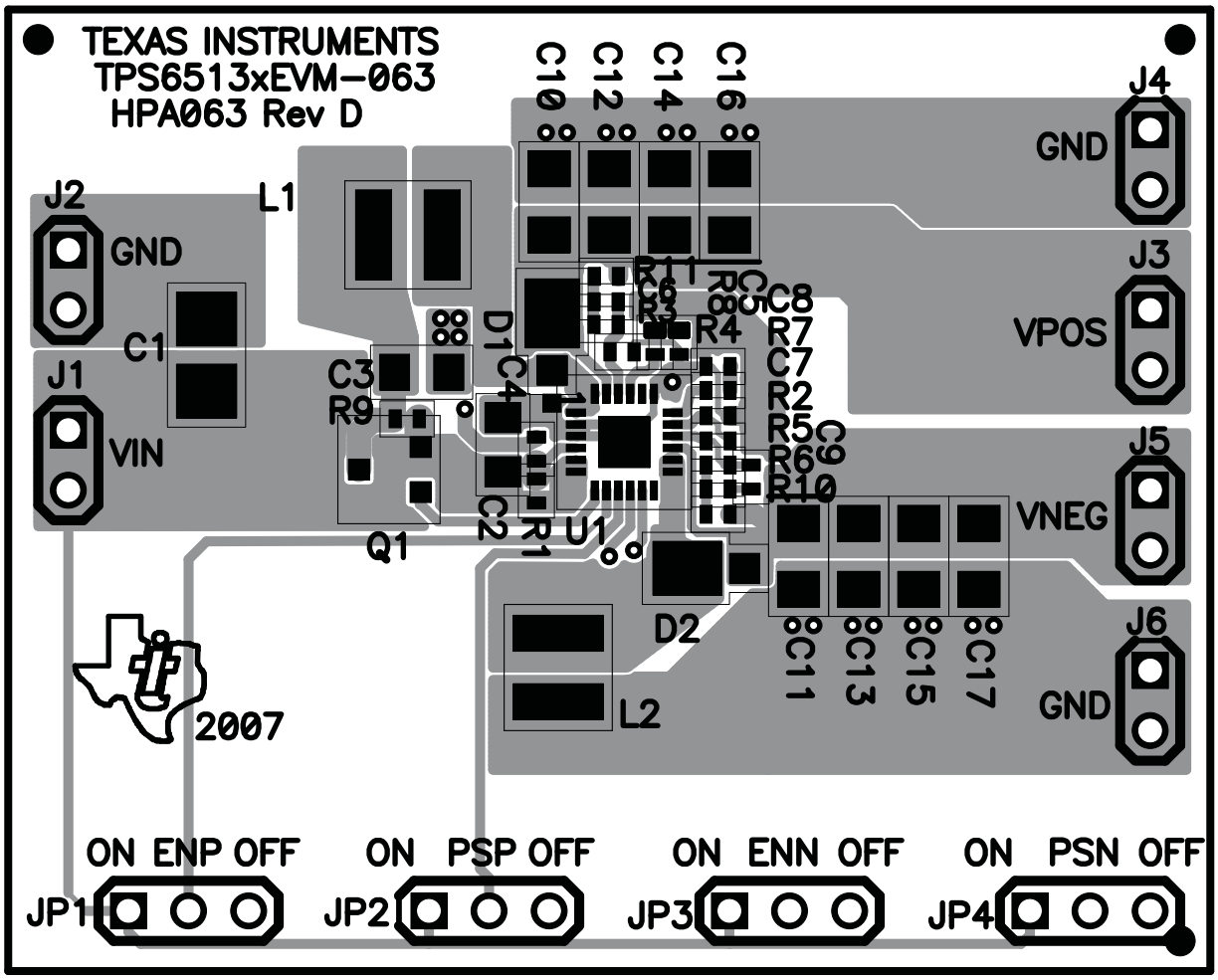

Figure 3. Top Assembly Layer

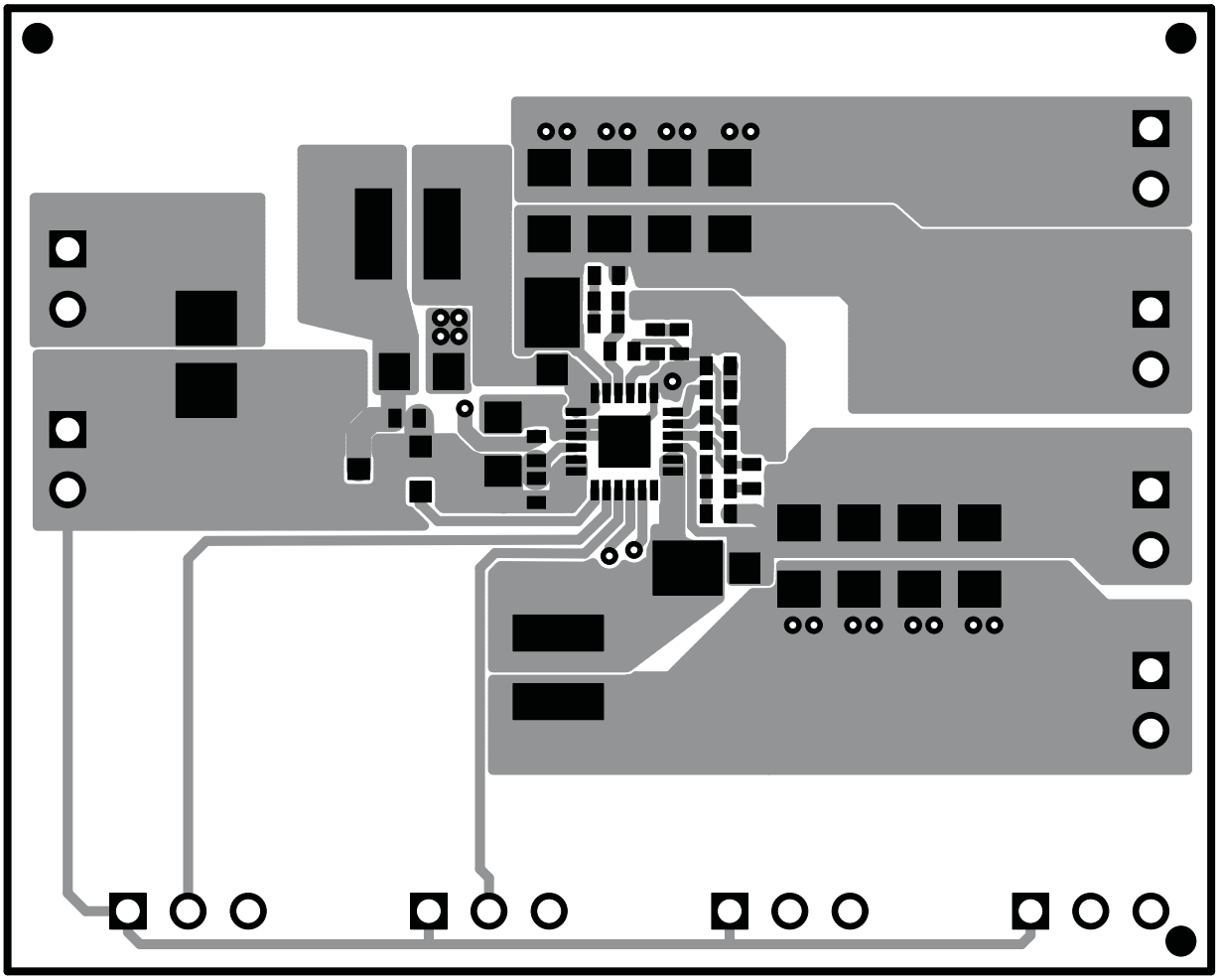

Figure 4. Top Layer

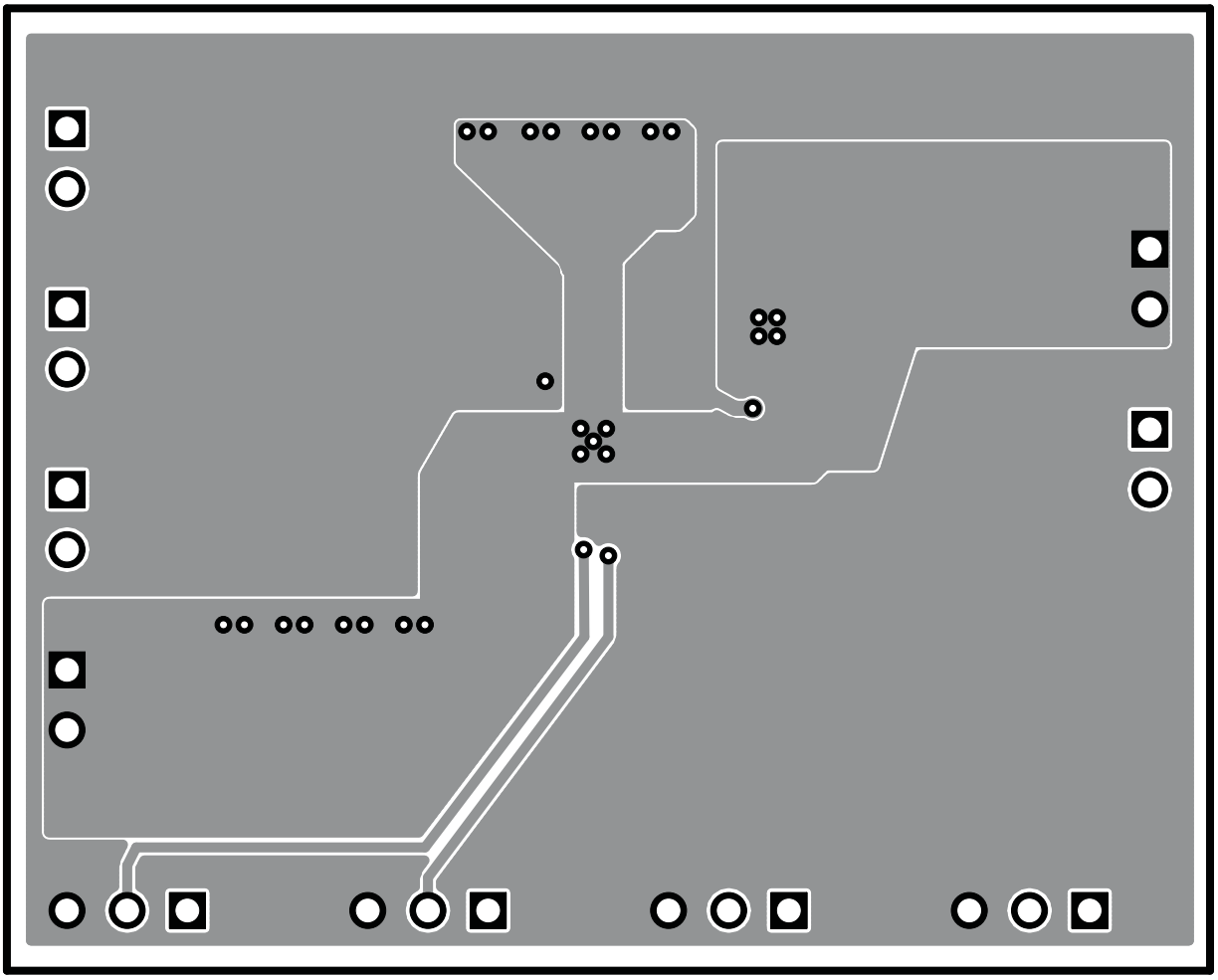

Figure 5. Bottom Layer

4 Bill of Materials and Schematic

4.1 Bill of Materials

Table 2. HPA063 Bill of Materials

QTY	RefDes	Value	DESCRIPTION	SIZE	Part Number	MFR
0	C1	Open	Capacitor, multi-pattern, SM 805 to 1210			
8	C10 - C17	4.7uF	Capacitor, Ceramic, 25V, X7R, 10%	1206	C3216X7R1E475KT	TDK
2	C2, C3	4.7uF	Capacitor, Ceramic, 6.3V, X5R, 10%	0805	C2012X5R0J475KT	TDK
1	C4	0.1uF	Capacitor, 10V, X5R, 10%	0402	C1005X5R1A104K	TDK
1	C5	0.01uF	Capacitor, 16V, X7R, 10%	0402	C1005X7R1C103K	TDK
1	C8	0.0047uF	Capacitor, 50V, C0G, 5%	402	STD	STD
1	C6	6.8pF	Capacitor, 50V, C0G, 5%	0402	C1005C0G1H6R8D	TDK
1	C7	0.22uF	Capacitor, 6.3V, X5R, 10%	0402	C1005X5R0J224K	TDK
1	C9	12pF	Capacitor, 50V, C0G, 5%	0402	C1005C0G1H120J	TDK
2	D1, D2		Diode, Schottky, 1A, 20V	457-04	MBRM120	On Semi
6	J1 - J6		Header, 2 pin, 100mil spacing, (36-pin strip)	0.100 x 2	PTC36SAAN	Sullins
4	JP1 - JP4		Header, 3 pin, 100mil spacing, (36-pin strip)	0.100 x 3	PTC36SAAN	Sullins
2	L1, L2	4.7uH	Inductor, SMT, 0.9A, 85milliohms	0.150 X 0.150	744031004	WE
1	Q1		MOSFET,P-ch, -12 V, 4 A, 51 milliOhm	SOT23	Si2323DS	Vishay
1	R1	100	Resistor, Chip, 1/16W, 1%	0402	Std	Std
1	R2	162k	Resistor, Chip, 1/16W, 1%	0402	Std	Std
1	R3	909k	Resistor, Chip, 1/16W, 1%	0402	Std	Std
1	R4	162k	Resistor, Chip, 1/16W, 1%	0402	Std	Std
1	R5	665k	Resistor, Chip, 1/16W, 1%	0402	Std	Std
1	R6	10k	Resistor, Chip, 1/16W, 1%	0402	Std	Std
3	R7, R10, R11, R8	0	Resistor, Chip, 1/16W, 5%	0402	Std	Std
0	R9	Open	Resistor, Chip, 1/16W, 1%	0402		
1	U1		IC, Positive and Negative Output DC-DC Converter	QFN24	TPS65130RGE	TI
1	--		PCB, 2 In x 1.6 In x 0.062 In		HPA063	Any
4	--		Shunt, 100 mil, Black	0.100	929950-00	

4.2 Schematics

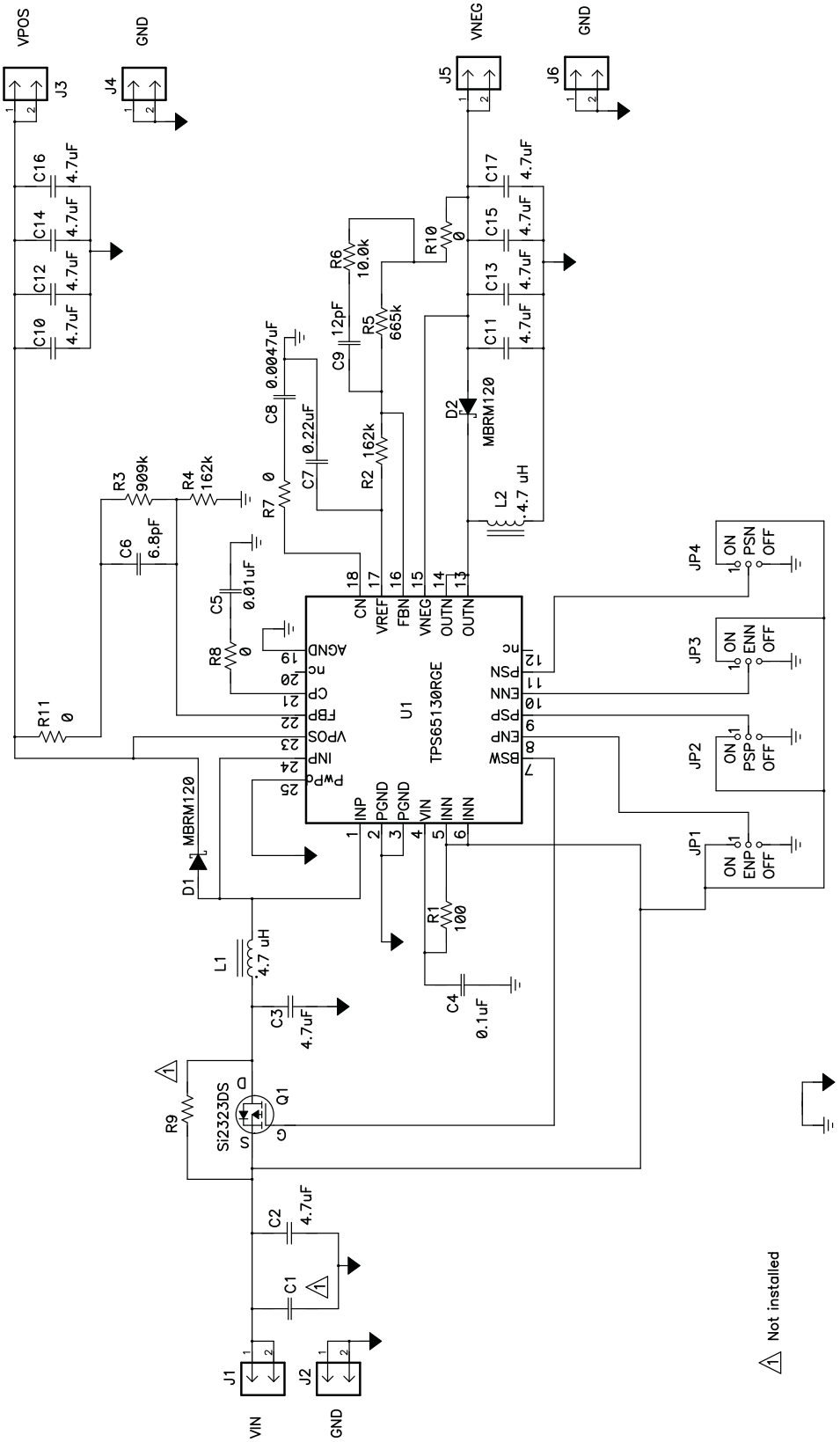

Figure 6. TPA65130EVM-063 Schematic

Related Documentation from Texas Instruments

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Data Sheets:	Literature Number:
TPS65130	SLVS493

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EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of 2.7 V to 5.5 V and the output voltage range of -15 V to 15 V .

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 125°C. The EVM is designed to operate properly with certain components above 125°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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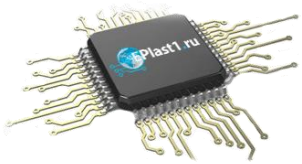

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