ATWILC1000B-MUT

ATWILC1000B-MUT IEEE® 802.11 b/g/n Link Controller SoC

Introduction

The ATWILC1000B is a single chip IEEE® 802.11 b/g/n Radio/Baseband/MAC link controller optimized for low-power mobile applications. The ATWILC1000B supports single stream 1x1 802.11n mode providing up to 72 Mbps PHY rate. The ATWILC1000B features a fully integrated Power Amplifier (PA), Low Noise Amplifier (LNA), Switch, and Power Management. The ATWILC1000B offers very low-power consumption while simultaneously providing high performance and minimal bill of materials.

The ATWILC1000B provides multiple peripheral interfaces including Universal Asynchronous Receiver/Transmitter (UART), Serial Peripheral Interface (SPI), Inter-Integrated Circuit (I^2C), and Secure Digital Input Output (SDIO). The clock source for the ATWILC1000B is provided by an external crystal at 26 MHz. The ATWILC1000B is available in both QFN and Wafer Level Chip Scale Package (WLCSP) packaging.

Features

- IEEE 802.1 b/g/n 20 MHz (1x1) Solution
- Single Spatial Stream in 2.4 GHz ISM Band
- Integrated PA and T/R Switch
- Superior Sensitivity and Range via Advanced PHY Signal Processing
- Advanced Equalization and Channel Estimation
- Advanced Carrier and Timing Synchronization
- Wi-Fi Direct® and Soft-AP Support
- Supports IEEE 802.11 WEP, WPA, WPA2 Security
- Superior MAC Throughput via Hardware Accelerated Two-Level A-MSDU/A-MPDU Frame Aggregation and Block Acknowledgment
- On-Chip Memory Management Engine to Reduce Host Load
- SPI, SDIO, and I^2C Host Interfaces
- Operating Temperature Ranges from -40°C to +85°C
- Power Save Modes:
  - <1 µA Deep Power-Down mode typical at 3.3V I/O
  - 280 µA Doze mode with chip settings preserved (used for beacon monitoring)
  - On-chip low-power sleep oscillator
  - Fast host wake up from Doze mode by a pin or host I/O transaction

Table of Contents

1. Ordering Information and IC Marking

The following table provides the ordering details of the ATWILC1000B IC.

Table 1-1. Ordering Details

Ordering Code[1]	Package Type	IC Marking
ATWILC1000B-MU-ABCD	5 x 5 QFN in Tape and Reel	ATWILC1000B
ATWILC1000B-UU-ABCD	3.24 x 3.24 mm WLCSP in Tape and Reel	ATWILC1000B

Note:

1. ABCD interprets as:
   "A" can be "Y" indicating Tray, or "T" indicating Tape and Reel.

   "BCD" equals to "042" for part assigned with MAC ID and blank for part with no MAC ID.

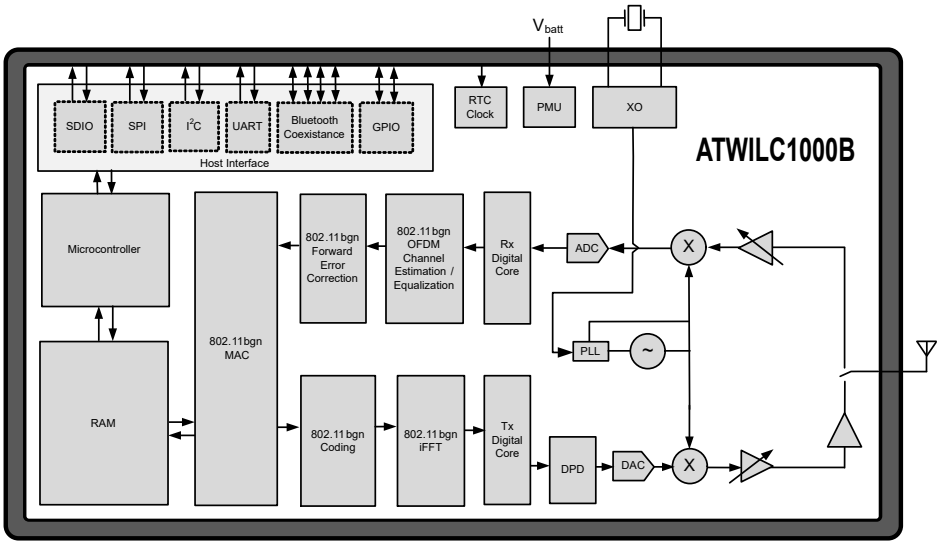
   The following table lists possible combinations for ordering the ATWILC1000B-MU and ATWILC1000B-UU.

Ordering Code	Description
ATWILC1000B-MU-T	No MAC ID and ship in Tape and Reel
ATWILC1000B-MU-Y	No MAC ID and ship in Tray
ATWILC1000B-MU-Y042	MAC ID assigned and ship in Tray
ATWILC1000B-MU-T042	MAC ID assigned and ship in Tape and Reel
ATWILC1000B-UU-T	No MAC ID and ship in Tape and Reel
ATWILC1000B-UU-Y	No MAC ID and ship in Tray
ATWILC1000B-UU-Y042	MAC ID assigned and ship in Tray
ATWILC1000B-UU-T042	MAC ID assigned and ship in Tape and Reel

2. Block Diagram

The following figure provides a basic overview of the ATWILC1000B IC.

Figure 2-1. ATWILC1000B Block Diagram



3. Pinout and Package Information

3.1 Pin Description

The ATWILC1000B is offered in an exposed pad 40-pin QFN package. This package has an exposed paddle that must be connected to the system board ground. The QFN package pin assignment and the WLCSP package pin assignment are shown in the following figures. The color shading is used to indicate the pin type as follows:

- Green – power
- Red – analog
- Blue – digital I/O
- Yellow – digital input
- Grey – unconnected or reserved

Figure 3-1. Pin Assignment

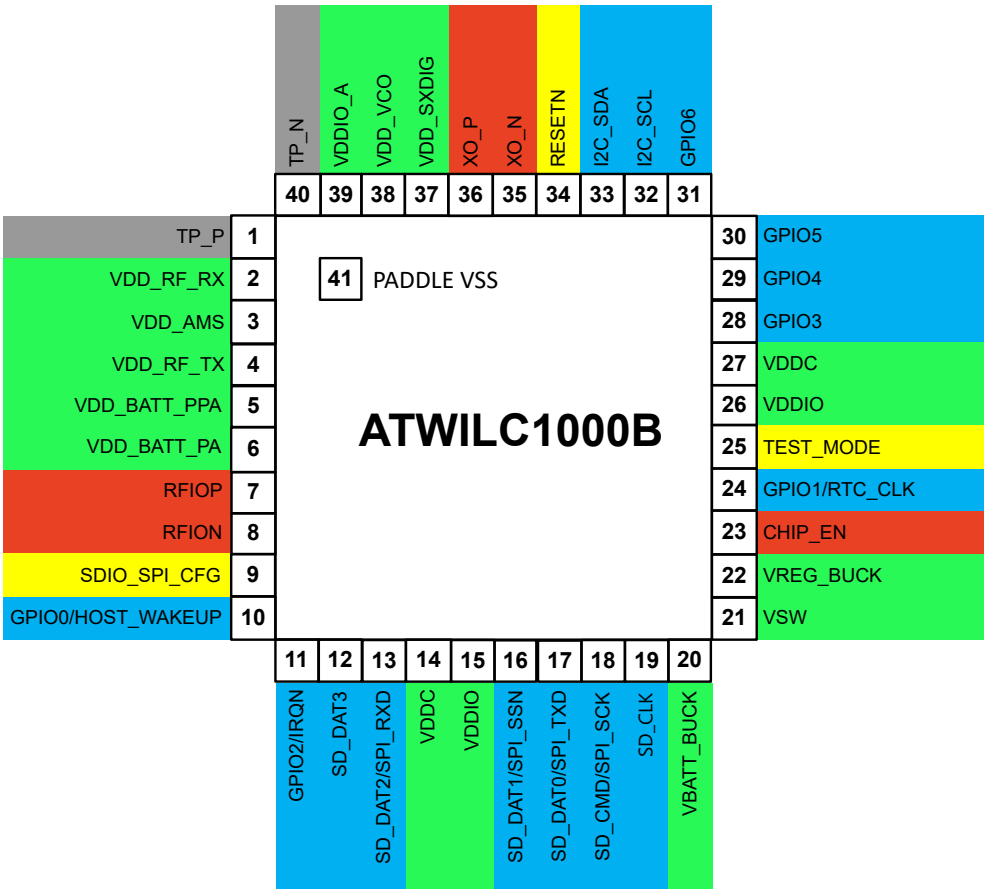
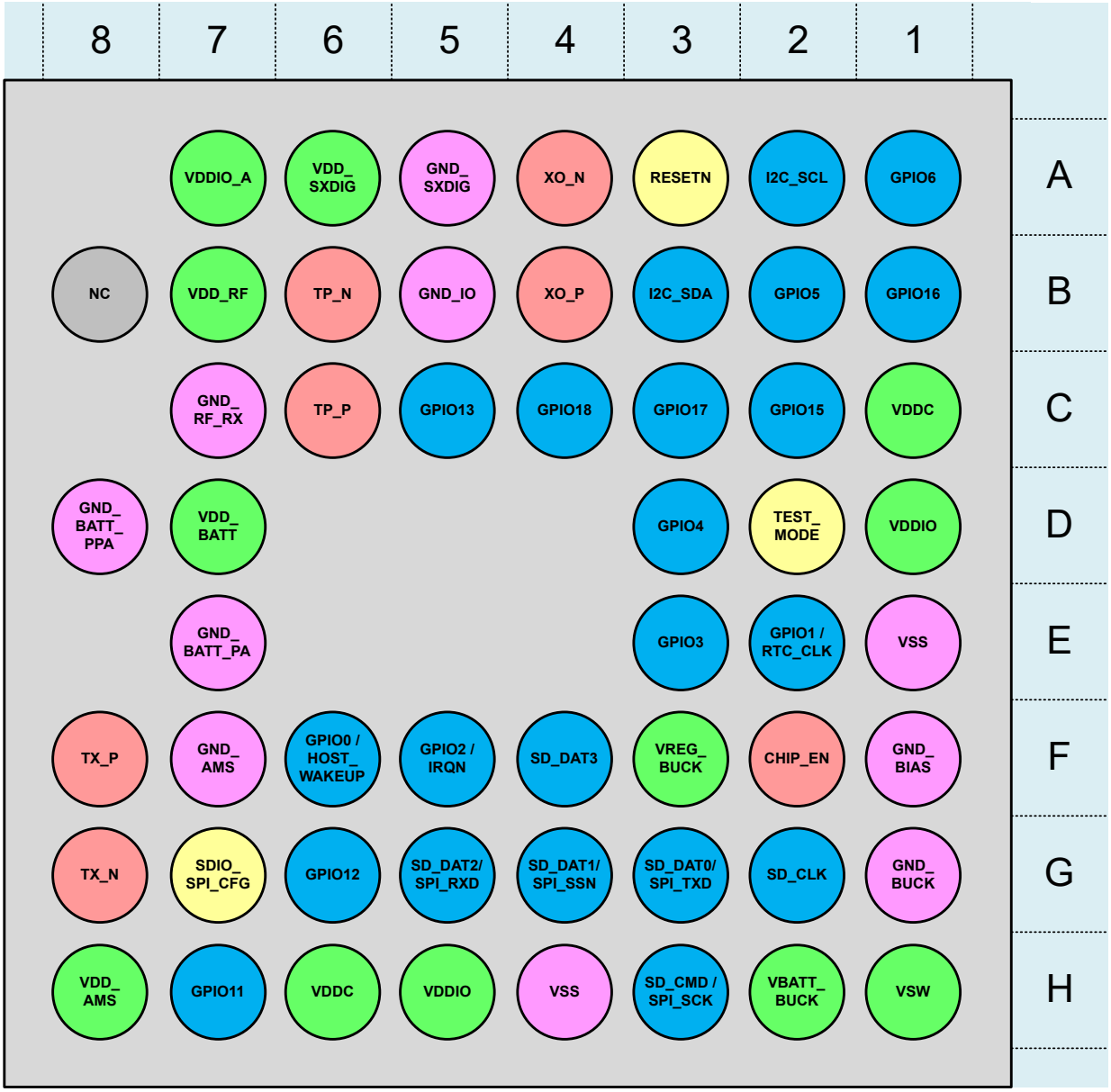


Figure 3-2. WLCSP Package Pin Assignment



The ATWILC1000B pins are described in the following table.

Table 3-1. Pin Description

QFN Pin Number	WLCSP Pin Number	Pin Name	Pin Type	Description
1	C6	TP_P	Analog	Test Pin/No Connect
2	B7	VDD_RF_RX	Power	Tuner RF Supply (see Section 9.1 Power Architecture)

.....continued

QFN Pin Number	WLCSP Pin Number	Pin Name	Pin Type	Description
3	H8	VDD_AMS	Power	Tuner BB Supply (see Section 9.1 Power Architecture)
4	-	VDD_RF_TX	Power	Tuner RF Supply (see Section 9.1 Power Architecture)
5	-	VDD_BATT_PPA	Power	PA 1ST Stage Supply (see Section 9.1 Power Architecture)
6	D7	VDD_BATT_PA	Power	PA 2ND Stage Supply (see Section 9.1 Power Architecture)
7	-	RFIOP	Analog	Positive RF Differential I/O (see Table 9-4)
8	-	RFION	Analog	Negative RF Differential I/O (see Table 9-4)
9	G7	SDIO_SPI_CFG	Digital Input	Tie to 1 for SPI, 0 for SDIO
10	F6	GPIO0/ HOST_WAKE	Digital I/O, Programmable Pull-up	GPIO0/SLEEP Mode Control
11	F5	GPIO2/IRQN	Digital I/O, Programmable Pull-up	GPIO2/Device Interrupt
12	F4	SD_DAT3	Digital I/O, Programmable Pull-up	SDIO Data3
13	G5	SD_DAT2/ SPI_RXD	Digital I/O, Programmable Pull-up	SDIO Data2/SPI Data RX
14	C1	VDDC	Power	Digital Core Power Supply (see Section 9.1 Power Architecture)

.....continued

QFN Pin Number	WLCSP Pin Number	Pin Name	Pin Type	Description
15	D1	VDDIO	Power	Digital I/O Power Supply (see Section 9.1 Power Architecture)
16	G4	SD_DAT1/ SPI_SSN	Digital I/O, Programmable Pull-up	SDIO Data1/SPI Slave Select
17	G3	SD_DAT0/ SPI_TXD	Digital I/O, Programmable Pull-up	SDIO Data0/SPI Data TX
18	H3	SD_CMD/ SPI_SCK	Digital I/O, Programmable Pull-up	SDIO Command/SPI Clock
19	G2	SD_CLK	Digital I/O, Programmable Pull-up	SDIO Clock
20	H2	VBATT_BUCK	Power	Battery Supply for DC/DC Converter (see Section 9.1 Power Architecture)
21	H1	VSW	Power	Switching output of DC/DC Converter (see Section 9.1 Power Architecture)
22	F3	VREG_BUCK	Power	Core Power from DC/DC Converter (see Section 9.1 Power Architecture)
23	F2	CHIP_EN	Analog	PMU Enable
24	E2	GPIO1/RTC_CLK	Digital I/O, Programmable Pull-up	GPIO1/32kHz Clock Input
25	D2	TEST_MODE	Digital Input	Test Mode – User must tie this pin to GND

.....continued

QFN Pin Number	WLCSP Pin Number	Pin Name	Pin Type	Description
26	H5	VDDIO	Power	Digital I/O Power Supply (see Section 9.1 Power Architecture)
27	H6	VDDC	Power	Digital Core Power Supply (see Section 9.1 Power Architecture)
28	E3	GPIO3	Digital I/O, Programmable Pull-up	GPIO3/ SPI_SCK_Flash
29	D3	GPIO4	Digital I/O, Programmable Pull-up	GPIO4/ SPI_SSN_Flash
30	B2	GPIO5	Digital I/O, Programmable Pull-up	GPIO5/ SPI_TXD_Flash
31	A1	GPIO6	Digital I/O, Programmable Pull-up	GPIO6/ SPI_RXD_Flash
32	A2	I2C_SCL	Digital I/O, Programmable Pull-up	I^2C Slave Clock (high-drive pad, see Table 4-3)
33	B3	I2C_SDA	Digital I/O, Programmable Pull-up	I^2C Slave Data (high-drive pad, see Table 4-3)
34	A3	RESETN	Digital Input	Active-Low Hard Reset
35	A4	XO_N	Analog	Crystal Oscillator N
36	B4	XO_P	Analog	Crystal Oscillator P
37	A6	VDD_SXDIG	Power	SX Power Supply (see Section 9.1 Power Architecture)
38	-	VDD_VCO	Power	VCO Power Supply (see Section 9.1 Power Architecture)

.....continued

QFN Pin Number	WLCSP Pin Number	Pin Name	Pin Type	Description
39	A7	VDDIO_A	Power	Tuner VDDIO Power Supply (see Section 9.1 Power Architecture)
40	B6	TP_N	Analog	Test Pin/No Connect
41(1)	-	PADDLE VSS	Ground	Connect to System Board Ground
-	A5	GND_SXDIG	Ground	SX Ground, Connect to System Board Ground
-	B1	GPIO16	Digital I/O, Programmable Pull-up	GPIO16
-	B5	GND_IO	Ground	I/O Ground, Connect to System Board Ground
-	B8	NC	None	Reserved/No Connect
-	C2	GPIO15	Digital I/O, Programmable Pull-up	GPIO15
-	C3	GPIO17	Digital I/O, Programmable Pull-up	GPIO17
-	C4	GPIO18	Digital I/O, Programmable Pull-up	GPIO18
-	C5	GPIO13	Digital I/O, Programmable Pull-up	GPIO13
-	C7	GND_RF_RX	Ground	RF Rx Ground, Connect to System Board Ground
-	D8	GND_BATT_PPA	Ground	PA 2nd Stage Ground, Connect to System Board Ground

.....continued

QFN Pin Number	WLCSP Pin Number	Pin Name	Pin Type	Description
-	E1	VSS	Ground	Connect to System Board Ground
-	E7	GND_BATT_PA	Ground	PA 1st Stage Ground, Connect to System Board Ground
-	F1	GND_BIAS	Ground	Bias Ground, Connect to System Board Ground
-	F7	GND_AMS	Ground	AMS Ground, Connect to System Board Ground
-	F8	TX_P	Analog	Positive RF Differential I/O
-	G1	GND_BUCK	Ground	DC/DC Converter Ground, Connect to System Board Ground
-	G6	GPIO12	Digital I/O, Programmable Pull-up	GPIO12
-	G8	TX_N	Analog	Negative RF Differential I/O
-	H4	VSS	Ground	Connect to System Board Ground
-	H7	GPIO11	Digital I/O, Programmable Pull-up	GPIO11

Note:

1. Applies to QFN package only. Pin 41, PADDLE_VSS must be soldered to GND providing good RF grounding and good heat dissipation.

Figure 3-3. WLCSP ATWILC1000B UU

8	7	6	5	4	3	2	1	
	VDDA_IO	VDDSXDIG	GNDSXDIG	XON	RESET	I2C_SCL	GPIO_6	A
NC	VDDRF	TPN	GNDIO	XOP	I2C_SDA	GPIO_5	GPIO_16	B
	GNDRF_RX	TPP	GPIO_13	GPIO_18	GPIO_17	GPIO_15	VDD	C
GNDBATT_PPA	VDDBATT				GPIO_4	TESTMODE	VDDIO	D
	GNDBATT_PA				GPIO_3	RTC_CLK	VSS	E
TXP	GNDAMS	HOST_WAKEUP	IRQN	SD_DAT3	VREGBUCK	CHIPEN	GND_BIAS	F
TXN	SDIO_SPI_CFG	GPIO_12	SD_DAT2	SD_DAT1	SD_DAT0_SPI_TXD	SD_CLK	GNDBUCK	G
VDDAMS	GPIO_11	VDD	VDDIO	VSS	SD_CMD_SPI_SCK	VBATT_BUCK	VSW	H

3.2 Package Description

The ATWILC1000B QFN package information is provided in the following table and the package view is shown in Figure 3-4.

Table 3-2. QFN Package Information

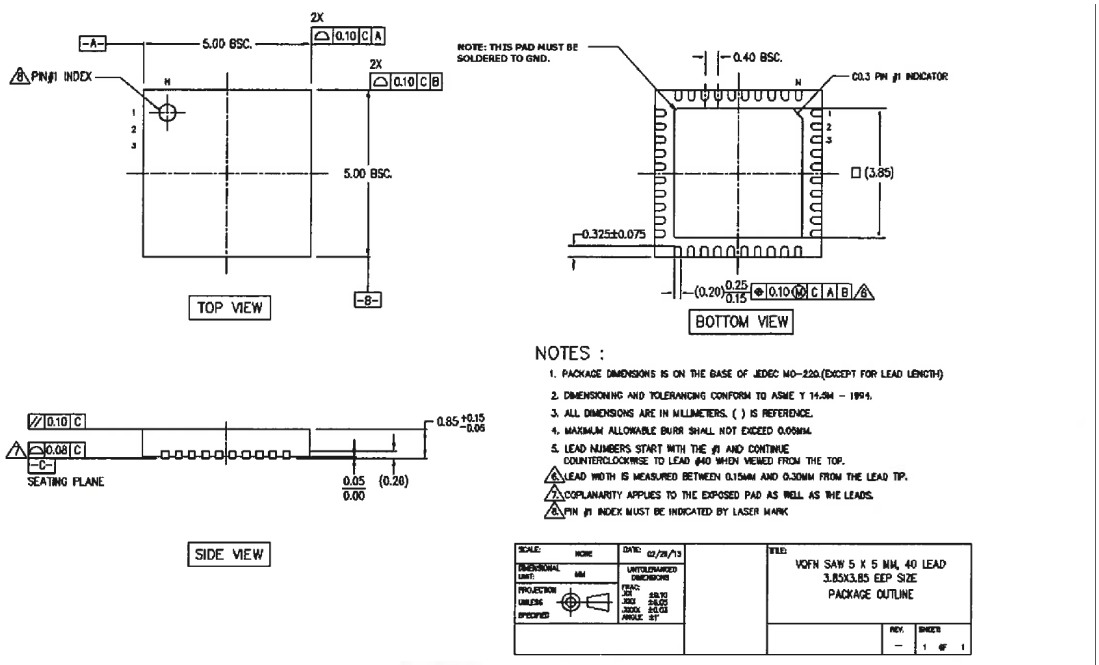
Parameter	Value	Unit	Tolerance
Package size	5 x 5	mm	±0.1 mm
QFN pad count	40	–	–
Total thickness	0.85	mm	+/0.15/-0.05mm
QFN pad pitch	0.40		–
Pad width	0.20		–
Exposed pad size	3.7 x 3.7		–

The ATWILC1000B WLCSP package information is provided in the following table and the package view is shown in the Figure 3-5.

Table 3-3. WLCSP Package Information

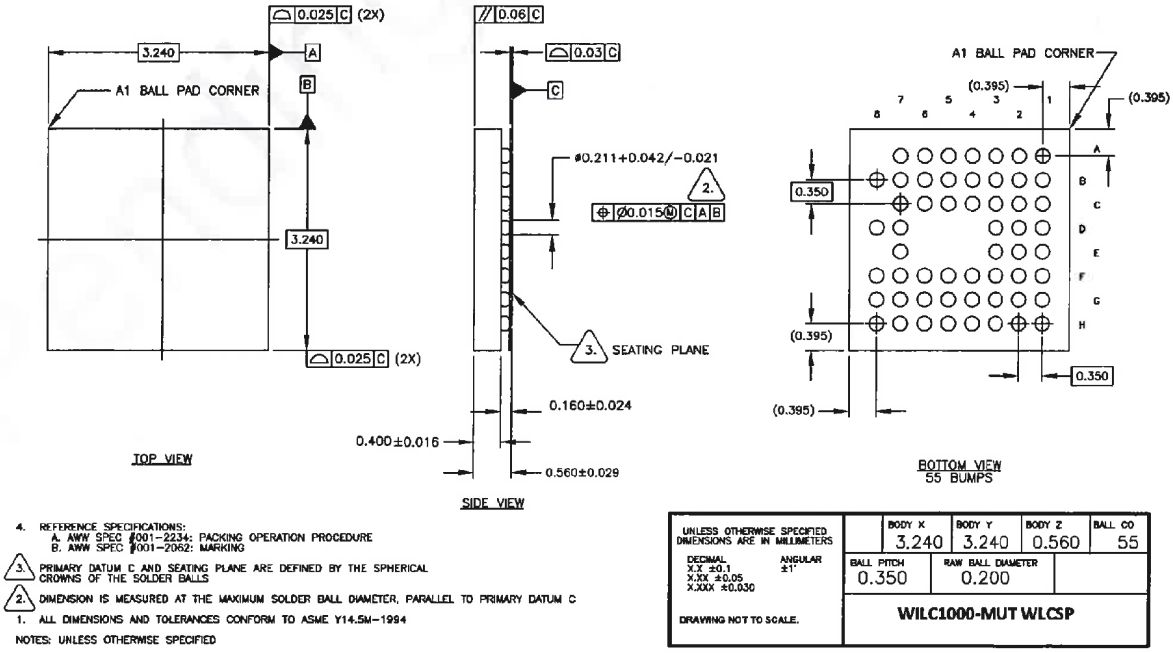
Parameter	Value	Unit	Tolerance
Package size	3.24 x 3.24	mm	±0.3 mm
Total thickness	0.56		±0.3 mm
I/O Pitch	0.35		–
Ball diameter	0.20		±0.3 mm

Figure 3-4. QFN Package



The QFN package is a qualified Green Package.

Figure 3-5. WLCSP Package



4. Electrical Specifications

4.1 Absolute Ratings

The values listed in this section are the peaked excursions ratings that can be tolerated by the device, and if sustained will cause irreparable damage to the device.

Table 4-1. Absolute Maximum Ratings

Characteristics	Symbol	Min.	Max.	Unit
Core supply voltage	VDDC	-0.3	1.5	V
I/O supply voltage	VDDIO	-0.3	5.0	
Battery supply voltage	VBATT	-0.3	5.0	
Digital input voltage	V_{IN} (1)	-0.3	VDDIO	
Analog input voltage	V_{AIN} (2)	-0.3	1.5	
ESD human body model	V_{ESDHBM} (3)	-1000, -2000 (3)	+1000, +2000 (3)	
Storage temperature	T_A	-65	150	ºC
Junction temperature	–	–	125	
RF input power max.	–	–	23	dBm

Note:

1. V_{IN} corresponds to all the digital pins.
2. V_{AIN} corresponds to the following analog pins: VDD_RF_RX, VDD_RF_TX, VDD_AMS, RFIOP, RFION, XO_N, XO_P, VDD_SXDIG, and VDD_VCO.
3. For V_{ESDHBM}, each pin is classified as Class 1, or Class 2, or both:
   - The Class 1 pins include all the pins (both analog and digital).
   - The Class 2 pins are all digital pins only.
   - V_{ESDHBM} is ±1 kV for Class 1 pins. V_{ESDHBM} is ±2 kV for Class 2 pins.

4.2 Recommended Operating Conditions

The recommended operating conditions for the ATWILC1000B are listed in the following table.

Table 4-2. Recommended Operating Conditions

Characteristics	Symbol	Min.	Typ.	Max.	Unit
I/O supply voltage	VDDIO	2.7	3.3	3.6	V
Battery supply voltage	VBATT	3.00	3.30	4.20	
Operating temperature	–	-40	–	85	ºC

Note:

1. The ATWILC1000B is functional across this range of voltages; however, optimal RF performance is ensured for VBATT in the range 3.0V < VBATT < 4.2V.
2. I/O supply voltage is applied to the VDDIO_A, and VDDIO pins.
3. Battery supply voltage is applied to the VDD_BATT_PPA, VDD_BATT_PA, and VBATT_BUCK pins.
4. See Table 9-4 for the details of power connections.

4.3 DC Electrical Characteristics

The following table provides the DC characteristics for the ATWILC1000B digital pads.

Table 4-3. DC Electrical Characteristics

Characteristic	Min.	Typ.	Max.	Unit
Input Low Voltage (V_{IL})	-0.30	–	0.60	V
Input High Voltage (V_{IH})	VDDIO-0.60	–	VDDIO+0.30	
Output Low Voltage (V_{OL})	–	–	0.45	
Output High Voltage (OV_{OH})	VDDIO-0.50	–	–	
Output Loading	–	–	20	pF
Digital Input Load	–	–	6	
Pad Drive Strength (regular pads (1))	10.6	13.5	–	mA
Pad Drive Strength (high-drive pads (1))	21.2	27	–	

Note:

1. The following are high-drive pads: I2C_SCL, I2C_SDA; all other pads are regular.

5. Clocking

5.1 Crystal Oscillator

The following table provides the crystal oscillator parameters of the ATWILC1000B.

Table 5-1. Crystal Oscillator Parameters

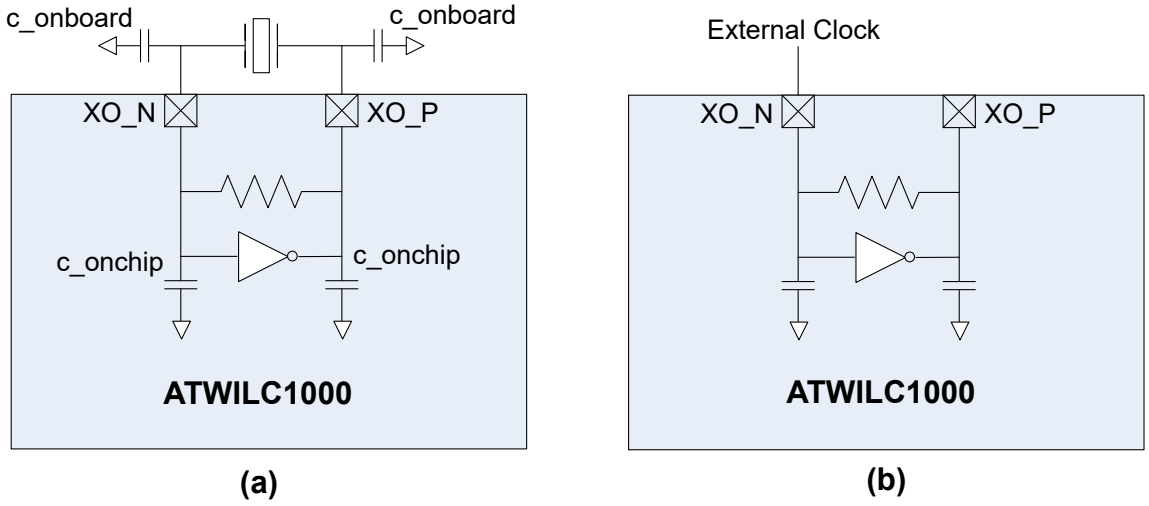
Parameter	Min.	Typ.	Max.	Unit
Crystal resonant frequency	–	26	–	MHz
Crystal equivalent series resistance	–	50	150	Ω
Stability – Initial offset(1)	-100	–	100	ppm
Stability - Temperature and aging	-25	–	25	

Note:

1. To ensure ±25 ppm under operating conditions, frequency offset calibration is required.

The following block diagram in figure "XO Connections - (a)" shows how the internal Crystal Oscillator (XO) is connected to the external crystal. The XO has 5 pF internal capacitance, (denoted as c_onchip in the following figure) on each terminal XO_P and XO_N. To bypass the crystal oscillator with an external reference, an external signal capable of driving 5 pF can be applied to the XO_N terminal as shown in following figure "XO Connections - (b)". The XO has 5 pF internal capacitance on each terminal XO_P and XO_N. This internal capacitance must be accounted for when calculating the external loading capacitance, c_onboard, for the XTAL.

Figure 5-1. XO Connections: (a) The Crystal Oscillator is Used, (b) The Crystal Oscillator is Bypassed



The following table specifies the electrical and performance requirements for the external clock.

Table 5-2. Bypass Clock Specification

Parameter	Min.	Typ.	Max.	Unit	Comments
Oscillation frequency	–	26	–	MHz	Must drive 5 pF load at desired frequency
Voltage swing	0.5	–	1.2	V_{PP}	Must be AC coupled
Stability – Temperature and aging	-25	–	+25	ppm	–
Phase noise	–	–	-130	dBc/Hz	At 10 kHz offset
Jitter (RMS)	–	–	<1	psec	Based on integrated phase noise spectrum from 1 kHz to 1 MHz

5.2 Low-Power Oscillator

The ATWILC1000B has an internally-generated 32 kHz clock to provide timing information for various sleep functions. Alternatively, the ATWILC1000B allows for an external 32kHz clock to be used for this purpose, which is provided through pin 24 (RTC_CLK). Software selects whether the internal clock or external clock is used.

The internal low-power clock is ring oscillator-based and has accuracy within 10,000 ppm. When using the internal low-power clock, the advance wake-up time in the Beacon Monitoring mode has to be increased by about 1% of the sleep time to compensate for the oscillator inaccuracy. For example, for the DTIM interval value of 1, wake-up time has to be increased by 1 ms.

For any application targeting very low-power consumption, an external 32 kHz RTC clock must be used.

6. CPU and Memory Subsystem

6.1 Processor

The ATWILC1000B has a Cortus APS3 32-bit processor. This processor performs many of the MAC functions, including but not limited to: association, authentication, power management, security key management, and MSDU aggregation/de-aggregation. In addition, the processor provides flexibility for various modes of operation, such as STA and AP modes.

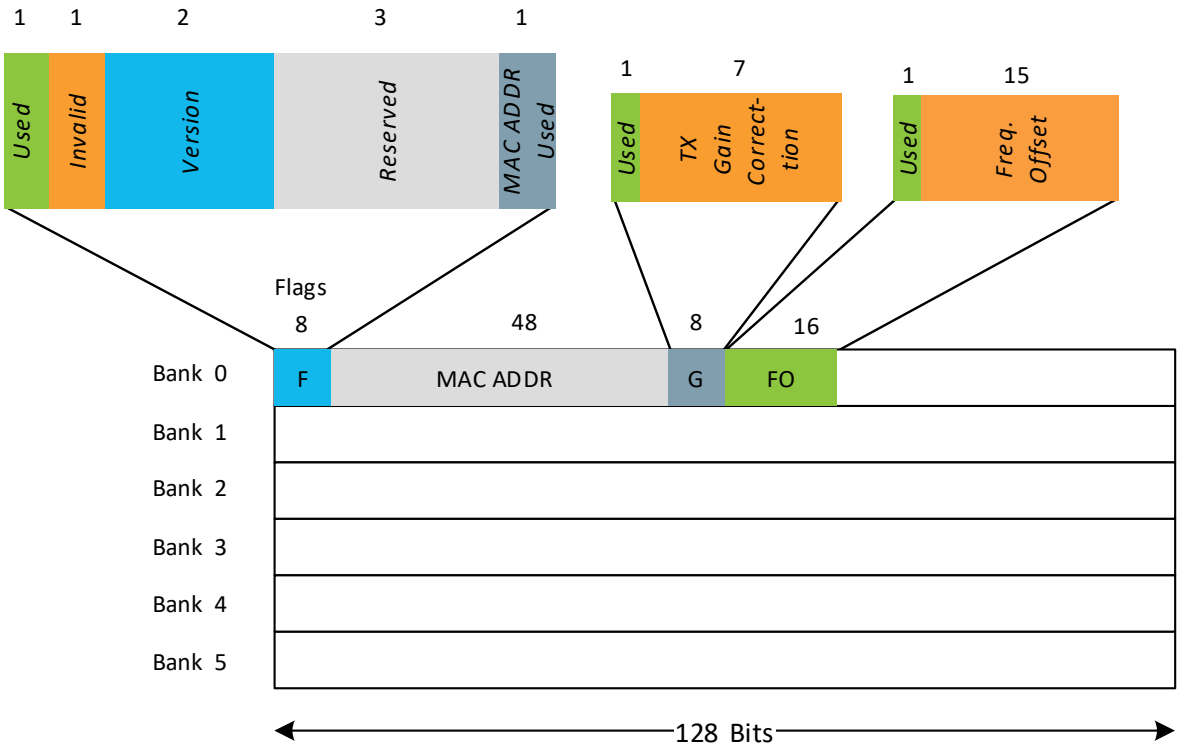
6.2 Memory Subsystem

The APS3 core uses a 128 KB instruction/boot ROM along with a 160 KB instruction RAM and a 64 KB data RAM. In addition, the device uses a 128 KB shared RAM, accessible by the processor and MAC, which allows the APS3 core to perform various data management tasks on the TX and RX data packets.

6.3 Nonvolatile Memory (eFuse)

The ATWILC1000B has 768 bits of nonvolatile eFuse memory that can be read by the CPU after device reset. This nonvolatile One-Time-Programmable (OTP) memory can be used to store customer-specific parameters, such as MAC address; various calibration information, such as TX power, crystal frequency offset, other software-specific configuration parameters, and so on. The eFuse is partitioned into six 128-bit banks. Each bank has the same bit map, which is shown in the following figure. The purpose of the first 80 bits in each bank is fixed, and the remaining 48 bits are general-purpose software dependent bits, or reserved for future use. Since each bank can be programmed independently, this allows for several updates of the device parameters following the initial programming, e.g., updating the MAC address. Refer to the ATWILC1000 Programming Guide for the eFuse programming instructions.

Figure 6-1. eFuse Bit Map



7. WLAN Subsystem

The WLAN subsystem is composed of the Media Access Controller (MAC) and the Physical Layer (PHY). The following two subsections describe the MAC and PHY in detail.

7.1 MAC

7.1.1 Features

The ATWILC1000B IEEE802.11 MAC supports the following functions:

- IEEE 802.11b/g/n
- IEEE 802.11e WMM QoS EDCA/PCF Multiple Access Categories Traffic Scheduling
- Advanced IEEE 802.11n Features:
  - Transmission and reception of aggregated MPDUs (A-MPDU)
  - Transmission and reception of aggregated MSDUs (A-MSDU)
  - Immediate Block Acknowledgment
  - Reduced Interframe Spacing (RIFS)
- Support for IEEE 802.11i and WFA Security with Key Management
  - WEP 64/128
  - WPA-TKIP
  - 128-bit WPA2 CCMP (AES)
- Support for WAPI Security
- Advanced Power Management
  - Standard 802.11 Power Save mode
  - Wi-Fi Alliance® WMM-PS (U-APSD)
- RTS-CTS and CTS-Self Support
- Supports Either STA or AP Mode in the Infrastructure Basic Service Set Mode
- Supports Independent Basic Service Set (IBSS)

7.1.2 Description

The ATWILC1000B MAC is designed to operate at low power while providing high data throughput. The IEEE 802.11 MAC functions are implemented with a combination of dedicated datapath engines, hardwired control logic, and a low-power, high-efficiency microprocessor. The combination of dedicated logic with a programmable processor provides optimal power efficiency and real-time response while providing the flexibility to accommodate evolving standards and future feature enhancements.

Dedicated datapath engines with heavy computational are used to implement datapath functions. For example, an FCS engine checks the CRC of the transmitting and receiving packets, and a cipher engine performs all the required encryption and decryption operations for the WEP, WPA-TKIP, WPA2 CCMP-AES, and WAPI security requirements.

Control functions which have real-time requirements are implemented using hardwired control logic modules. These logic modules offer real-time response while maintaining configurability via the processor. Examples of hardwired control logic modules are: the channel access control module (implements EDCA/HCCA, Beacon TX control, interframe spacing, and so on.), protocol timer module (responsible for the Network Access Vector, back-off timing, timing synchronization function, and slot management), MPDU handling module, aggregation/deaggregation module, block ACK controller

(implements the protocol requirements for burst block communication), and TX/RX control FSMs (coordinate data movement between PHY-MAC interface, cipher engine, and the DMA interface to the TX/RX FIFOs).

The MAC functions that are implemented in software on the microprocessor have the following characteristics:

- Functions with high memory requirements or complex data structures. Examples are association table management and power save queuing.
- Functions with low computational load or without critical real-time requirements. Examples are authentication and association.
- Functions which need flexibility and upgradeability. Examples are beacon frame processing and QoS scheduling.

7.2 PHY

7.2.1 Features

The ATWILC1000B IEEE 802.11 PHY supports the following functions:

- Single Antenna 1x1 Stream in 20 MHz Channels
- Supports IEEE 802.11b DSSS-CCK Modulation: 1, 2, 5.5, and 11 Mbps
- Supports IEEE 802.11g OFDM Modulation: 6, 9, 12,18, 24, 36, 48, and 54 Mbps
- Supports IEEE 802.11n HT Modulations MCS0-7, 20 MHz, 800 and 400 ns guard interval: 6.5, 7.2, 13.0, 14.4, 19.5, 21.7, 26.0, 28.9, 39.0, 43.3, 52.0, 57.8, 58.5, 65.0, and 72.2 Mbps
- IEEE 802.11n Mixed Mode Operation
- Per Packet TX Power Control
- Advanced Channel Estimation/Equalization, Automatic Gain Control, CCA, Carrier/Symbol Recovery, and Frame Detection

7.2.2 Description

The ATWILC1000B WLAN PHY is designed to achieve reliable and power-efficient physical layer communication specified by IEEE 802.11 b/g/n in Single Stream mode with 20 MHz bandwidth. Advanced algorithms are used to achieve maximum throughput in a real-world communication environment with impairments and interference. The PHY implements all the required functions such as FFT, filtering, FEC (Viterbi decoder), frequency and timing acquisition and tracking, channel estimation and equalization, carrier sensing and clear channel assessment, as well as the automatic gain control.

7.3 Radio

This section describes the properties and characteristics of the ATWILC1000B and Wi-Fi radio transmit and receive performance capabilities of the device. The performance measurements are taken at the RF pin assuming 50Ω impedance; the RF performance is assured for room temperature of 25°C with a derating of 2-3dB at boundary conditions.

Measurements were taken under typical conditions: VBATT at 3.3V; VDDIO at 3.3V ,and temperature at +25ºC.

Table 7-1. Features and Properties

Feature	Description
Part Number	ATWILC1000B
WLAN Standard	IEEE 802.11b/g/n, Wi-Fi compliant
Host Interface	SPI, SDIO
Dimension	L x W x H: 21.7 x 14.7 x 2.1 (typical) mm
Frequency range	2.412 GHz ~ 2.472 GHz (2.4 GHz ISM band)
Number of channels	11 for North America, 13 for Europe
Modulation	802.11b: DQPSK, DBPSK, CCK 802.11g/n: OFDM/64-QAM,16-QAM, QPSK, BPSK
Data rate	802.11b: 1, 2, 5.5, 11 Mbps 802.11g: 6, 9, 12, 18, 24, 36, 48, 54 Mbps
Data rate (20 MHz ,short GI,400ns)	802.11n: 7.2, 14.4, 21.7, 28.9, 43.3, 57.8, 65,72.2 Mbps
Operating temperature(1)	-40°C to 85°C
Storage temperature	-40°C to 125°C
Humidity	Operating humidity 10% to 95% non-condensing Storage humidity 5% to 95% non-condensing

Note:

1. RF performance is ensured at room temperature of 25°C with a 2-3db change at boundary conditions.

7.3.1 Receiver Performance

The following are typical conditions for radio receiver performance:

VBATT at 3.3V; VDDIO at 3.3V; temperature at 25°C and WLAN Channel 6 (2437 MHz).

The table below provides the receiver performance characteristics for the ATWILC1000B.

Table 7-2. Receiver Performance

Parameter	Description	Min.	Typ.	Max.	Unit
Frequency	-	2,412	-	2,472	MHz
Sensitivity 802.11b	1 Mbps DSSS	-	-94	-	dBm
	2 Mbps DSSS	-	-91	-	
	5.5 Mbps DSSS	-	-89	-	
	11 Mbps DSSS	-	-86	-	

.....continued

Parameter	Description	Min.	Typ.	Max.	Unit
Sensitivity 802.11g	6 Mbps OFDM	-	-88	-	dBm
	9 Mbps OFDM	-	-87	-	
	12 Mbps OFDM	-	-86	-	
	18 Mbps OFDM	-	-84	-	
	24 Mbps OFDM	-	-82	-	
	36 Mbps OFDM	-	-78	-	
	48 Mbps OFDM	-	-74	-	
	54 Mbps OFDM	-	-73	-	
Sensitivity 802.11n (BW at 20 MHz)	MCS 0	-	-87	-	dBm
	MCS 1	-	-85	-	
	MCS 2	-	-83	-	
	MCS 3	-	-80	-	
	MCS 4	-	-76	-	
	MCS 5	-	-73	-	
	MCS 6	-	-71	-	
	MCS 7	-	-69	-	
Maximum Receive Signal Level	1-11 Mbps DSSS	-	0	-	dBm
	6-54 Mbps OFDM	-	-5	-	
	MCS 0 – 7	-	-5	-	
Adjacent Channel Rejection	1 Mbps DSSS (30 MHz offset)	-	50	-	dB
	11 Mbps DSSS (25 MHz offset)	-	43	-	
	6 Mbps OFDM (25 MHz offset)	-	40	-	
	54 Mbps OFDM (25 MHz offset)	-	25	-	
	MCS 0 – 20 MHz BW (25 MHz offset)	-	40	-	
	MCS 7 – 20 MHz BW (25 MHz offset)	-	20	-	

.....continued					
Parameter	**Description**	**Min.**	**Typ.**	**Max.**	**Unit**
Cellular Blocker Immunity	776-794 MHz CDMA	-	-14	-	dBm
	824-849 MHz GSM	-	-10	-	
	880-915 MHz GSM	-	-10	-	
	1710-1785 MHz GSM	-	-15	-	
	1850-1910 MHz GSM	-	-15	-	
	1850-1910 MHz WCDMA	-	-24	-	
	1920-1980 MHz WCDMA	-	-24	-	

7.3.2 Transmitter Performance

The following are typical conditions for radio transmitter performance:

VBAT=3.3V; VDDIO=3.3V; temperature at 25°C and WLAN Channel 6 (2437 MHz).

The following table provides the transmitter performance characteristics for the ATWILC1000B.

Table 7-3. Transmitter Performance

Parameter	Description	Min.	Typ.	Max.	Unit
Frequency	-	2,412		2,472	MHz
Output power(1)-(2), ON_Transmit	802.11b 1Mbps	-	17.6	-	dBm
	802.11b 11Mbps	-	18.2	-	
	802.11g 6Mbps	-	18.7	-	
	802.11g 54Mbps	-	16.7	-	
	802.11n MCS 0	-	17.3	-	
	802.11n MCS 7	-	13.8	-	
TX power accuracy	-	-	±1.5 (2)		dB
Carrier suppression	802.11b mode	-	-19.4	-	dBc
	802.11g mode	-	-27.5	-	
	802.11n mode	-	-21.1	-	

.....continued

Parameter	Description	Min.	Typ.	Max.	Unit
Out of band Transmit Power	76-108	-	-125	-	dBm/Hz
	776-794	-	-125	-	
	869-960	-	-125	-	
	925-960	-	-125	-	
	1570-1580	-	-125	-	
	1805-1880	-	-125	-	
	1930-1990	-	-125	-	
	2110-2170	-	-125	-	
Harmonic output power(4)	2nd	-	-28	-	dBm/MHz
	3rd	-	-33	-	
	4th	-	-40	-	
	5th	-	-28	-	

Note:

1. Measured at 802.11 specification compliant EVM/Spectral mask.
2. Measured after RF matching network.
3. Operating temperature range is -40ºC to +85ºC. RF performance is ensured at a room temperature range of 25ºC with 2-3dB change at boundary conditions.
4. Measured at 11 Mbps, DG (Digital Gain) = -7, WLAN Channel 6 (2437 MHz).
5. With respect to TX power, different (higher/lower) RF output power settings may be used for specific antennas and/or enclosures, in which case re-certification may be required.
6. The availability of some specific channels and/or operational frequency bands are country dependent and should be programmed at the host product factory to match the intended destination. Regulatory bodies prohibit exposing the settings to the end user. This requirement needs to be taken care of via host implementation.

8. External Interfaces

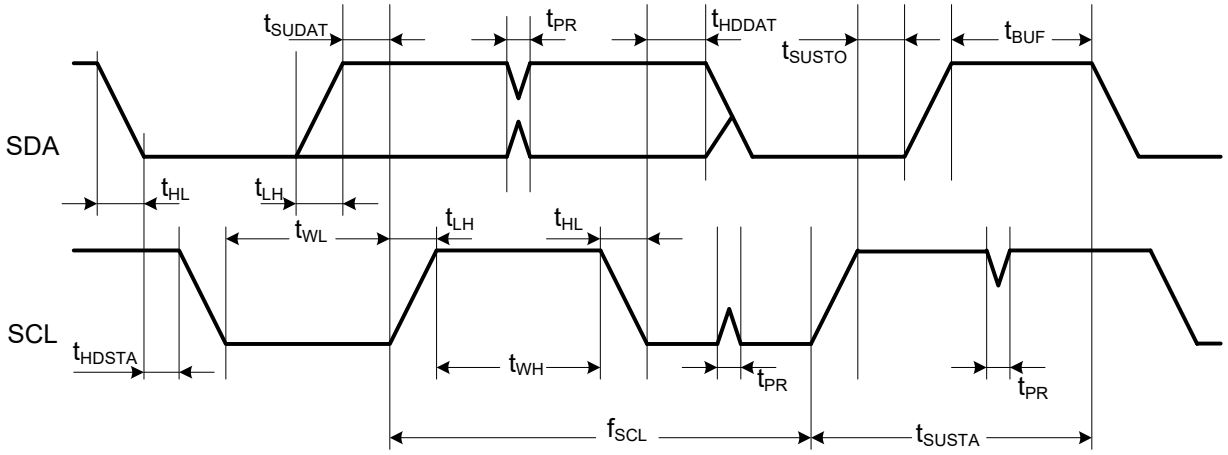
The ATWILC1000B external interfaces include:

- I²C slave for control
- SPI slave and SDIO slave for control and data transfer
- SPI master for external Flash
- I²C master for external EEPROM
- UART Debug Interface
- General Purpose Input/Output (GPIO) pins

8.1 I²C Slave Interface

The I²C Slave interface, used primarily for control by the host processor, is a two-wire serial interface consisting of a serial data line (SDA, Pin 33) and a serial clock (SCL, pin 32). It responds to the seven bit address value 0x60. The ATWILC1000B I²C supports I²C bus Version 2.1 - 2000 and can operate in Standard mode (with data rates up to 100 Kb/s) and Fast mode (with data rates up to 400 Kb/s). The I²C Slave is a synchronous serial interface. The SDA line is a bidirectional signal and changes only while the SCL line is low, except for STOP, START, and RESTART conditions. The output drivers are open-drain to perform wire-AND functions on the bus. The maximum number of devices on the bus is limited by only the maximum capacitance specification of 400 pF. Data is transmitted in byte packages. For specific information, refer to the Philips Specification entitled “The I²C -Bus Specification, Version 2.1”. The I²C Slave timing is provided in the following figure.

Figure 8-1. I²C Slave Timing Diagram



The I²C Slave timing parameters are provided in the following table.

Table 8-1. I²C Slave Timing Parameters

Parameter	Symbol	Min.	Max.	Unit	Remarks
SCL clock frequency	f_{SCL}	0	400	kHz	–
SCL low pulse width	t_{WL}	1.3	–	µs	–
SCL high pulse width	t_{WH}	0.6	–		–

.....continued					
Parameter	**Symbol**	**Min.**	**Max.**	**Unit**	**Remarks**
SCL, SDA fall time	t_{HL}	–	300	ns	–
SCL, SDA rise time	t_{LH}	–	300		This is dictated by external components
START setup time	t_{SUSTA}	0.6	–	µs	–
START hold time	t_{HDSTA}	0.6	–		–
SDA setup time	t_{SUDAT}	100	–	ns	–
SDA hold time	t_{HDDAT}	0 40	–		Slave and master default master programming option
STOP setup time	t_{SUSTO}	0.6	–	µs	–
Bus free time between STOP and START	t_{BUF}	1.3	–		–
Glitch pulse reject	t_{PR}	0	50	ns	–

8.2 I²C Master Interface

The ATWILC1000B provides an I²C bus master, which is intended primarily for accessing an external EEPROM memory through a software-defined protocol. The I²C Master is a two-wire serial interface consisting of a serial data line (SDA) and a serial clock line (SCL). SDA can be configured on one of the following pins: SD_CLK (pin 19), GPIO1 (pin 24), GPIO6 (pin 31), or I2C_SDA (pin 33). SCL can be configured on one of the following pins: GPIO0 (pin 10), SD_DAT3 (pin 12), GPIO4 (pin 29), or I2C_SCL (pin 32). For more specific instructions refer to the ATWILC1000 Programming Guide.

The I²C master interface supports three speeds:

- Standard mode (100 kb/s)
- Fast mode (400 kb/s)
- High-Speed mode (3.4 Mb/s)

The timing diagram of the I²C master interface is the same as that of the I²C slave interface (see Figure 8-1). The timing parameters of I²C master are shown in the following table.

Table 8-2. I²C Master Timing Parameters

Parameter	Symbol	Standard Mode		Fast Mode		High-Speed Mode		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
SCL clock frequency	f_{SCL}	0	100	0	400	0	3400	kHz
SCL high pulse width	t_{WH}	4	–	0.6	–	0.06	–	µs
SCL low pulse width	t_{WL}	4.7	–	1.3	–	0.16	–	

.....continued

Parameter	Symbol	Standard Mode		Fast Mode		High-Speed Mode		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
SCL fall time	t_{HLSCL}	–	300	–	300	10	40	ns
SDA fall time	t_{HLSDA}	–	300		300	10	80	
SCL rise time	t_{LHSCL}	–	1000	–	300	10	40	
SDA rise time	t_{LHSDA}	–	1000	–	300	10	80	
START setup time	t_{SUSTA}	4.7	–	0.6	–	0.16	–	µs
START hold time	t_{HDSTA}	4	–	0.6	–	0.16	–	
SDA setup time	t_{SUDAT}	250	–	100	–	10	–	ns
SDA hold time	t_{HDDAT}	5	–	40	–	0	70	
STOP setup time	t_{SUSTO}	4	–	0.6	–	0.16	–	µs
Bus free time between STOP and START	t_{BUF}	4.7	–	1.3	–	–	–	
Glitch pulse reject	t_{PR}	–	–	0	50	–	–	

8.3 SPI Slave Interface

The ATWILC1000B provides a Serial Peripheral Interface (SPI) that operates as an SPI slave. The SPI Slave interface can be used for control and for serial I/O of 802.11 data. The SPI Slave pins are mapped as shown in the the following table. The RXD pin is same as Master Output, Slave Input (MOSI), and the TXD pin is same as Master Input, Slave Output (MISO). The SPI Slave is a full-duplex slave-synchronous serial interface that is available immediately following reset when pin 9 (SDIO_SPI_CFG) is tied to VDDIO.

Table 8-3. SPI Slave Interface Pin Mapping

Pin Number	SPI Function
9	CFG: Must be tied to VDDIO
16	SSN: Active Low Slave Select
18	SCK: Serial Clock
13	RXD: Serial Data Receive (MOSI)
17	TXD: Serial Data Transmit (MISO)

When the SPI is not selected, i.e., when SSN is high, the SPI interface does not interfere with data transfers between the serial-master and other serial-slave devices. When the serial slave is not selected, its transmitted data output is buffered, resulting in a high impedance drive onto the serial master receive line.

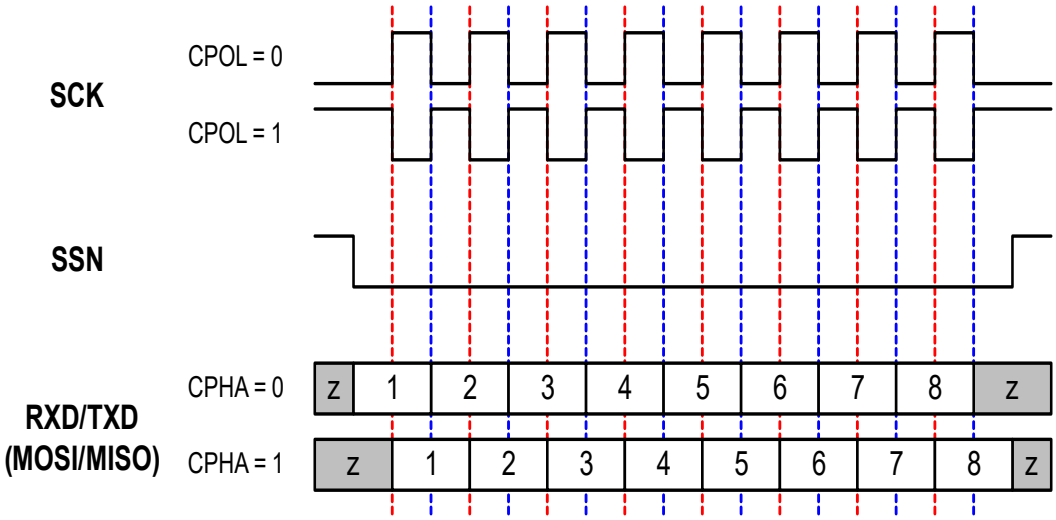
The SPI Slave interface responds to a protocol that allows an external host to read or write any register in the chip as well as initiate DMA transfers. For more details of the SPI protocol and more specific instructions, refer to the ATWILC1000 Programming Guide.

The SPI Slave interface supports four standard modes as determined by the Clock Polarity (CPOL) and Clock Phase (CPHA) settings. These modes are illustrated in table SPI Slave Modes and Figure 8-2. The red lines in this figure correspond to Clock Phase = 0 and the blue lines correspond to Clock Phase = 1.

Table 8-4. SPI Slave Modes

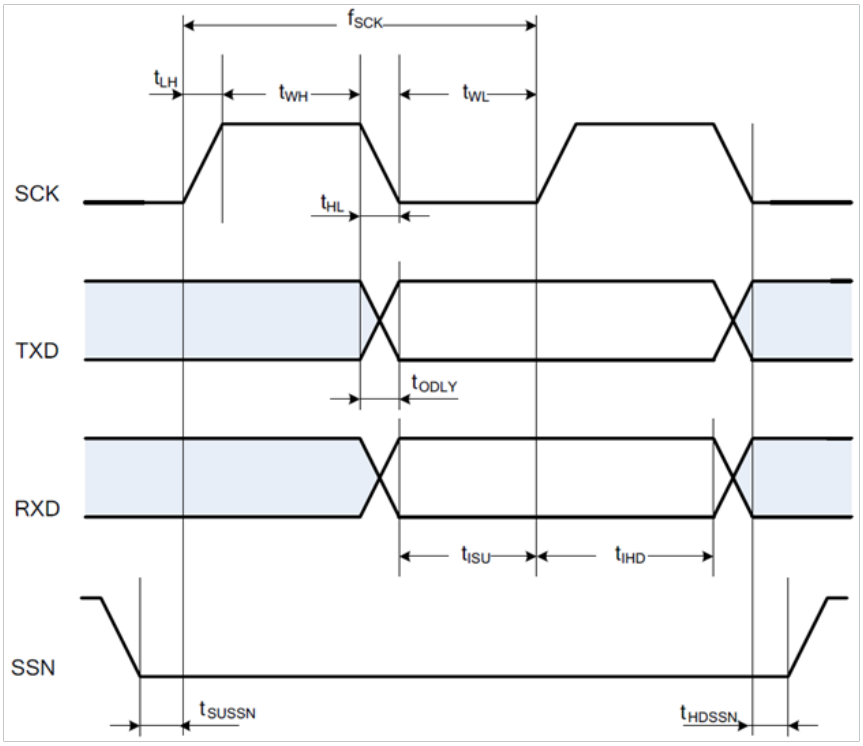
Mode	CPOL	CPHA
0	0	0
1	0	1
2	1	0
3	1	1

Figure 8-2. SPI Slave Clock Polarity and Clock Phase Timing



The SPI slave timing is provided in the following figure.

Figure 8-3. SPI Slave Timing Diagram



The SPI slave timing parameters are provided in the following table.

Table 8-5. SPI Slave Timing Parameters

Parameter	Symbol	Min.	Max.	Unit
Clock input frequency	f_{SCK}	–	48	MHz
Clock low pulse width	t_{WL}	15	–	ns
Clock high pulse width	t_{WH}	15	–	
Clock rise time	t_{LH}	–	10	
Clock fall time	t_{HL}	–	10	
Input setup time	t_{ISU}	5	–	
Input hold time	t_{IHD}	5	–	
Output delay	t_{ODLY}	0	20	
Slave select setup time	t_{SUSSN}	5	–	
Slave select hold time	t_{HDSSN}	5	–	

8.4 SPI Master Interface

The ATWILC1000B provides an SPI master interface for accessing external Flash memory. The SPI master pins are mapped as shown in the following table. The TXD pin is same as Master Output, Slave Input (MOSI), and the RXD pin is same as Master Input, Slave Output (MISO). The SPI master interface supports all four standard modes of clock polarity and clock phase shown in Table 8-4. External SPI Flash

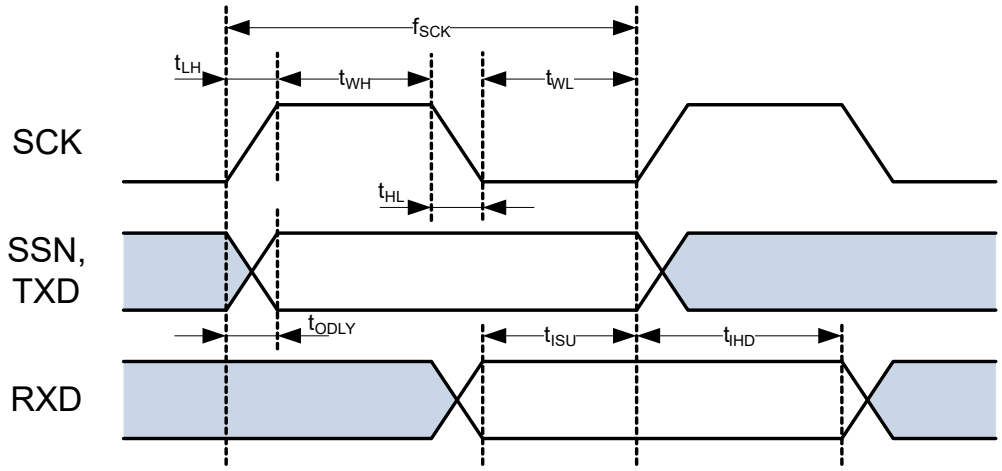
memory is accessed by a processor programming commands to the SPI master interface, which in turn initiates a SPI master access to the Flash. For more specific instructions, refer to the ATWILC1000 Programming Guide.

Table 8-6. SPI Master Interface Pin Mapping

Pin Number	Pin Name	SPI Function
28	GPIO3	SCK: Serial Clock Output
29	GPIO4	SCK: Active-Low Slave Select Output
30	GPIO5	TXD: Serial Data Transmit Output (MOSI)
31	GPIO6	RXD: Serial Data Receive Input (MISO)

The SPI master timing is provided in the following figure.

Figure 8-4. SPI Master Timing Diagram



The SPI master timing parameters are provided in the following table.

Table 8-7. SPI Master Timing Parameters

Parameter	Symbol	Min.	Max.	Unit
Clock output frequency	f_{SCK}	–	48	MHz
Clock low pulse width	t_{WL}	5	–	ns
Clock high pulse width	t_{WH}	5	–	
Clock rise time	t_{LH}	–	5	
Clock fall time	t_{HL}	–	5	
Input setup time	t_{ISU}	5	–	
Input hold time	t_{IHD}	5	–	
Output delay	t_{ODLY}	0	5	

8.5 SDIO Slave Interface

The ATWILC1000B SDIO Slave is a full speed interface. The interface supports the 1-bit/4-bit SD Transfer mode at the clock range of 0 to 50 MHz. The host can use this interface to read and write from any register within the chip as well as configure the ATWILC1000B for data DMA. To use this interface, pin 9 (SDIO_SPI_CFG) must be grounded. The SDIO slave pins are mapped as shown in the following table.

Table 8-8. SDIO Interface Pin Mapping

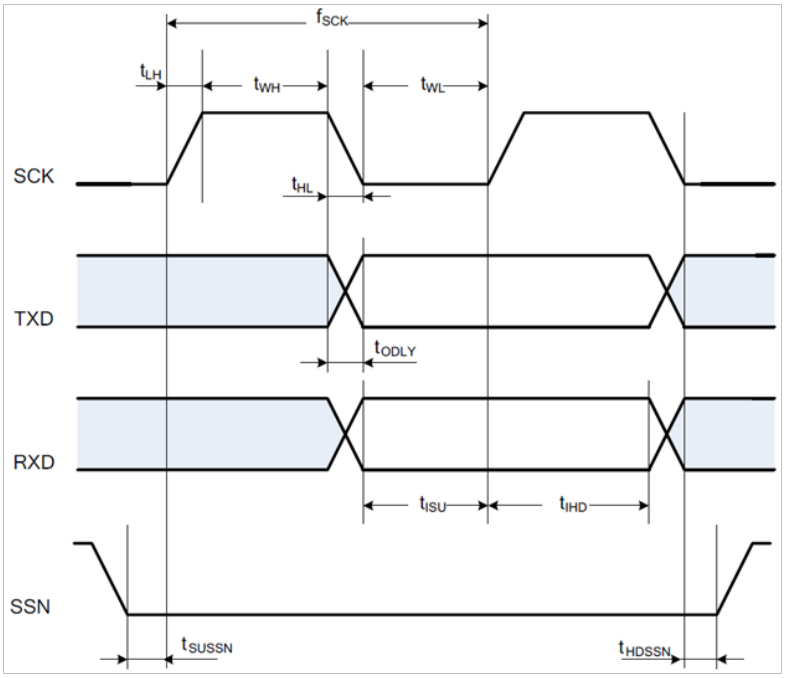
Pin Number	SPI Function
9	CFG: Must be tied to ground
12	DAT3: Data 3
13	DAT2: Data 2
16	DAT1: Data 1
17	DAT0: Data 0
18	CMD: Command
19	CLK: Clock

When the SDIO card is inserted into an SDIO aware host, the detection of the card will be via the means described in SDIO specification. During the normal initialization and interrogation of the card by the host, the card identifies itself as an SDIO device. The host software obtains the card information in a tuple (linked list) format and determines if that card's I/O function(s) are acceptable to activate. If the card is acceptable, it is allowed to power-up fully and start the I/O function(s) built into it. The SD memory card communication is based on an advanced 9-pin interface (clock, command, four data and three power lines) designed to operate at a maximum operating frequency of 50 MHz. The SDIO slave interface has the following features:

- Meets SDIO card specification version 2.0
- Host clock rate variable between 0 to 50 MHz
- 1 bit/4-bit SD bus modes supported
- Allows card to interrupt host
- Responds to direct read/write (IO52) and extended read/write (IO53) transactions
- Supports Suspend/Resume operation

The SDIO slave interface timing is provided in the following figure.

Figure 8-5. SDIO Slave Timing Diagram



The SDIO slave timing parameters are provided in the following table.

Table 8-9. SDIO Slave Timing Parameters

Parameter	Symbol	Min.	Max.	Unit
Clock input frequency	f_{PP}	0	50	MHz
Clock low pulse width	t_{WL}	10	–	ns
Clock high pulse width	t_{WH}	10	–	
Clock rise time	t_{LH}	–	10	
Clock fall time	t_{HL}	–	10	
Input setup time	t_{ISU}	5	–	
Input hold time	t_{IH}	5	–	
Output delay	t_{ODLY}	0	14	

8.6 UART Debug Interface

ATWILC1000B has a Universal Asynchronous Receiver/Transmitter (UART) interface on pin 13, SD-DATA2/SPI-RxD and pin 17, SD-DATA0/SPI-TXD. This interface should be used only for debugging purposes. The UART is compatible with the RS-232 standard, where ATWILC1000B-MUT operates as Data Terminal Equipment (DTE). It has a two-pin RXD/TXD interface.

The default configuration for accessing the UART interface of ATWILC1000B-MUT is as follows:

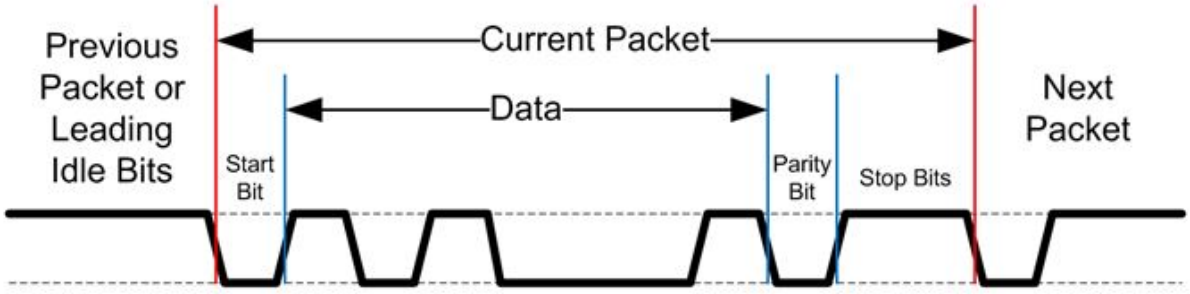
- Baud rate: 115200
- Data: 8 bit
- Parity: None

- Stop bit: 1 bit
- Flow control: None

It also has Rx and Tx FIFOs, which ensures reliable high speed reception and low software overhead transmission. FIFO size is 4x8 for both Rx and Tx direction. The UART has status registers that show the number of received characters available in the FIFO and various error conditions; in addition, it has the ability to generate interrupts based on these status bits.

An example of UART receiving or transmitting a single packet is shown in the following figure. This example shows 7-bit data (0x45), odd parity, and two stop bits.

Figure 8-6. Example of UART RX or TX Packet



8.7 GPIOs

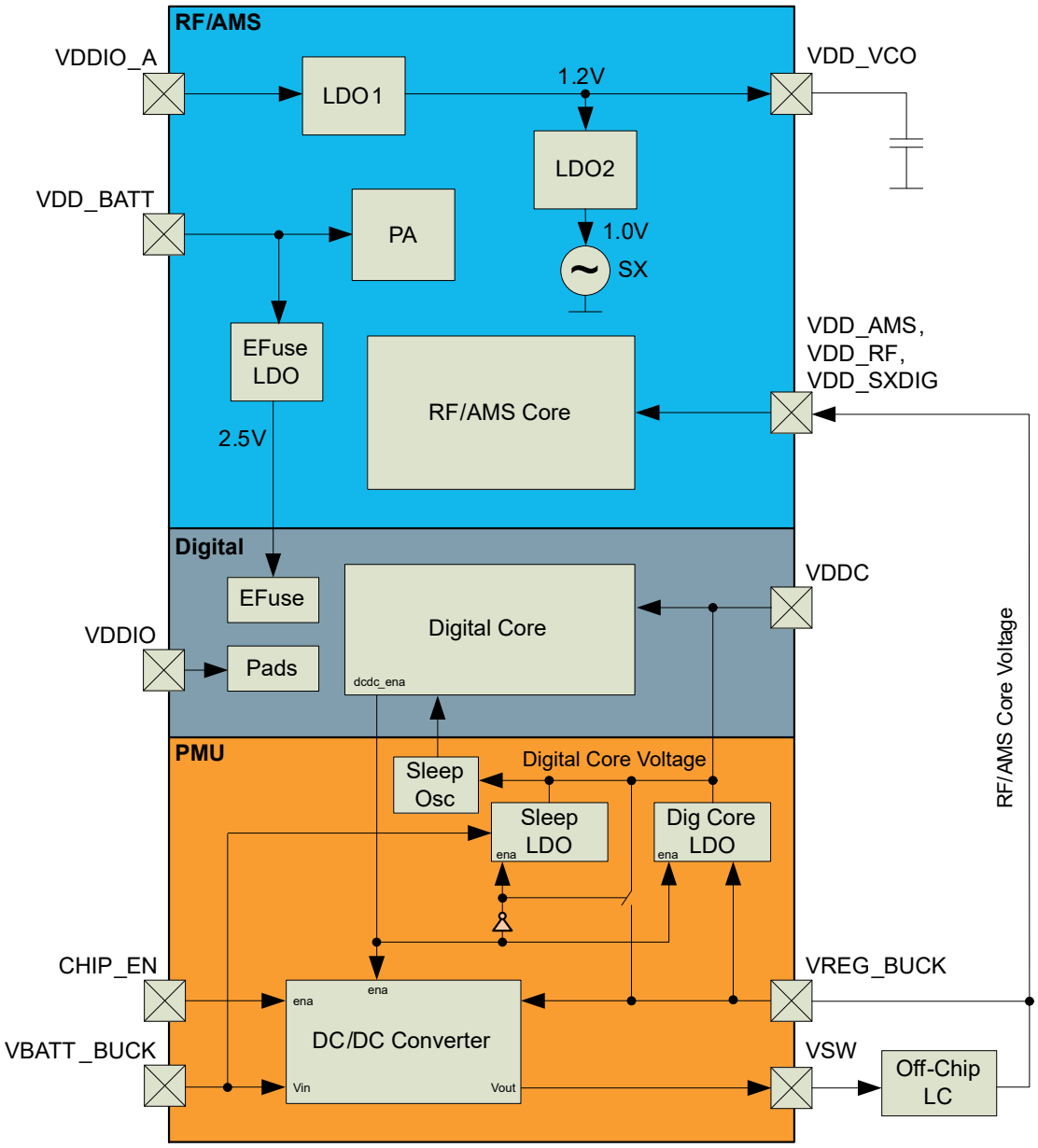
Nine General Purpose Input/Output (GPIO) pins, labeled GPIO 0-8, are available to allow for application specific functions. Each GPIO pin can be programmed as an input (the value of the pin can be read by the host or internal processor) or as an output (the output values can be programmed by the host or internal processor), where the default mode after power-up is input. GPIOs 7 and 8 are only available when the host does not use the SDIO interface, which shares two of its pins with these GPIOs. Therefore, for SDIO-based applications, seven GPIOs (0-6) are available. For more specific usage instructions refer to the ATWILC1000 Programming Guide.

9. Power Management

9.1 Power Architecture

The ATWILC1000B uses an innovative power architecture to eliminate the need for external regulators and reduce the number of off-chip components. This architecture is shown in the following figure. The Power Management Unit (PMU) has a DC/DC Converter that converts VBATT to the core supply used by the digital and RF/AMS blocks. The PA and eFuse are supplied by dedicated LDOs, and the VCO is supplied by a separate LDO structure. The power connections in the following figure provide a conceptual framework for understanding the ATWILC1000B power architecture.

Figure 9-1. Power Architecture



The following table provides the typical values for the digital and RF/AMS core voltages.

Table 9-1. PMU Output Voltages

Parameter	Typical
RF/AMS core voltage (VREG_BUCK)	1.35V
Digital core voltage (VDDC)	1.10V

Refer to the reference design for an example of power supply connections, including proper isolation of the supplies used by the digital and RF/AMS blocks.

9.2 Power Consumption

The ATWILC1000B has several device states:

- ON_Transmit – Device is actively transmitting an 802.11 signal
- ON_Receive – Device is actively receiving an 802.11 signal
- ON_Doze – Device is on but is neither transmitting nor receiving
- Power_Down – Device core supply off (leakage)

The following pins are used to switch between the ON and Power_Down states:

- CHIP_EN – Device pin (pin 23) used to enable DC/DC Converter
- VDDIO – I/O supply voltage from external supply

In the ON states, VDDIO is on and CHIP_EN is high (at VDDIO voltage level). To switch between the ON states and Power_Down state, CHIP_EN has to change between high and low (GND) voltage. When VDDIO is off and CHIP_EN is low, the chip is powered off with no leakage (also see 9.3 Power-Up/Down Sequence).

9.2.1 Current Consumption in Various Device States

The following table provides the ATWILC1000B current consumption in various device states.

Table 9-2. Current Consumption

Device State	Code Rate	Output Power (dBm)	Current Consumption(1)	
			I_{VBATT}	I_{VDDIO}
ON_Transmit	802.11b 1 Mbps	17.6	266 mA	22 mA
	802.11b 11 Mbps	18.5	239 mA	22 mA
	802.11g 6 Mbps	18.6	249 mA	22 mA
	802.11g 54 Mbps	16.9	173 mA	22 mA
	802.11n MCS 0	17.7	253 mA	22 mA
	802.11n MCS 7	14.0	164 mA	22 mA

.....continued

Device State	Code Rate	Output Power (dBm)	Current Consumption(1)	
			I_{VBATT}	I_{VDDIO}
ON_Receive	802.11b 1 Mbps	N/A	63 mA	22 mA
	802.11b 11 Mbps	N/A	63 mA	22 mA
	802.11g 6 Mbps	N/A	63 mA	22 mA
	802.11g 54 Mbps	N/A	63 mA	22 mA
	802.11n MCS 0	N/A	63 mA	22 mA
	802.11n MCS 7	N/A	63 mA	22 mA
ON_Doze	N/A	N/A	380 µA	<10 µA
Power_Down	N/A	N/A	1.25 µA (2)	

Note:

1. The power consumption values are measured when VBAT is 3.6V and VDDIO is 2.8V at 25°C.

9.2.2 Controlling the Device States

Table "Device States" shows how to switch between the device states using the following:

- CHIP_EN – Device pin (pin #23) used to enable DC/DC Converter
- VDDIO – I/O supply voltage from external supply

Table 9-3. Device States

Device State	CHIP_EN	VDDIO	Power Consumption (1), (2)	
			I_{VBATT}	I_{VDDIO}
ON_Transmit	VDDIO	On	172mA @ 18dBm (≤18Mbps) 230mA @ 18dBm (>18Mbps)	2mA
ON_Receive	VDDIO	On	60mA	2mA
ON_Doze	VDDIO	ON	280µA	<10µA
Power_Down	GND	On	<0.5µA	<0.2µA

Note:

1. Conditions: VBAT @ 3.6v, I/O@1.8V.
2. Power consumption numbers are preliminary.

9.2.3 Restrictions for Power States

When no power is supplied to the device, i.e., the DC/DC converter output and VDDIO are both off (at ground potential). In this case, a voltage cannot be applied to the device pins because each pin contains an ESD diode from the pin to supply. This diode turns on when voltage higher than one diode-drop is supplied to the pin.

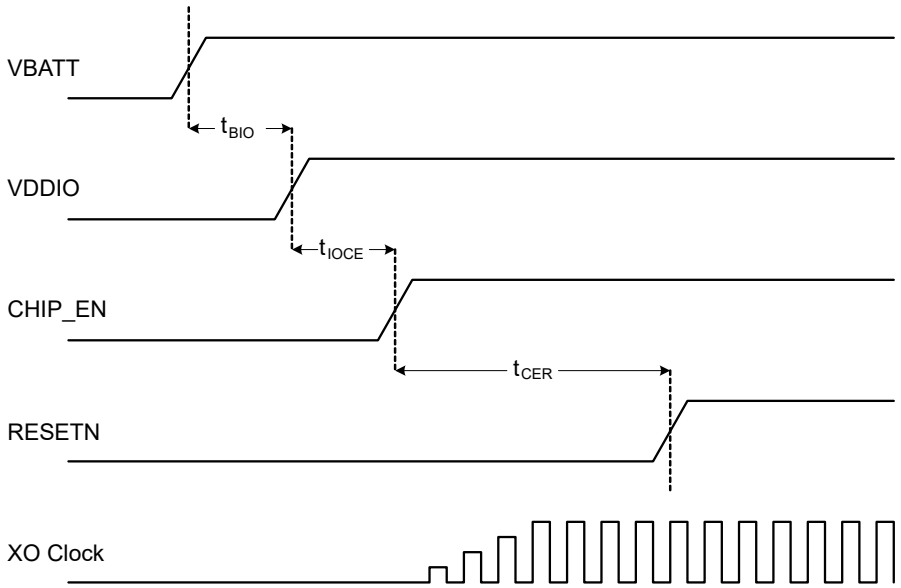
If a voltage must be applied to the signal pads while the chip is in a low power state, the VDDIO supply must be on, so the SLEEP or Power_Down state must be used.

Similarly, to prevent the pin-to-ground diode from turning on, do not apply a voltage that is more than one diode-drop below ground to any pin.

9.3 Power-Up/Down Sequence

The power-up/down sequence for the ATWILC1000B is shown in the following figure.

Figure 9-2. Power-Up/Down Sequence



The timing parameters are provided in the following table.

Table 9-4. Power-Up/Down Sequence Timing

Parameter	Min.	Max.	Unit	Description	Notes
t_A	0	–	ms	VBATT rise to VDDIO rise	VBATT and VDDIO can rise simultaneously or can be tied together. VDDIO must not rise before VBATT.
t_B	0	–		VDDIO rise to CHIP_EN rise	CHIP_EN must not rise before VDDIO. CHIP_EN must be driven high or low, not left floating.
t_C	5	–		CHIP_EN rise to RESETN rise	This delay is needed because XO clock must stabilize before RESETN removal. RESETN must be driven high or low, not left floating.
t_A	0	–		VDDIO fall to VBATT fall	VBATT and VDDIO can fall simultaneously or can be tied together. VBATT must not fall before VDDIO.
t_B	0	–		CHIP_EN fall to VDDIO fall	VDDIO must not fall before CHIP_EN. CHIP_EN and RESETN can fall simultaneously.
t_C	0	–		RESETN fall to VDDIO fall	VDDIO must not fall before RESETN. RESETN and CHIP_EN can fall simultaneously.

9.4 Digital I/O Pin Behavior During Power-up Sequences

The following table represents digital I/O pin states corresponding to device power modes.

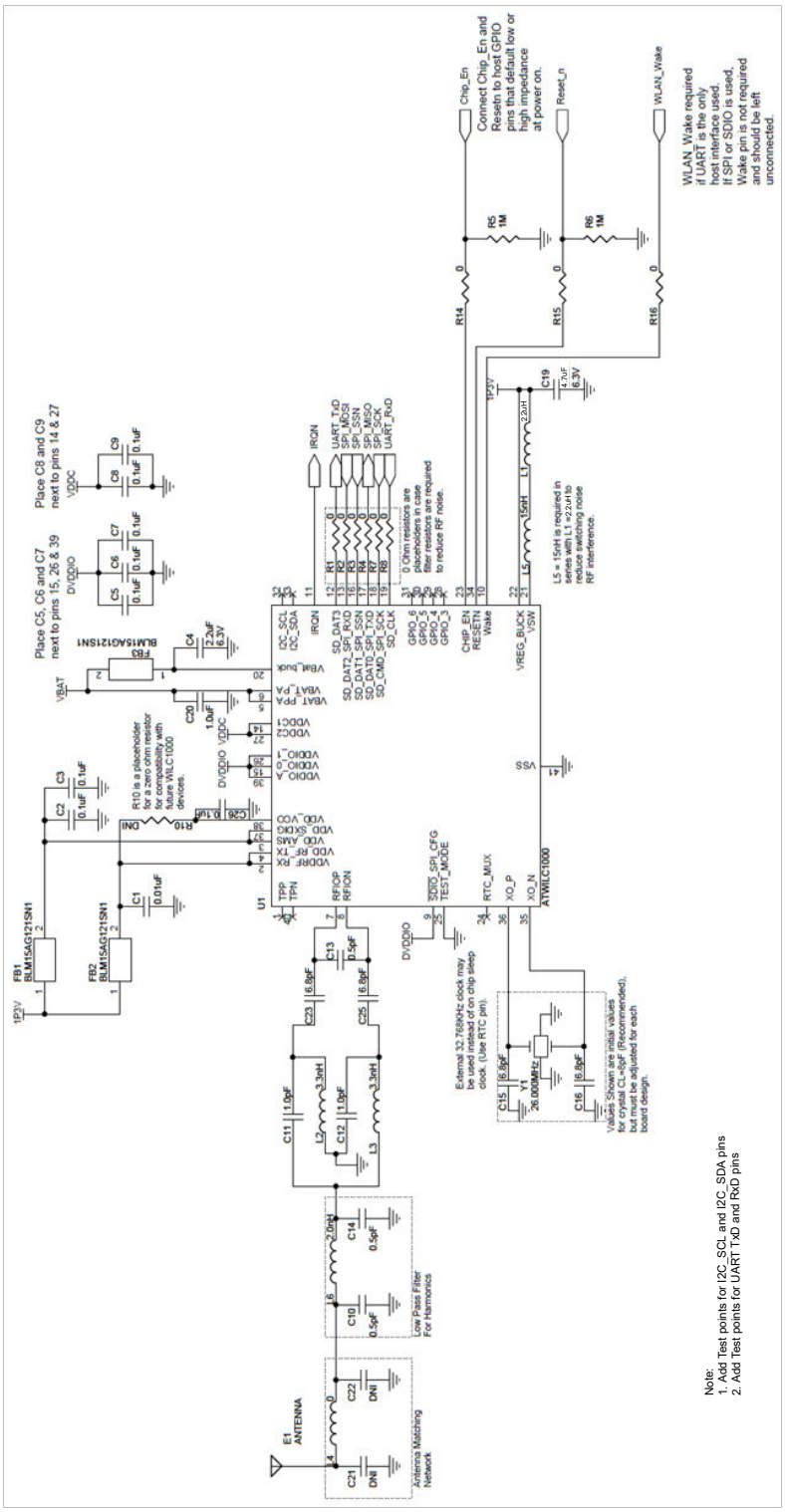
Table 9-5. Digital I/O Pin Behavior in Different Device States

Device State	VDDIO	CHIP_EN	RESETN	Output Driver	Input Driver	Pull-Up/Down Resistor (96kΩ)
Power_Down: core supply off	High	Low	Low	Disabled (Hi-Z)	Disabled	Disabled
Power-On Reset: core supply on, hard reset on	High	High	Low	Disabled (Hi-Z)	Disabled	Enabled
Power-On Default: core supply on, device out of reset but not programmed yet	High	High	High	Disabled (Hi-Z)	Enabled	Enabled
On_Doze/ On_Transmit/ On_Receive: core supply on, device programmed by firmware	High	High	High	Programmed by firmware for each pin: Enabled or Disabled	Opposite of output driver state	Programmed by firmware for each pin: Enabled or Disabled

10. Reference Design

The ATWILC1000B reference design schematic is shown in the following figure.

Figure 10-1. ATWILC1000B Reference Schematic



11. Reflow Profile Information

This section provides the guidelines for the reflow process to get ATWILC1000B soldered to the customer's design.

11.1 Storage Condition

11.1.1 Moisture Barrier Bag Before Opening

A moisture barrier bag must be stored in a temperature of less than 30°C with humidity under 85% RH. The calculated shelf life for the dry-packed product shall be 12 months from the date the bag is sealed.

11.1.2 Moisture Barrier Bag Open

Humidity indicator cards must be blue, indicating that the humidity is <30%.

11.2 Solder Paste

SnAgCu eutectic solder with melting temperature of 217°C is most commonly used for lead-free solder reflow application. This alloy is widely accepted in the semiconductor industry due to its low cost, relatively low melting temperature, and good thermal fatigue resistance. Some recommended pastes include NC-SMQ® 230 flux and Indalloy® 241 solder paste made up of 95.5 Sn/3.8 Ag/0.7 Cu or SENJU N705-GRN3360-K2-V Type 3, no clean paste.

11.3 Stencil Design

The recommended stencil is laser-cut, stainless-steel type with thickness of 100 µm to 130 µm and approximately a 1:1 ratio of stencil opening to pad dimension. To improve paste release, a positive taper with bottom opening 25 µm larger than the top is utilized. Local manufacturing experience may find other combinations of stencil thickness and aperture size to get good results.

11.4 Printing Process

The printing process requires no significant changes compared to Sn/Pb solder. Any guidelines recommended by the paste manufacturers to accommodate paste specific characteristics should be followed. Post-print inspection and paste volume measurement is very critical to ensure good print quality and uniform paste.

11.5 Baking Conditions

ATWILC1000B is rated at MSL level 3. After the sealed bag is opened, no baking is required within 168 hours as long as the devices are held at ≤ 30°C/60% RH or stored at < 10% RH.

ATWILC1000B requires baking before mounting if:

- The sealed bag has been open for more than 168 hours
- The humidity indicator card reads more than 10%
- SIPs need to be baked for eight hours at 125°C

11.6 Soldering and Reflow Condition

Optimization of the reflow process is the most critical factor considered for lead-free soldering. The development of an optimal profile must account the paste characteristics, the size of the board, the density of the components, the mix of the larger and smaller components, and the peak temperature requirements of the components. An optimized reflow process is the key to ensuring a successful lead-free assembly and achieves high yield and long-term solder joint reliability.

Temperature Profiling

Temperature profiling must be performed for all new board designs by attaching thermocouples at the solder joints, on the top surface of the larger components, and at multiple locations of the boards. This is to ensure that all components are heated to a temperature above the minimum reflow temperatures and the smaller components do not exceed the maximum temperature limit. The SnAgCu solder alloy melts at ~217°C, so the reflow temperature peak at joint level must be 15 to 20°C higher than melting temperature. The targeted solder joint temperature for the SnAgCu solder must be ~235°C. For larger or sophisticated boards with a large mix of components, it is also important to ensure that the temperature difference across the board is less than 10 degrees to minimize board warpage. The maximum temperature at the component body must not exceed the MSL3 qualification specification.

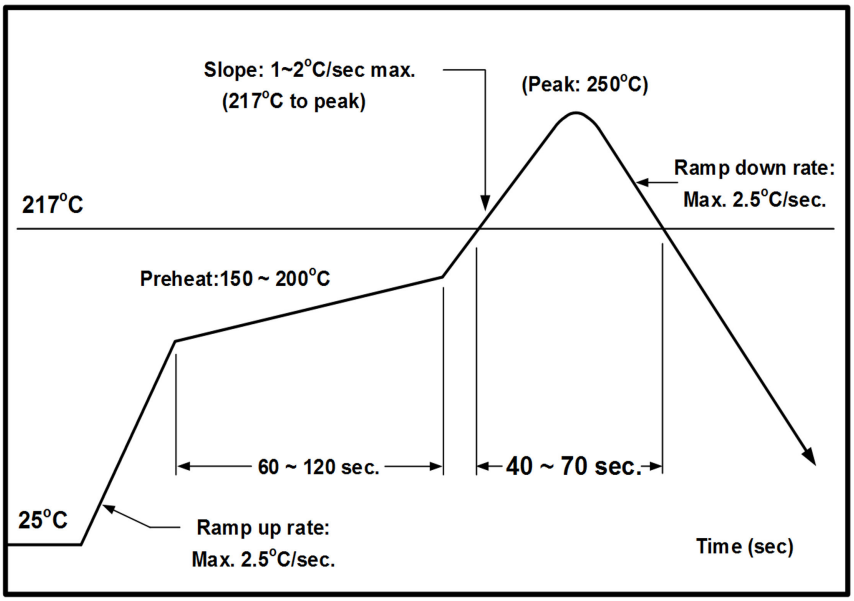
11.6.1 Reflow Oven

It is strongly recommended that a reflow oven equipped with more heating zones and Nitrogen atmosphere be used for lead-free assembly. Nitrogen atmosphere has shown to improve the wet-ability and reduce temperature gradient across the board. It can also enhance the appearance of the solder joints by reducing the effects of oxidation.

The following items should also be observed in the reflow process.

1. Some recommended pastes include:
   - NC-SMQ® 230 flux and Indalloy® 241 solder paste made up of 95.5 Sn/3.8 Ag/0.7 Cu
   - SENJU N705-GRN3360-K2-V Type 3, no clean paste
2. Allowable reflow soldering iterations:
   - Three times based on the following reflow soldering profile (refer following Figure).
3. Temperature profile:
   - Reflow soldering shall be done according to the following temperature profile (refer to the following figure).
   - Peak temperature: 250°C.

Figure 11-1. Solder Reflow Profile



Cleaning

The exposed ground paddle helps to self-align ATWILC1000B, avoiding pad misalignment. The use of no-clean solder pastes is recommended. Full drying of no-clean paste fluxes must be ensured as a result of the reflow process. This may require longer reflow profiles and/or peak temperatures toward the high end of the process window as recommended by the solder paste vendor. It is believed that uncured flux residues could lead to corrosion and/or shorting in accelerated testing and possibly the field.

Rework

Rework is to remove the mounted SIP package and replace with a new unit. It is recommended that once ATWILC1000B has been removed it should never be reused. During the rework process, the mounted ATWILC1000B and PCB are heated partially, and ATWILC1000B is removed. It is recommended to heat-proof the proximity of the mounted parts and junctions and use the best nozzle for rework that is suited to the module size.

12. Reference Documentation and Support

The following table provides the set of collateral documents to ease integration and device ramp.

Table 12-1. Reference Documents

Title	Content
Design Files Package	User Guide, Schematic, PCB layout, Gerber, BOM and System notes on: RF/ Radio Full Test Report, radiation pattern, design guidelines, temperature performance, ESD.
Platform Getting started Guide	How-to-use package: Out of the Box starting guide, HW limitations and notes, SW Quick start guidelines.
HW Design Guide	Best practices and recommendations to design a board with the product, including: Antenna Design for Wi-Fi (layout recommendations, types of antennas, impedance matching, using a power amplifier etc.), SPI/UART protocol between Wi-Fi SoC and the Host MCU.
SW Design Guide	Integration guide with clear description of: High level Arch, overview on how to write a networking application, list all API, parameters and structures. Features of the device, SPI/handshake protocol between device and host MCU, flow/sequence/ state diagram, and timing.
SW Programmer Guide	Explains in detail the flow chart and how to use each API to implement all generic use cases (e.g. start AP, start STA, provisioning, UDP, TCP, http, TLS, p2p, errors management, connection/transfer recovery mechanism/state diagram) – usage and sample application note.

For a complete listing of development-support tools and documentation, visit the ATWILC1000 webpage, or refer to the customer support section on options to contact the nearest Microchip field representative.

13. Document Revision History

Revision	Date	Section	Description
A	12/2018	Document	• Updated from Atmel to Microchip template. • Assigned a new Microchip document number. Previous version is Atmel 42351 revision D. • ISBN number added.

Document Revision History-Atmel

Doc. Rev.	Date	Comments
42351D	05/2015	DS update to Rev. B offering. Changes from ATWILC1000A to ATWILC1000B: 1. Added second UART, increased UART data rates. 2. Increased instruction RAM size from 128KB to 160KB. 3. Updated pin MUX table: added new options for various interfaces. 4. Improved description of Coexistence interface. 5. Added VDD_VCO switch and connection in the power architecture. 6. Updated power consumption numbers. 7. Updated reference schematic. 8. Changed RTC_CLK pad definition from pull-down to pull-up
42351C	02/2015	DS update new Atmel format.
42351B	11/2014	Major document update, new sections added, replaced text in most sections, new and updated drawings.
42351A	07/2014	Initial document release.

The Microchip Web Site

Microchip provides online support via our web site at http://www.microchip.com/. This web site is used as a means to make files and information easily available to customers. Accessible by using your favorite Internet browser, the web site contains the following information:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQ), technical support requests, online discussion groups, Microchip consultant program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

Customer Change Notification Service

Microchip's customer notification service helps keep customers current on Microchip products. Subscribers will receive e-mail notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.

To register, access the Microchip web site at http://www.microchip.com/. Under "Support", click on "Customer Change Notification" and follow the registration instructions.

Customer Support

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Field Application Engineer (FAE)
- Technical Support

Customers should contact their distributor, representative or Field Application Engineer (FAE) for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in the back of this document.

Technical support is available through the web site at: http://www.microchip.com/support

Microchip Devices Code Protection Feature

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.

- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as “unbreakable.”

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip’s code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Legal Notice

Trademarks

ISBN: 978-1-5224-3998-1

Quality Management System Certified by DNV

ISO/TS 16949

Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

Worldwide Sales and Service

AMERICAS	ASIA/PACIFIC	ASIA/PACIFIC	EUROPE
Corporate Office 2355 West Chandler Blvd. Chandler, AZ 85224-6199 Tel: 480-792-7200 Fax: 480-792-7277 Technical Support: http://www.microchip.com/support Web Address: www.microchip.com **Atlanta** Duluth, GA Tel: 678-957-9614 Fax: 678-957-1455 **Austin, TX** Tel: 512-257-3370 **Boston** Westborough, MA Tel: 774-760-0087 Fax: 774-760-0088 **Chicago** Itasca, IL Tel: 630-285-0071 Fax: 630-285-0075 **Dallas** Addison, TX Tel: 972-818-7423 Fax: 972-818-2924 **Detroit** Novi, MI Tel: 248-848-4000 **Houston, TX** Tel: 281-894-5983 **Indianapolis** Noblesville, IN Tel: 317-773-8323 Fax: 317-773-5453 Tel: 317-536-2380 **Los Angeles** Mission Viejo, CA Tel: 949-462-9523 Fax: 949-462-9608 Tel: 951-273-7800 **Raleigh, NC** Tel: 919-844-7510 **New York, NY** Tel: 631-435-6000 **San Jose, CA** Tel: 408-735-9110 Tel: 408-436-4270 **Canada - Toronto** Tel: 905-695-1980 Fax: 905-695-2078	**Australia - Sydney** Tel: 61-2-9868-6733 **China - Beijing** Tel: 86-10-8569-7000 **China - Chengdu** Tel: 86-28-8665-5511 **China - Chongqing** Tel: 86-23-8980-9588 **China - Dongguan** Tel: 86-769-8702-9880 **China - Guangzhou** Tel: 86-20-8755-8029 **China - Hangzhou** Tel: 86-571-8792-8115 **China - Hong Kong SAR** Tel: 852-2943-5100 **China - Nanjing** Tel: 86-25-8473-2460 **China - Qingdao** Tel: 86-532-8502-7355 **China - Shanghai** Tel: 86-21-3326-8000 **China - Shenyang** Tel: 86-24-2334-2829 **China - Shenzhen** Tel: 86-755-8864-2200 **China - Suzhou** Tel: 86-186-6233-1526 **China - Wuhan** Tel: 86-27-5980-5300 **China - Xian** Tel: 86-29-8833-7252 **China - Xiamen** Tel: 86-592-2388138 **China - Zhuhai** Tel: 86-756-3210040	**India - Bangalore** Tel: 91-80-3090-4444 **India - New Delhi** Tel: 91-11-4160-8631 **India - Pune** Tel: 91-20-4121-0141 **Japan - Osaka** Tel: 81-6-6152-7160 **Japan - Tokyo** Tel: 81-3-6880- 3770 **Korea - Daegu** Tel: 82-53-744-4301 **Korea - Seoul** Tel: 82-2-554-7200 **Malaysia - Kuala Lumpur** Tel: 60-3-7651-7906 **Malaysia - Penang** Tel: 60-4-227-8870 **Philippines - Manila** Tel: 63-2-634-9065 **Singapore** Tel: 65-6334-8870 **Taiwan - Hsin Chu** Tel: 886-3-577-8366 **Taiwan - Kaohsiung** Tel: 886-7-213-7830 **Taiwan - Taipei** Tel: 886-2-2508-8600 **Thailand - Bangkok** Tel: 66-2-694-1351 **Vietnam - Ho Chi Minh** Tel: 84-28-5448-2100	**Austria - Wels** Tel: 43-7242-2244-39 Fax: 43-7242-2244-393 **Denmark - Copenhagen** Tel: 45-4450-2828 Fax: 45-4485-2829 **Finland - Espoo** Tel: 358-9-4520-820 **France - Paris** Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79 **Germany - Garching** Tel: 49-8931-9700 **Germany - Haan** Tel: 49-2129-3766400 **Germany - Heilbronn** Tel: 49-7131-67-3636 **Germany - Karlsruhe** Tel: 49-721-625370 **Germany - Munich** Tel: 49-89-627-144-0 Fax: 49-89-627-144-44 **Germany - Rosenheim** Tel: 49-8031-354-560 **Israel - Ra'anana** Tel: 972-9-744-7705 **Italy - Milan** Tel: 39-0331-742611 Fax: 39-0331-466781 **Italy - Padova** Tel: 39-049-7625286 **Netherlands - Drunen** Tel: 31-416-690399 Fax: 31-416-690340 **Norway - Trondheim** Tel: 47-72884388 **Poland - Warsaw** Tel: 48-22-3325737 **Romania - Bucharest** Tel: 40-21-407-87-50 **Spain - Madrid** Tel: 34-91-708-08-90 Fax: 34-91-708-08-91 **Sweden - Gothenberg** Tel: 46-31-704-60-40 **Sweden - Stockholm** Tel: 46-8-5090-4654 **UK - Wokingham** Tel: 44-118-921-5800 Fax: 44-118-921-5820

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Microchip:

ATWILC1000B-MU-T ATWILC1000B-UU-T ATWILC1000B-MU-Y ATWILC1000B-UU-Y

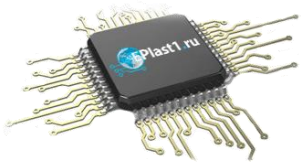
Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits,General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

Телефон: 8 (812) 309 58 32 (многоканальный)
Факс: 8 (812) 320-02-42
Электронная почта: org@eplast1.ru
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.