W25N512GVxIR

3V 512M-BIT
SERIAL SLC NAND FLASH MEMORY WITH DUAL/QUAD SPI & BUFFER READ MODE

Publication Release Date: February 13, 2019
Revision A

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1. GENERAL DESCRIPTIONS

The W25N512GV (512M-bit) Serial SLC NAND Flash Memory provides a storage solution for systems with limited space, pins and power. The W25N SpiFlash family incorporates the popular SPI interface and the traditional large NAND non-volatile memory space. They are ideal for code shadowing to RAM, executing code directly from Dual/Quad SPI (XIP) and storing voice, text and data. The device operates on a single 2.7V to 3.6V power supply with current consumption as low as 25mA active, 10µA for standby and 1µA for deep power down. All W25N SpiFlash family devices are offered in space-saving packages which were impossible to use in the past for the typical NAND flash memory.

The W25N512GV 512M-bit memory array is organized into 32,768 programmable pages of 2,048-bytes each. The entire page can be programmed at one time using the data from the 2,048-Byte internal buffer. Pages can be erased in groups of 64 (128KB block erase). The W25N512GV has 512 erasable blocks.

The W25N512GV supports the standard Serial Peripheral Interface (SPI), Dual/Quad I/O SPI: Serial Clock, Chip Select, Serial Data I/O0 (DI), I/O1 (DO), I/O2 (/WP), and I/O3 (/HOLD). SPI clock frequencies of up to 166MHz are supported allowing equivalent clock rates of 332MHz (166MHz x 2) for Dual I/O and 664MHz (166MHz x 4) for Quad I/O when using the Fast Read Dual/Quad I/O instructions.

A Hold pin, Write Protect pin and programmable write protection, provide further control flexibility. Additionally, the device supports JEDEC standard manufacturer and device ID, one 2,048-Byte Unique ID page, one 2,048-Byte parameter page and ten 2,048-Byte OTP pages. To provide better NAND flash memory manageability, user configurable internal ECC, bad block management are also available in W25N512GV.

2. FEATURES

- **New W25N Family of SpiFlash Memories**
  - W25N512GV: 512M-bit / 64M-Byte
  - Standard SPI: CLK, /CS, DI, DO, /WP, /Hold
  - Dual SPI: CLK, /CS, IO_0, IO_1, /WP, /Hold
  - Quad SPI: CLK, /CS, IO_0, IO_1, IO_2, IO_3
  - Compatible SPI serial flash commands
- **Highest Performance Serial NAND Flash**
  - 166MHz Standard/Dual/Quad SPI clocks
  - 332/664MHz equivalent Dual/Quad SPI
  - 25µS Page Read Time (60µS with ECC)
  - Fast Program/Erase performance
  - More than 100,000 erase/program cycles(4)
  - More than 10-year data retention
- **Low Power, Wide Temperature Range**
  - Single 2.7 to 3.6V supply
  - 25mA active, 10µA standby, 1µA DPD(3)
  - -40°C to +85°C operating range
- **Flexible Architecture with 128KB blocks**
  - Uniform 128K-Byte Block Erase
  - Flexible page data load methods
- **Advanced Features**
  - On chip 1-Bit ECC for memory array
  - ECC status bits indicate ECC results
  - Bad block management and LUT(1) access
  - Software and Hardware Write-Protect
  - Power Supply Lock-Down and OTP protection
  - 2KB Unique ID and 2KB parameter pages
  - Ten 2KB OTP pages(2)
- **Space Efficient Packaging**
  - 8-pad WSON 6x5-mm
  - 8-pad WSON 8x6-mm
  - 16-pin SOIC 300-mil
  - 24-ball TFBGA 8x6-mm
  - Contact Winbond for other package options

Notes:
1. LUT stands for Look-Up Table.
2. OTP pages can only be programmed.
3. DPD stands for Deep Power Down.
4. Endurance specification is based on the on-chip ECC or 1bit/528 byte ECC(Error Correcting Code)

3. PACKAGE TYPES AND PIN CONFIGURATIONS

W25N512GV is offered in an 8-pad WSON 6x5-mm (package code P), 8x6-mm (package code E), a 16-pin SOIC 300-mil (package code F) and two 24-ball 8x6-mm TFBGA (package code B) packages as shown in Figure 1a-c respectively. Package diagrams and dimensions are illustrated at the end of this datasheet.

3.1 Pad Configuration WSON 6x5-mm / 8x6-mm

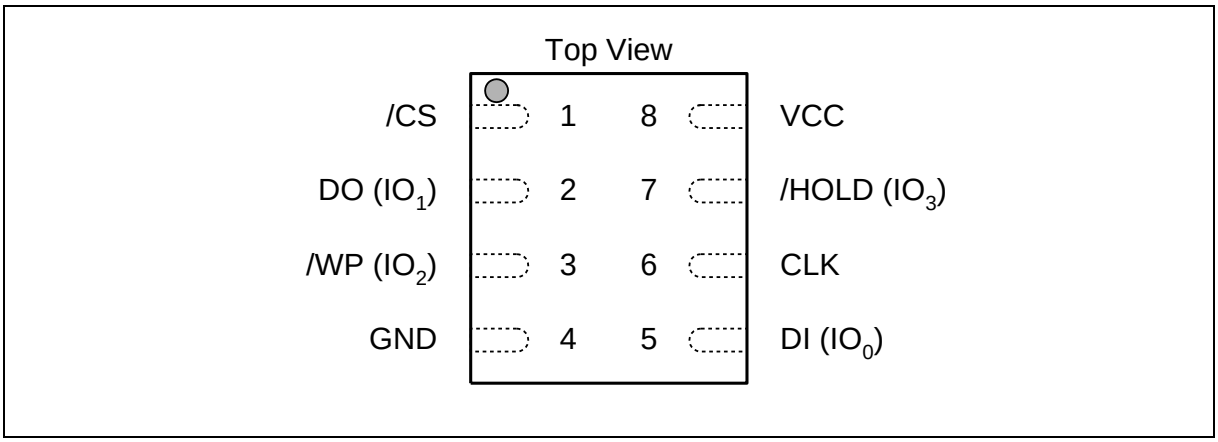


Figure 1a. W25N512GV Pad Assignments, 8-pad WSON 6x5-mm / 8x6-mm (Package Code P, E)

3.2 Pad Description WSON 6x5-mm / 8x6-mm

PAD NO.	PAD NAME	I/O	FUNCTION
1	/CS	I	Chip Select Input
2	DO (IO1)	I/O	Data Output (Data Input Output 1)(1)
3	/WP (IO2)	I/O	Write Protect Input (Data Input Output 2)(2)
4	GND		Ground
5	DI (IO0)	I/O	Data Input (Data Input Output 0)(1)
6	CLK	I	Serial Clock Input
7	/HOLD (IO3)	I/O	Hold Input (Data Input Output 3)(2)
8	VCC		Power Supply

Notes:

1. IO0 and IO1 are used for Standard and Dual SPI instructions
2. IO0 – IO3 are used for Quad SPI instructions, /WP & /HOLD functions are only available for Standard/Dual SPI.

3.3 Pin Configuration SOIC 300-mil

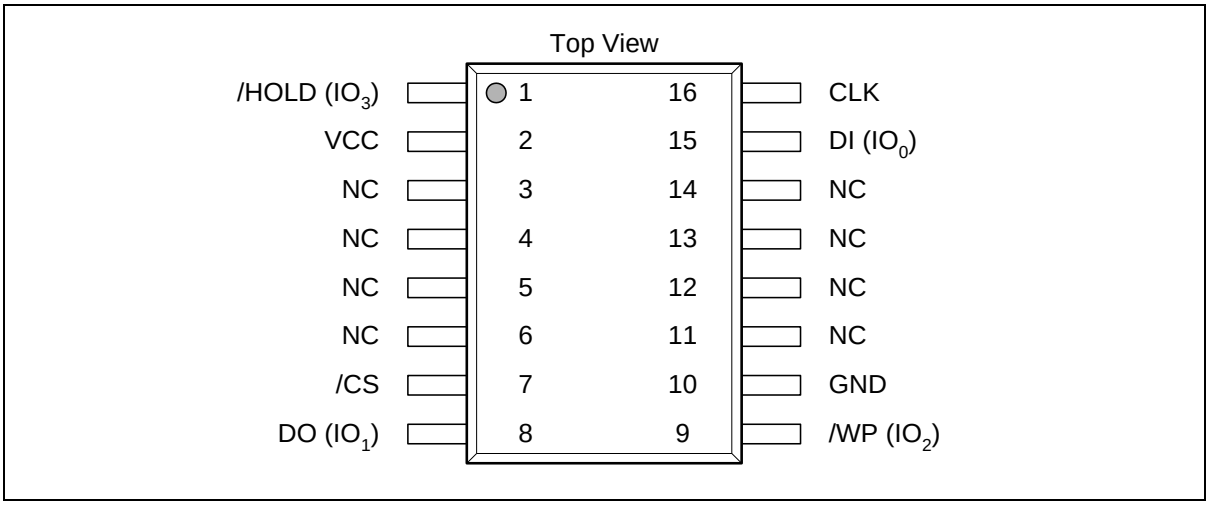


Figure 1b. W25N512GV Pin Assignments, 16-pin SOIC 300-mil (Package Code F)

3.4 Pin Description SOIC 300-mil

PIN NO.	PIN NAME	I/O	FUNCTION
1	/HOLD (IO3)	I/O	Hold Input (Data Input Output 3)(2)
2	VCC		Power Supply
3	N/C		No Connect
4	N/C		No Connect
5	N/C		No Connect
6	N/C		No Connect
7	/CS	I	Chip Select Input
8	DO (IO1)	I/O	Data Output (Data Input Output 1)(1)
9	/WP (IO2)	I/O	Write Protect Input (Data Input Output 2)(2)
10	GND		Ground
11	N/C		No Connect
12	N/C		No Connect
13	N/C		No Connect
14	N/C		No Connect
15	DI (IO0)	I/O	Data Input (Data Input Output 0)(1)
16	CLK	I	Serial Clock Input

Notes:

1. IO0 and IO1 are used for Standard and Dual SPI instructions
2. IO0 – IO3 are used for Quad SPI instructions, /WP & /HOLD functions are only available for Standard/Dual SPI.

3.5 Ball Configuration TFBGA 8x6-mm (5x5 Ball Array)

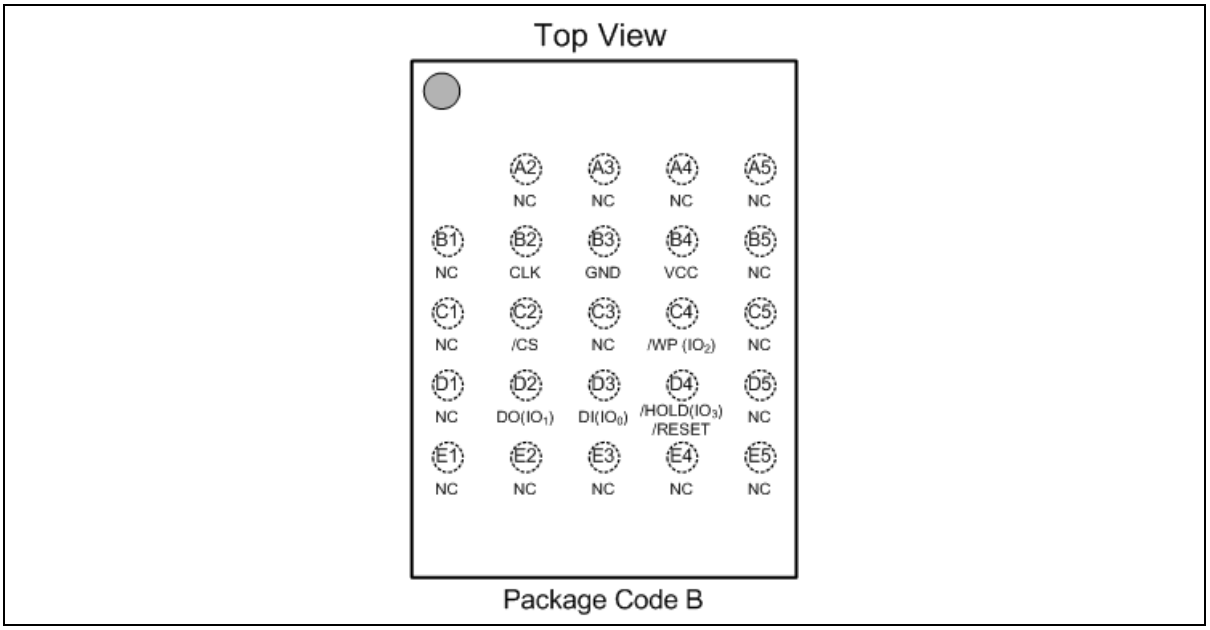


Figure 1c. W25N512GV Ball Assignments, 24-ball TFBGA 8x6-mm (Package Code B)

3.6 Ball Description TFBGA 8x6-mm

BALL NO.	PIN NAME	I/O	FUNCTION
B2	CLK	I	Serial Clock Input
B3	GND		Ground
B4	VCC		Power Supply
C2	/CS	I	Chip Select Input
C4	/WP (IO2)	I/O	Write Protect Input (Data Input Output 2)(2)
D2	DO (IO1)	I/O	Data Output (Data Input Output 1)(1)
D3	DI (IO0)	I/O	Data Input (Data Input Output 0)(1)
D4	/HOLD (IO3)	I/O	Hold Input (Data Input Output 3)(2)
Multiple	NC		No Connect

Notes:

1. IO0 and IO1 are used for Standard and Dual SPI instructions
2. IO0 – IO3 are used for Quad SPI instructions, /WP & /HOLD functions are only available for Standard/Dual SPI.

4. PIN DESCRIPTIONS

4.1 Chip Select (/CS)

The SPI Chip Select (/CS) pin enables and disables device operation. When /CS is high the device is deselected and the Serial Data Output (DO, or IO0, IO1, IO2, IO3) pins are at high impedance. When deselected, the devices power consumption will be at standby levels unless an internal erase, program or write status register cycle is in progress. When /CS is brought low the device will be selected, power consumption will increase to active levels and instructions can be written to and data read from the device. After power-up, /CS must transition from high to low before a new instruction will be accepted. The /CS input must track the VCC supply level at power-up and power-down (see “Write Protection” and Figure 27b). If needed, a pull-up resistor on the /CS pin can be used to accomplish this.

4.2 Serial Data Input, Output and IOs (DI, DO and IO0, IO1, IO2, IO3)

The W25N512GV supports standard SPI, Dual SPI and Quad SPI operation. Standard SPI instructions use the unidirectional DI (input) pin to serially write instructions, addresses or data to the device on the rising edge of the Serial Clock (CLK) input pin. Standard SPI also uses the unidirectional DO (output) to read data or status from the device on the falling edge of CLK.

Dual and Quad SPI instructions use the bidirectional IO pins to serially write instructions, addresses or data to the device on the rising edge of CLK and read data or status from the device on the falling edge of CLK.

4.3 Write Protect (/WP)

The Write Protect (/WP) pin can be used to prevent the Status Register from being written. Used in conjunction with the Status Register’s Block Protect bits BP[3:0] and Status Register Protect SRP bits SRP[1:0], a portion as small as one 128KB Block or up to the entire memory array can be hardware protected. The WP-E bit in the Protection Register (SR-1) controls the functions of the /WP pin.

When WP-E=0, the device is in the Software Protection mode that only SR-1 can be protected. The /WP pin functions as a data I/O pin for the Quad SPI operations, as well as an active low input pin for the Write Protection function for SR-1. Refer to section 7.1.3 for detail information.

When WP-E=1, the device is in the Hardware Protection mode that /WP becomes a dedicated active low input pin for the Write Protection of the entire device. If /WP is tied to GND, all “Write/Program/Erase” functions are disabled. The entire device (including all registers, memory array, OTP pages) will become read-only. Quad SPI read operations are also disabled when WP-E is set to 1.

4.4 HOLD (/HOLD)

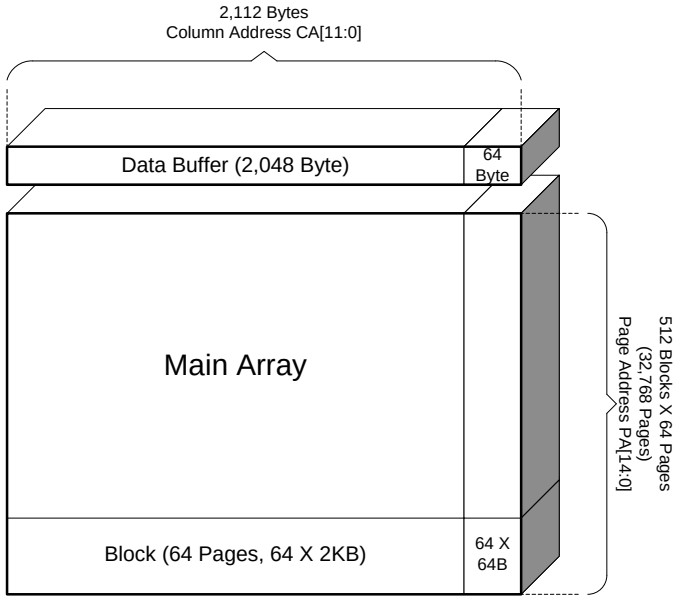
During Standard and Dual SPI operations, the /HOLD pin allows the device to be paused while it is actively selected. When /HOLD is brought low, while /CS is low, the DO pin will be at high impedance and signals on the DI and CLK pins will be ignored (don’t care). When /HOLD is brought high, device operation can resume. The /HOLD function can be useful when multiple devices are sharing the same SPI signals. The /HOLD pin is active low.

When a Quad SPI Read/Buffer Load command is issued, /HOLD pin will become a data I/O pin for the Quad operations and no HOLD function is available until the current Quad operation finishes. /HOLD (IO3) must be driven high by the host, or an external pull-up resistor must be placed on the PCB, in order to avoid allowing the /HOLD input to float.

4.5 Serial Clock (CLK)

The SPI Serial Clock Input (CLK) pin provides the timing for serial input and output operations. ("See SPI Operations")

5. BLOCK DIAGRAM



Address Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SpiFlash (up to 128M-Bit)	X	X	X	X	X	X	X	X	64KB Block Addr (256 Blocks)								Page Address (256 Pages)								Byte Address (0-255 Byte)							
SpiFlash (up to 32G-Bit)	64KB Block Address																Page Address (256 Pages)								Byte Address (0-255 Byte)							
Serial NAND (512M-Bit)	X	X	X	X	X	**Page Address (PA) [14:0]**															**Column Address (CA) [11:0]**											
	X	X	X	X	X	128KB Block Addr (1024 Blocks)									Page Addr (64 Pages)						Ext	Byte Address (0-2047 Byte)										

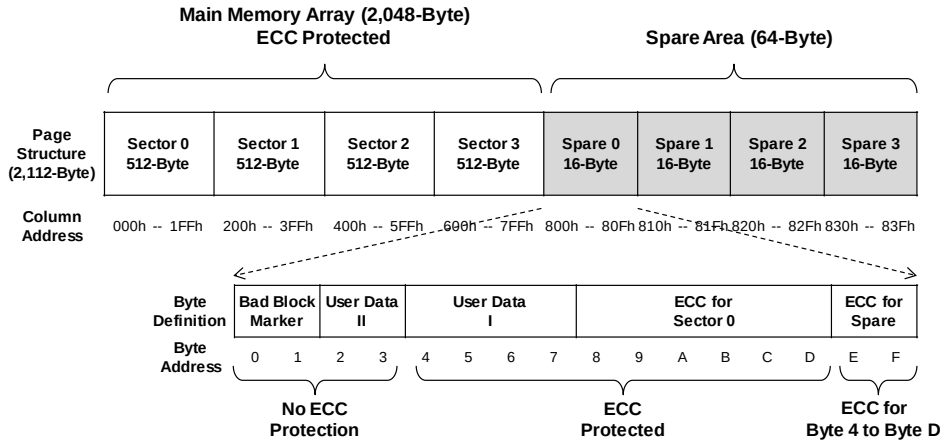


Figure 2. W25N512GV Flash Memory Architecture and Addressing

6. FUNCTIONAL DESCRIPTIONS

6.1 Device Operation Flow

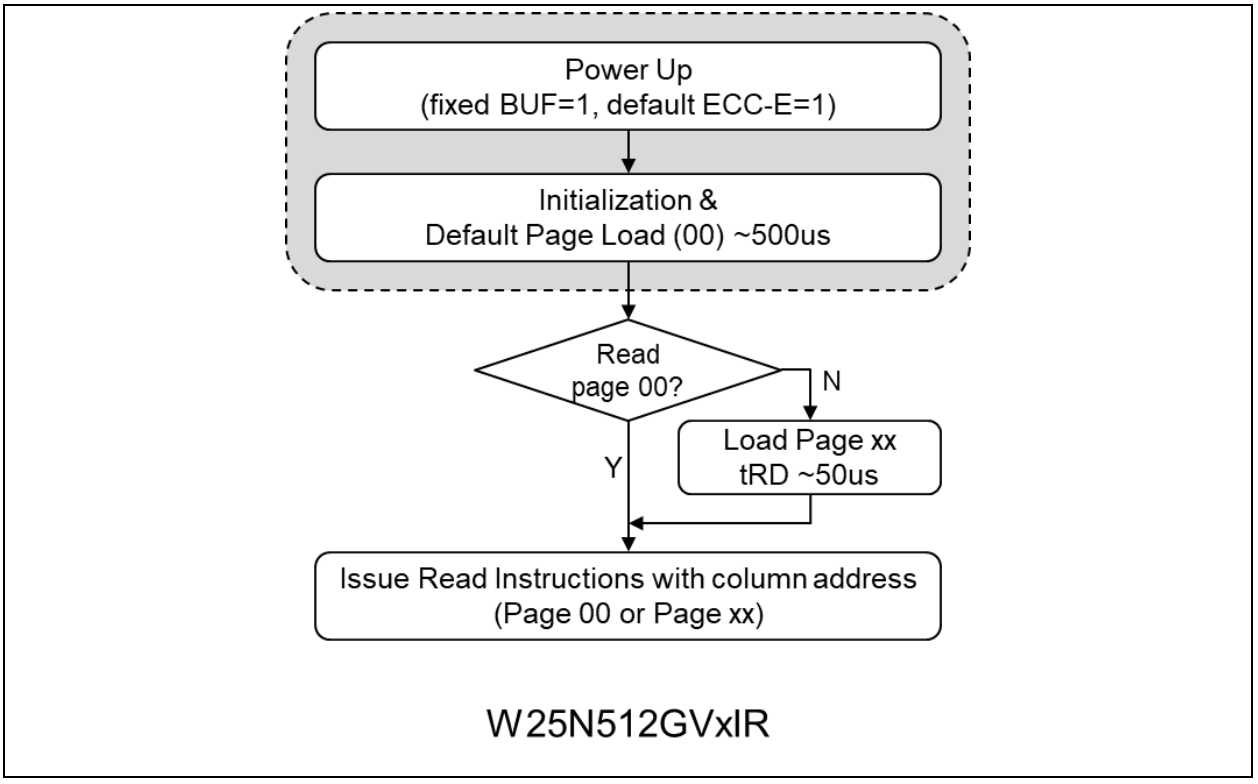


Figure 3. W25N512GV Flash Memory Operation Diagram

6.1.1 Standard SPI Instructions

The W25N512GV is accessed through an SPI compatible bus consisting of four signals: Serial Clock (CLK), Chip Select (/CS), Serial Data Input (DI) and Serial Data Output (DO). Standard SPI instructions use the DI input pin to serially write instructions, addresses or data to the device on the rising edge of CLK. The DO output pin is used to read data or status from the device on the falling edge of CLK.

SPI bus operation Mode 0 (0,0) and 3 (1,1) are supported. The primary difference between Mode 0 and Mode 3 concerns the normal state of the CLK signal when the SPI bus master is in standby and data is not being transferred to the Serial Flash. For Mode 0, the CLK signal is normally low on the falling and rising edges of /CS. For Mode 3, the CLK signal is normally high on the falling and rising edges of /CS.

6.1.2 Dual SPI Instructions

The W25N512GV supports Dual SPI operation when using instructions such as “Fast Read Dual Output (3Bh)” and “Fast Read Dual I/O (BBh)”. These instructions allow data to be transferred to or from the device at two to three times the rate of ordinary Serial Flash devices. The Dual SPI Read instructions are ideal for quickly downloading code to RAM upon power-up (code-shadowing) or for executing non-speed-critical code directly from the SPI bus (XIP). When using Dual SPI instructions, the DI and DO pins become bidirectional I/O pins: IO0 and IO1.

6.1.3 Quad SPI Instructions

The W25N512GV supports Quad SPI operation when using instructions such as “Fast Read Quad Output (6Bh)”, “Fast Read Quad I/O (EBh)” and “Quad Program Data Load (32h/34h)”. These instructions allow data to be transferred to or from the device four to six times the rate of ordinary Serial Flash. The Quad Read instructions offer a significant improvement in continuous and random access transfer rates allowing fast code-shadowing to RAM or execution directly from the SPI bus (XIP). When using Quad SPI instructions the DI and DO pins become bidirectional IO0 and IO1, and the /WP and /HOLD pins become IO2 and IO3 respectively.

6.1.4 Hold Function

For Standard SPI and Dual SPI operations, the /HOLD signal allows the W25N512GV operation to be paused while it is actively selected (when /CS is low). The /HOLD function may be useful in cases where the SPI data and clock signals are shared with other devices. For example, consider if the page buffer was only partially written when a priority interrupt requires use of the SPI bus. In this case the /HOLD function can save the state of the instruction and the data in the buffer so programming can resume where it left off once the bus is available again. The /HOLD function is only available for standard SPI and Dual SPI operation, not during Quad SPI. When a Quad SPI command is issued, /HOLD pin will act as a dedicated IO pin (IO3).

To initiate a /HOLD condition, the device must be selected with /CS low. A /HOLD condition will activate on the falling edge of the /HOLD signal if the CLK signal is already low. If the CLK is not already low the /HOLD condition will activate after the next falling edge of CLK. The /HOLD condition will terminate on the rising edge of the /HOLD signal if the CLK signal is already low. If the CLK is not already low the /HOLD condition will terminate after the next falling edge of CLK. During a /HOLD condition, the Serial Data Output (DO) is high impedance, and Serial Data Input (DI) and Serial Clock (CLK) are ignored. The Chip Select (/CS) signal should be kept active (low) for the full duration of the /HOLD operation to avoid resetting the internal logic state of the device.

6.2 Write Protection

Applications that use non-volatile memory must take into consideration the possibility of noise and other adverse system conditions that may compromise data integrity. To address this concern, the W25N512GV provides several means to protect the data from inadvertent writes.

- Device resets when VCC is below threshold
- Write enable/disable instructions and automatic write disable after erase or program
- Software and Hardware (/WP pin) write protection using Protection Register (SR-1)
- Lock Down write protection for Protection Register (SR-1) until the next power-up
- One Time Program (OTP) write protection for memory array using Protection Register (SR-1)
- Hardware write protection using /WP pin when WP-E is set to 1

Upon power-up or at power-down, the W25N512GV will maintain a reset condition while VCC is below the threshold value of V_{WI}, (See Power-up Timing and Voltage Levels and Figure 27a). While reset, all operations are disabled and no instructions are recognized. During power-up and after the VCC voltage exceeds V_{WI}, all program and erase related instructions are further disabled for a time delay of t_{PUW}. This includes the Write Enable, Program Execute, Block Erase, Chip Erase and the Write Status Register instructions. Note that the chip select pin (/CS) must track the VCC supply level at power-up until the VCC-min level and t_{VSL} time delay is reached, and it must also track the VCC supply level at power-down to prevent adverse command sequence. If needed a pull-up resister on /CS can be used to accomplish this.

After power-up the device is automatically placed in a write-disabled state with the Status Register Write Enable Latch (WEL) set to a 0. A Write Enable instruction must be issued before a Program Execute, Block Erase, Chip Erase or Bad Block Management instruction will be accepted. After completing a program or erase instruction the Write Enable Latch (WEL) is automatically cleared to a write-disabled state of 0.

Software controlled write protection is facilitated using the Write Status Register instruction and setting the Status Register Protect (SRP0, SRP1) and Block Protect (TB, BP[3:0]) bits. These settings allow a portion or the entire memory array to be configured as read only. Used in conjunction with the Write Protect (/WP) pin, changes to the Status Register can be enabled or disabled under hardware control. See Protection Register section for further information.

The WP-E bit in Protection Register (SR-1) is used to enable the hardware protection. When WP-E is set to 1, bringing /WP low in the system will block any Write/Program/Erase command to the W25N512GV, the device will become read-only. The Quad SPI operations are also disabled when WP-E is set to 1.

7. PROTECTION, CONFIGURATION AND STATUS REGISTERS

Three Status Registers are provided for W25N512GV: Protection Register (SR-1), Configuration Register (SR-2) & Status Register (SR-3). Each register is accessed by Read Status Register and Write Status Register commands combined with 1-Byte Register Address respectively.

The Read Status Register instruction (05h / 0Fh) can be used to provide status on the availability of the flash memory array, whether the device is write enabled or disabled, the state of write protection, Read modes, Protection Register/OTP area lock status, Erase/Program results, ECC usage/status. The Write Status Register instruction can be used to configure the device write protection features, Software/Hardware write protection, Read modes, enable/disable ECC, Protection Register/OTP area lock. Write access to the Status Register is controlled by the state of the non-volatile Status Register Protect bits (SRP0, SRP1), the Write Enable instruction, and when WP-E is set to 1, the /WP pin.

7.1 Protection Register / Status Register-1 (Volatile Writable, OTP lockable)

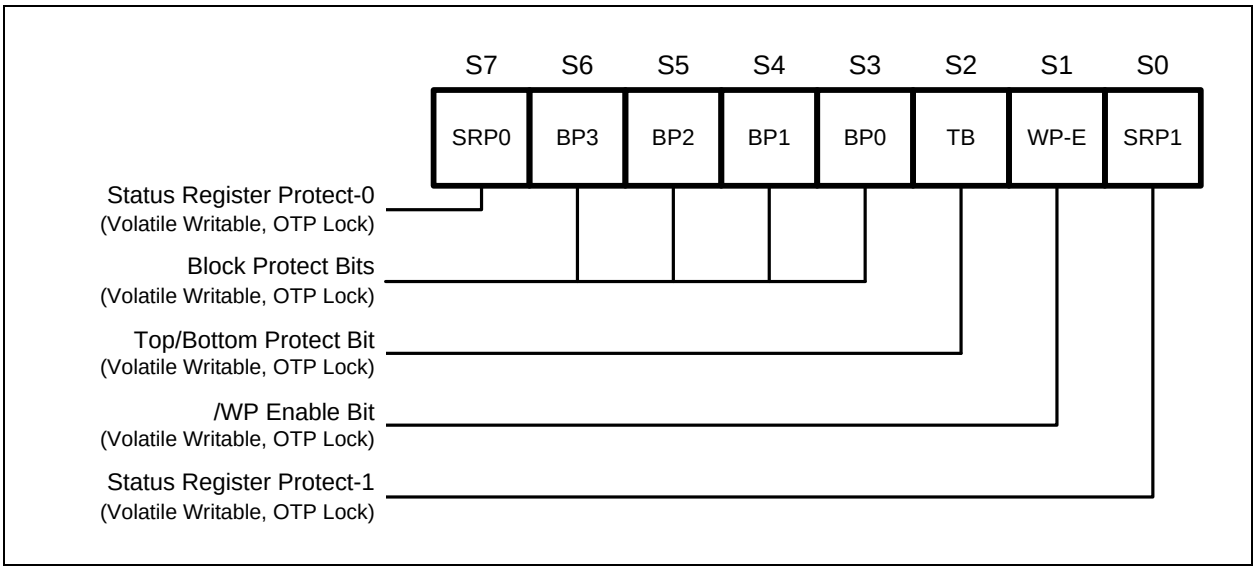


Figure 4a. Protection Register / Status Register-1 (Address Axh)

7.1.1 Block Protect Bits (BP3, BP2, BP1, BP0, TB) – *Volatile Writable, OTP lockable*

The Block Protect bits (BP3, BP2, BP1, BP0 & TB) are volatile read/write bits in the status register-1 (S6, S5, S4, S3 & S2) that provide Write Protection control and status. Block Protect bits can be set using the Write Status Register Instruction. All, none or a portion of the memory array can be protected from Program and Erase instructions (see Status Register Memory Protection table). The default values for the Block Protection bits are 1 after power up to protect the entire array. If the SR1-L bit in the Configuration Register (SR-2) is set to 1, the default values will the values that are OTP locked.

7.1.2 Write Protection Enable Bit (WP-E) – *Volatile Writable, OTP lockable*

The Write Protection Enable bit (WP-E) is a volatile read/write bits in the status register-1 (S1). The WP-E bit, in conjunction with SRP1 & SRP0, controls the method of write protection: software protection, hardware protection, power supply lock-down or one time programmable (OTP) protection, /WP pin functionality, and Quad SPI operation enable/disable. When WP-E = 0 (default value), the device is in Software Protection mode, /WP & /HOLD pins are multiplexed as IO pins, and Quad program/read functions are enabled all the time. When WP-E is set to 1, the device is in Hardware Protection mode, all Quad functions are disabled and /WP & /HOLD pins become dedicated control input pins.

7.1.3 Status Register Protect Bits (SRP1, SRP0) – *Volatile Writable, OTP lockable*

The Status Register Protect bits (SRP1 and SRP0) are volatile read/write bits in the status register (S0 and S7). The SRP bits control the method of write protection: software protection, hardware protection, power supply lock-down or one time programmable (OTP) protection.

Software Protection (Driven by Controller, Quad Program/Read is enabled)				
SRP1	**SRP0**	**WP-E**	**/WP / IO2**	**Descriptions**
0	0	0	X	No /WP functionality */WP pin will always function as IO2*
0	1	0	0	SR-1 cannot be changed (/WP = 0 during Write Status) */WP pin will function as IO2 for Quad operations*
0	1	0	1	SR-1 can be changed (/WP = 1 during Write Status) */WP pin will function as IO2 for Quad operations*
1	0	0	X	Power Lock Down(1) SR-1 */WP pin will always function as IO2*
1	1	0	X	Enter OTP mode to protect SR-1 (allow SR1-L=1) */WP pin will always function as IO2*

Hardware Protection (System Circuit / PCB layout, Quad Program/Read is disabled)				
SRP1	**SRP0**	**WP-E**	**/WP only**	**Descriptions**
0	X	1	VCC	SR-1 can be changed
1	0	1	VCC	Power Lock-Down(1) SR-1
1	1	1	VCC	Enter OTP mode to protect SR-1 (allow SR1-L=1)
X	X	1	GND	All "Write/Program/Erase" commands are blocked Entire device (SRs, Array, OTP area) is read-only

Notes:

1. When SRP1, SRP0 = (1, 0), a power-down, power-up cycle will change SRP1, SRP0 to (0, 0) state.

7.2 Configuration Register / Status Register-2 (Volatile Writable)

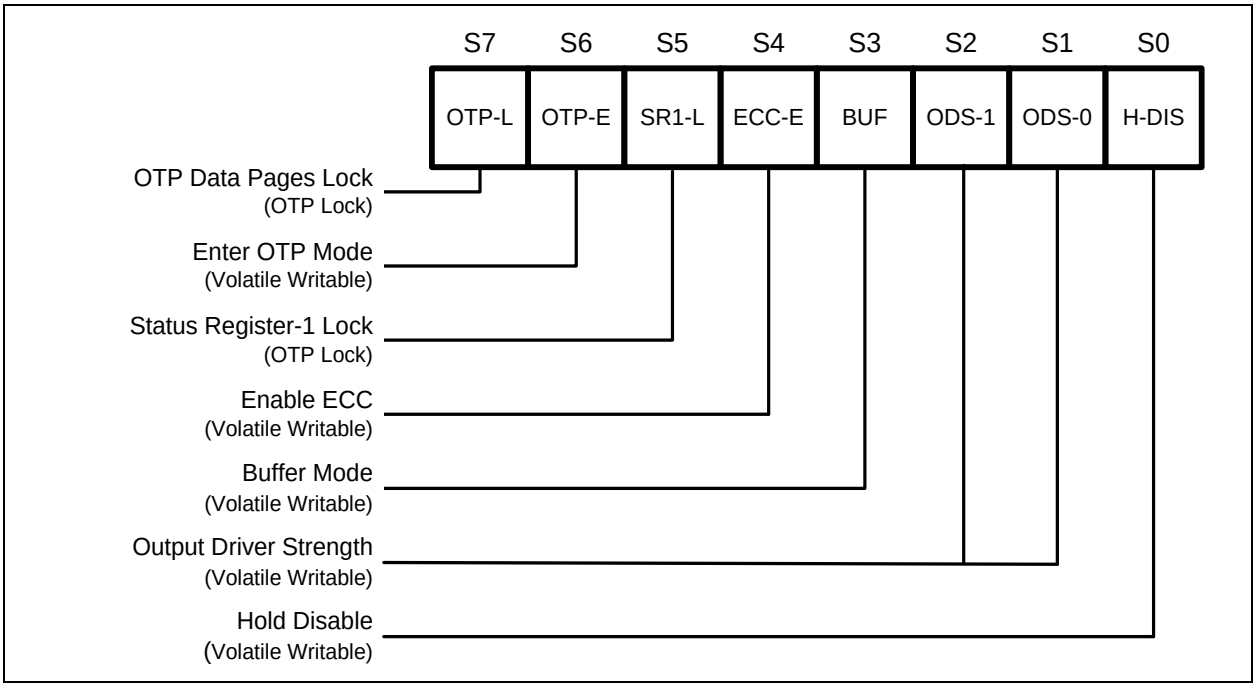


Figure 4b. Configuration Register / Status Register-2 (Address Bxh)

7.2.1 One Time Program Lock Bit (OTP-L) – *OTP lockable*

In addition to the main memory array, W25N512GV also provides an OTP area for the system to store critical data that cannot be changed once it's locked. The OTP area consists of 10 pages of 2,112-Byte each. The default data in the OTP area are FFh. Only Program command can be issued to the OTP area to change the data from "1" to "0", and data is not reversible ("0" to "1") by the Erase command. Once the correct data is programmed in and verified, the system developer can set OTP-L bit to 1, so that the entire OTP area will be locked to prevent further alteration to the data.

7.2.2 Enter OTP Access Mode Bit (OTP-E) – *Volatile Writable*

The OTP-E bit must be set to 1 in order to use the standard Program/Read commands to access the OTP area as well as to read the Unique ID / Parameter Page information. The default value after power up or a RESET command is 0.

7.2.3 Status Register-1 Lock Bit (SR1-L) – *OTP lockable*

The SR1-L lock bit is used to OTP lock the values in the Protection Register (SR-1). Depending on the settings in the SR-1, the device can be configured to have a portion of or up to the entire array to be write-protected, and the setting can be OTP locked by setting SR1-L bit to 1. SR1-L bit can only be set to 1 permanently when SRP1 & SRP0 are set to (1,1), and OTP Access Mode must be entered (OTP-E=1) to execute the programming. Please refer to 8.2.26 for detailed information.

7.2.4 ECC Enable Bit (ECC-E) – *Volatile Writable*

W25N512GV has a built-in ECC algorithm that can be used to preserve the data integrity. Internal ECC calculation is done during page programming, and the result is stored in the extra 64-Byte area for each page. During the data read operation, ECC engine will verify the data values according to the previously stored ECC information and to make necessary corrections if needed. The verification and correction status is indicated by the ECC Status Bits. ECC function is enabled by default when power on (ECC-E=1), and it will not be reset to 0 by the Device Reset command.

7.2.5 Buffer Read / Continuous Read Mode Bit (BUF) – *Volatile Writable*

W25N512GVxIR provides a simple mode for read operations, Buffer Read Mode (BUF=1). Prior to any Read operation, a Page Data Read command is needed to initiate the data transfer from a specified page in the memory array to the Data Buffer. By default, after power up, the data in page 0 will be automatically loaded into the Data Buffer and the device is ready to accept any read commands.

The Buffer Read Mode (BUF=1) requires a Column Address to start outputting the existing data inside the Data Buffer, and once it reaches the end of the data buffer (Byte 2,111), DO (IO1) pin will become high-Z state.

The default value of BUF bit after power up is 1. BUF bit is locked to 1 for W25N512GVxIR to offer Buffer Read Mode only. For BUF=0 setting, please refer to W25N512GVxIG/IT datasheet.

BUF	ECC-E	Read Mode (Starting from Buffer)	ECC Status	Data Output Structure
1	0	Buffer Read	N/A	2,048 + 64
1	1	Buffer Read	Page based	2,048 + 64

7.2.6 Output Driver Strength (ODS-1, ODS-0) – *Volatile Writable*

ODS-1, ODS-0	Output Driver Strength
0, 0	100%
0, 1	75%
1, 0	50% (default)
1, 1	25%

7.2.7 Hold Disable (H-DIS) - *Volatile Writable*

When the Hold Disable (H-DIS) bit set to 1, the hold function would be disabled. If the user wants to use the hold function, the H-DIS bit has to be set 0.

7.3 Status Register-3 (Status Only)

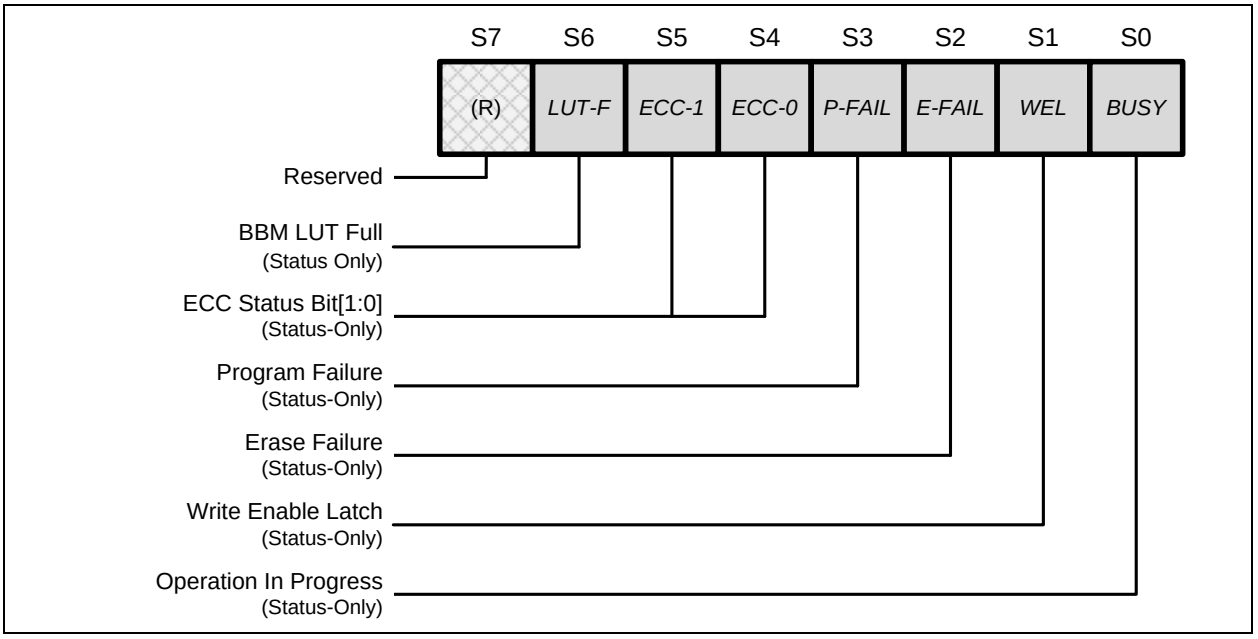


Figure 4c. Status Register-3 (Address Cxh)

7.3.1 Look-Up Table Full (LUT-F) – *Status Only*

To facilitate the NAND flash memory bad block management, the W25N512GV is equipped with an internal Bad Block Management Look-Up-Table (BBM LUT). Up to 10 bad memory blocks may be replaced by a good memory block respectively. The addresses of the blocks are stored in the internal Look-Up Table as Logical Block Address (LBA, the bad block) & Physical Block Address (PBA, the good block). The LUT-F bit indicates whether the 10 memory block links have been fully utilized or not. The default value of LUT-F is 0, once all 10 links are used, LUT-F will become 1, and no more memory block links may be established.

7.3.2 Cumulative ECC Status (ECC-1, ECC-0) – *Status Only*

ECC function is used in NAND flash memory to correct limited memory errors during read operations. The ECC Status Bits (ECC-1, ECC-0) should be checked after the completion of a Read operation to verify the data integrity. The ECC Status bits values are don't care if ECC-E=0. These bits will be cleared to 0 after a power cycle or a RESET command.

ECC Status		Descriptions
ECC-1	ECC-0	
0	0	Entire data output is **successful**, without any ECC correction.
0	1	Entire data output is **successful**, with 1~4 bit/page ECC corrections in either a single page or multiple pages.
1	0	Entire data output contains **more than 4 bits errors only in a single page which cannot be repaired by ECC**.
1	1	N/A

7.3.3 Program/Erase Failure (P-FAIL, E-FAIL) – *Status Only*

The Program/Erase Failure Bits are used to indicate whether the internally-controlled Program/Erase operation was executed successfully or not. These bits will also be set respectively when the Program or Erase command is issued to a locked or protected memory array or OTP area. Both bits will be cleared at the beginning of the Program Execute or Block/Chip Erase instructions as well as the device RESET instruction.

7.3.4 Write Enable Latch (WEL) – *Status Only*

Write Enable Latch (WEL) is a read only bit in the status register (S1) that is set to 1 after executing a Write Enable Instruction. The WEL status bit is cleared to 0 when the device is write disabled. A write disable state occurs upon power-up or after any of the following instructions: Write Disable, Program Execute, Block/Chip Erase, Page Data Read, Program Execute for OTP pages and Bad Block Management.

7.3.5 Erase/Program In Progress (BUSY) – *Status Only*

BUSY is a read only bit in the status register (S0) that is set to a 1 state when the device is powering up or executing a Page Data Read, Bad Block Management, Program Execute, Block/Chip Erase, Program Execute for OTP area or OTP Locking instruction. During this time the device will ignore further instructions except for the Read Status Register and Read JEDEC ID instructions. When the program, erase or write status register instruction has completed, the BUSY bit will be cleared to a 0 state indicating the device is ready for further instructions.

7.3.6 Reserved Bits – *Non Functional*

There are a few reserved Status Register bits that may be read out as a “0” or “1”. It is recommended to ignore the values of those bits. During a “Write Status Register” instruction, the Reserved Bits can be written as “0”, but there will not be any effects.

7.4 W25N512GV Status Register Memory Protection

STATUS REGISTER[1]					W25N512GV (512M-BIT / 64M-BYTE) MEMORY PROTECTION[2]			
TB	BP3	BP2	BP1	BP0	PROTECTED BLOCK(S)	PROTECTED PAGE ADDRESS PA[15:0]	PROTECTED DENSITY	PROTECTED PORTION
X	0	0	0	0	NONE	NONE	NONE	NONE
0	0	0	0	1	511	7FC0h - 7FFFh	128KB	Upper 1/512
0	0	0	1	0	510 & 511	7F80h - 7FFFh	256KB	Upper 1/256
0	0	0	1	1	508 thru 511	7F00h - 7FFFh	512KB	Upper 1/128
0	0	1	0	0	504 thru 511	7E00h - 7FFFh	1MB	Upper 1/64
0	0	1	0	1	496 thru 511	7C00h - 7FFFh	2MB	Upper 1/32
0	0	1	1	0	480 thru 511	7800h - 7FFFh	4MB	Upper 1/16
0	0	1	1	1	448 thru 511	7000h - 7FFFh	8MB	Upper 1/8
0	1	0	0	0	384 thru 511	6000h - 7FFFh	16MB	Upper 1/4
0	1	0	0	1	256 thru 511	4000h - 7FFFh	32MB	Upper 1/2
1	0	0	0	1	0	0000h - 003Fh	128KB	Lower 1/512
1	0	0	1	0	0 & 1	0000h - 007Fh	256KB	Lower 1/256
1	0	0	1	1	0 thru 3	0000h - 00FFh	512KB	Lower 1/128
1	0	1	0	0	0 thru 7	0000h - 01FFh	1MB	Lower 1/64
1	0	1	0	1	0 thru 15	0000h - 03FFh	2MB	Lower 1/32
1	0	1	1	0	0 thru 31	0000h - 07FFh	4MB	Lower 1/16
1	0	1	1	1	0 thru 63	0000h - 0FFFh	8MB	Lower 1/8
1	1	0	0	0	0 thru 127	0000h - 1FFFh	16MB	Lower 1/4
1	1	0	0	1	0 thru 255	0000h - 3FFFh	32MB	Lower 1/2
X	1	0	1	X	0 thru 511	0000h - 7FFFh	64MB	ALL
X	1	1	X	X	0 thru 511	0000h - 7FFFh	64MB	ALL

Notes:

1. X = don't care
2. If any Erase or Program command specifies a memory region that contains protected data portion, this command will be ignored.

8. INSTRUCTIONS

The Standard/Dual/Quad SPI instruction set of the W25N512GV consists of 31 basic instructions that are fully controlled through the SPI bus (see Instruction Set Table1, 2). Instructions are initiated with the falling edge of Chip Select (/CS). The first byte of data clocked into the DI input provides the instruction code. Data on the DI input is sampled on the rising edge of clock with most significant bit (MSB) first.

Instructions vary in length from a single byte to several bytes and may be followed by address bytes, data bytes, dummy bytes (don't care), and in some cases, a combination. Instructions are completed with the rising edge of edge /CS. Clock relative timing diagrams for each instruction are included in Figures 5 through 26. All read instructions can be completed after any clocked bit. However, all instructions that Write, Program or Erase must complete on a byte boundary (/CS driven high after a full 8-bits have been clocked) otherwise the instruction will be ignored. This feature further protects the device from inadvertent writes. Additionally, while the device is performing Program or Erase operation, BBM management, Page Data Read or OTP locking operations, BUSY bit will be high, and all instructions except for Read Status Register or Read JEDEC ID will be ignored until the current operation cycle has completed.

8.1 Device ID and Instruction Set Tables

8.1.1 Manufacturer and Device Identification

MANUFACTURER ID	**(MF7 - MF0)**
Winbond Serial Flash	EFh
Device ID	**(ID15 - ID0)**
W25N512GV	AA20h

8.1.2 Instruction Set Table (Buffer Read, BUF = 1 locked)(11)

Commands	OpCode	Byte2	Byte3	Byte4	Byte5	Byte6	Byte7	Byte8	Byte9
Device RESET	**FFh**								
JEDEC ID	**9Fh**	Dummy	***EFh***	***AAh***	***20h***				
Read Status Register	**0Fh / 05h**	SR Addr	***S7-0***	***S7-0***	***S7-0***	***S7-0***	***S7-0***	***S7-0***	***S7-0***
Write Status Register	**1Fh / 01h**	SR Addr	S7-0						
Write Enable	**06h**								
Write Disable	**04h**								
BB Management (Swap Blocks)	**A1h**	LBA	LBA	PBA	PBA				
Read BBM LUT	**A5h**	Dummy	***LBA0***	***LBA0***	***PBA0***	***PBA0***	***LBA1***	***LBA1***	***PBA1***
Block Erase	**D8h**	Dummy	**PA15-8**	**PA7-0**					
Program Data Load (Reset Buffer)	**02h**	**CA15-8**	**CA7-0**	Data-0	Data-1	Data-2	Data-3	Data-4	Data-5
Random Program Data Load	**84h**	**CA15-8**	**CA7-0**	Data-0	Data-1	Data-2	Data-3	Data-4	Data-5
Quad Program Data Load (Reset Buffer)	**32h**	**CA15-8**	**CA7-0**	Data-0 / 4	Data-1 / 4	Data-2 / 4	Data-3 / 4	Data-4 / 4	Data-5 / 4
Random Quad Program Data Load	**34h**	**CA15-8**	**CA7-0**	Data-0 / 4	Data-1 / 4	Data-2 / 4	Data-3 / 4	Data-4 / 4	Data-5 / 4
Program Execute	**10h**	Dummy	**PA15-8**	**PA7-0**					
Page Data Read	**13h**	Dummy	**PA15-8**	**PA7-0**					
Read	**03h**	**CA15-8**	**CA7-0**	Dummy	***D7-0***	***D7-0***	***D7-0***	***D7-0***	***D7-0***
Fast Read	**0Bh**	**CA15-8**	**CA7-0**	Dummy	***D7-0***	***D7-0***	***D7-0***	***D7-0***	***D7-0***
Fast Read Dual Output	**3Bh**	**CA15-8**	**CA7-0**	Dummy	***D7-0 / 2***	***D7-0 / 2***	***D7-0 / 2***	***D7-0 / 2***	***D7-0 / 2***
Fast Read Quad Output	**6Bh**	**CA15-8**	**CA7-0**	Dummy	***D7-0 / 4***	***D7-0 / 4***	***D7-0 / 4***	***D7-0 / 4***	***D7-0 / 4***
Fast Read Dual I/O	**BBh**	**CA15-8 / 2**	**CA7-0 / 2**	Dummy / 2	***D7-0 / 2***	***D7-0 / 2***	***D7-0 / 2***	***D7-0 / 2***	***D7-0 / 2***
Fast Read Quad I/O	**EBh**	**CA15-8 / 4**	**CA7-0 / 4**	Dummy / 4	Dummy / 4	***D7-0 / 4***	***D7-0 / 4***	***D7-0 / 4***	***D7-0 / 4***
Deep Power-Down	**B9h**								
Release Power-Down	**ABh**								
Chip Erase	**C7h/60h**								
Enable Reset	**66h**								
Reset Device	**99h**								

Notes:

1. ***Output*** designates data output from the device.

2. Column Address (CA) only requires CA[11:0], CA[15:12] are considered as dummy bits.

3. Page Address (PA) requires 15 bits. PA[14:6] is the address for 128KB blocks (total 512 blocks), PA[5:0] is the address for 2KB pages (total 64 pages for each block).

4. Logical and Physical Block Address (LBA & PBA) each consists of 16 bits. LBA[9:0] & PBA[9:0] are effective Block Addresses. LBA[15:14] is used for additional information.

5. Status Register Addresses:
   Status Register 1 / Protection Register: Addr = Axh
   Status Register 2 / Configuration Register: Addr = Bxh
   Status Register 3 / Status Register: Addr = Cxh

6. Dual SPI Address Input (**CA15-8 / 2** and **CA7-0 / 2**) format:
   IO0 = x, x, CA10, CA8, CA6, CA4, CA2, CA0
   IO1 = x, x, CA11, CA9, CA7, CA5, CA3, CA1

7. Dual SPI Data Output (***D7-0 / 2***) format:
   IO0 = D6, D4, D2, D0, ……
   IO1 = D7, D5, D3, D1, ……

8. Quad SPI Address Input (**CA15-8 / 4** and **CA7-0 / 4**) format:
   IO0 = x, CA8, CA4, CA0
   IO1 = x, CA9, CA5, CA1
   IO2 = x, CA10, CA6, CA2
   IO3 = x, CA11, CA7, CA3

9. Quad SPI Data Input/Output (***D7-0 / 4***) format:
   IO0 = D4, D0, ……
   IO1 = D5, D1, ……
   IO2 = D6, D2, ……
   IO3 = D7, D3, ……

10. All Quad Program/Read commands are disabled when WP-E bit is set to 1 in the Protection Register.

11. For all Read operations in the Buffer Read Mode, as soon as /CS signal is brought to high to terminate the read operation, the device will be ready to accept new instructions and all the data inside the Data Buffer will remain unchanged from the previous Page Data Read instruction.

8.2 Instruction Descriptions

8.2.1 Device Reset (FFh), Enable Reset (66h) and Reset Device (99h)

Because of the small package and the limitation on the number of pins, the W25N512GV provide a software Reset instruction instead of a dedicated RESET pin. Once the Reset instruction is accepted, any on-going internal operations will be terminated and the device state bits will follow the below table. Once the Reset command is accepted by the device, the device will take approximately tRST to reset, depending on the current operation the device is performing, tRST can be 5us~500us. During this period, no command will be accepted.

Data corruption may happen if there is an on-going internal Erase or Program operation when Reset command sequence is accepted by the device. It is recommended to check the BUSY bit in Status Register before issuing the Reset command.

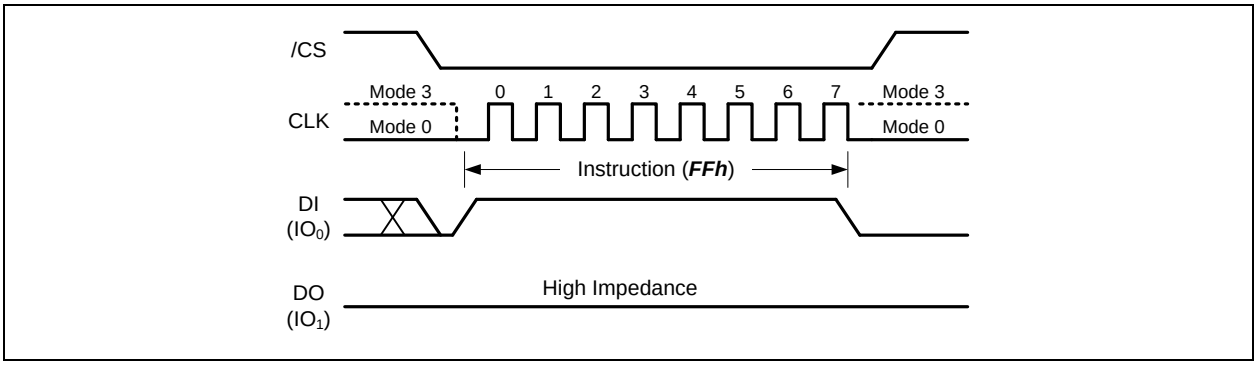


Figure 5a. Device Reset Instruction

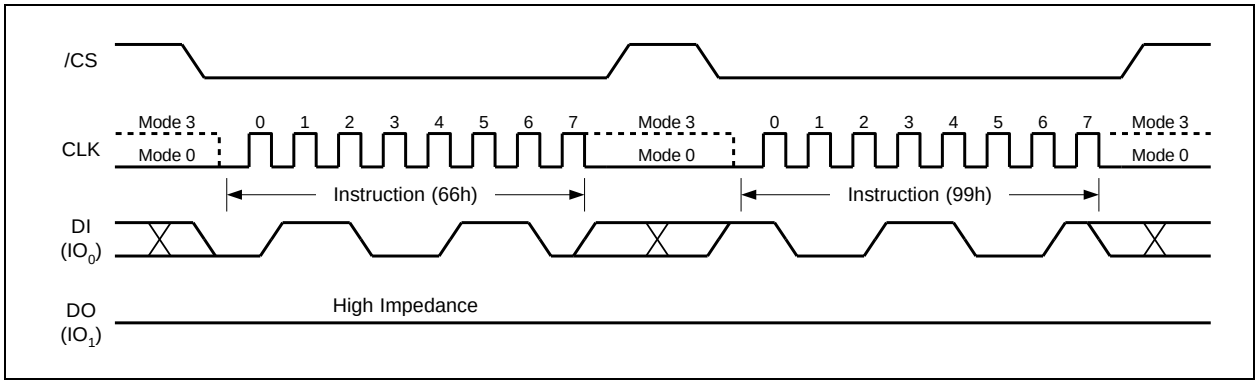


Figure 5b. Enable Reset and Reset Instruction Sequence

Register	Address	Bits	Shipment Default	Power Up after LUT is full	Power Up after OTP area locked	Power Up after SR-1 locked	After Reset (FFh) Command	After Reset (66h+99h) Command or HW Reset
Protection Register	Axh	BP[3:0], TB	1111, 1	1111, 1	1111, 1	xxxx, x (locked)	No Change	1111, 1
		SRP[1:0]	0 0	0 0	0 0	1 1 (locked)	No Change	0 0
		WP-E	0	0	0	x (locked)	No Change	0
Configuration Register	Bxh	OTP-L	0	0	1	0	Clear to 0 before OTP set	Clear to 0 before OTP set
		OTP-E	0	0	0	0	0	0
		SR1-L	0	0	0	1	Clear to 0 before OTP set	Clear to 0 before OTP set
		ECC-E	1	1	1	1	No Change	1
		BUF	1	1	1	1	No Change	1
		ODS[1:0]	1 0	1 0	1 0	1 0	No Change	1 0
		H-DIS	1	1	1	1	No Change	1
Status Register	Cxh	LUT-F	0	1	0	0	No Change	No Change
		ECC-1	0	0	0	0	0	0
		ECC-0	0	0	0	0	0	0
		P-FAIL	0	0	0	0	0	0
		E-FAIL	0	0	0	0	0	0
		WEL	0	0	0	0	0	0
Page 0 Reload			Page 0 reload	Page 0 reload	Page 0 reload	Page 0 reload	Fix no reload	Option page reload (default no reload)

Default values of the Status Registers after power up and Device Reset

8.2.2 Read JEDEC ID (9Fh)

The Read JEDEC ID instruction is compatible with the JEDEC standard for SPI compatible serial memories that was adopted in 2003. The instruction is initiated by driving the /CS pin low and shifting the instruction code “9Fh” followed by 8 dummy clocks. The JEDEC assigned Manufacturer ID byte for Winbond (EFh) and two Device ID bytes are then shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 6. For memory type and capacity values refer to Manufacturer and Device Identification table.

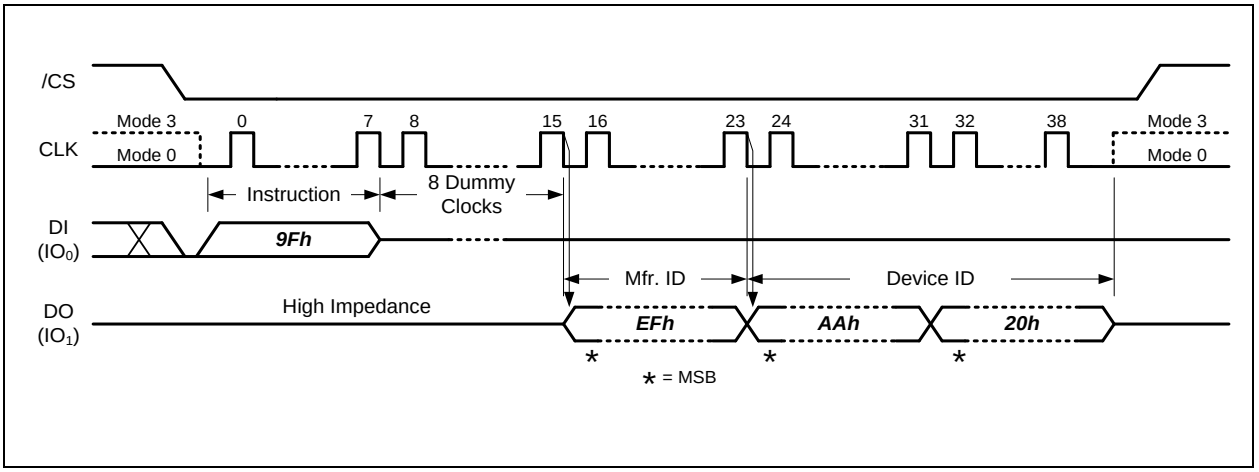


Figure 6. Read JEDEC ID Instruction

8.2.3 Read Status Register (0Fh / 05h)

The Read Status Register instructions allow the 8-bit Status Registers to be read. The instruction is entered by driving /CS low and shifting the instruction code “0Fh or 05h” into the DI pin on the rising edge of CLK followed by an 8-bit Status Register Address. The status register bits are then shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first as shown in Figure 7. Refer to section 7.1-3 for Status Register descriptions.

The Read Status Register instruction may be used at any time, even while a Program or Erase cycle is in progress. This allows the BUSY status bit to be checked to determine when the cycle is complete and if the device can accept another instruction. The Status Register can be read continuously. The instruction is completed by driving /CS high.

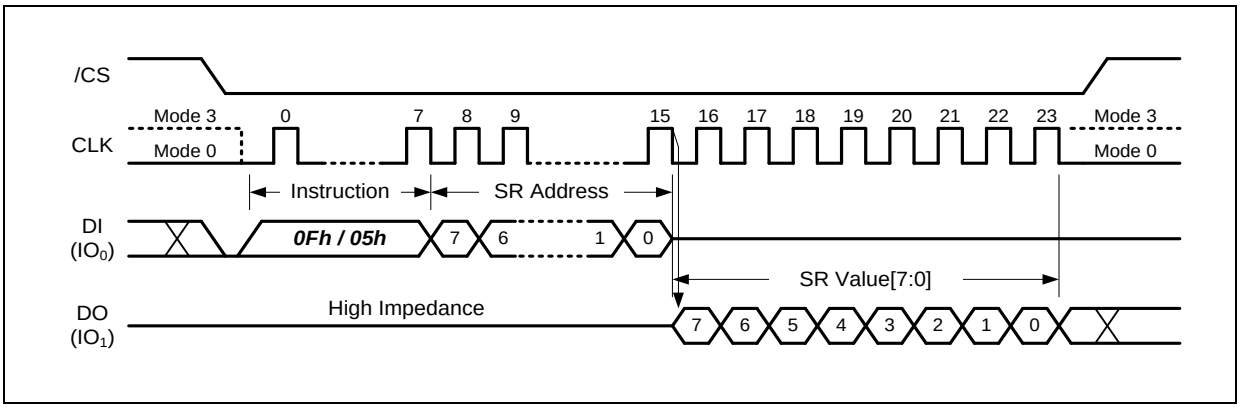


Figure 7. Read Status Register Instruction

8.2.4 Write Status Register (1Fh / 01h)

The Write Status Register instruction allows the Status Registers to be written. The writable Status Register bits include: SRP[1:0], TB, BP[3:0] and WP-E bit in Status Register-1; OTP-L, OTP-E, SR1-L, ECC-E and BUF bit in Status Register-2. All other Status Register bit locations are read-only and will not be affected by the Write Status Register instruction.

To write the Status Register bits, the instruction is entered by driving /CS low, sending the instruction code "1Fh or 01h", followed by an 8-bit Status Register Address, and then writing the status register data byte as illustrated in Figure 8.

Refer to section 7.1-3 for Status Register descriptions. After power up, factory default for BP[3:0], TB, ECC-E bits are 1, while other bits are 0.

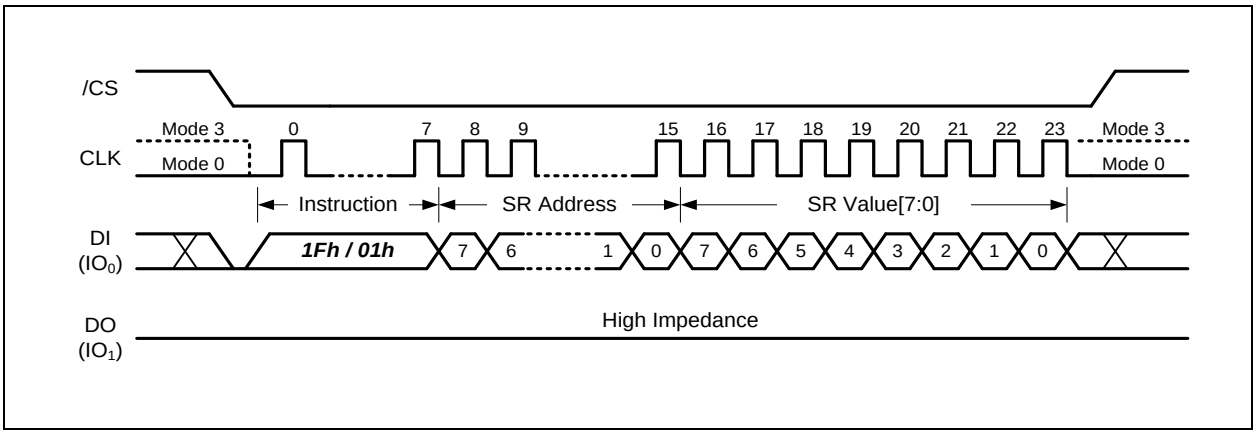


Figure 8. Write Status Register-1/2/3 Instruction

8.2.5 Write Enable (06h)

The Write Enable instruction (Figure 9) sets the Write Enable Latch (WEL) bit in the Status Register to a 1. The WEL bit must be set prior to every Page Program, Quad Page Program, Block Erase, Chip Erase and Bad Block Management instruction. The Write Enable instruction is entered by driving /CS low, shifting the instruction code “06h” into the Data Input (DI) pin on the rising edge of CLK, and then driving /CS high.

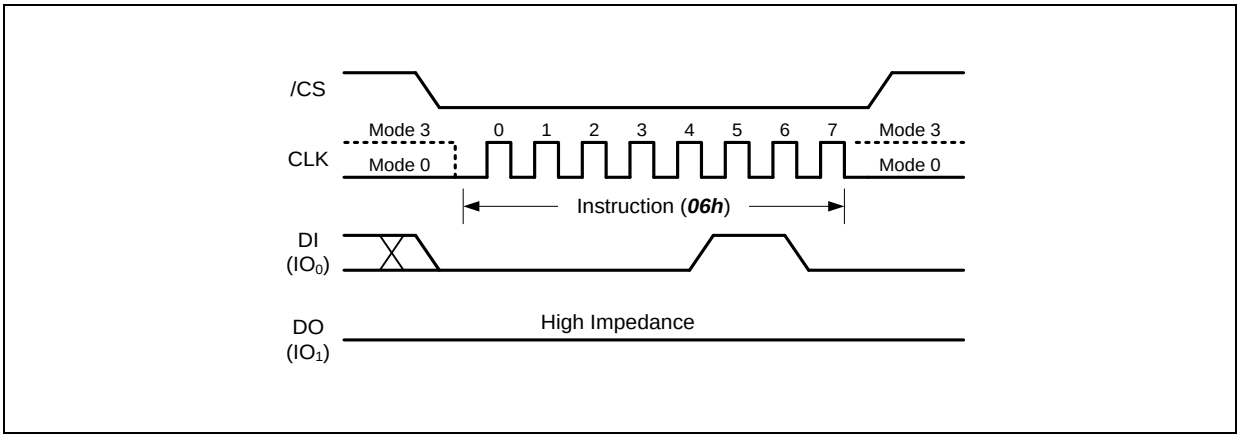


Figure 9. Write Enable Instruction

8.2.6 Write Disable (04h)

The Write Disable instruction (Figure 10) resets the Write Enable Latch (WEL) bit in the Status Register to a 0. The Write Disable instruction is entered by driving /CS low, shifting the instruction code “04h” into the DI pin and then driving /CS high. Note that the WEL bit is automatically reset after Power-up and upon completion of the Page Program, Quad Page Program, Block Erase, Chip Erase, Reset and Bad Block Management instructions.

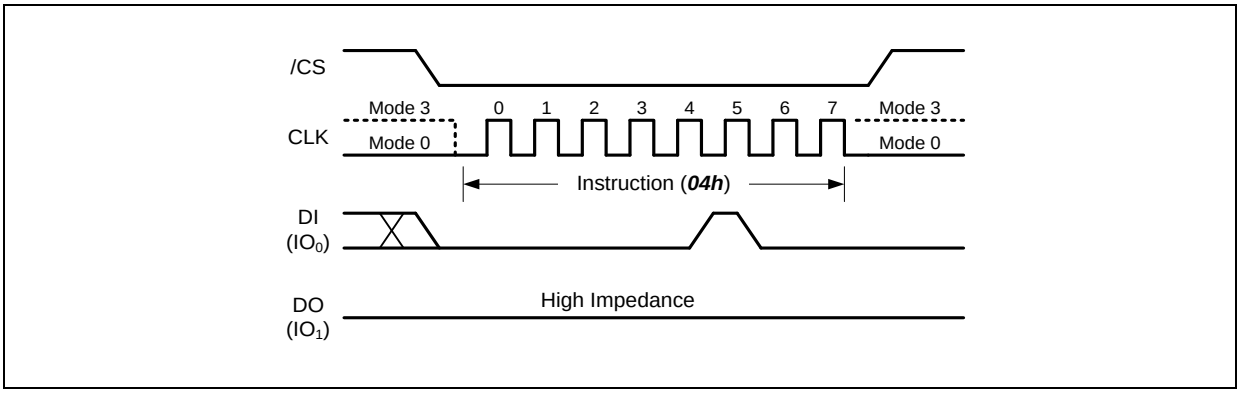


Figure 10. Write Disable Instruction

8.2.7 Bad Block Management (A1h)

Due to large NAND memory density size and the technology limitation, NAND memory devices are allowed to be shipped to the end customers with certain amount of “Bad Blocks” found in the factory testing. Up to 2% of the memory blocks can be marked as “Bad Blocks” upon shipment, which is a maximum of 10 blocks for W25N512GV. In order to identify these bad blocks, it is recommended to scan the entire memory array for bad block markers set in the factory. A “Bad Block Marker” is a non-FFh data byte stored at Byte 0 of Page 0 for each bad block. An additional marker is also stored in the first byte of the 64-Byte spare area.

W25N512GV offers a convenient method to manage the bad blocks typically found in NAND flash memory after extensive use. The “Bad Block Management” command is initiated by shifting the instruction code “A1h” into the DI pin and followed by the 16-bit “Logical Block Address” and 16-bit “Physical Block Address” as illustrated in Figure 11. A Write Enable instruction must be executed before the device will accept the Bad Block Management Instructions (Status Register bit WEL= 1). The logical block address is the address for the “bad” block that will be replaced by the “good” block indicated by the physical block address.

Once a Bad Block Management command is successfully executed, the specified LBA-PBA link will be added to the internal Look Up Table (LUT). Up to 10 links can be established in the non-volatile LUT. If all 10 links have been written, the LUT-F bit in the Status Register will become a 1, and no more LBA-PBA links can be established. Therefore, prior to issuing the Bad Block Management command, the LUT-F bit value can be checked or a “Read BBM Look Up Table” command can be issued to confirm if spare links are still available in the LUT.

Registering the same address in multiple PBAs is prohibited. It may cause unexpected behavior.

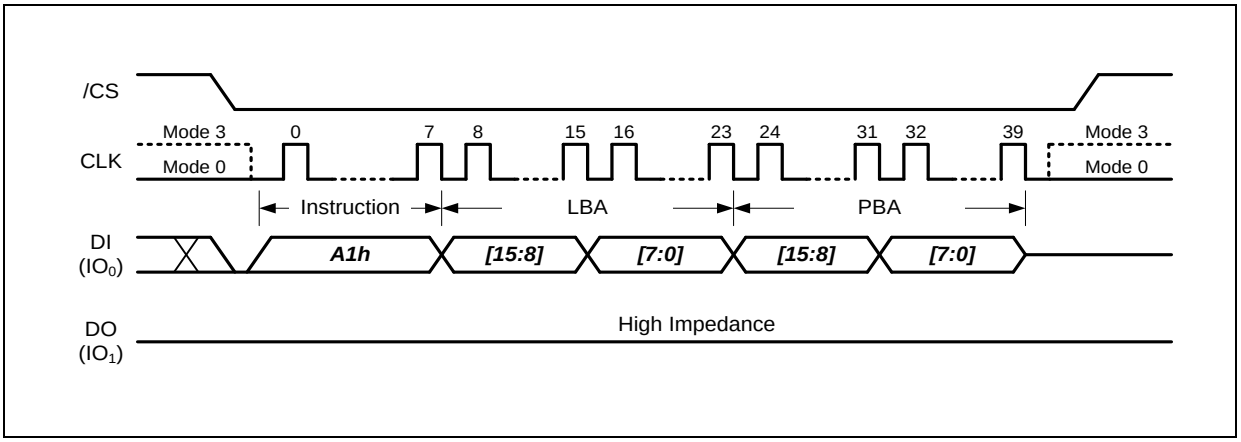


Figure 11. Bad Block Management Instruction

8.2.8 Read BBM Look Up Table (A5h)

The internal Look Up Table (LUT) consists of 10 Logical-Physical memory block links (from LBA0/PBA0 to LBA9/PBA9). The “Read BBM Look Up Table” command can be used to check the existing address links stored inside the LUT.

The “Read BBM Look Up Table” command is initiated by shifting the instruction code “A5h” into the DI pin and followed by 8-bit dummy clocks, at the falling edge of the 16th clocks, the device will start to output the 16-bit “Logical Block Address” and the 16-bit “Physical Block Address” as illustrated in Figure 12. All block address links will be output sequentially starting from the first link (LBA0 & PBA0) in the LUT. If there are available links that are unused, the output will contain all “00h” data.

The MSB bits LBA[15:14] of each link are used to indicate the status of the link.

LBA[15] (Enable)	LBA[14] (Invalid)	Descriptions
0	0	This link is available to use.
1	0	This link is enabled and it is a valid link.
1	1	This link was enabled, but it is not valid any more.
0	1	Not applicable.

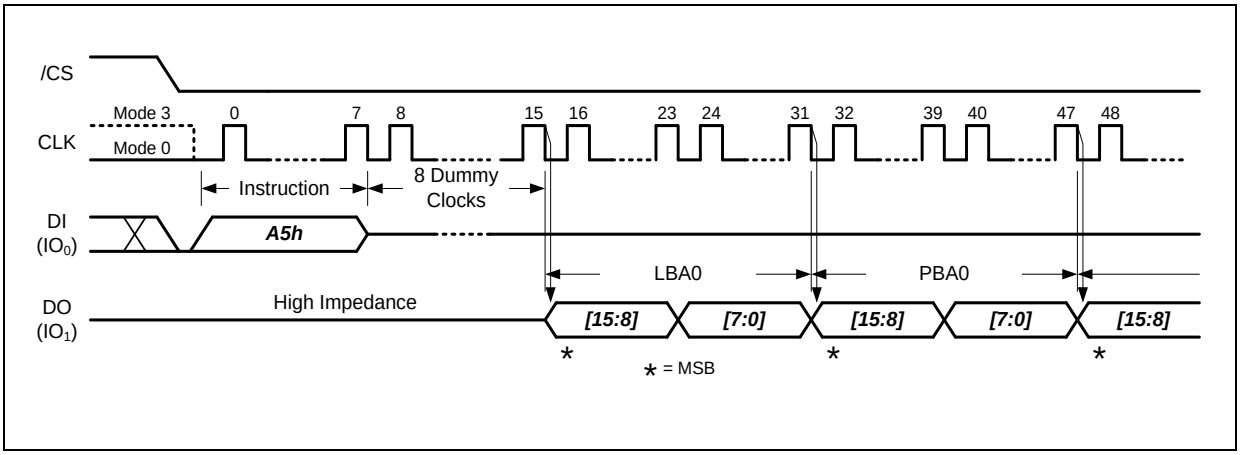


Figure 12. Read BBM Look Up Table Instruction

8.2.9 128KB Block Erase (D8h)

The 128KB Block Erase instruction sets all memory within a specified block (64-Pages, 128K-Bytes) to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Block Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code “D8h” followed by 8-bit dummy clocks and the 16-bit page address. The Block Erase instruction sequence is shown in Figure 13.

The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Block Erase instruction will not be executed. After /CS is driven high, the self-timed Block Erase instruction will commence for a time duration of t_{BE} (See AC Characteristics). While the Block Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Block Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Block Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Block Erase instruction will not be executed if the addressed block is protected by the Block Protect (TB, BP2, BP1, and BP0) bits.

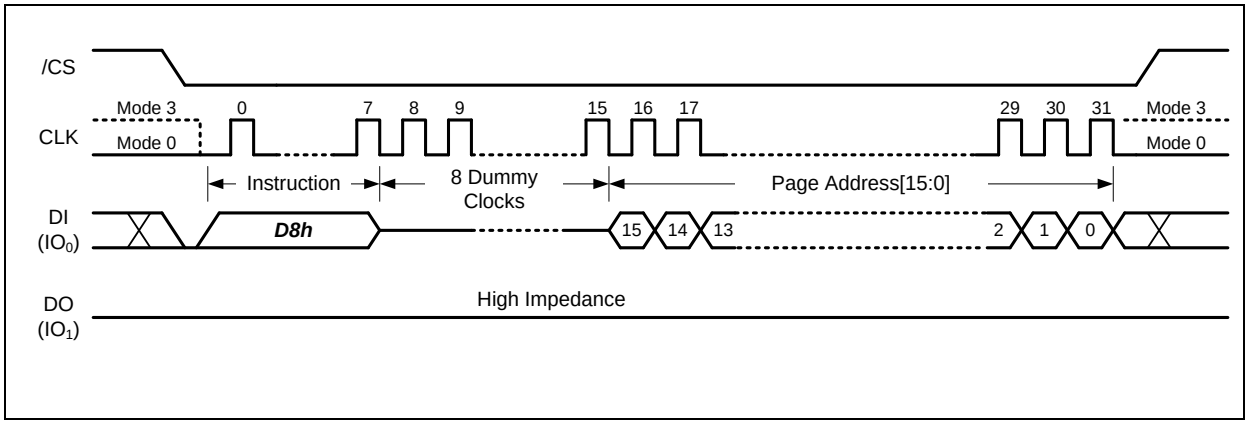


Figure 13. 128KB Block Erase Instruction

8.2.10 Load Program Data (02h) / Random Load Program Data (84h)

The Program operation allows from one byte to 2,112 bytes (a page) of data to be programmed at previously erased (FFh) memory locations. A Program operation involves two steps: 1. Load the program data into the Data Buffer. 2. Issue “Program Execute” command to transfer the data from Data Buffer to the specified memory page.

A Write Enable instruction must be executed before the device will accept the Load Program Data Instructions (Status Register bit WEL= 1). The “Load Program Data” or “Random Load Program Data” instruction is initiated by driving the /CS pin low then shifting the instruction code “02h” or “84h” followed by a 16-bit column address (only CA[11:0] is effective) and at least one byte of data into the DI pin. The /CS pin must be held low for the entire length of the instruction while data is being sent to the device. If the number of data bytes sent to the device exceeds the number of data bytes in the Data Buffer, the extra data will be ignored by the device. The Load Program Data instruction sequence is shown in Figure 14.

Both “Load Program Data” and “Random Load Program Data” instructions share the same command sequence. The difference is that “Load Program Data” instruction will reset the unused the data bytes in the Data Buffer to FFh value, while “Random Load Program Data” instruction will only update the data bytes that are specified by the command input sequence, the rest of the Data Buffer will remain unchanged.

If internal ECC algorithm is enabled, all 2,112 bytes of data will be accepted, but the bytes designated for ECC parity bits in the extra 64 bytes section will be overwritten by the ECC calculation. If the ECC-E bit is set to a 0 to disable the internal ECC, the extra 64 bytes section can be used for external ECC purpose or other usage.

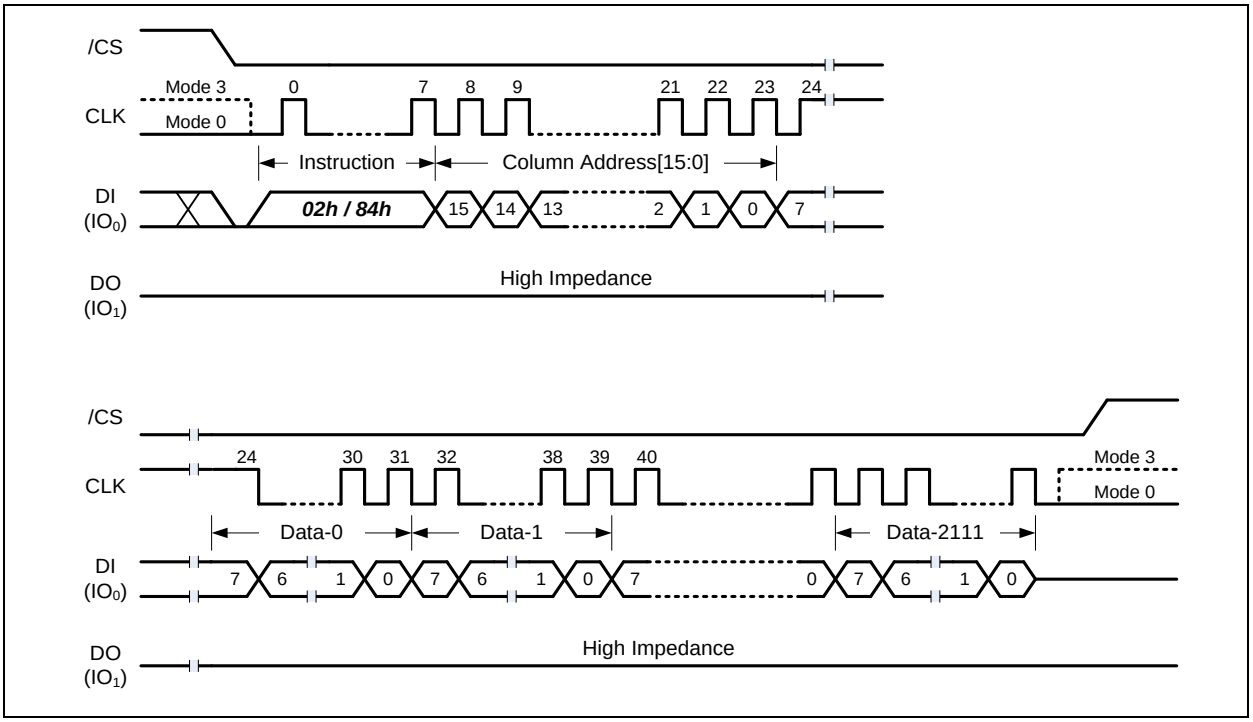


Figure 14. Load / Random Load Program Data Instruction

8.2.11 Quad Load Program Data (32h) / Quad Random Load Program Data (34h)

The “Quad Load Program Data” and “Quad Random Load Program Data” instructions are identical to the “Load Program Data” and “Random Load Program Data” in terms of operation sequence and functionality. The only difference is that “Quad Load” instructions will input the data bytes from all four IO pins instead of the single DI pin. This method will significantly shorten the data input time when a large amount of data needs to be loaded into the Data Buffer. The instruction sequence is illustrated in Figure 15.

Both “Quad Load Program Data” and “Quad Random Load Program Data” instructions share the same command sequence. The difference is that “Quad Load Program Data” instruction will reset the unused the data bytes in the Data Buffer to FFh value, while “Quad Random Load Program Data” instruction will only update the data bytes that are specified by the command input sequence, the rest of the Data Buffer will remain unchanged.

When WP-E bit in the Status Register is set to a 1, all Quad SPI instructions are disabled.

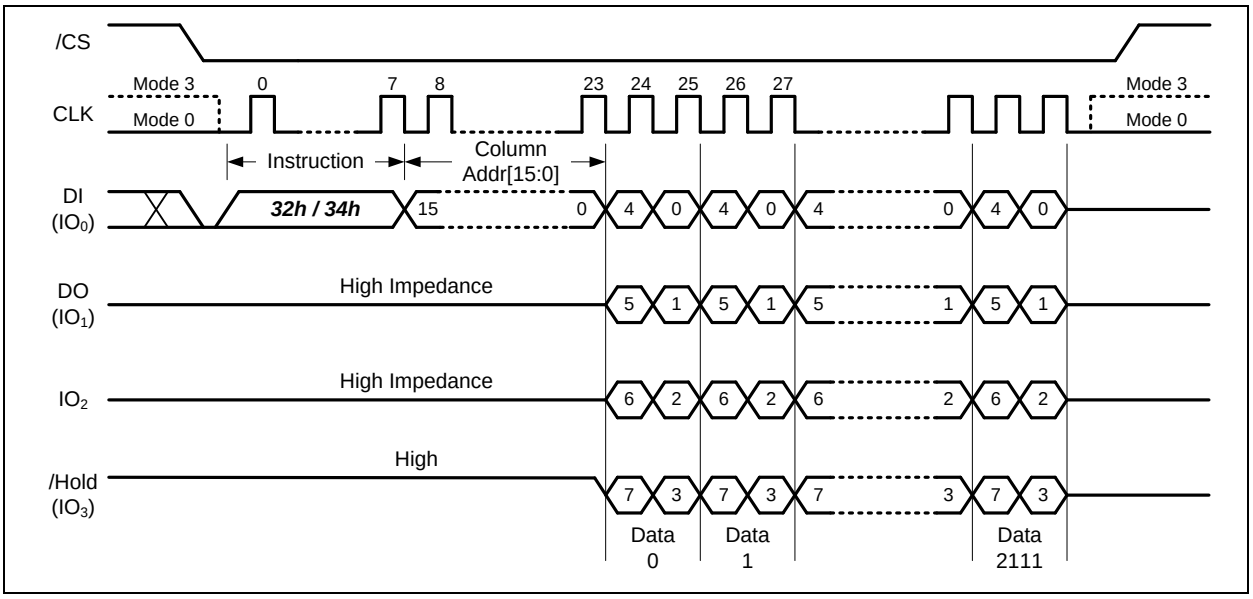


Figure 15. Quad Load / Quad Random Load Program Data Instruction

8.2.12 Program Execute (10h)

The Program Execute instruction is the second step of the Program operation. After the program data are loaded into the 2,112-Byte Data Buffer (or 2,048 bytes when ECC is enabled), the Program Execute instruction will program the Data Buffer content into the physical memory page that is specified in the instruction. The instruction is initiated by driving the /CS pin low then shifting the instruction code “10h” followed by 8-bit dummy clocks and the 16-bit Page Address into the DI pin as shown in Figure 16.

After /CS is driven high to complete the instruction cycle, the self-timed Program Execute instruction will commence for a time duration of tpp (See AC Characteristics). While the Program Execute cycle is in progress, the Read Status Register instruction may still be used for checking the status of the BUSY bit. The BUSY bit is a 1 during the Program Execute cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Program Execute cycle has finished, the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Program Execute instruction will not be executed if the addressed page is protected by the Block Protect (TB, BP2, BP1, and BP0) bits. Only 4 partial page program times are allowed on every single page.

The pages within the block have to be programmed sequentially from the lower order page address to the higher order page address within the block. Programming pages out of sequence is prohibited.

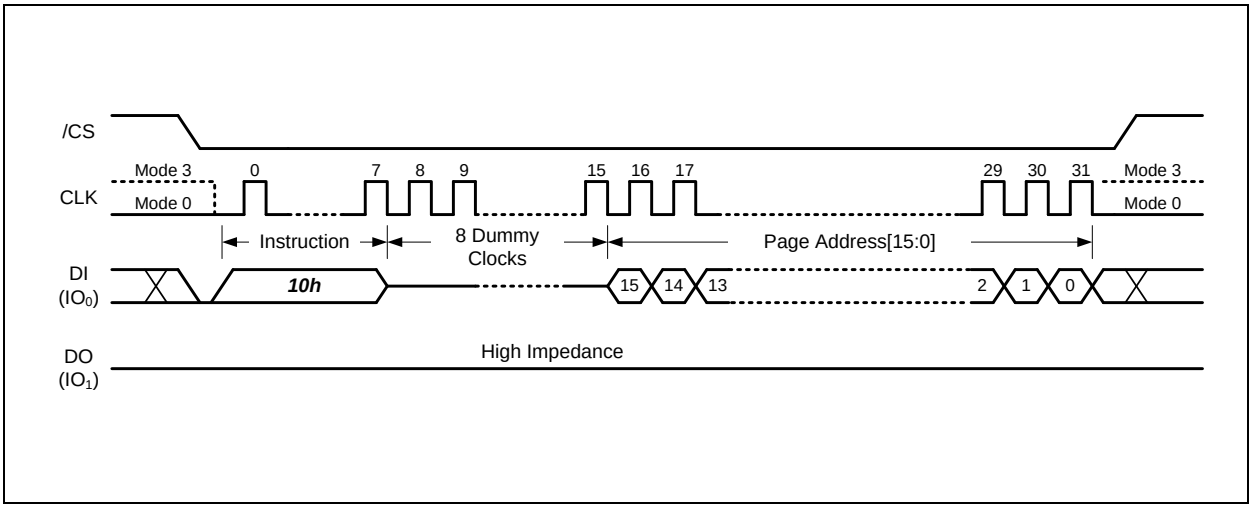


Figure 16. Program Execute Instruction

8.2.13 Page Data Read (13h)

The Page Data Read instruction will transfer the data of the specified memory page into the 2,112-Byte Data Buffer. The instruction is initiated by driving the /CS pin low then shifting the instruction code “13h” followed by 8-bit dummy clocks and the 16-bit Page Address into the DI pin as shown in Figure 17.

After /CS is driven high to complete the instruction cycle, the self-timed Read Page Data instruction will commence for a time duration of tRD (See AC Characteristics). While the Read Page Data cycle is in progress, the Read Status Register instruction may still be used for checking the status of the BUSY bit. The BUSY bit is a 1 during the Read Page Data cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again.

After the 2,112 bytes of page data are loaded into the Data Buffer, several Read instructions can be issued to access the Data Buffer and read out the data.

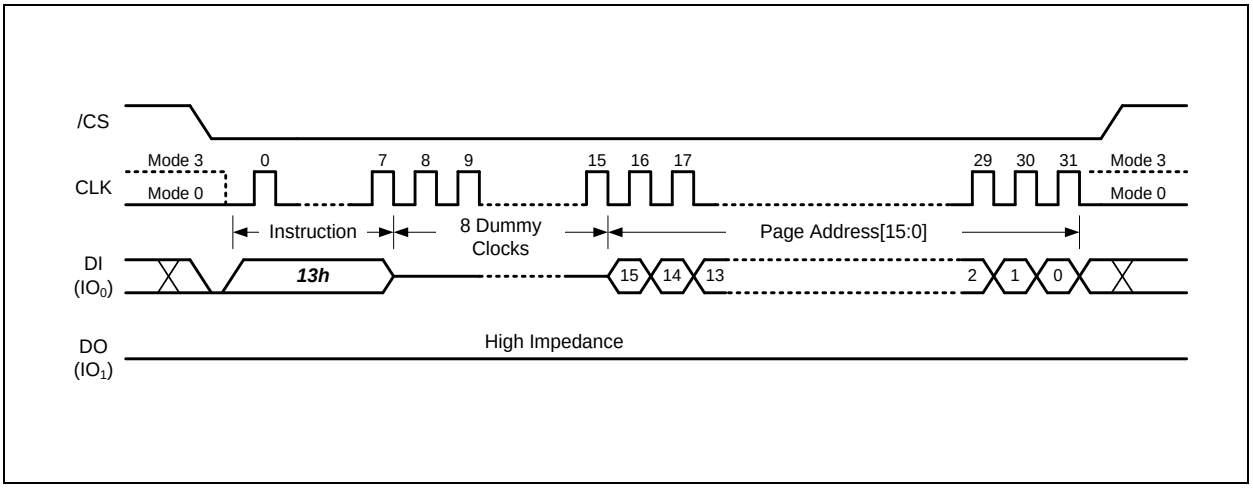


Figure 17. Page Data Read Instruction

8.2.14 Read Data (03h)

The Read Data instruction allows one or more data bytes to be sequentially read from the Data Buffer after executing the Read Page Data instruction. The Read Data instruction is initiated by driving the /CS pin low and then shifting the instruction code “03h” followed by the 16-bit Column Address and 8-bit dummy clocks or a 24-bit dummy clocks into the DI pin. After the address is received, the data byte of the addressed Data Buffer location will be shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first. The address is automatically incremented to the next higher address after each byte of data is shifted out allowing for a continuous stream of data. The instruction is completed by driving /CS high.

The Read Data instruction sequence is shown in Figure 18. When BUF=1, the device is in the Buffer Read Mode. The data output sequence will start from the Data Buffer location specified by the 16-bit Column Address and continue to the end of the Data Buffer. Once the last byte of data is output, the output pin will become Hi-Z state.

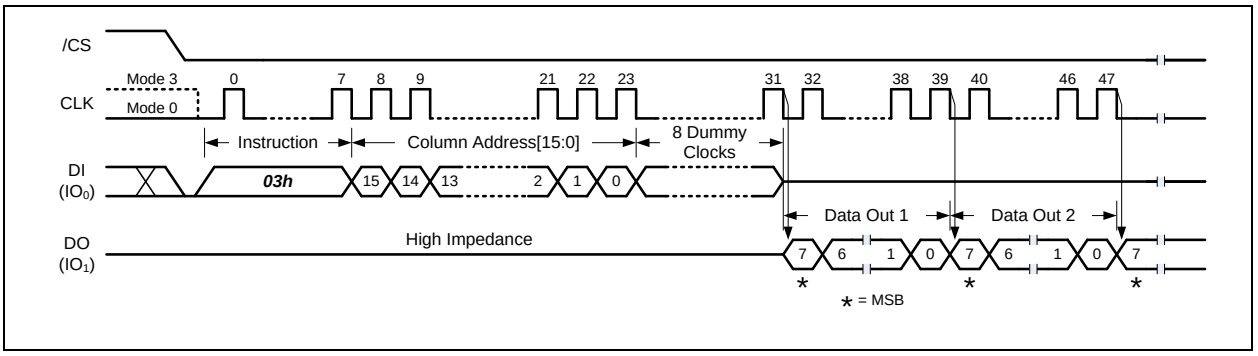


Figure 18. Read Data Instruction (Buffer Read Mode, BUF=1)

8.2.15 Fast Read (0Bh)

The Fast Read instruction allows one or more data bytes to be sequentially read from the Data Buffer after executing the Read Page Data instruction. The Fast Read instruction is initiated by driving the /CS pin low and then shifting the instruction code “0Bh” followed by the 16-bit Column Address and 8-bit dummy clocks or a 32-bit dummy clocks into the DI pin. After the address is received, the data byte of the addressed Data Buffer location will be shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first. The address is automatically incremented to the next higher address after each byte of data is shifted out allowing for a continuous stream of data. The instruction is completed by driving /CS high.

The Fast Read instruction sequence is shown in Figure 19. When BUF=1, the device is in the Buffer Read Mode. The data output sequence will start from the Data Buffer location specified by the 16-bit Column Address and continue to the end of the Data Buffer. Once the last byte of data is output, the output pin will become Hi-Z state.

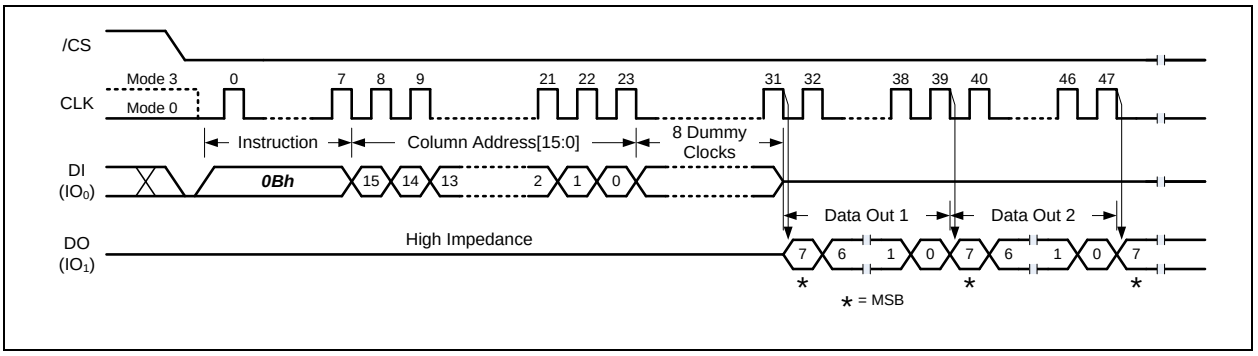


Figure 19. Fast Read Instruction (Buffer Read Mode, BUF=1)

8.2.16 Fast Read Dual Output (3Bh)

The Fast Read Dual Output (3Bh) instruction is similar to the standard Fast Read (0Bh) instruction except that data is output on two pins; IO_0 and IO_1. This allows data to be transferred at twice the rate of standard SPI devices.

The Fast Read Dual Output instruction sequence is shown in Figure 20. When BUF=1, the device is in the Buffer Read Mode. The data output sequence will start from the Data Buffer location specified by the 16-bit Column Address and continue to the end of the Data Buffer. Once the last byte of data is output, the output pin will become Hi-Z state.

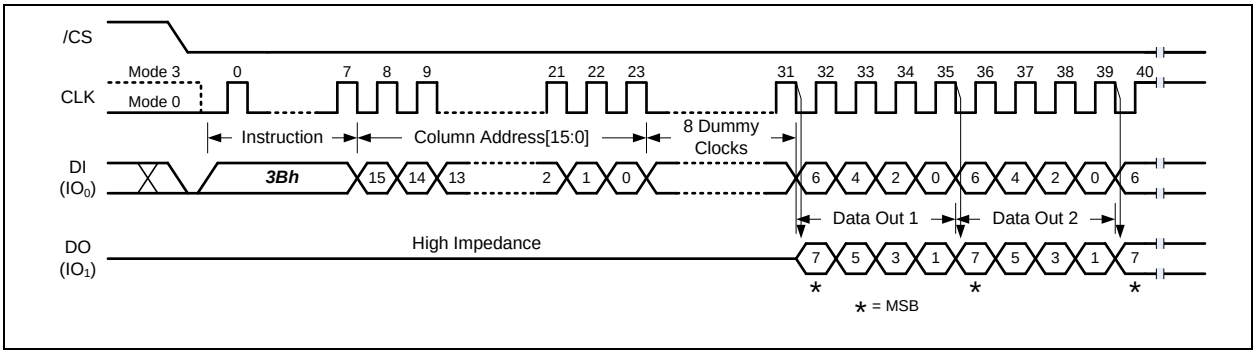


Figure 20. Fast Read Dual Output Instruction (Buffer Read Mode, BUF=1)

8.2.17 Fast Read Quad Output (6Bh)

The Fast Read Quad Output (6Bh) instruction is similar to the Fast Read Dual Output (3Bh) instruction except that data is output on four pins, IO_0, IO_1, IO_2, and IO_3. The Fast Read Quad Output Instruction allows data to be transferred at four times the rate of standard SPI devices.

The Fast Read Quad Output instruction sequence is shown in Figure 21. When BUF=1, the device is in the Buffer Read Mode. The data output sequence will start from the Data Buffer location specified by the 16-bit Column Address and continue to the end of the Data Buffer. Once the last byte of data is output, the output pin will become Hi-Z state.

When WP-E bit in the Status Register is set to a 1, this instruction is disabled.

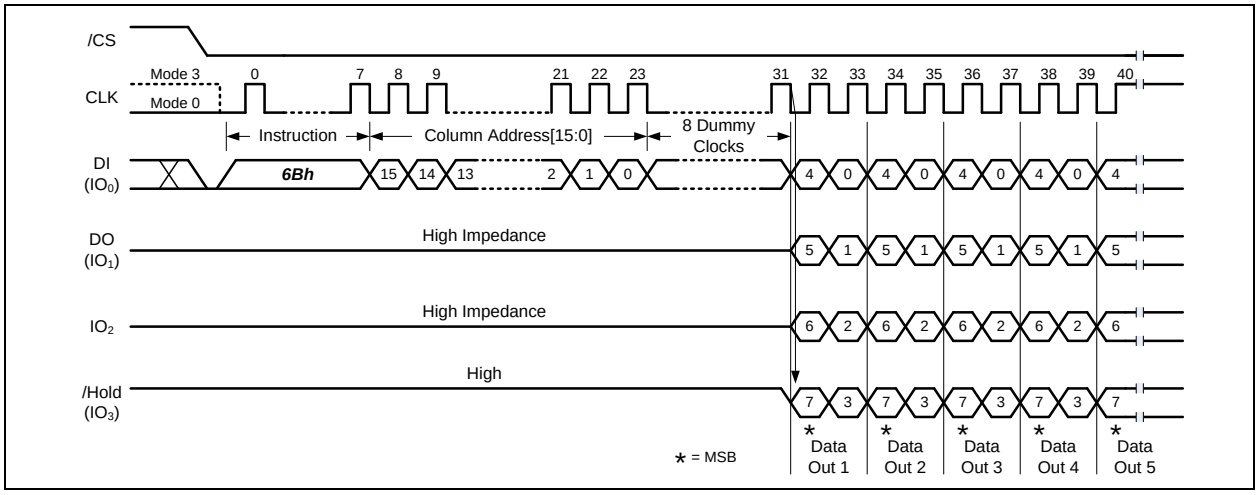


Figure 21. Fast Read Quad Output Instruction (Buffer Read Mode, BUF=1)

8.2.18 Fast Read Dual I/O (BBh)

The Fast Read Dual I/O (BBh) instruction allows for improved random access while maintaining two IO pins, IO_0 and IO_1. It is similar to the Fast Read Dual Output (3Bh) instruction but with the capability to input the Column Address or the dummy clocks two bits per clock. This reduced instruction overhead may allow for code execution (XIP) directly from the Dual SPI in some applications.

The Fast Read Quad Output instruction sequence is shown in Figure 22. When BUF=1, the device is in the Buffer Read Mode. The data output sequence will start from the Data Buffer location specified by the 16-bit Column Address and continue to the end of the Data Buffer. Once the last byte of data is output, the output pin will become Hi-Z state.

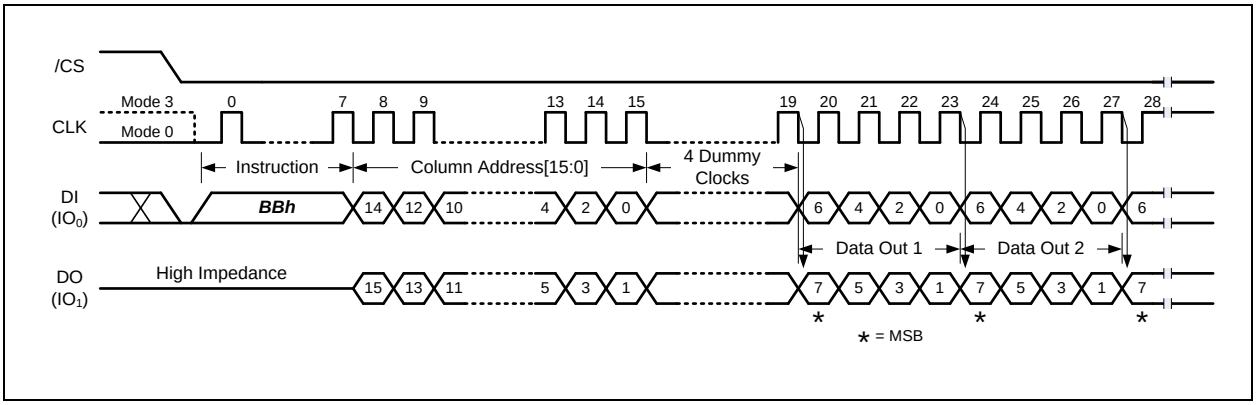


Figure 22. Fast Read Dual I/O Instruction (Buffer Read Mode, BUF=1)

8.2.19 Fast Read Quad I/O (EBh)

The Fast Read Quad I/O (EBh) instruction is similar to the Fast Read Dual I/O (BBh) instruction except that address and data bits are input and output through four pins IO_0, IO_1, IO_2 and IO_3 prior to the data output. The Quad I/O dramatically reduces instruction overhead allowing faster random access for code execution (XIP) directly from the Quad SPI.

The Fast Read Quad Output instruction sequence is shown in Figure 23. When BUF=1, the device is in the Buffer Read Mode. The data output sequence will start from the Data Buffer location specified by the 16-bit Column Address and continue to the end of the Data Buffer. Once the last byte of data is output, the output pin will become Hi-Z state.

When WP-E bit in the Status Register is set to a 1, this instruction is disabled.

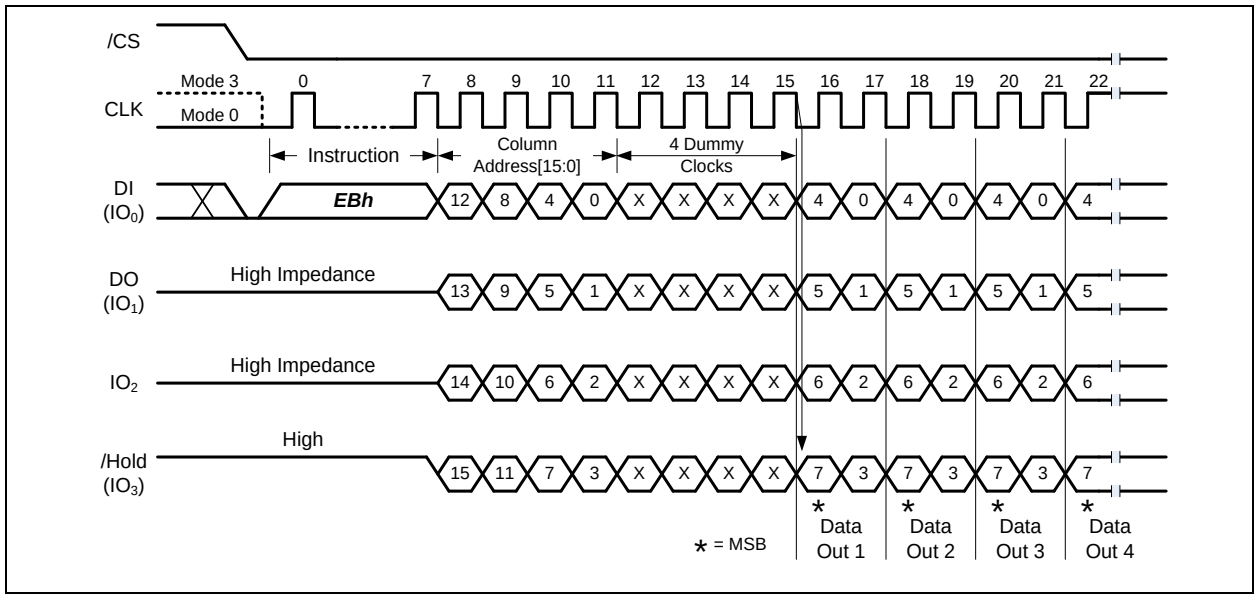


Figure 23. Fast Read Quad I/O Instruction (Buffer Read Mode, BUF=1)

8.2.20 Accessing Unique ID / Parameter / OTP Pages (OTP-E=1)

In addition to the main memory array, the W25N512GV is also equipped with one Unique ID Page, one Parameter Page, and ten OTP Pages.

Page Address	Page Name	Descriptions	Data Length
00h	Unique ID Page	Factory programmed, Read Only	32-Byte x 16
01h	Parameter Page	Factory programmed, Read Only	256-Byte x 3
02h	OTP Page [0]	Program Only, OTP lockable	2,112-Byte
…	OTP Pages [1:8]	Program Only, OTP lockable	2,112-Byte
0Bh	OTP Page [9]	Program Only, OTP lockable	2,112-Byte

To access these additional data pages, the OTP-E bit in Status Register-2 must be set to "1" first. Then, Read operations can be performed on Unique ID and Parameter Pages, Read and Program operations can be performed on the OTP pages if it's not already locked. To return to the main memory array operation, OTP-E bit needs to be to set to 0.

Read Operations

A "Page Data Read" command must be issued followed by a specific page address shown in the table above to load the page data into the main Data Buffer. After the device finishes the data loading (BUSY=0), all Read commands may be used to read the Data Buffer starting from any specified Column Address. Please note all Read commands must now follow the "Buffer Read Mode" command structure (CA[15:0], number of dummy clocks) regardless the previous BUF bit setting. ECC can also be enabled for the OTP page read operations to ensure the data integrity.

Program and OTP Lock Operations

OTP pages provide the additional space (2K-Byte x 10) to store important data or security information that can be locked to prevent further modification in the field. These OTP pages are in an erased state set in the factory, and can only be programmed (change data from "1" to "0") until being locked by OTP-L bit in the Configuration/Status Register-2. OTP-E must be first set to "1" to enable the access to these OTP pages, then the program data must be loaded into the main Data Buffer using any "Program Data Load" commands. The "Program Execute" command followed by a specific OTP Page Address is used to initiate the data transfer from the Data Buffer to the OTP page. When ECC is enabled, ECC calculation will be performed during "Program Execute", and the ECC information will be stored into the 64-Byte spare area.

Once the OTP pages are correctly programmed, OTP-L bit can be used to permanently lock these pages so that no further modification is possible. While still in the "OTP Access Mode" (OTP-E=1), user needs to set OTP-L bit in the Configuration/Status Register-2 to "1", and issue a "Program Execute" command(Page address is "don't care"). After the device finishes the OTP lock setting (BUSY=0), the user can set OTP-E to "0" to return to the main memory array operation.

SR1-L OTP Lock Operation

The Protection/Status Register-1 contains protection bits that can be set to protect either a portion or the entire memory array from being Programmed/Erased or set the device to either Software Write Protection (WP-E=0) or Hardware Write Protection (WP-E=1). Once the BP[3:0], TB, WP-E bits are set correctly, SRP1 and SRP0 should also be set to "1"s as well to allow SR1-L bit being set to "1" to permanently lock the protection settings in the Status Register-1 (SR1). Similar to the OTP-L setting procedure above, in order to set SR1-L lock bit, the device must enter the "OTP Access Mode" (OTP-E=1) first, and SR1-L bit should be set to "1" prior to the "Program Execute" command(Page address is "don't care"). Once SR1-L is set to "1" (BUSY=0), the user can set OTP-E to "0" to return to the main memory array operation.

8.2.21 Parameter Page Data Definitions

The Parameter Page contains 3 identical copies of the 256-Byte Parameter Data. The table below lists all the key data byte locations. All other unspecified byte locations have 00h data as default.

Byte Number	Descriptions	Values
0~3	Parameter page signature	4Fh, 4Eh, 46h, 49h
4~5	Revision number	00h, 00h
6~7	Feature supported	00h, 00h
8~9	Optional command supported	02h, 00h
10~31	Reserved	All 00h
32~43	Device manufacturer	57h, 49h, 4Eh, 42h, 4Fh, 4Eh, 44h, 20h, 20h, 20h, 20h, 20h
44~63	Device model	57h, 32h, 35h, 4Eh, 35h, 31h, 32h, 47h, 56h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h
64	JEDEC manufacturer ID	EFh
65~66	Date code	00h, 00h
67~79	Reserved	All 00h
80~83	Number of data bytes per page	00h, 08h, 00h, 00h
84~85	Number of spare bytes per page	40h, 00h
86~91	Reserved	All 00h
92~95	Number of pages per block	40h, 00h, 00h, 00h
96~99	Number of blocks per logical unit	00h, 02h, 00h, 00h
100	Number of logical units	01h
101	Number of address bytes	00h
102	Number of bits per cell	01h
103~104	Bad blocks maximum per unit	0Ah, 00h
105~106	Block endurance	01h, 05h
107	Guaranteed valid blocks at beginning of target	01h
108~109	Block endurance for guaranteed valid blocks	00h, 00h
110	Number of programs per page	04h
111	Reserved	00h
112	Number of ECC bits	00h
113	Number of plane address bits	00h
114	Multi-plane operation attributes	00h
115~127	Reserved	All 00h
128	I/O pin capacitance, maximum	08h
129~132	Reserved	All 00h
133~134	Maximum page program time (us)	BCh, 02h
135~136	Maximum block erase time (us)	10h, 27h
137~138	Maximum page read time (us)	32h, 00h
139~163	Reserved	All 00h
164~165	Vendor specific revision number	00h, 00h
166~253	Vendor specific	All 00h
254~255	Integrity CRC	Set at test
256~511	Value of bytes 0~255	
512~767	Value of bytes 0~255	
768+	Reserved	

8.2.22 Deep Power-Down (B9h)

Although the standby current during normal operation is relatively low, standby current can be further reduced with the Deep Power-Down instruction. The lower power consumption makes the Power-Down instruction especially useful for battery powered applications (See ICC1 and ICC2 in AC Characteristics). The instruction is initiated by driving the /CS pin low and shifting the instruction code “B9h” as shown in Figure 24.

The /CS pin must be driven high after the eighth bit has been latched. If this is not done the Power-down instruction will not be executed. After /CS is driven high, the power-down state will entered within the time duration of t_{DP} (See AC Characteristics). While in the power-down state only the Release Power-down / Device ID (ABh) instruction, which restores the device to normal operation, will be recognized. All other instructions are ignored. This includes the Read Status Register instruction, which is always available during normal operation. Ignoring all but one instruction makes the Power Down state a useful condition for securing maximum write protection. The device always powers-up in the normal operation with the standby current of ICC1.

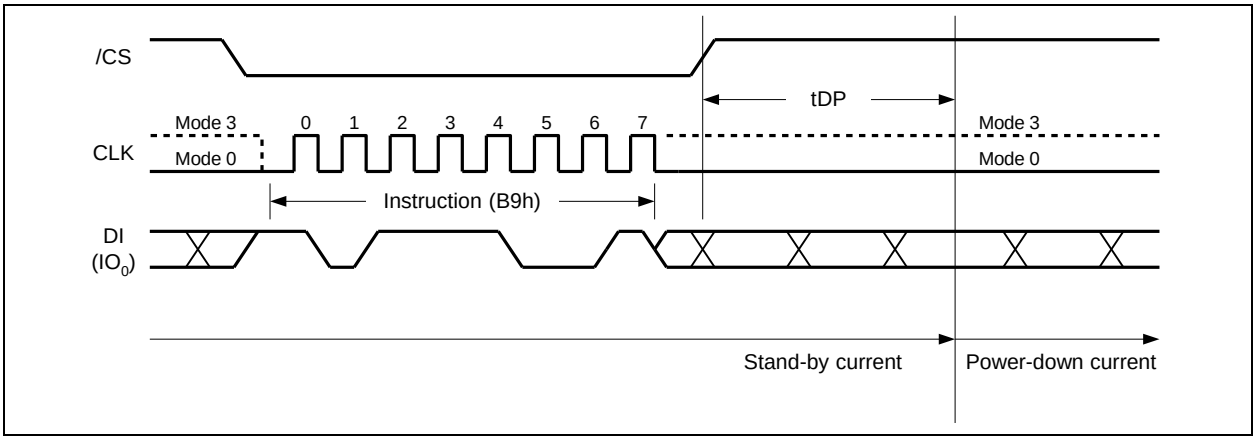


Figure 24. Deep Power-Down Instruction

8.2.23 Release Power-Down (ABh)

The Release from Power-Down instruction is used to release the device from the power-down state.

To release the device from the power-down state, the instruction is issued by driving the /CS pin low, shifting the instruction code “ABh” and driving /CS high as shown in Figure 25. Release from power-down will take the time duration of tRES (See AC Characteristics) before the device will resume normal operation and other instructions are accepted. The /CS pin must remain high during the tRES time duration.

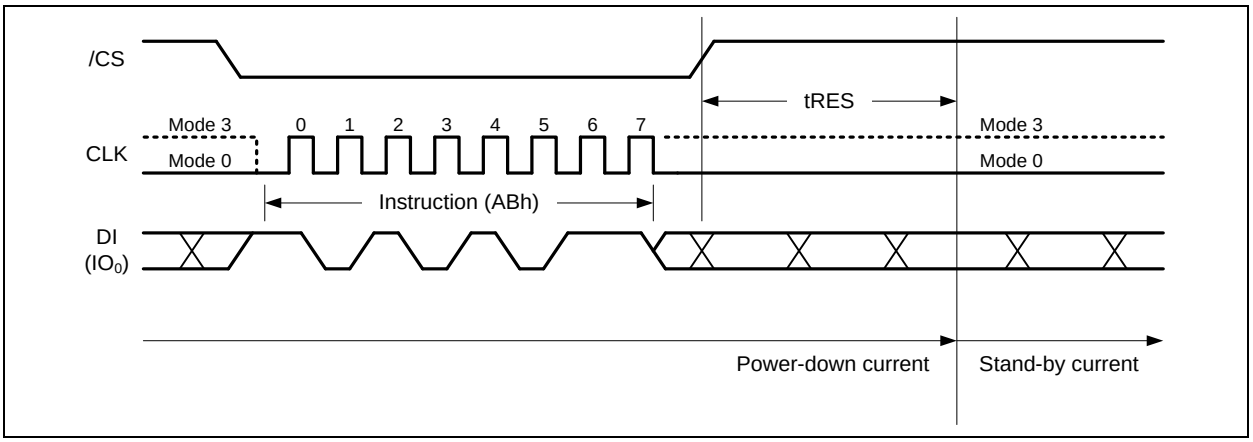


Figure 25. Release Power-down Instruction

8.2.24 Chip Erase (C7h / 60h)

The Chip Erase instruction sets all memory within the device to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Chip Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code “C7h” or “60h”. The Chip Erase instruction sequence is shown in Figure 26.

The /CS pin must be driven high after the eighth bit has been latched. If this is not done the Chip Erase instruction will not be executed. After /CS is driven high, the self-timed Chip Erase instruction will commence for a time duration of t_{CE} (See AC Characteristics). While the Chip Erase cycle is in progress, the Read Status Register instruction may still be accessed to check the status of the BUSY bit. The BUSY bit is a 1 during the Chip Erase cycle and becomes a 0 when finished and the device is ready to accept other instructions again. After the Chip Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Chip Erase instruction will not be executed if any memory region is protected by the Block Protect (TB, BP3, BP2, BP1, and BP0) bits.

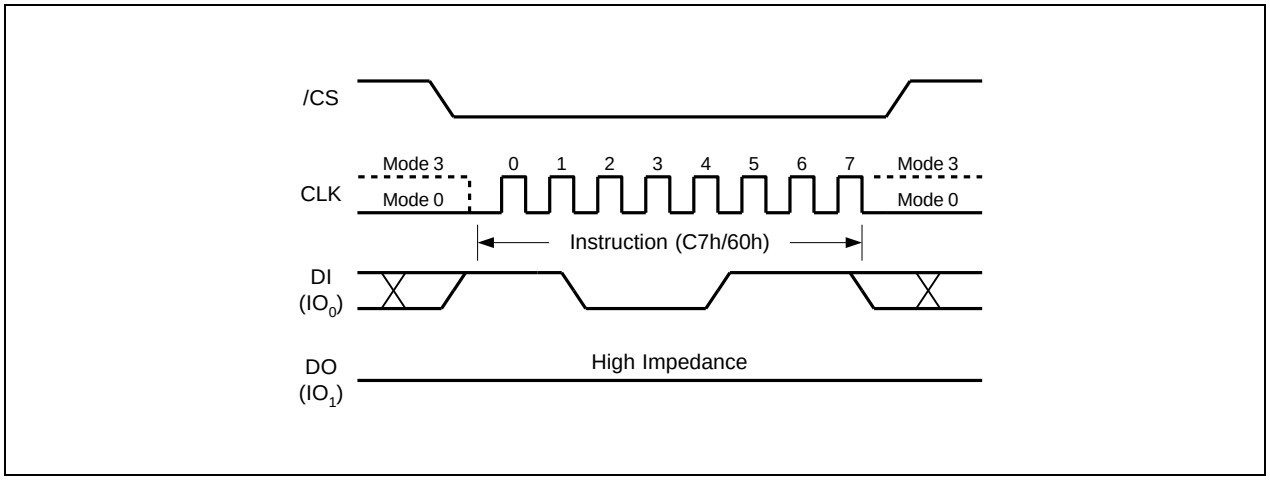


Figure 26. Chip Erase Instruction

9. ELECTRICAL CHARACTERISTICS

9.1 Absolute Maximum Ratings(1)

PARAMETERS	SYMBOL	CONDITIONS	RANGE	UNIT
Supply Voltage	VCC		–0.6 to +4.6	V
Voltage Applied to Any Pin	VIO	Relative to Ground	–0.6 to +4.6	V
Transient Voltage on any Pin	VIOT	<20nS Transient Relative to Ground	–2.0 to VCC+2.0	V
Storage Temperature	TSTG		–65 to +150	°C
Lead Temperature	TLEAD		See Note (2)	°C
Electrostatic Discharge Voltage	VESD	Human Body Model(3)	–2000 to +2000	V

Notes:

1. This device has been designed and tested for the specified operation ranges. Proper operation outside of these levels is not guaranteed. Exposure to absolute maximum ratings may affect device reliability. Exposure beyond absolute maximum ratings may cause permanent damage.
2. Compliant with JEDEC Standard J-STD-20C for small body Sn-Pb or Pb-free (Green) assembly and the European directive on restrictions on hazardous substances (RoHS) 2002/95/EU.
3. JEDEC Standard JESD22-A114A (C1=100pF, R1=1500 ohms, R2=500 ohms).

9.2 Operating Ranges

PARAMETER	SYMBOL	CONDITIONS	SPEC		UNIT
			MIN	MAX	
Supply Voltage	VCC		2.7	3.6	V
Ambient Temperature, Operating	TA	Industrial	–40	+85	°C

9.3 Power-up Power-down Timing Requirements

PARAMETER	SYMBOL	SPEC		UNIT
		MIN	MAX	
VCC (min) to /CS Low	t_{VSL}[1]	200		µs
Time Delay Before Write Instruction	t_{PUW}[1]	1		ms

Note:

1. These parameters are characterized only.

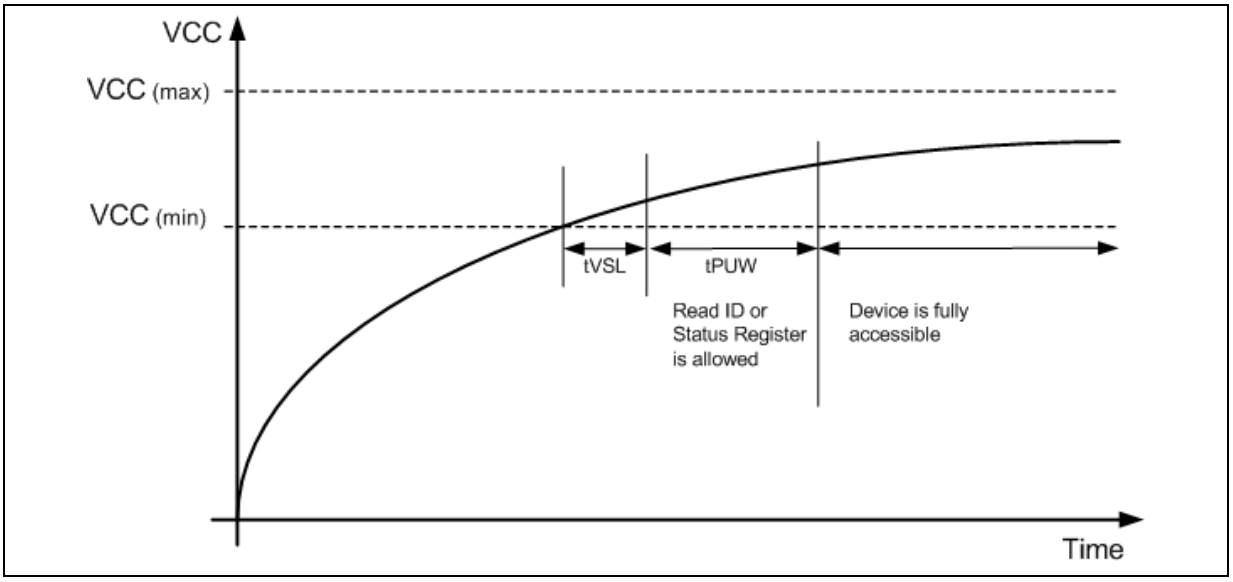


Figure 27a. Power-up Timing and Voltage Levels

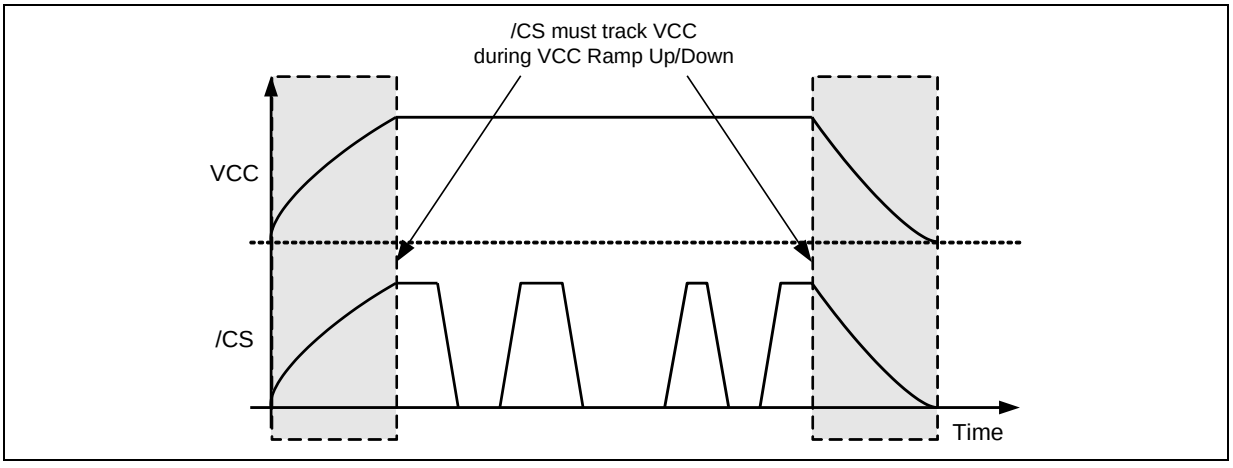


Figure 27b. Power-up, Power-Down Requirement

9.4 DC Electrical Characteristics

PARAMETER	SYMBOL	CONDITIONS	SPEC			UNIT
			MIN	TYP	MAX	
Input Capacitance	C_{IN}(1)	V_{IN} = 0V(1)			6	pF
Output Capacitance	C_{out}(1)	V_{OUT} = 0V(1)			8	pF
Input Leakage	I_{LI}				±2	µA
I/O Leakage	I_{LO}				±2	µA
Standby Current	I_{CC1}	/CS = VCC, VIN = GND or VCC		10	50	µA
Deep Power-Down Current	I_{CC2}	/CS = VCC, VIN = GND or VCC		1	10	µA
Read Current	I_{CC3}	C = 0.1 VCC / 0.9 VCC DO = Open		25	35	mA
Current Page Program	I_{CC4}	/CS = VCC		25	35	mA
Current Block/Chip Erase	I_{CC5}	/CS = VCC		25	35	mA
Input Low Voltage	V_{IL}		- 0.5		VCC x 0.3	V
Input High Voltage	V_{IH}		VCC x 0.7		VCC + 0.4	V
Output Low Voltage	V_{OL}	I_{OL} = 2.1mA			0.4	V
Output High Voltage	V_{OH}	I_{OH} = –400µA	2.4			V

Notes:

1. Tested on sample basis and specified through design and characterization data. TA = 25° C, VCC = 3.0V.

9.5 AC Measurement Conditions

PARAMETER	SYMBOL	SPEC		UNIT
		MIN	MAX	
Load Capacitance	C_L		30	pF
Input Rise and Fall Times	T_R, T_F		5	ns
Input Pulse Voltages	V_{IN}	0.1 VCC to 0.9 VCC		V
Input Timing Reference Voltages	IN	0.3 VCC to 0.7 VCC		V
Output Timing Reference Voltages	OUT	0.5 VCC		V

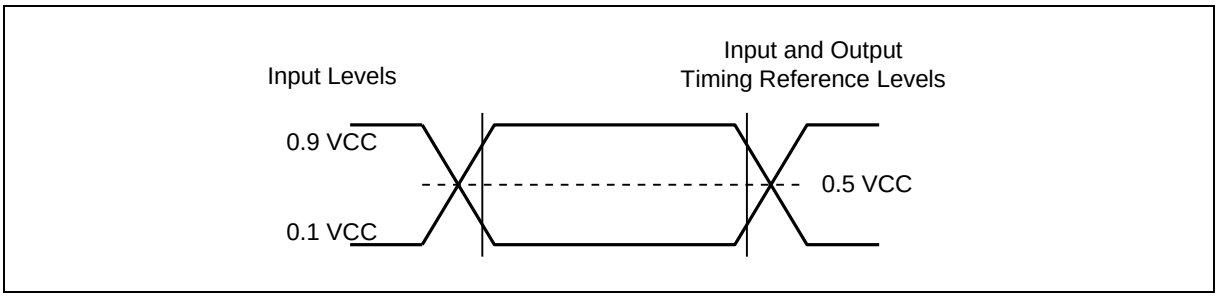


Figure 28. AC Measurement I/O Waveform

9.6 AC Electrical Characteristics(3)

DESCRIPTION	SYMBOL	ALT	SPEC			UNIT
			MIN	TYP	MAX	
Clock frequency for all instructions	F_R	f_{C1}	D.C.		166	MHz
Clock High, Low Time for all instructions	t_{CLH}, t_{CLL}(1)		4			ns
Clock Rise Time peak to peak	t_{CLCH}(2)		0.1			V/ns
Clock Fall Time peak to peak	t_{CHCL}(2)		0.1			V/ns
/CS Active Setup Time relative to CLK	t_{SLCH}	t_{CSS}	5			ns
/CS Not Active Hold Time relative to CLK	t_{CHSL}		5			ns
Data In Setup Time	t_{DVCH}	t_{DSU}	2			ns
Data In Hold Time	t_{CHDX}	t_{DH}	3			ns
/CS Active Hold Time relative to CLK	t_{CHSH}		3			ns
/CS Not Active Setup Time relative to CLK	t_{SHCH}		3			ns
/CS Deselect Time (for Array Read → Array Read)	t_{SHSL1}	t_{CSH}	10			ns
/CS Deselect Time (for Erase, Program or Read Status Registers → Read Status Registers)	t_{SHSL2}	t_{CSH}	50			ns
Output Disable Time	t_{SHQZ}(2)	t_{DIS}			7	ns
Clock Low to Output Valid	t_{CLQV}	t_V			6	ns
Output Hold Time	t_{CLQX}	t_{HO}	2			ns
/HOLD Active Setup Time relative to CLK	t_{HLCH}		5			ns
/HOLD Active Hold Time relative to CLK	t_{CHHH}		5			ns

Continued – next page

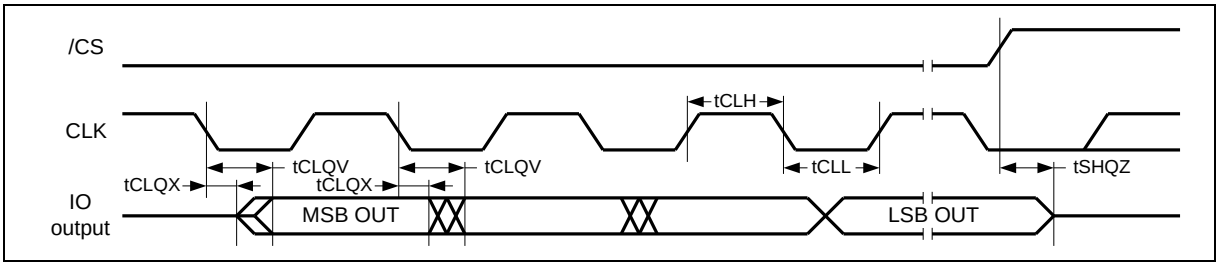
AC Electrical Characteristics (cont'd)

DESCRIPTION	SYMBOL	ALT	SPEC			UNIT
			MIN	TYP	MAX	
/HOLD Not Active Setup Time relative to CLK	t_{HHCH}		5			ns
/HOLD Not Active Hold Time relative to CLK	t_{CHHL}		5			ns
/HOLD to Output Low-Z	t_{HHQX}[2]	t_{LZ}			7	ns
/HOLD to Output High-Z	t_{HLQZ}[2]	t_{HZ}			12	ns
Write Protect Setup Time Before /CS Low	t_{WHSL}		20			ns
Write Protect Hold Time After /CS High	t_{SHWL}		100			ns
Status Register Write Time	t_{W}				50	ns
/CS High to Deep Power-Down Mode	t_{DP}[2]				3	µs
/CS High to Standby Mode (Release DPD)	t_{RES}[2]				3	µs
/CS High to next Instruction after Reset during Page Data Read / Program Execute / Block Erase / Chip Erase	t_{RST}[2]				5/10/500	µs
/CS High to next instruction after Reset with page 0 data load option	t_{RST2}				100	us
Read Page Data Time (ECC disabled)	t_{RD1}				25	µs
Read Page Data Time (ECC enabled)	t_{RD2}				60	µs
Page Program, OTP Lock, BBM Management Time	t_{PP}			250	700	us
Block Erase Time	t_{BE}			2	10	ms
Chip Erase Time	t_{CE}			1	5	s
Number of partial page programs	NoP				4	times

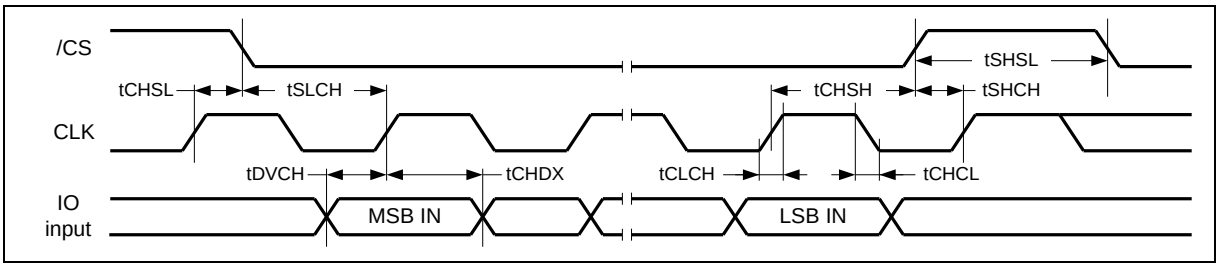
Notes:

1. Clock high + Clock low must be less than or equal to 1/fc.
2. Value guaranteed by design and/or characterization, not 100% tested in production.
3. Tested on sample basis and specified through design and characterization data. TA = 25° C, VCC = 3.0V.

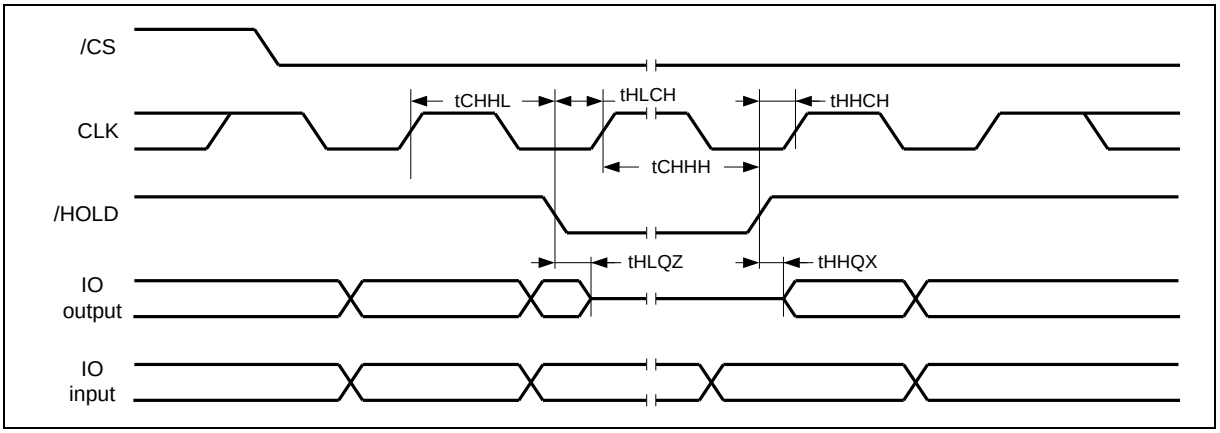
9.7 Serial Output Timing



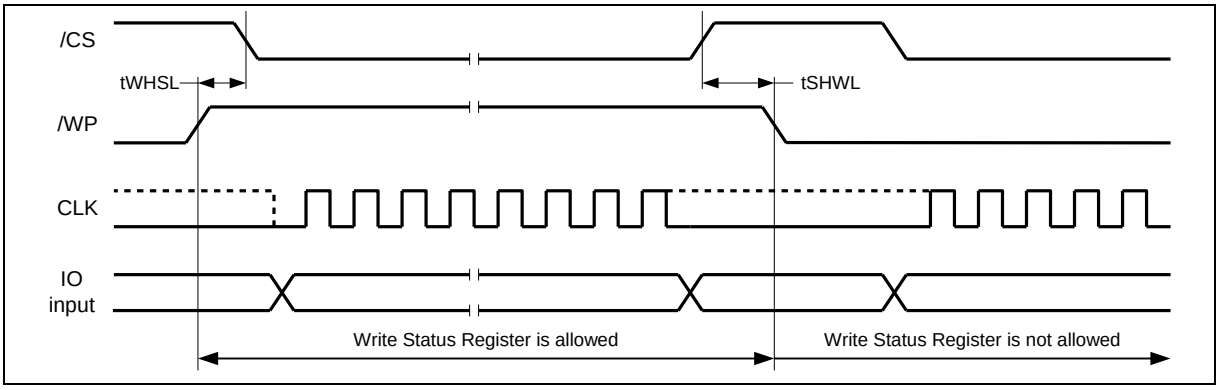
9.8 Serial Input Timing



9.9 /HOLD Timing



9.10 /WP Timing



10. INVALID BLOCK MANAGEMENT

10.1 Invalid blocks

The W25N512GV may have initial invalid blocks when it ships from factory. Also, additional invalid blocks may develop during the use of the device. Nvb represents the minimum number of valid blocks in the total number of available blocks (See the below table). An invalid block is defined as blocks that contain one or more bad bits. Block 0, block address 00h is guaranteed to be a valid block at the time of shipment.

Parameter	Symbol	Min	Max	Unit
Valid block number	Nvb	502	512	blocks

Valid Block Number

10.2 Initial invalid blocks

Initial invalid blocks are defined as blocks that contain one or more invalid bits when shipped from factory.

Although the device contains initial invalid blocks, a valid block of the device is of the same quality and reliability as all valid blocks in the device with reference to AC and DC specifications. The W25N512GV has internal circuits to isolate each block from other blocks and therefore, the invalid blocks will not affect the performance of the entire device.

Before the device is shipped from the factory, it will be erased and invalid blocks are marked. All initial invalid blocks are marked with non-FFh at the 1st byte of main array and the 1st byte of spare area on the 1st page. The initial invalid block information cannot be recovered if inadvertently erased. Therefore, software should be created to initially check for invalid blocks by reading the marked locations before performing any program or erase operation, and create a table of initial invalid blocks as following flow chart.

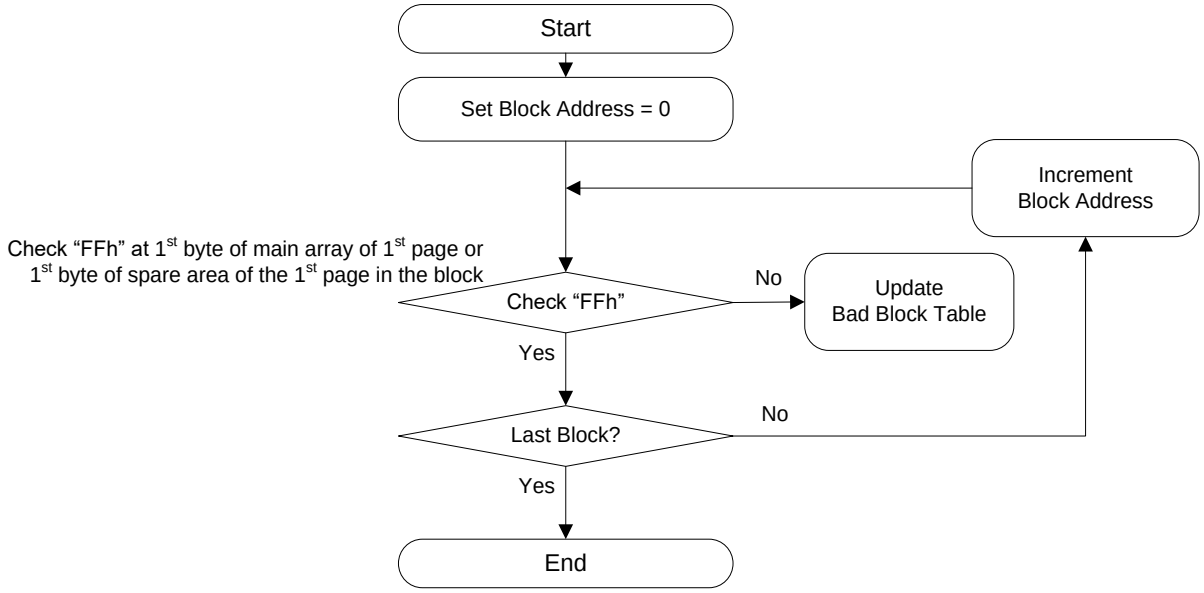
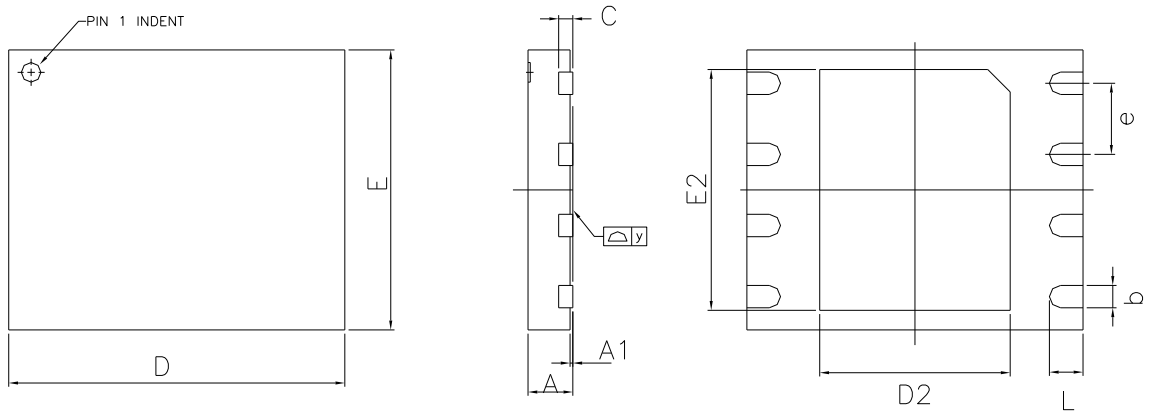


Figure 29. Flow chart of create initial invalid block table

11. PACKAGE SPECIFICATIONS

11.1 8-Pad WSON 6x5-mm (Package Code P)

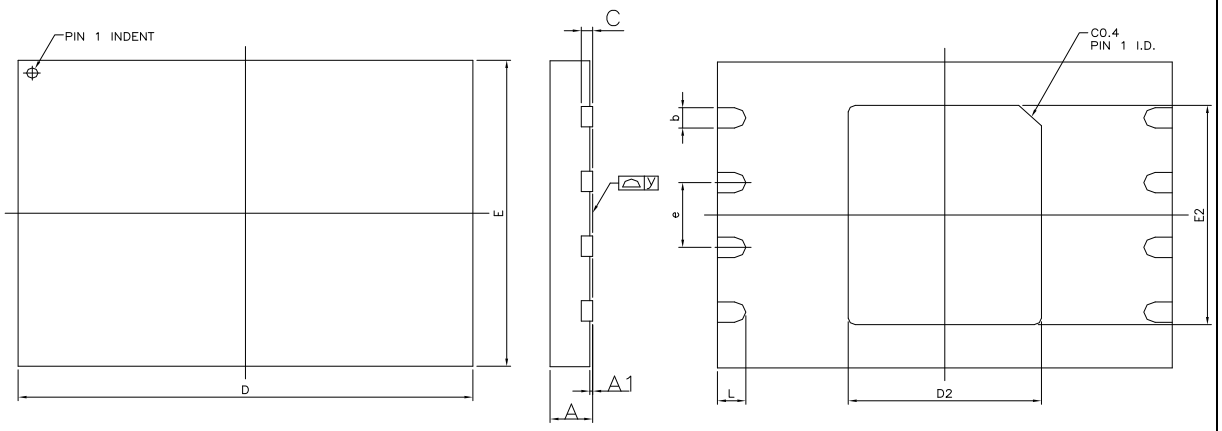


Symbol	Millimeters			Inches		
	Min	Nom	Max	Min	Nom	Max
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	0.02	0.05	0.000	0.001	0.002
b	0.35	0.40	0.48	0.014	0.016	0.019
C	---	0.20 REF	---	---	0.008 REF	---
D	5.90	6.00	6.10	0.232	0.236	0.240
D2	3.35	3.40	3.45	0.132	0.134	0.136
E	4.90	5.00	5.10	0.193	0.197	0.201
E2	4.25	4.30	4.35	0.167	0.169	0.171
e	1.27 BSC			0.050 BSC		
L	0.55	0.60	0.65	0.022	0.024	0.026
y	0.00	---	0.075	0.000	---	0.003

Note:

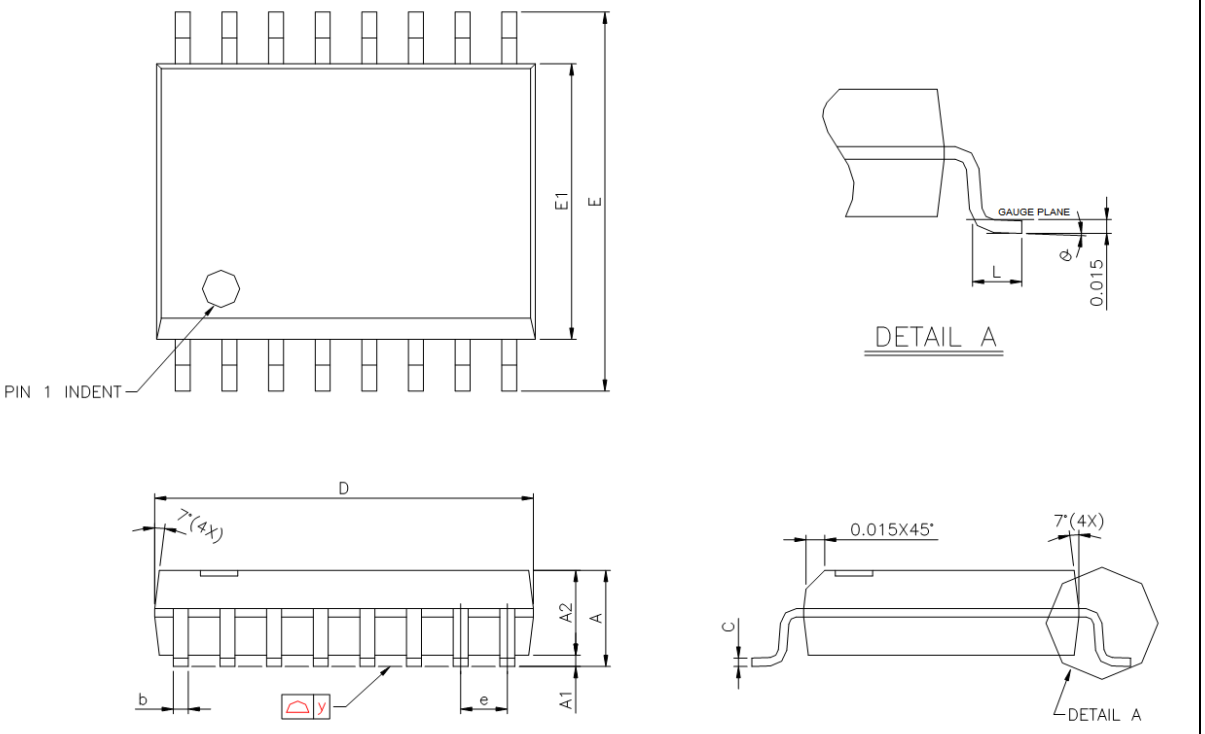
The metal pad area on the bottom center of the package is not connected to any internal electrical signals. It can be left floating or connected to the device ground (GND pin). Avoid placement of exposed PCB vias under the pad.

11.2 8-Pad WSON 8x6-mm (Package Code E)



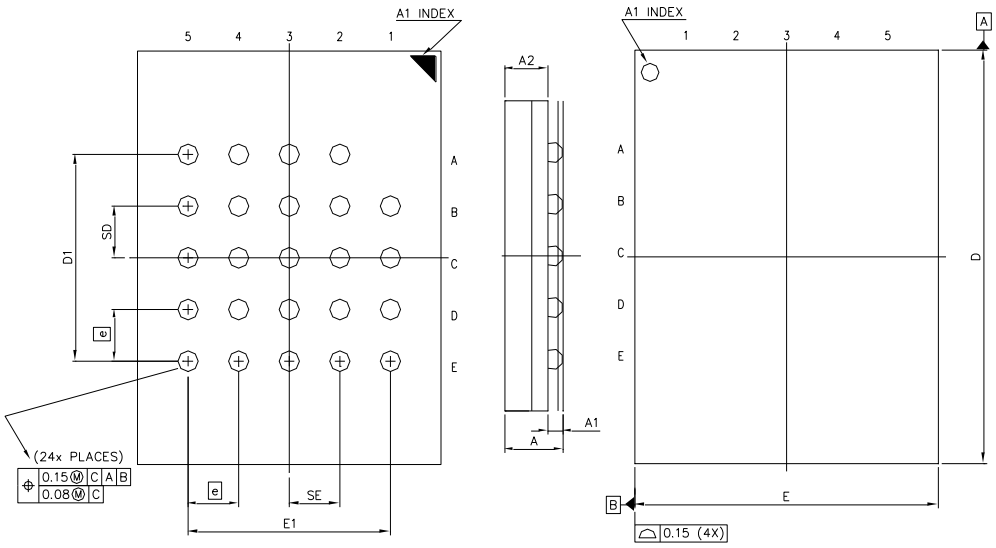
Symbol	Millimeters			Inches		
	Min	Nom	Max	Min	Nom	Max
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	0.02	0.05	0.000	0.001	0.002
b	0.35	0.40	0.48	0.014	0.016	0.019
C	---	0.20 REF	---	---	0.008 REF	---
D	7.90	8.00	8.10	0.311	0.315	0.319
D2	3.35	3.40	3.45	0.132	0.134	0.136
E	5.90	6.00	6.10	0.232	0.236	0.240
E2	4.25	4.30	4.35	0.167	0.169	0.171
e	---	1.27	---	---	0.050	---
L	0.45	0.50	0.55	0.018	0.020	0.022
y	0.00	---	0.050	0.000	---	0.002

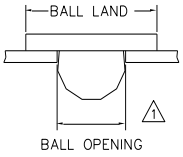
11.3 16-Pin SOIC 300-mil (Package Code F)



Symbol	Millimeters			Inches		
	Min	Nom	Max	Min	Nom	Max
A	2.36	2.49	2.64	0.093	0.098	0.104
A1	0.10	---	0.30	0.004	---	0.012
A2	---	2.31	---	---	0.091	---
b	0.33	0.41	0.51	0.013	0.016	0.020
C	0.18	0.23	0.28	0.007	0.009	0.011
D	10.08	10.31	10.49	0.397	0.406	0.413
E	10.01	10.31	10.64	0.394	0.406	0.419
E1	7.39	7.49	7.59	0.291	0.295	0.299
e	1.27 BSC			0.050 BSC		
L	0.38	0.81	1.27	0.015	0.032	0.050
y	---	---	0.076	---	---	0.003
θ	0°	---	8°	0°	---	8°

11.4 24-Ball TFBGA 8x6-mm (Package Code B, 5x5-1 Ball Array)

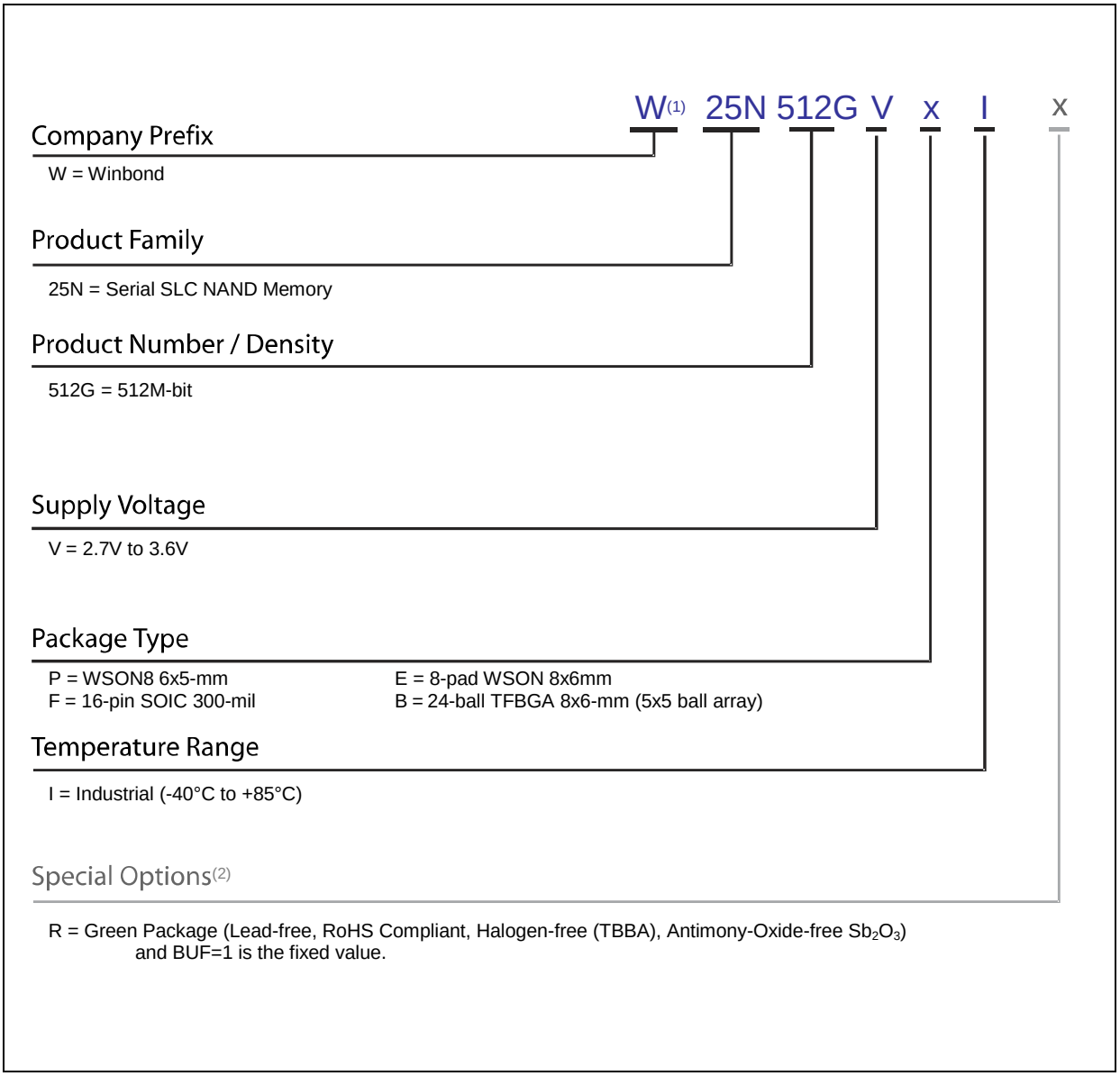




Note:
Ball land: 0.45mm. Ball Opening: 0.35mm
PCB ball land suggested <= 0.35mm

Symbol	Millimeters			Inches		
	Min	Nom	Max	Min	Nom	Max
A	---	---	1.20	---	---	0.047
A1	0.25	0.30	0.35	0.010	0.012	0.014
A2	---	0.85	---	---	0.033	---
b	0.35	0.40	0.45	0.014	0.016	0.018
D	7.90	8.00	8.10	0.311	0.315	0.319
D1	4.00 BSC			0.157 BSC		
E	5.90	6.00	6.10	0.232	0.236	0.240
E1	4.00 BSC			0.157 BSC		
SE	1.00 TYP			0.039 TYP		
SD	1.00 TYP			0.039 TYP		
e	1.00 BSC			0.039 BSC		

12. ORDERING INFORMATION



Notes:

1. The “W” prefix is not included on the part marking.
2. Standard bulk shipments are in tray for WSON and TFBGA packages. For other packing options, please specify when placing orders.

12.1 Valid Part Numbers and Top Side Marking

The following table provides the valid part numbers for the W25N512GV SpiFlash Memory. Please contact Winbond for specific availability by density and package type. Winbond SpiFlash memories use a 12-digit Product Number for ordering. However, due to limited space, the Top Side Marking on all packages uses an abbreviated 11-digit number.

Industrial Temperature:

PACKAGE TYPE	DENSITY	PRODUCT NUMBER	TOP SIDE MARKING
P WSON-8 6x5mm	512M-bit	W25N512GVPIR	25N512GVPIR
E WSON-8 8x6mm	512M-bit	W25N512GVEIR	25N512GVEIR
F SOIC-16 300mil	512M-bit	W25N512GVFIR	25N512GVFIR
B TFBGA-24 8x6mm (5x5-1 Ball Array)	512M-bit	W25N512GVBIR	25N512GVBIR

Note:
W25N512GVxIR: BUF=1 (Buffer Read Mode) is the fixed value. BUF bit can't be written to 0.

13. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A	02/13/2019		New Create Datasheet

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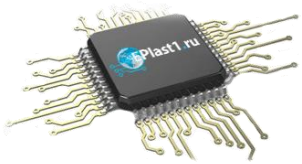
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

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