TOSHIBA Field Effect Transistor Silicon P/N Channel MOS Type(π-MOSVI)

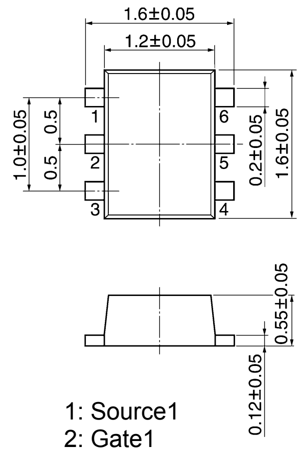
SSM6L16FE

High Speed Switching Applications

Analog Switch Applications

- Small package
- Low on-resistance Q1: $R_{DS(ON)} = 4\ \Omega$ (max) (@$V_{GS} = 2.5$ V)
  Q2: $R_{DS(ON)} = 12\ \Omega$ (max) (@$V_{GS} = -2.5$ V)

Unit: mm



1: Source1
2: Gate1
3: Drain2
4: Source2
5: Gate2
6: Drain1

ES6

JEDEC	―
JEITA	―
TOSHIBA	2-2N1D

Weight: 3 mg (typ.)

Q1 Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Drain-Source voltage		V_{DSS}	20	V
Gate-Source voltage		V_{GSS}	±10	V
Drain current	DC	I_D	100	mA
	Pulse	I_{DP}	200	

Q2 Absolute Maximum Ratings (Ta = 25°C)

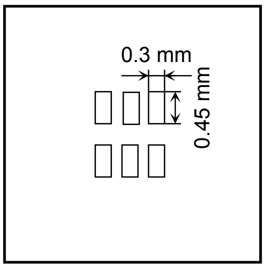
Characteristics		Symbol	Rating	Unit
Drain-Source voltage		V_{DSS}	-20	V
Gate-Source voltage		V_{GSS}	±10	V
Drain current	DC	I_D	-100	mA
	Pulse	I_{DP}	-200	

Absolute Maximum Ratings (Q1, Q2 Common) (Ta = 25°C)

Characteristics	Symbol	Rating	Unit
Power dissipation	P_D (Note 1)	150	mW
Channel temperature	T_{ch}	150	°C
Storage temperature range	T_{stg}	−55 to 150	°C

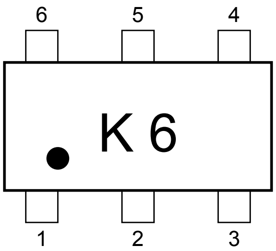
Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Total rating, mounted on FR4 board
(25.4 mm × 25.4 mm × 1.6 mm, Cu Pad: 0.135 mm^2 × 6)

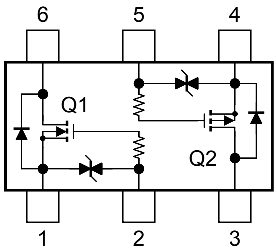


Start of commercial production
2002-03

Marking



Equivalent Circuit (top view)



Handling Precaution

When handling individual devices (which are not yet mounted on a circuit board), ensure that the environment is protected against static electricity. Operators should wear anti-static clothing, and containers and other objects that come into direct contact with devices should be made of anti-static materials.

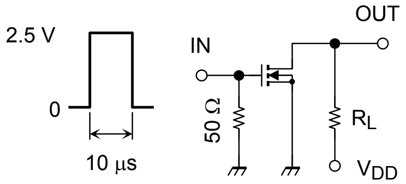
Q1 Electrical Characteristics (Ta = 25°C)

Characteristic		Symbol	Test Condition	MIN.	TYP.	MAX.	UNIT
Gate leakage current		I_{GSS}	V_{GS} = ±10 V, V_{DS} = 0	—	—	±1	μA
Drain-Source breakdown voltage		$V_{(BR)\ DSS}$	I_D = 0.1 mA, V_{GS} = 0	20	—	—	V
Drain cut-off current		I_{DSS}	V_{DS} = 20 V, V_{GS} = 0	—	—	1	μA
Gate threshold voltage		V_{th}	V_{DS} = 3 V, I_D = 0.1 mA	0.6	—	1.1	V
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = 3 V, I_D = 10 mA (Note2)	40	—	—	mS
Drain-Source on-resistance		$R_{DS\ (ON)}$	I_D = 10 mA, V_{GS} = 4 V (Note2)	—	1.5	3.0	Ω
			I_D = 10 mA, V_{GS} = 2.5 V (Note2)	—	2.2	4.0	
			I_D = 1 mA, V_{GS} = 1.5 V (Note2)	—	5.2	15	
Input capacitance		C_{iss}	V_{DS} = 3 V, V_{GS} = 0, f = 1 MHz	—	9.3	—	pF
Reverse transfer capacitance		C_{rss}		—	4.5	—	pF
Output capacitance		C_{oss}		—	9.8	—	pF
Switching time	Turn-on time	t_{on}	V_{DD} = 3 V, I_D = 10 mA, V_{GS} = 0 to 2.5 V	—	70	—	ns
	Turn-off time	t_{off}		—	125	—	

Note2: Pulse test

Switching Time Test Circuit

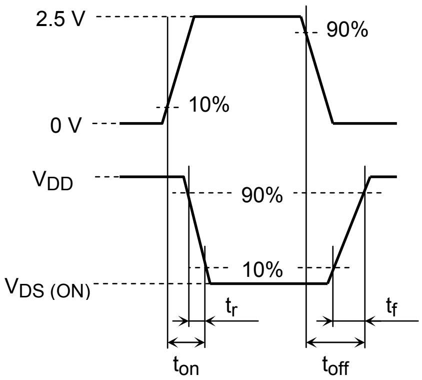
(a) Test circuit



V_{DD} = 3 V
Duty ≤ 1%
V_{IN}: t_r, t_f < 5 ns
(Z_{out} = 50 Ω)
Common Source
Ta = 25°C

(b) V_{IN}

(c) V_{OUT}



Precaution

V_{th} can be expressed as the voltage between the gate and source when the low operating current value is I_D = 0.1 mA for this product. For normal switching operation, $V_{GS\ (on)}$ requires a higher voltage than V_{th} and $V_{GS\ (off)}$ requires a lower voltage than V_{th}. (The relationship can be established as follows: $V_{GS\ (off)} < V_{th} < V_{GS\ (on)}$.)

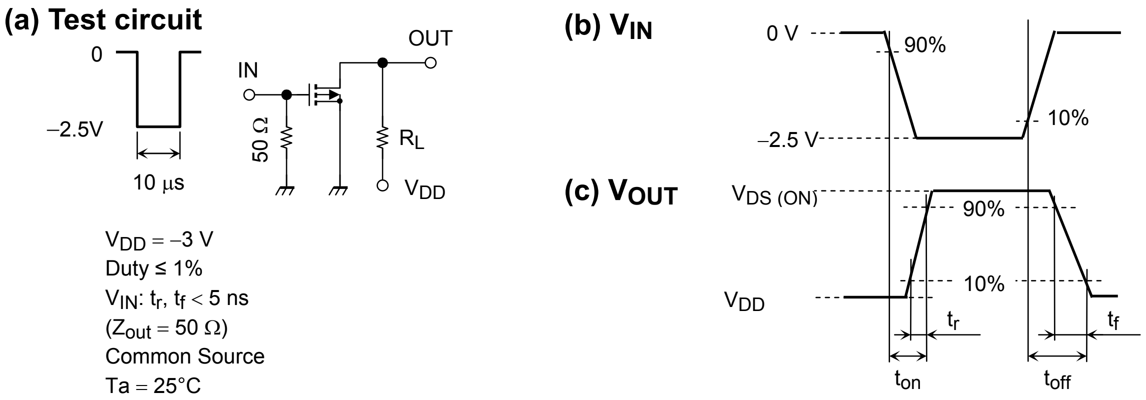
Be sure to take this into consideration when using the device.

Q2 Electrical Characteristics (Ta = 25°C)

Characteristic		Symbol	Test Condition	MIN.	TYP.	MAX.	UNIT
Gate leakage current		I_{GSS}	V_{GS} = ±10 V, V_{DS} = 0	—	—	±1	μA
Drain-Source breakdown voltage		$V_{(BR)DSS}$	I_D = −0.1 mA, V_{GS} = 0	−20	—	—	V
Drain cut-off current		I_{DSS}	V_{DS} = −20 V, V_{GS} = 0	—	—	−1	μA
Gate threshold voltage		V_{th}	V_{DS} = −3 V, I_D = −0.1 mA	−0.6	—	−1.1	V
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = −3 V, I_D = −10 mA (Note3)	25	—	—	mS
Drain-Source on-resistance		$R_{DS(ON)}$	I_D = −10 mA, V_{GS} = −4 V (Note3)	—	6	8	Ω
			I_D = −10 mA, V_{GS} = −2.5 V (Note3)	—	8	12	
			I_D = −1 mA, V_{GS} = −1.5 V (Note3)	—	18	45	
Input capacitance		C_{iss}	V_{DS} = −3 V, V_{GS} = 0, f = 1 MHz	—	11	—	pF
Reverse transfer capacitance		C_{rss}		—	3.7	—	pF
Output capacitance		C_{oss}		—	10	—	pF
Switching time	Turn-on time	t_{on}	V_{DD} = −3 V, I_D = − 10 mA, V_{GS} = 0 to −2.5 V	—	130	—	ns
	Turn-off time	t_{off}		—	190	—	

Note3: Pulse test

Switching Time Test Circuit

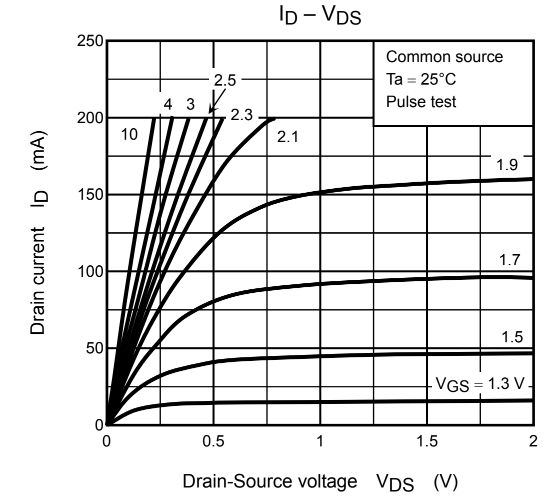


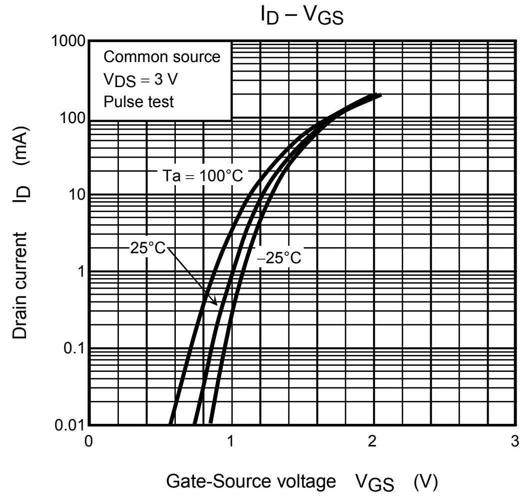
Precaution

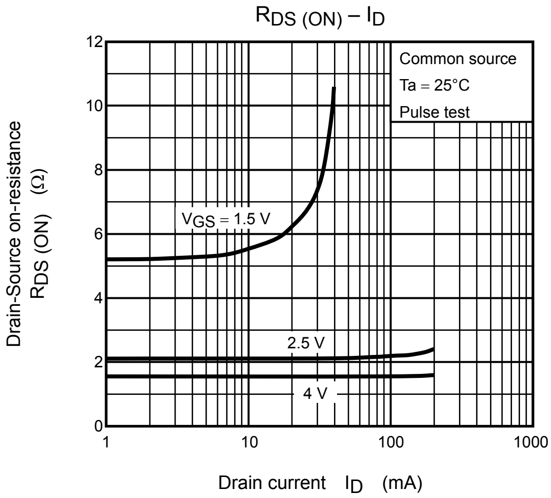
V_{th} can be expressed as the voltage between the gate and source when the low operating current value is I_D = - 0.1 mA for this product. For normal switching operation, $V_{GS\ (on)}$ requires a higher voltage than V_{th} and $V_{GS\ (off)}$ requires a lower voltage than V_{th}. (The relationship can be established as follows: $V_{GS\ (off)} < V_{th} < V_{GS\ (on)}$.)

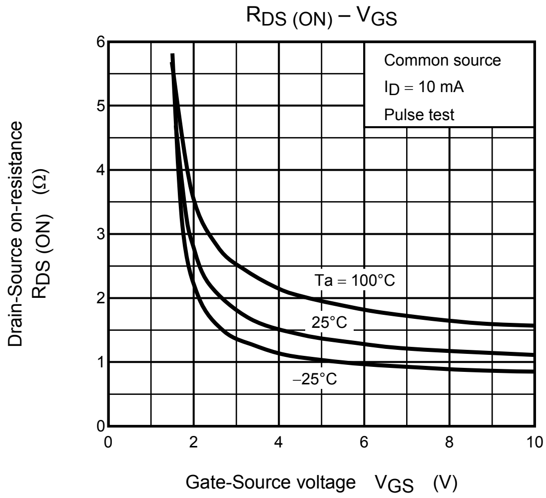
Be sure to take this into consideration when using the device.

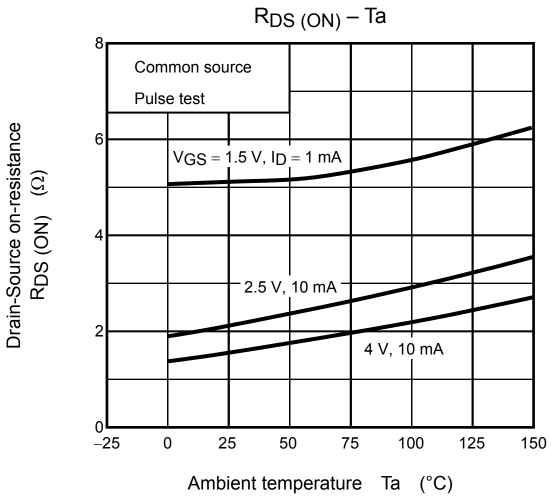
Q1 (N-ch MOSFET)

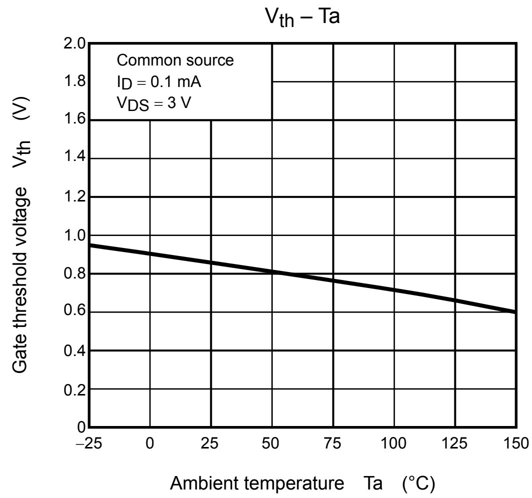




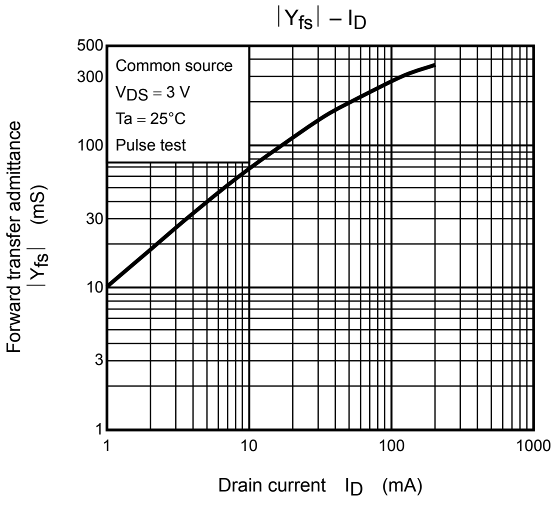


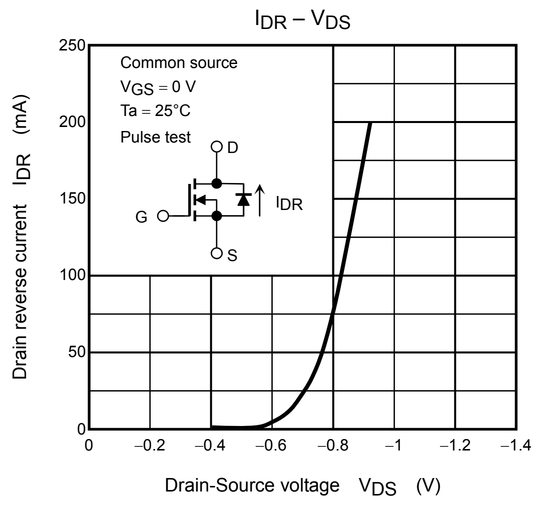


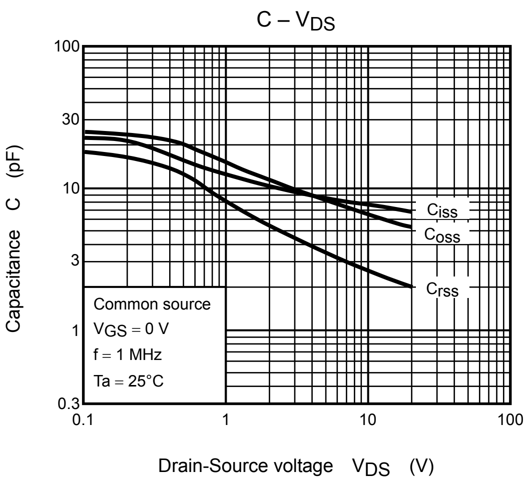


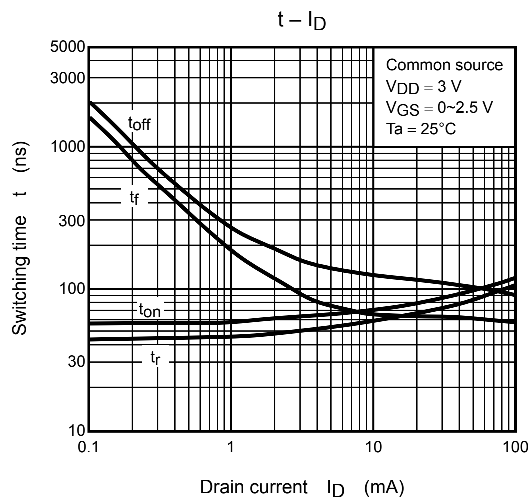


Q1 (N-ch MOSFET)

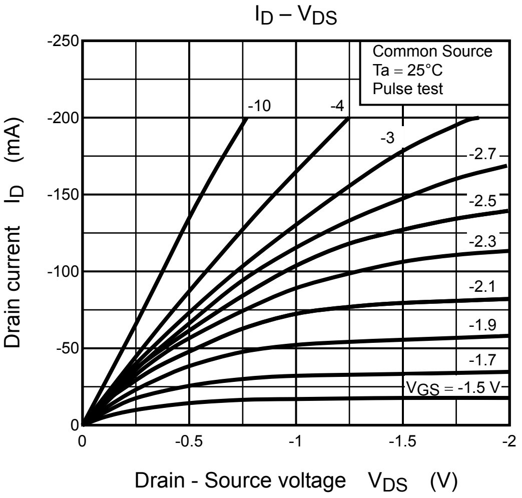


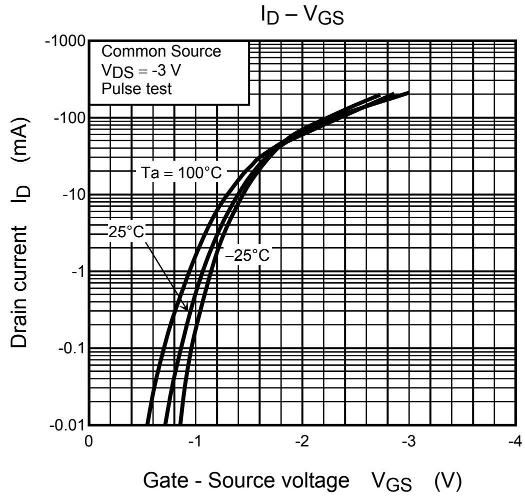


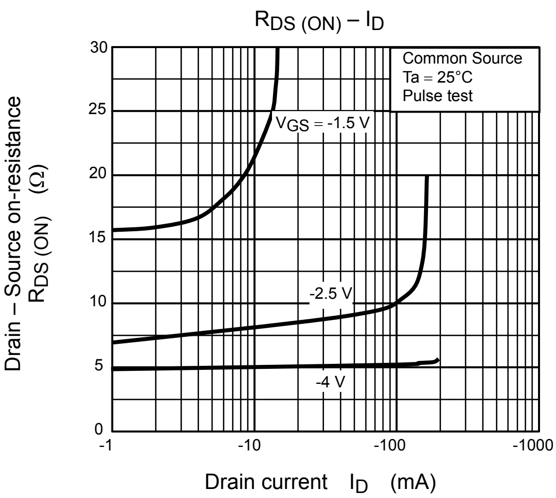


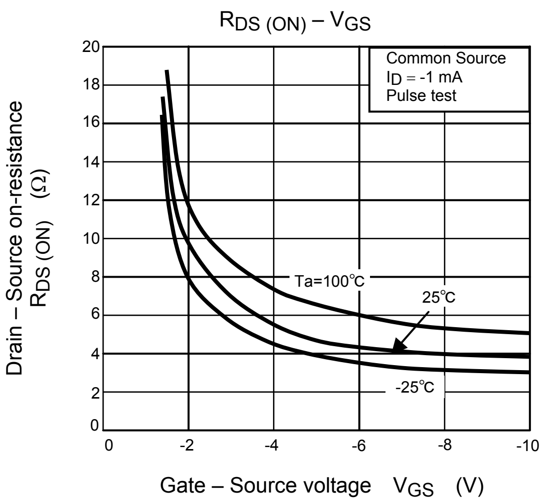


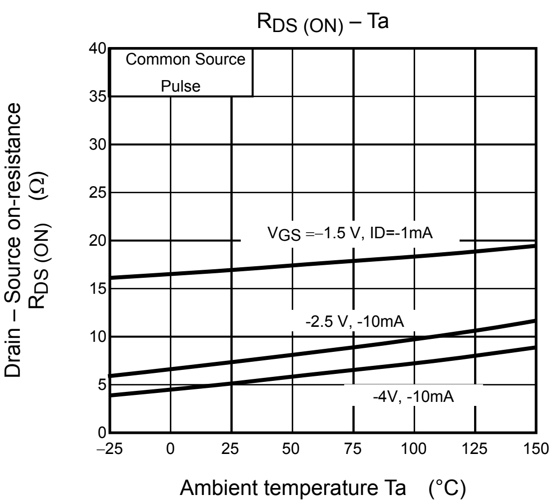
Q2 (P-ch MOSFET)

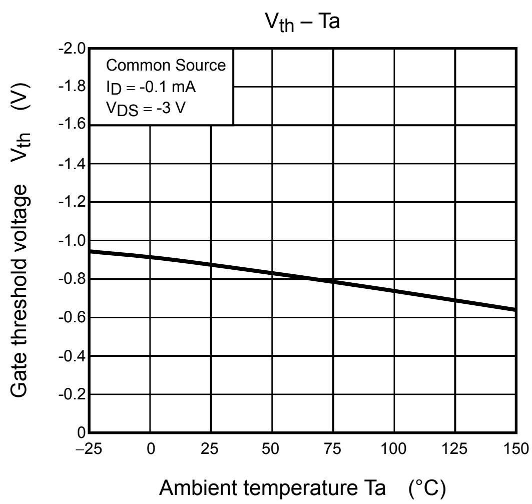




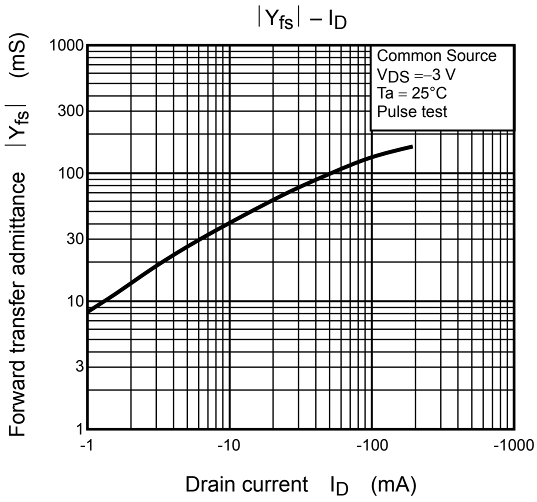


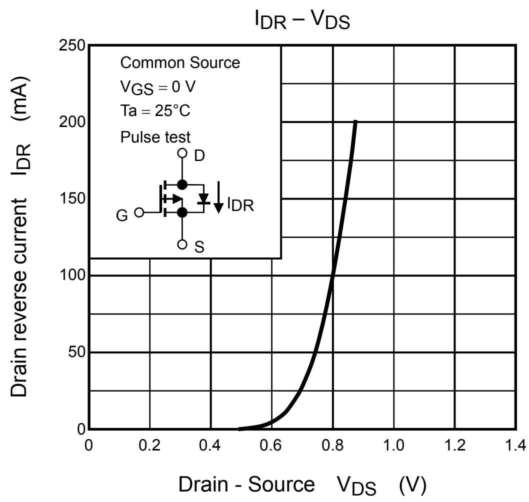


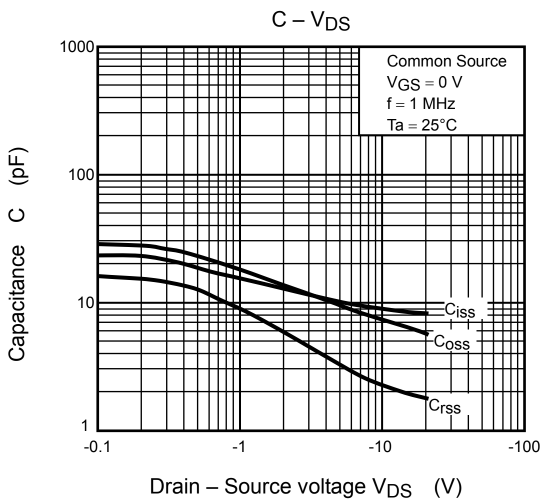


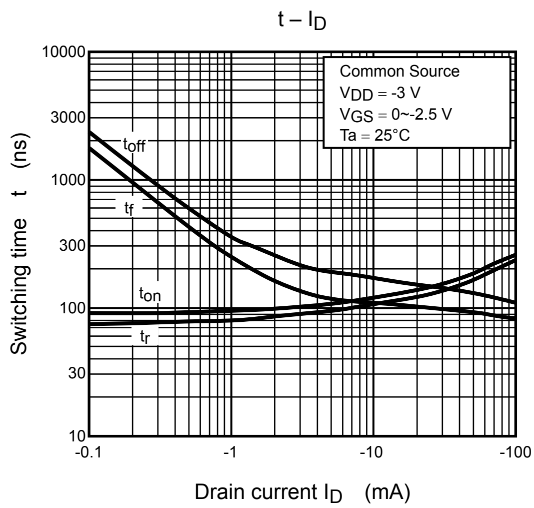


Q2 (P-ch MOSFET)

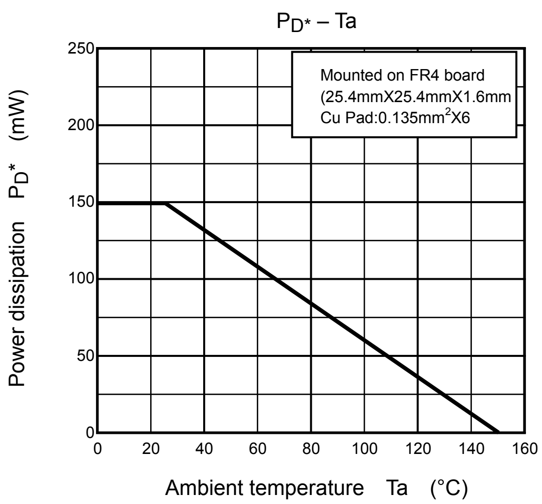








Common Characteristics



*:Total rating

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- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.

Как с нами связаться

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