Features

- High-density, High-performance, Electrically-erasable Complex Programmable Logic Device
  - 3.0 to 3.6V Operating Range
  - 64 Macrocells
  - 5 Product Terms per Macrocell, Expandable up to 40 per Macrocell
  - 44, 68, 84, 100 Pins
  - 15 ns Maximum Pin-to-pin Delay
  - Registered Operation up to 77 MHz
  - Enhanced Routing Resources
- In-System Programmability (ISP) via JTAG
- Flexible Logic Macrocell
  - D/T/Latch Configurable Flip-flops
  - Global and Individual Register Control Signals
  - Global and Individual Output Enable
  - Programmable Output Slew Rate
  - Programmable Output Open-collector Option
  - Maximum Logic Utilization by Burying a Register with a COM Output
- Advanced Power Management Features
  - Automatic 5 µA Standby for "L" Version
  - Pin-controlled 100 µA Standby Mode (Typical)
  - Programmable Pin-keeper Circuits on Inputs and I/Os
  - Reduced-power Feature per Macrocell
- Available in Commercial and Industrial Temperature Ranges
- Available in 44-, 68-, and 84-lead PLCC; 44- and 100-lead TQFP; and 100-lead PQFP
- Advanced EE Technology
  - 100% Tested
  - Completely Reprogrammable
  - 10,000 Program/Erase Cycles
  - 20 Year Data Retention
  - 2000V ESD Protection
  - 200 mA Latch-up Immunity
- JTAG Boundary-scan Testing to IEEE Std. 1149.1-1990 and 1149.1a-1993 Supported
- PCI-compliant
- Security Fuse Feature

Enhanced Features

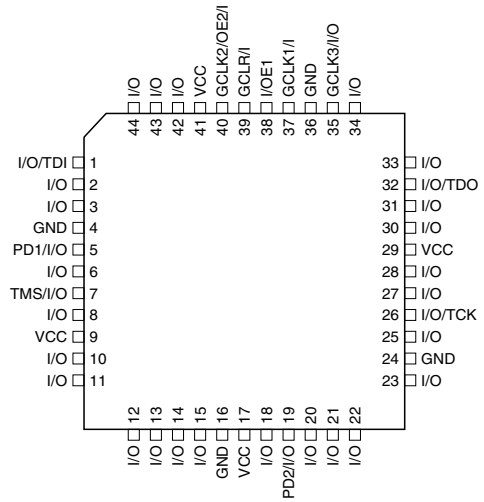
- Improved Connectivity (Additional Feedback Routing, Alternate Input Routing)
- Output Enable Product Terms
- Transparent-latch Mode
- Combinatorial Output with Registered Feedback within Any Macrocell
- Three Global Clock Pins
- ITD (Input Transition Detection) Circuits on Global Clocks, Inputs and I/O
- Fast Registered Input from Product Term
- Programmable "Pin-keeper" Option
- V_{CC} Power-up Reset Option
- Pull-up Option on JTAG Pins TMS and TDI
- Advanced Power Management Features
  - Edge-controlled Power-down "L"
  - Individual Macrocell Power Option
  - Disable ITD on Global Clocks, Inputs and I/O

Low-voltage, Complex Programmable Logic Device

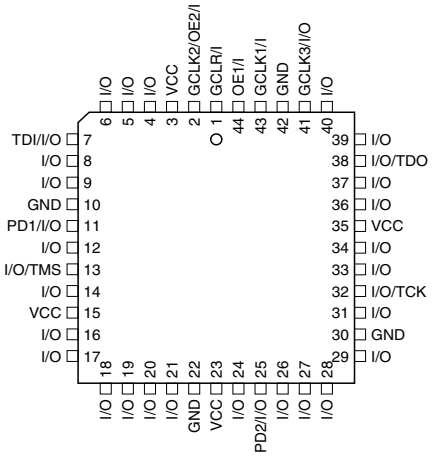
ATF1504ASV
ATF1504ASVL

Rev. 1409I–PLD–2/03

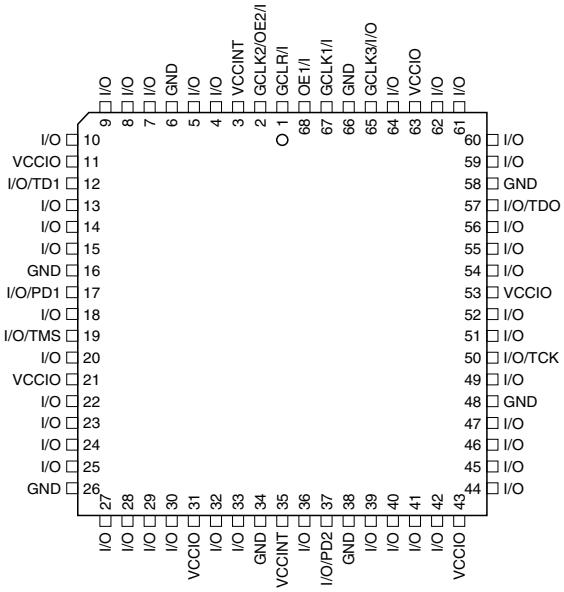
44-lead TQFP
Top View



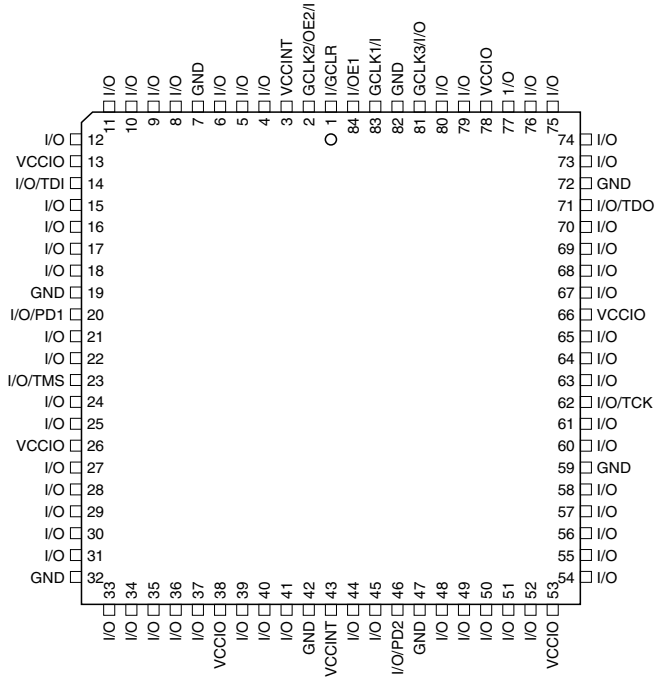
44-lead PLCC
Top View



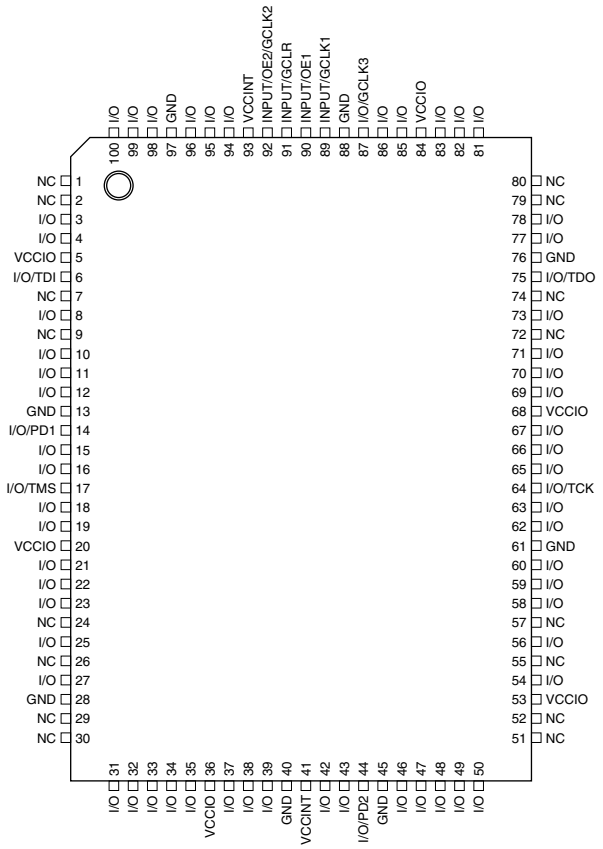
68-lead PLCC
Top View



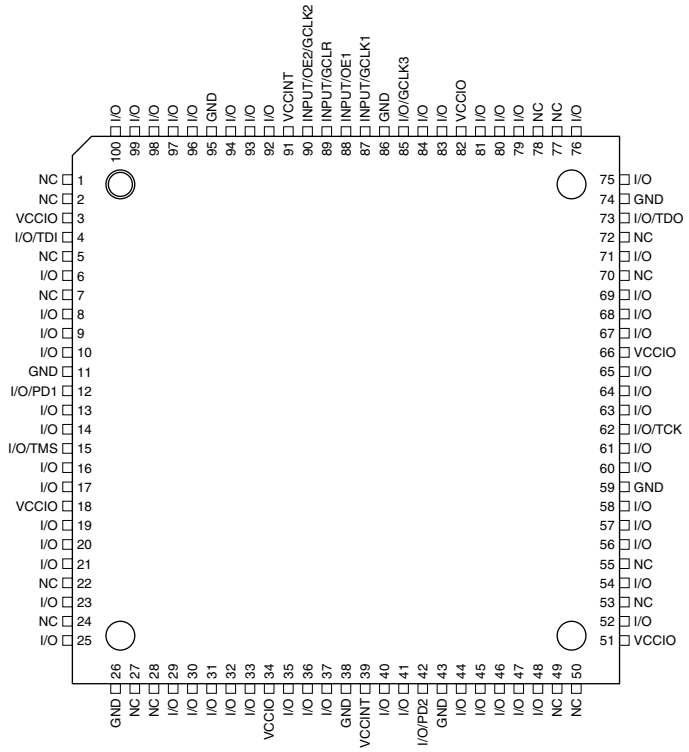
84-lead PLCC
Top View



100-lead PQFP
Top View



100-lead TQFP
Top View



Description

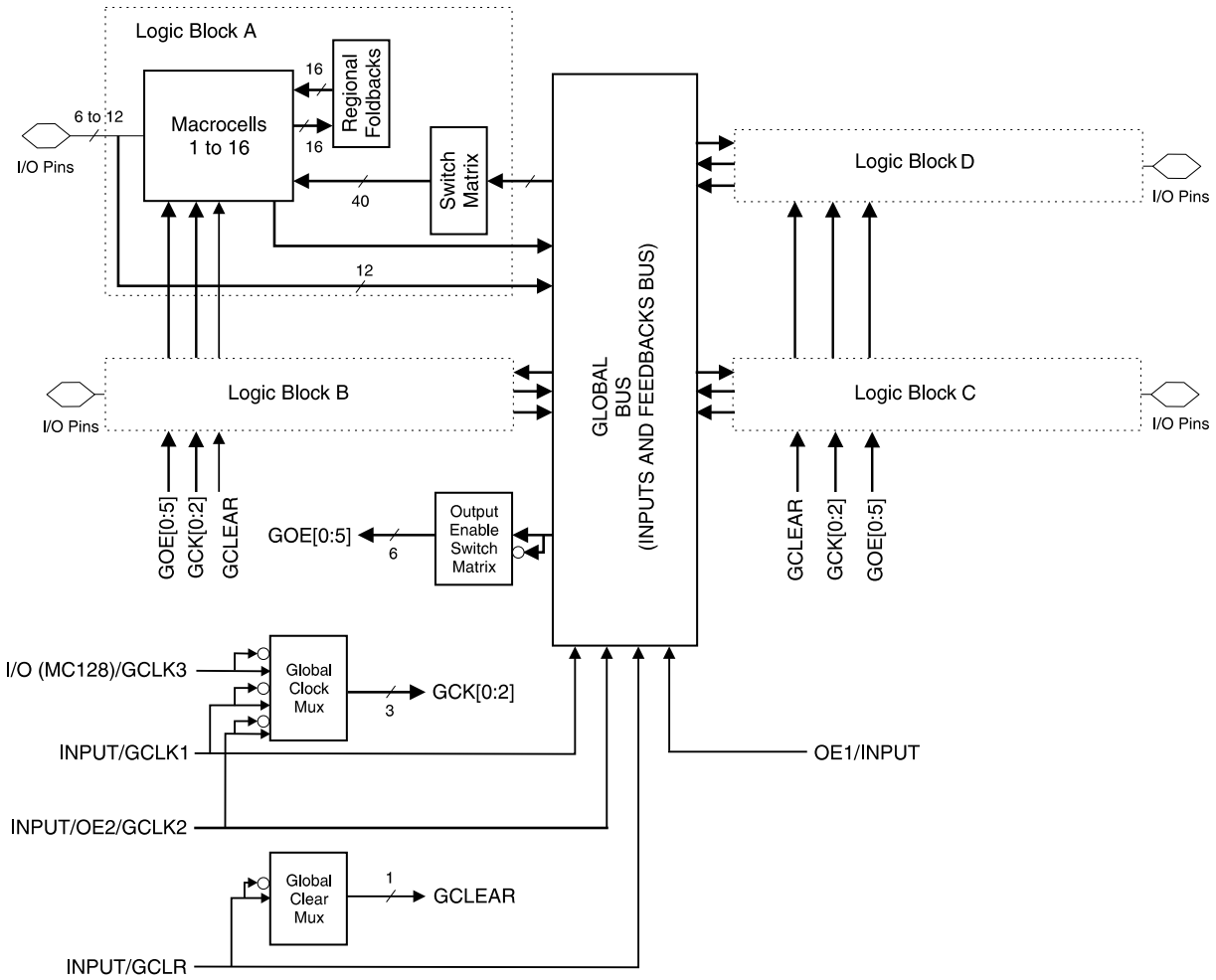
The ATF1504ASV(L) is a high-performance, high-density complex programmable logic device (CPLD) that utilizes Atmel's proven electrically-erasable memory technology. With 64 logic macrocells and up to 68 inputs, it easily integrates logic from several TTL, SSI, MSI, LSI and classic PLDs. The ATF1504ASV(L)'s enhanced routing switch matrices increase usable gate count and the odds of successful pin-locked design modifications.

The ATF1504ASV(L) has up to 68 bi-directional I/O pins and four dedicated input pins, depending on the type of device package selected. Each dedicated pin can also serve as a global control signal, register clock, register reset or output enable. Each of these control signals can be selected for use individually within each macrocell.

Each of the 64 macrocells generates a buried feedback that goes to the global bus. Each input and I/O pin also feeds into the global bus. The switch matrix in each logic block then selects 40 individual signals from the global bus. Each macrocell also generates a foldback logic term that goes to a regional bus. Cascade logic between macrocells in the ATF1504ASV(L) allows fast, efficient generation of complex logic functions. The ATF1504ASV(L) contains four such logic chains, each capable of creating sum term logic with a fan-in of up to 40 product terms.

The ATF1504ASV(L) macrocell, shown in Figure 1, is flexible enough to support highly-complex logic functions operating at high speed. The macrocell consists of five sections: product terms and product term select multiplexer, OR/XOR/CASCADE logic, a flip-flop, output select and enable, and logic array inputs.

Block Diagram



Unused product terms are automatically disabled by the compiler to decrease power consumption. A security fuse, when programmed, protects the contents of the ATF1504ASV(L). Two bytes (16 bits) of User Signature are accessible to the user for purposes such as storing project name, part number, revision or date. The User Signature is accessible regardless of the state of the security fuse.

The ATF1504ASV(L) device is an in-system programmable (ISP) device. It uses the industry-standard 4-pin JTAG interface (IEEE Std. 1149.1), and is fully-compliant with JTAG's Boundary-scan Description Language (BSDL). ISP allows the device to be programmed without removing it from the printed circuit board. In addition to simplifying the manufacturing flow, ISP also allows design modifications to be made in the field via software.

Product Terms and Select Mux

Each ATF1504ASV(L) macrocell has five product terms. Each product term receives as its inputs all signals from both the global bus and regional bus.

The product term select multiplexer (PTMUX) allocates the five product terms as needed to the macrocell logic gates and control signals. The PTMUX programming is determined by the design compiler, which selects the optimum macrocell configuration.

OR/XOR/CASCADE Logic

The ATF1504ASV(L)'s logic structure is designed to efficiently support all types of logic. Within a single macrocell, all the product terms can be routed to the OR gate, creating a 5-input AND/OR sum term. With the addition of the CASIN from neighboring macrocells, this can be expanded to as many as 40 product terms with little additional delay.

The macrocell's XOR gate allows efficient implementation of compare and arithmetic functions. One input to the XOR comes from the OR sum term. The other XOR input can be a product term or a fixed high- or low-level. For combinatorial outputs, the fixed level input allows polarity selection. For registered functions, the fixed levels allow DeMorgan minimization of product terms. The XOR gate is also used to emulate T- and JK-type flip-flops.

Flip-flop

The ATF1504ASV(L)'s flip-flop has very flexible data and control functions. The data input can come from either the XOR gate, from a separate product term or directly from the I/O pin. Selecting the separate product term allows creation of a buried registered feedback within a combinatorial output macrocell. (This feature is automatically implemented by the fitter software). In addition to D, T, JK and SR operation, the flip-flop can also be configured as a flow-through latch. In this mode, data passes through when the clock is high and is latched when the clock is low.

The clock itself can either be one of the Global CLK Signal (GCK[0 : 2]) or an individual product term. The flip-flop changes state on the clock's rising edge. When the GCK signal is used as the clock, one of the macrocell product terms can be selected as a clock enable. When the clock enable function is active and the enable signal (product term) is low, all clock edges are ignored. The flip-flop's asynchronous reset signal (AR) can be either the Global Clear (GCLEAR), a product term, or always off. AR can also be a logic OR of GCLEAR with a product term. The asynchronous preset (AP) can be a product term or always off.

Extra Feedback

The ATF1504ASV(L) macrocell output can be selected as registered or combinatorial. The extra buried feedback signal can be either combinatorial or a registered signal regardless of whether the output is combinatorial or registered. (This enhancement function is automatically implemented by the fitter software.) Feedback of a buried combinatorial output allows the creation of a second latch within a macrocell.

I/O Control

The output enable multiplexer (MOE) controls the output enable signal. Each I/O can be individually configured as an input, output or for bi-directional operation. The output enable for each macrocell can be selected from the true or compliment of the two output enable pins, a subset of the I/O pins, or a subset of the I/O macrocells. This selection is automatically done by the fitter software when the I/O is configured as an input, all macrocell resources are still available, including the buried feedback, expander and cascade logic.

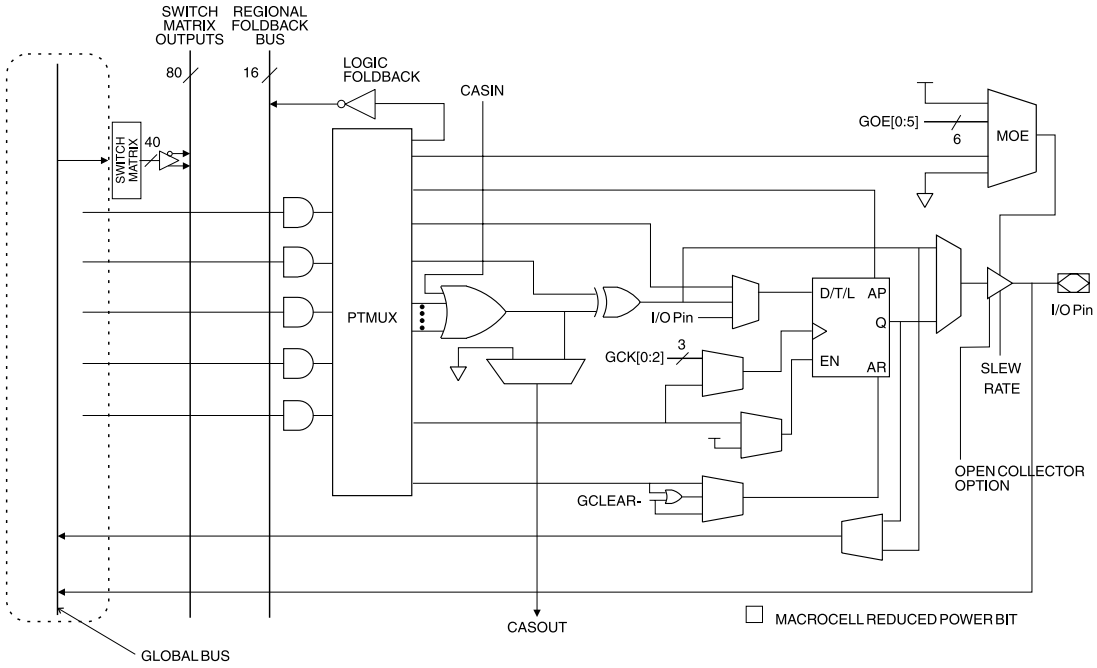
Global Bus/Switch Matrix

The global bus contains all input and I/O pin signals as well as the buried feedback signal from all 64 macrocells. The switch matrix in each logic block receives as its inputs all signals from the global bus. Under software control, up to 40 of these signals can be selected as inputs to the logic block.

Foldback Bus

Each macrocell also generates a foldback product term. This signal goes to the regional bus and is available to four macrocells. The foldback is an inverse polarity of one of the macrocell's product terms. The four foldback terms in each region allow generation of high fan-in sum terms (up to nine product terms) with little additional delay.

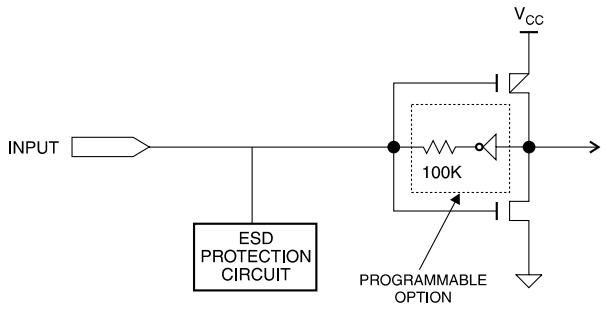
Figure 1. ATF1504ASV(L) Macrocell



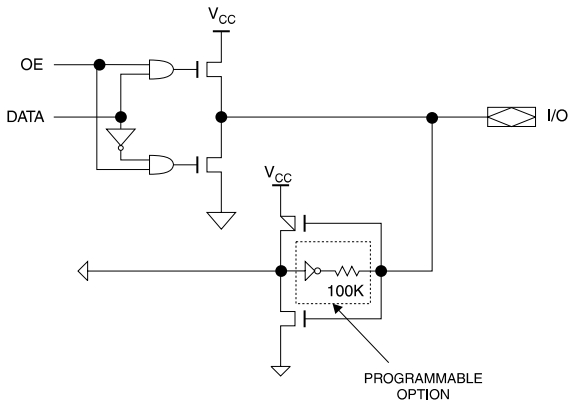
Programmable Pin-keeper Option for Inputs and I/Os

The ATF1504ASV(L) offers the option of programming all input and I/O pins so that pin keeper circuits can be utilized. When any pin is driven high or low and then subsequently left floating, it will stay at that previous high- or low-level. This circuitry prevents unused input and I/O lines from floating to intermediate voltage levels, which causes unnecessary power consumption and system noise. The keeper circuits eliminate the need for external pull-up resistors and eliminate their DC power consumption.

Input Diagram



I/O Diagram



Speed/Power Management

The ATF1504ASV(L) has several built-in speed and power management features. The ATF1504ASV(L) contains circuitry that automatically puts the device into a low power standby mode when no logic transitions are occurring. This not only reduces power consumption during inactive periods, but also provides proportional power savings for most applications running at system speeds below 5 MHz. This feature may be selected as a device option.

To further reduce power, each ATF1504ASV(L) macrocell has a reduced-power bit feature. This feature allows individual macrocells to be configured for maximum power savings. This feature may be selected as a design option.

All ATF1504ASV(L) also have an optional power-down mode. In this mode, current drops to below 5 mA. When the power-down option is selected, either PD1 or PD2 pins (or both) can be used to power down the part. The power-down option is selected in the design source file. When enabled, the device goes into power down when either PD1 or PD2 is high. In the power-down mode, all internal logic signals are latched and held, as are any enabled outputs.

All pin transitions are ignored until the PD pin is brought low. When the power-down feature is enabled, the PD1 or PD2 pin cannot be used as a logic input or output. However, the pin's macrocell may still be used to generate buried foldback and cascade logic signals.

All power-down AC characteristic parameters are computed from external input or I/O pins, with reduced-power bit turned on. For macrocells in reduced-power mode (reduced-power bit turned on), the reduced-power adder, t_{RPA}, must be added to the AC parameters, which include the data paths t_{LAD}, t_{LAC}, t_{IC}, t_{ACL}, t_{ACH} and t_{SEXP}.

The ATF1504ASV(L) macrocell also has an option whereby the power can be reduced on a per macrocell basis. By enabling this power-down option, macrocells that are not used in an application can be turned down, thereby reducing the overall power consumption of the device.

Each output also has individual slew rate control. This may be used to reduce system noise by slowing down outputs that do not need to operate at maximum speed. Outputs default to slow switching, and may be specified as fast switching in the design file.

Design Software Support

ATF1504ASV(L) designs are supported by several industry standard third party tools. Automated fitters allow logic synthesis using a variety of high-level description languages and formats.

Power-up Reset

The ATF1504ASV is designed with a power-up reset, a feature critical for state machine initialization. At a point delayed slightly from V_{CC} crossing V_{RST}, all registers will be initialized, and the state of each output will depend on the polarity of its buffer. However, due to the asynchronous nature of reset and uncertainty of how V_{CC} actually rises in the system, the following conditions are required:

1. The V_{CC} rise must be monotonic,
2. After reset occurs, all input and feedback setup times must be met before driving the clock pin high, and,
3. The clock must remain stable during T_D.

The ATF1504ASV has two options for the hysteresis about the reset level, V_{RST}, Small and Large. To ensure a robust operating environment in applications where the device is operated near 3.0V, Atmel recommends that during the fitting process users configure the device with the Power-up Reset hysteresis set to Large. For conversions, Atmel POF2JED users should include the flag “-power_reset” on the command line after “filename.POF”. To allow the registers to be properly reinitialized with the Large hysteresis option selected, the following condition is added:

4. If V_{CC} falls below 2.0V, it must shut off completely before the device is turned on again.

When the Large hysteresis option is active, I_{CC} is reduced by several hundred microamps as well.

Security Fuse Usage

A single fuse is provided to prevent unauthorized copying of the ATF1504ASV(L) fuse patterns. Once programmed, fuse verify is inhibited. However, the 16-bit User Signature remains accessible.

Programming

ATF1504ASV(L) devices are in-system programmable (ISP) devices utilizing the 4-pin JTAG protocol. This capability eliminates package handling normally required for programming and facilitates rapid design iterations and field changes.

Atmel provides ISP hardware and software to allow programming of the ATF1504ASV(L) via the PC. ISP is performed by using either a download cable, a comparable board tester or a simple microprocessor interface.

To facilitate ISP programming by the Automated Test Equipment (ATE) vendors. Serial Vector Format (SVF) files can be created by Atmel provided software utilities.

ATF1504ASV(L) devices can also be programmed using standard third-party programmers. With third-party programmer the JTAG ISP port can be disabled thereby allowing four additional I/O pins to be used for logic.

Contact your local Atmel representatives or Atmel PLD applications for details.

ISP Programming Protection

The ATF1504ASV(L) has a special feature that locks the device and prevents the inputs and I/O from driving if the programming process is interrupted for any reason. The inputs and I/O default to high-Z state during such a condition. In addition the pin keeper option preserves the former state during device programming, if this circuit were previously programmed on the device. This prevents disturbing the operation of other circuits in the system while the ATF1504ASV(L) is being programmed via ISP.

All ATF1504ASV(L) devices are initially shipped in the erased state thereby making them ready to use for ISP.

Note: For more information refer to the “Designing for In-System Programmability with Atmel CPLDs” application note.

DC and AC Operating Conditions

	Commercial	Industrial
Operating Temperature (Ambient))	0°C - 70°C	-40°C - 85°C
V_{CC} (3.3V) Power Supply	3.0V - 3.6V	3.0V - 3.6V

DC Characteristics

Symbol	Parameter	Condition			Min	Typ	Max	Units
I_{IL}	Input or I/O Low Leakage Current	$V_{IN} = V_{CC}$				-2	-10	µA
I_{IH}	Input or I/O High Leakage Current					2	10	
I_{OZ}	Tri-State Output Off-State Current	$V_O = V_{CC}$ or GND			-40		40	µA
I_{CC1}	Power Supply Current, Standby	V_{CC} = Max V_{IN} = 0, V_{CC}	Std Mode	Com.		60		mA
				Ind.		75		mA
			"L" Mode	Com.		5		µA
				Ind.		5		µA
I_{CC2}	Power Supply Current, Power-down Mode	V_{CC} = Max V_{IN} = 0, V_{CC}	"PD" Mode			0.1	5	mA
I_{CC3}(2)	Reduced-power Mode Supply Current, Standby	V_{CC} = Max V_{IN} = 0, V_{CC}	Std Power	Com		40		ma
				Ind		55		
V_{IL}	Input Low Voltage				-0.3		0.8	V
V_{IH}	Input High Voltage				1.7		V_{CCIO} + 0.3	V
V_{OL}	Output Low Voltage (TTL)	$V_{IN} = V_{IH}$ or V_{IL} V_{CCIO} = Min, I_{OL} = 8 mA		Com.			0.45	V
				Ind.			0.45	
	Output Low Voltage (CMOS)	$V_{IN} = V_{IH}$ or V_{IL} V_{CC} = Min, I_{OL} = 0.1 mA		Com.			0.2	V
				Ind.			0.2	V
V_{OH}	Output High Voltage - 3.3V (TTL)	$V_{IN} = V_{IH}$ or V_{IL} V_{CCIO} = Min, I_{OH} = -2.0 mA			2.4			V
	Output High Voltage - 3.3V (CMOS)	$V_{IN} = V_{IH}$ or V_{IL} V_{CCIO} = Min, I_{OH} = -0.1 mA			V_{CCIO} - 0.2			V

Notes: 1. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 sec.
2. When microcell reduced-power feature is enabled.

Pin Capacitance

	Typ	Max	Units	Conditions
C_{IN}		8	pF	V_{IN} = 0V; f = 1.0 MHz
$C_{I/O}$		8	pF	V_{OUT} = 0V; f = 1.0 MHz

Note: Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.
The OGI pin (high-voltage pin during programming) has a maximum capacitance of 12 pF.

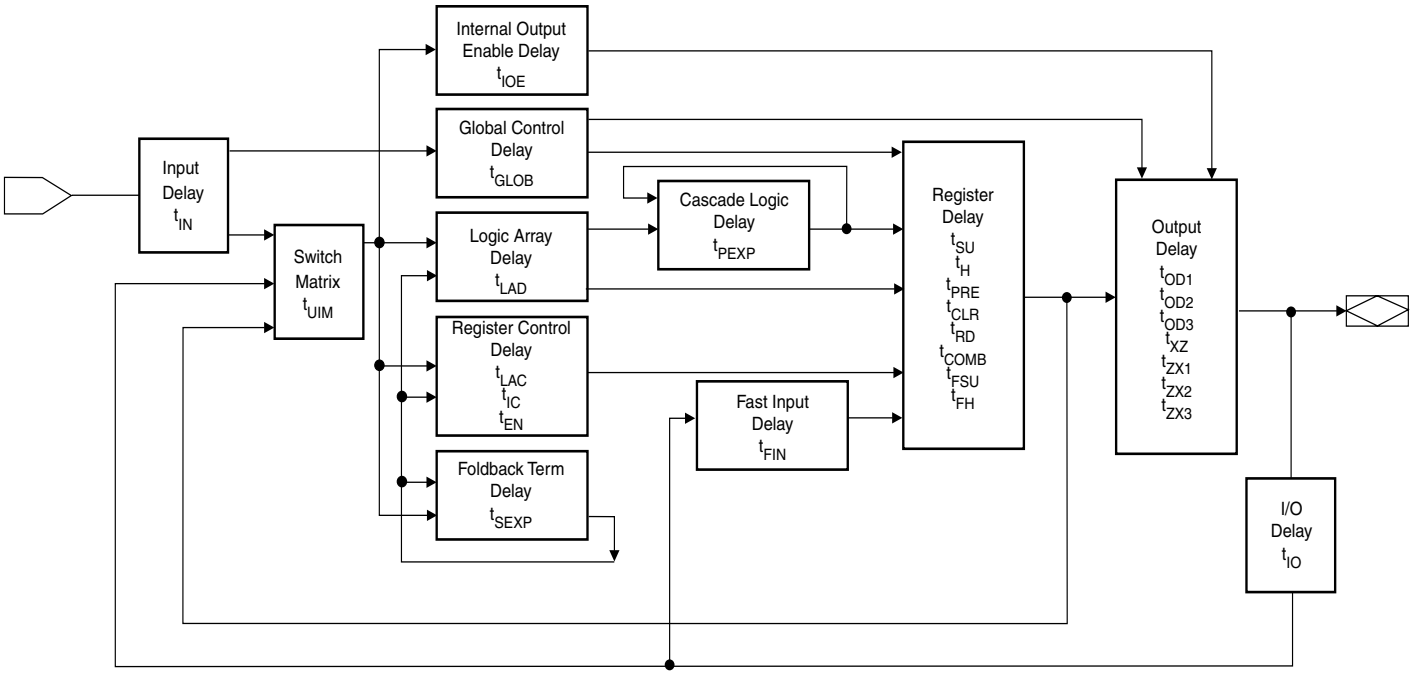
Absolute Maximum Ratings*

Temperature Under Bias	-40°C to +85°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V(1)
Voltage on Input Pins with Respect to Ground During Programming	-2.0V to +14.0V(1)
Programming Voltage with Respect to Ground	-2.0V to +14.0V(1)

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.6V DC, which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} + 0.75V DC, which may overshoot to 7.0V for pulses of less than 20 ns.

Timing Model



AC Characteristics

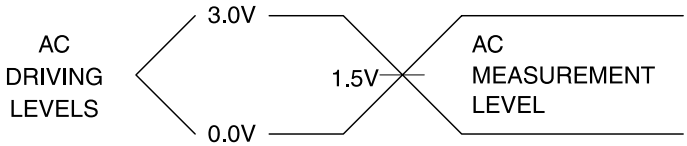
Symbol	Parameter	-15		-20		Units
		Min	Max	Min	Max	
t_{PD1}	Input or Feedback to Non-Registered Output	3	15		20	ns
t_{PD2}	I/O Input or Feedback to Non-Registered Feedback	3	12		16	ns
t_{SU}	Global Clock Setup Time	11		13.5		ns
t_{H}	Global Clock Hold Time	0		0		ns
t_{FSU}	Global Clock Setup Time of Fast Input	3		3		ns
t_{FH}	Global Clock Hold Time of Fast Input	1.0		2		MHz
t_{COP}	Global Clock to Output Delay		9		12	ns
t_{CH}	Global Clock High Time	5		6		ns
t_{CL}	Global Clock Low Time	5		6		ns
t_{ASU}	Array Clock Setup Time	5		7		ns
t_{AH}	Array Clock Hold Time	4		4		ns
t_{ACOP}	Array Clock Output Delay		15		18.5	ns
t_{ACH}	Array Clock High Time	6		8		ns
t_{ACL}	Array Clock Low Time	6		8		ns
t_{CNT}	Minimum Clock Global Period		13		17	ns
f_{CNT}	Maximum Internal Global Clock Frequency	76.9		66		MHz
t_{ACNT}	Minimum Array Clock Period		13		17	ns
f_{ACNT}	Maximum Internal Array Clock Frequency	76.9		58.8		MHz
f_{MAX}	Maximum Clock Frequency	100		83.3		MHz
t_{IN}	Input Pad and Buffer Delay		2		2.5	ns
t_{IO}	I/O Input Pad and Buffer Delay		2		2.5	ns
t_{FIN}	Fast Input Delay		2		2	ns
t_{SEXP}	Foldback Term Delay		8		10	ns
t_{PEXP}	Cascade Logic Delay		1		1	ns
t_{LAD}	Logic Array Delay		6		8	ns
t_{LAC}	Logic Control Delay		3.5		4.5	ns
t_{IOE}	Internal Output Enable Delay		3		3	ns
t_{OD1}	Output Buffer and Pad Delay (Slow slew rate = OFF; V_{CCIO} = 5V; C_L = 35 pF)		3		4	ns
t_{OD2}	Output Buffer and Pad Delay (Slow slew rate = OFF; V_{CCIO} = 3.3V; C_L = 35 pF)		3		4	ns
t_{OD3}	Output Buffer and Pad Delay (Slow slew rate = ON; V_{CCIO} = 5V or 3.3V; C_L = 35 pF)		5		6	ns
t_{ZX1}	Output Buffer Enable Delay (Slow slew rate = OFF; V_{CCIO} = 5.0V; C_L = 35 pF)		7		9	ns

AC Characteristics (Continued)

Symbol	Parameter	-15		-20		Units
		Min	Max	Min	Max	
t_{ZX2}	Output Buffer Enable Delay (Slow slew rate = OFF; V_{CCIO} = 3.3V; C_L = 35 pF)		7		9	ns
t_{ZX3}	Output Buffer Enable Delay (Slow slew rate = ON; V_{CCIO} = 5.0V/3.3V; C_L = 35 pF)		10		11	ns
t_{XZ}	Output Buffer Disable Delay (C_L = 5 pF)		6		7	ns
t_{SU}	Register Setup Time	5		6		ns
t_H	Register Hold Time	4		5		ns
t_{FSU}	Register Setup Time of Fast Input	2		2		ns
t_{FH}	Register Hold Time of Fast Input	2		2		ns
t_{RD}	Register Delay		2		2.5	ns
t_{COMB}	Combinatorial Delay		2		3	ns
t_{IC}	Array Clock Delay		6		7	ns
t_{EN}	Register Enable Time		6		7	ns
t_{GLOB}	Global Control Delay		2		3	ns
t_{PRE}	Register Preset Time		4		5	ns
t_{CLR}	Register Clear Time		4		5	ns
t_{UIM}	Switch Matrix Delay		2		2.5	ns
t_{RPA}	Reduced-power Adder[2]		10		13	ns

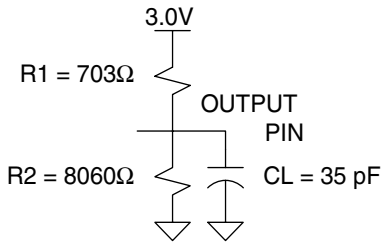
Notes: 1. See ordering information for valid part numbers.
2. The t_{RPA} parameter must be added to the t_{LAD}, t_{LAC},t_{TIC}, t_{ACL}, and t_{SEXP} parameters for macrocells running in the reduced-power mode.
3. See ordering information for valid part numbers.

Input Test Waveforms and Measurement Levels



t_R, t_F = 1.5 ns typical

Output AC Test Loads



Power-down Mode

The ATF1504ASV(L) includes an optional pin-controlled power-down feature. When this mode is enabled, the PD pin acts as the power-down pin. When the PD pin is high, the device supply current is reduced to less than 3 mA. During power down, all output data and internal logic states are latched internally and held. Therefore, all registered and combinatorial output data remain valid. Any outputs that were in a High-Z state at the onset will remain at High-Z. During power down, all input signals except the power-down pin are blocked. Input and I/O hold latches remain active to ensure that pins do not float to indeterminate levels, further reducing system power. The power-down mode feature is enabled in the logic design file or as a fitted or translated s/w option. Designs using the power-down pin may not use the PD pin as a logic array input. However, all other PD pin macrocell resources may still be used, including the buried feedback and foldback product term array inputs.

Power Down AC Characteristics(1)(2)

		-15		-20		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Units**
t_{IVDH}	Valid I, I/O before PD High	15		20		ns
t_{GVDH}	Valid OE(2) before PD High	15		20		ns
t_{CVDH}	Valid Clock(2) before PD High	15		20		ns
t_{DHIX}	I, I/O Don't Care after PD High		25		30	ns
t_{DHGX}	OE(2) Don't Care after PD High		25		30	ns
t_{DHCX}	Clock(2) Don't Care after PD High		25		30	ns
t_{DLIV}	PD Low to Valid I, I/O		1		1	µs
t_{DLGV}	PD Low to Valid OE (Pin or Term)		1		1	µs
t_{DLCV}	PD Low to Valid Clock (Pin or Term)		1		1	µs
t_{DLOV}	PD Low to Valid Output		1		1	µs

Notes: 1. For slow slew outputs, add t_{SSO}.
2. Pin or product term.
3. Includes t_{RPA} for reduced-power bit enabled.

JTAG-BST/ISP Overview

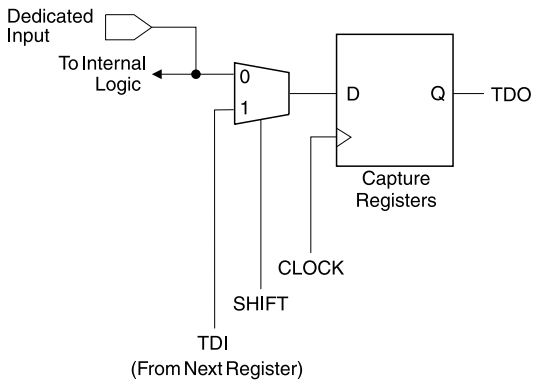
The JTAG boundary-scan testing is controlled by the Test Access Port (TAP) controller in the ATF1504ASV(L). The boundary-scan technique involves the inclusion of a shift-register stage (contained in a boundary-scan cell) adjacent to each component so that signals at component boundaries can be controlled and observed using scan testing principles. Each input pin and I/O pin has its own boundary-scan cell (BSC) in order to support boundary-scan testing. The ATF1504ASV(L) does not currently include a Test Reset (TRST) input pin because the TAP controller is automatically reset at power-up. The five JTAG modes supported include: SAMPLE/PRELOAD, EXTEST, BYPASS, IDCODE and HIGHZ. The ATF1504ASV(L)'s ISP can be fully described using JTAG's BSDL as described in IEEE Standard 1149.1b. This allows ATF1504ASV(L) programming to be described and implemented using any one of the third-party development tools supporting this standard.

The ATF1504ASV(L) has the option of using four JTAG-standard I/O pins for boundary-scan testing (BST) and in-system programming (ISP) purposes. The ATF1504ASV(L) is programmable through the four JTAG pins using the IEEE standard JTAG programming protocol established by IEEE Standard 1149.1 using 5V TTL-level programming signals from the ISP interface for in-system programming. The JTAG feature is a programmable option. If JTAG (BST or ISP) is not needed, then the four JTAG control pins are available as I/O pins.

JTAG Boundary-scan Cell (BSC) Testing

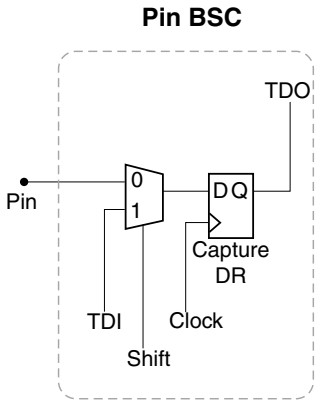
The ATF1504ASV(L) contains up to 68 I/O pins and four input pins, depending on the device type and package type selected. Each input pin and I/O pin has its own boundary-scan cell (BSC) in order to support boundary-scan testing as described in detail by IEEE Standard 1149.1. A typical BSC consists of three capture registers or scan registers and up to two update registers. There are two types of BSCs, one for input or I/O pin, and one for the macrocells. The BSCs in the device are chained together through the capture registers. Input to the capture register chain is fed in from the TDI pin while the output is directed to the TDO pin. Capture registers are used to capture active device data signals, to shift data in and out of the device and to load data into the update registers. Control signals are generated internally by the JTAG TAP controller. The BSC configuration for the input and I/O pins and macrocells are shown below.

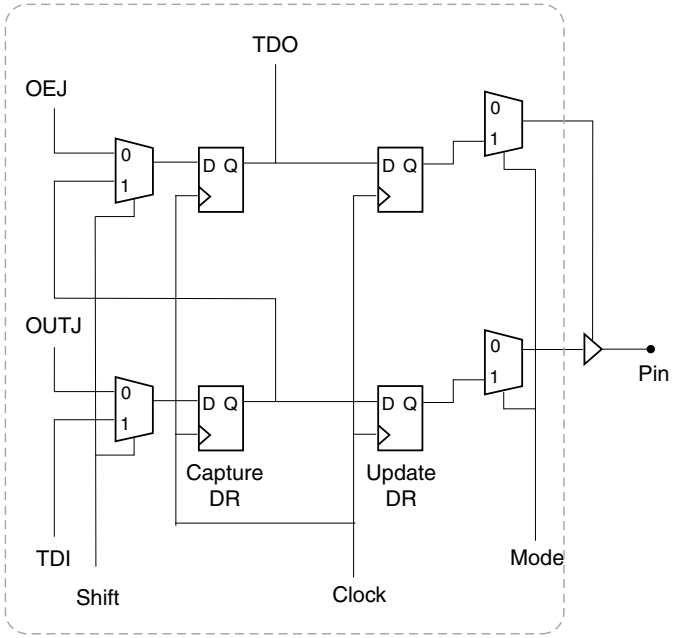
BSC Configuration for Input and I/O Pins (Except JTAG TAP Pins)



Note: The ATF1504ASV(L) has pull-up option on TMS and TDI pins. This feature is selected as a design option.

BSC Configuration for Macrocell





Macrocell BSC

ATF1504ASV Dedicated Pinouts

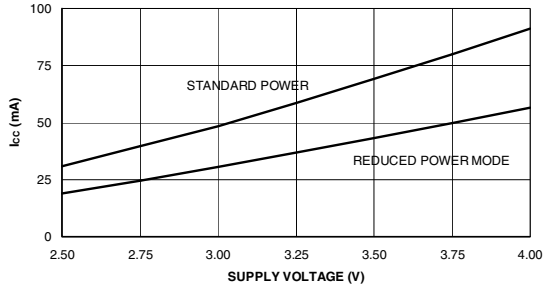
Dedicated Pin	44-lead TQFP	44-lead J-lead	68-lead J-lead	84-lead J-lead	100-lead PQFP	100-lead TQFP
INPUT/OE2/GCLK2	40	2	2	2	92	90
INPUT/GCLR	39	1	1	1	91	89
INPUT/OE1	38	44	68	84	90	88
INPUT/GCLK1	37	43	67	83	89	87
I/O /GCLK3	35	41	65	81	87	85
I/O / PD (1,2)	5, 19	11, 25	17, 37	20, 46	14, 44	12, 42
I/O / TDI (JTAG)	1	7	12	14	6	4
I/O / TMS (JTAG)	7	13	19	23	17	15
I/O / TCK (JTAG)	26	32	50	62	64	62
I/O / TDO (JTAG)	32	38	57	71	75	73
GND	4, 16, 24, 36	10, 22, 30, 42	6, 16, 26, 34, 38, 48, 58, 66	7, 19, 32, 42, 47, 59, 72, 82	13, 28, 40, 45, 61, 76, 88, 97	11, 26, 38, 43, 59, 74, 86, 95
V_{CC}	9, 17, 29, 41	3, 15, 23, 35	3, 11, 21, 31, 35, 43, 53, 63	3,13, 26, 38, 43, 53, 66, 78	5, 20, 36, 41, 53, 68, 84, 93	3, 18, 34, 39, 51, 66, 82, 91
N/C	–	–	–	–	1, 2, 7, 9, 24, 26, 29, 30, 51, 52, 55, 57, 72, 74, 79, 80	1, 2, 5, 7, 22, 24, 27, 28, 49, 50, 53, 55, 70, 72, 77, 78
# of Signal Pins	36	36	52	68	68	68
# User I/O Pins	32	32	48	64	64	64

OE (1, 2)	Global OE pins
GCLR	Global Clear pin
GCLK (1, 2, 3)	Global Clock pins
PD (1, 2)	Power-down pins
TDI, TMS, TCK, TDO	JTAG pins used for boundary-scan testing or in-system programming
GND	Ground pins
VCC	VCC pins for the device

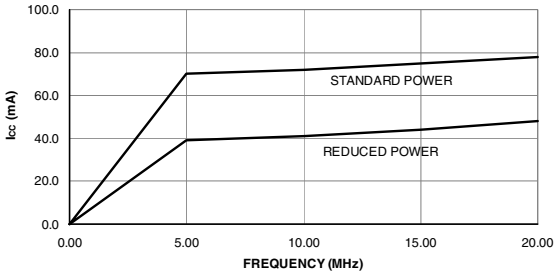
ATF1504ASV I/O Pinouts

MC	PLC	44-lead PLCC	44-lead TQFP	68-lead PLCC	84-lead PLCC	100-lead PQFP	100-lead TQFP	MC	PLC	44-lead PLCC	44-lead TQFP	68-lead PLCC	84-lead PLCC	100-lead PQFP	100-lead TQFP
1	A	12	6	18	22	16	14	33	C	24	18	36	44	42	40
2	A	-	-	-	21	15	13	34	C	-	-	-	45	43	41
3	A/ **PD1**	11	5	17	20	14	12	35	C/ **PD2**	25	19	37	46	44	42
4	A	9	3	15	18	12	10	36	C	26	20	39	48	46	44
5	A	8	2	14	17	11	9	37	C	27	21	40	49	47	45
6	A	-	-	13	16	10	8	38	C	-	-	41	50	48	46
7	A	-	-	-	15	8	6	39	C	-	-	-	51	49	47
8/ **TDI**	A	7	1	12	14	6	4	40	C	28	22	42	52	50	48
9	A	-	-	10	12	4	100	41	C	29	23	44	54	54	52
10	A	-	-	-	11	3	99	42	C	-	-	-	55	56	54
11	A	6	44	9	10	100	98	43	C	-	-	45	56	58	56
12	A	-	-	8	9	99	97	44	C	-	-	46	57	59	57
13	A	-	-	7	8	98	96	45	C	-	-	47	58	60	58
14	A	5	43	5	6	96	94	46	C	31	25	49	60	62	60
15	A	-	-	-	5	95	93	47	C	-	-	-	61	63	61
16	A	4	42	4	4	94	92	48/ **TCK**	C	32	26	50	62	64	62
17	B	21	15	33	41	39	37	49	D	33	27	51	63	65	63
18	B	-	-	-	40	38	36	50	D	-	-	-	64	66	64
19	B	20	14	32	39	37	35	51	D	34	28	52	65	67	65
20	B	19	13	30	37	35	33	52	D	36	30	54	67	69	67
21	B	18	12	29	36	34	32	53	D	37	31	55	68	70	68
22	B	-	-	28	35	33	31	54	D	-	-	56	69	71	69
23	B	-	-	-	34	32	30	55	D	-	-	-	70	73	71
24	B	17	11	27	33	31	29	56/ **TDO**	D	38	32	57	71	75	73
25	B	16	10	25	31	27	25	57	D	39	33	59	73	77	75
26	B	-	-	-	30	25	23	58	D	-	-	-	74	78	76
27	B	-	-	24	29	23	21	59	D	-	-	60	75	81	79
28	B	-	-	23	28	22	20	60	D	-	-	61	76	82	80
29	B	-	-	22	27	21	19	61	D	-	-	62	77	83	81
30	B	14	8	20	25	19	17	62	D	40	34	64	79	85	83
31	B	-	-	-	24	18	16	63	D	-	-	-	80	86	84
32/ **TMS**	B	13	7	19	23	17	15	64	D/ **GCLK3**	41	35	65	81	87	85

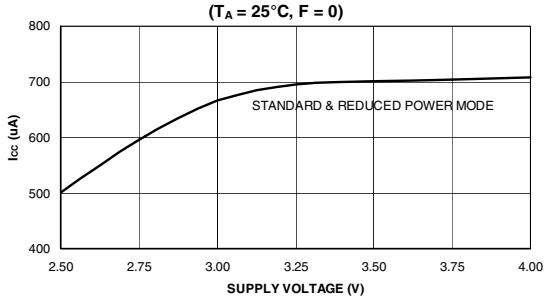
SUPPLY CURRENT VS. SUPPLY VOLTAGE
(T_A = 25°C, F = 0)



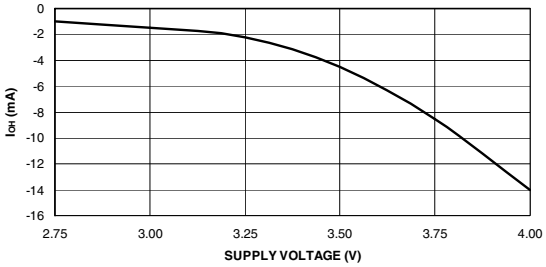
SUPPLY CURRENT VS. FREQUENCY
LOW-POWER ("L") VERSION
(T_A = 25°C)



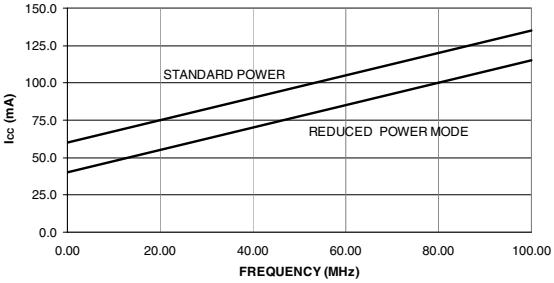
SUPPLY CURRENT VS. SUPPLY VOLTAGE
PIN-CONTROLLED POWER-DOWN MODE
(T_A = 25°C, F = 0)



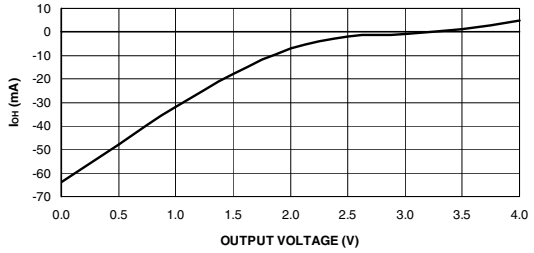
OUTPUT SOURCE CURRENT
VS. SUPPLY VOLTAGE
(V_{OH} = 2.4V, T_A = 25°C)



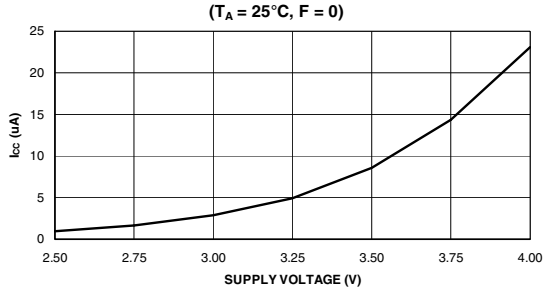
SUPPLY CURRENT VS. FREQUENCY
STANDARD POWER (T_A = 25°C)



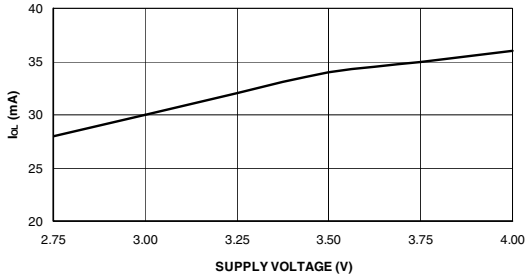
OUTPUT SOURCE CURRENT
VS. OUTPUT VOLTAGE
(V_{CC} = 3.3V, T_A = 25°C)



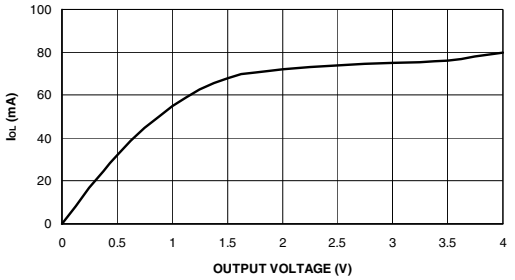
SUPPLY CURRENT VS. SUPPLY VOLTAGE
LOW-POWER ("L") VERSION
(T_A = 25°C, F = 0)



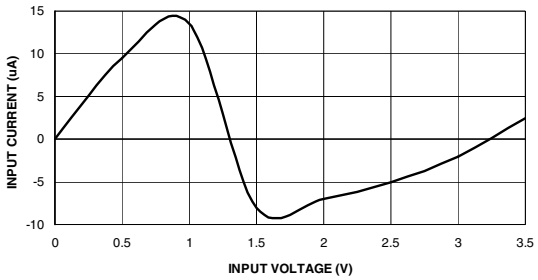
OUTPUT SINK CURRENT VS. SUPPLY VOLTAGE
(V_{OL} = 0.5V, T_A = 25°C)



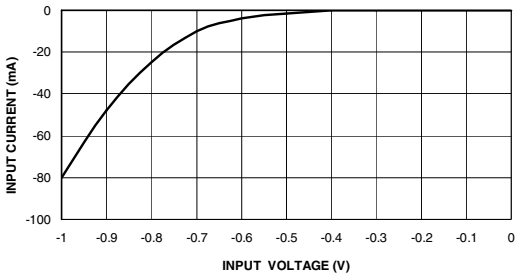
OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE
(V_{CC} = 3.3V, T_A = 25°C)



INPUT CURRENT VS. INPUT VOLTAGE
(V_{CC} = 3.3V, T_A = 25°C)



INPUT CLAMP CURRENT VS. INPUT VOLTAGE
(V_{CC} = 3.3V, T_A = 25°C)



ATF1504ASV(L) Ordering Information

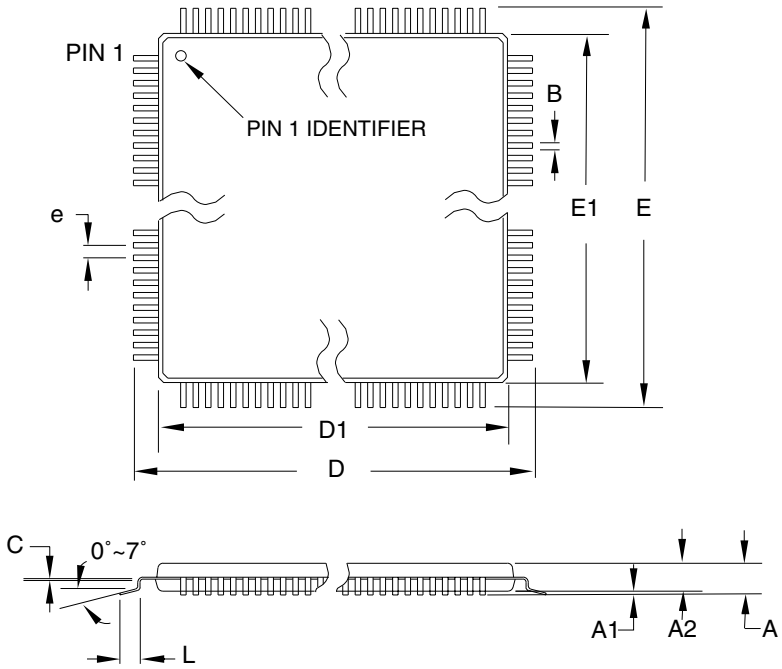
t_{PD} (ns)	t_{CO1} (ns)	f_{MAX} (MHz)	Ordering Code	Package	Operation Range
15	8	100	ATF1504ASV-15 AC44	44A	Commercial (0°C to 70°C)
			ATF1504ASV-15 JC44	44J	
			ATF1504ASV-15 JC68	68J	
			ATF1504ASV-15 JC84	84J	
			ATF1504ASV-15 QC100	100Q1	
			ATF1500ASV-15 AC100	100A	
15	8	100	ATF1504ASV-15 AI44	44A	Industrial (-40°C to +85°C)
			ATF1504ASV-15 JI44	44J	
			ATF1504ASV-15 JI68	68J	
			ATF1504ASV-15 JI84	84J	
			ATF1504ASV-15 QI100	100Q1	
			ATF1504ASV-15 AI100	100A	
20	12	83.3	ATF1504ASVL-20 AC44	44A	Commercial (0°C to 70°C)
			ATF1504ASVL-20 JC44	44J	
			ATF1504ASVL-20 JC68	68J	
			ATF1504ASVL-20 JC84	84J	
			ATF1504ASVL-20 QC100	100Q1	
			ATF1504ASVL-20 AC100	100A	
20	12	83.3	ATF1504ASVL-20 AI44	44A	Industrial (-40°C to +85°C)
			ATF1504ASVL-20 JI44	44J	
			ATF1504ASVL-20 JI68	68J	
			ATF1504ASVL-20 JI84	84J	
			ATF1504ASVL-20 QI100	100Q1	
			ATF1504ASVL-20 AI100	100A	

Using “C” Product for Industrial

There is very little risk in using “C” devices for industrial applications because the V_{CC} conditions for 3.3V products are the same for commercial and industrial (there is only 15°C difference at the high end of the temperature range). To use commercial product for industrial temperature ranges, de-rate I_{CC} by 15%.

Packaging Information

44A – TQFP



COMMON DIMENSIONS
(Unit of Measure = mm)

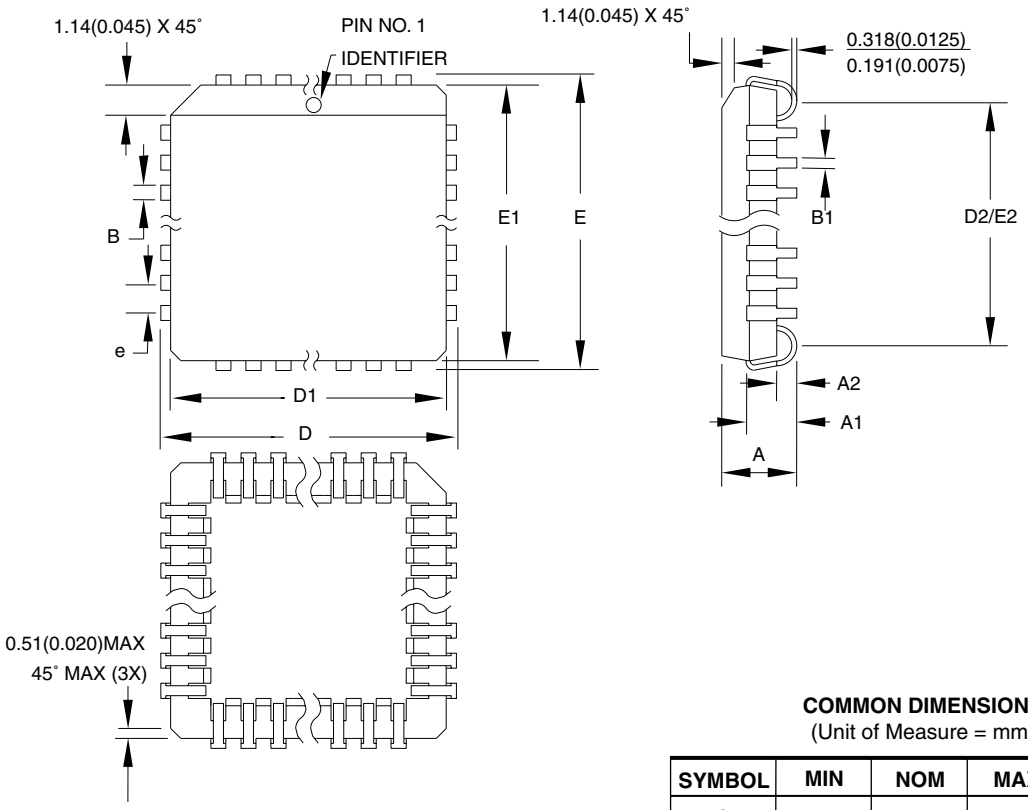
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	11.75	12.00	12.25	
D1	9.90	10.00	10.10	Note 2
E	11.75	12.00	12.25	
E1	9.90	10.00	10.10	Note 2
B	0.30	–	0.45	
C	0.09	–	0.20	
L	0.45	–	0.75	
e	0.80 TYP			

Notes:
1. This package conforms to JEDEC reference MS-026, Variation ACB.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10 mm maximum.

10/5/2001

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**44A,** 44-lead, 10 x 10 mm Body Size, 1.0 mm Body Thickness, 0.8 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)	44A	B

44J – PLCC



COMMON DIMENSIONS
(Unit of Measure = mm)

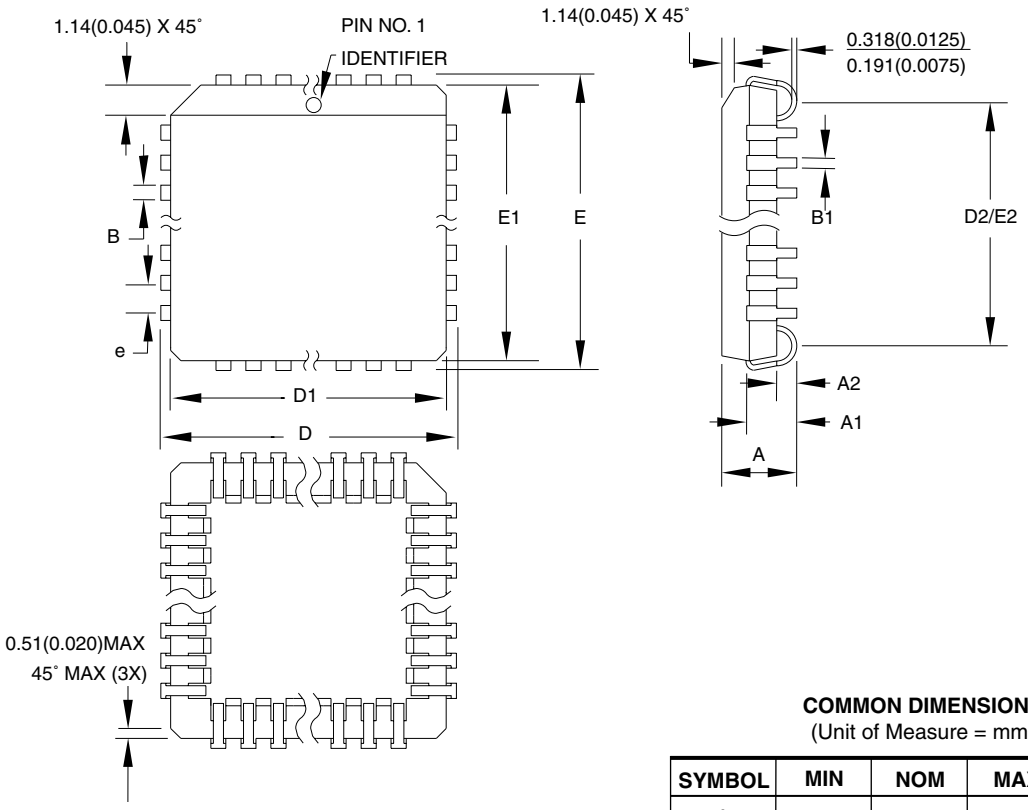
SYMBOL	MIN	NOM	MAX	NOTE
A	4.191	–	4.572	
A1	2.286	–	3.048	
A2	0.508	–	–	
D	17.399	–	17.653	
D1	16.510	–	16.662	Note 2
E	17.399	–	17.653	
E1	16.510	–	16.662	Note 2
D2/E2	14.986	–	16.002	
B	0.660	–	0.813	
B1	0.330	–	0.533	
e	1.270 TYP			

Notes:
1. This package conforms to JEDEC reference MS-018, Variation AC.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
3. Lead coplanarity is 0.004" (0.102 mm) maximum.

10/04/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**44J**, 44-lead, Plastic J-leaded Chip Carrier (PLCC)	44J	B

68J – PLCC



COMMON DIMENSIONS
(Unit of Measure = mm)

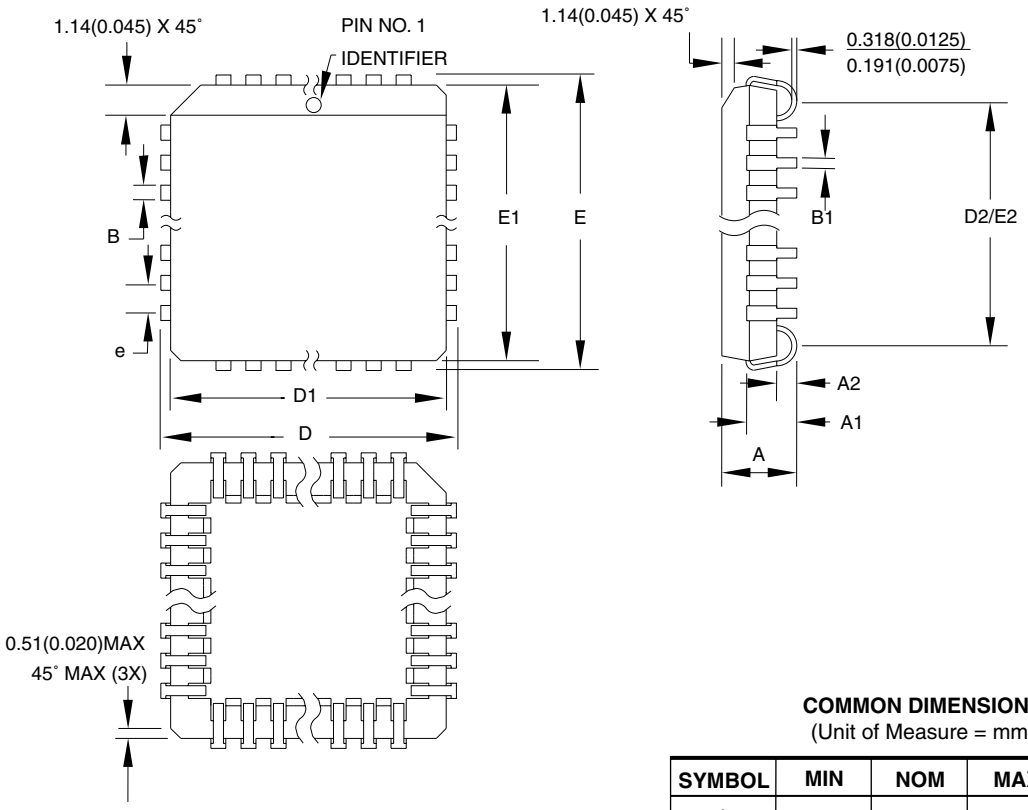
SYMBOL	MIN	NOM	MAX	NOTE
A	4.191	–	4.572	
A1	2.286	–	3.048	
A2	0.508	–	–	
D	25.019	–	25.273	
D1	24.130	–	24.333	Note 2
E	25.019	–	25.273	
E1	24.130	–	24.333	Note 2
D2/E2	22.606	–	23.622	
B	0.660	–	0.813	
B1	0.330	–	0.533	
e	1.270 TYP			

Notes:
1. This package conforms to JEDEC reference MS-018, Variation AE.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
3. Lead coplanarity is 0.004" (0.102 mm) maximum.

10/04/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**68J**, 68-lead, Plastic J-leaded Chip Carrier (PLCC)	68J	B

84J – PLCC



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	4.191	–	4.572	
A1	2.286	–	3.048	
A2	0.508	–	–	
D	30.099	–	30.353	
D1	29.210	–	29.413	Note 2
E	30.099	–	30.353	
E1	29.210	–	29.413	Note 2
D2/E2	27.686	–	28.702	
B	0.660	–	0.813	
B1	0.330	–	0.533	
e	1.270 TYP			

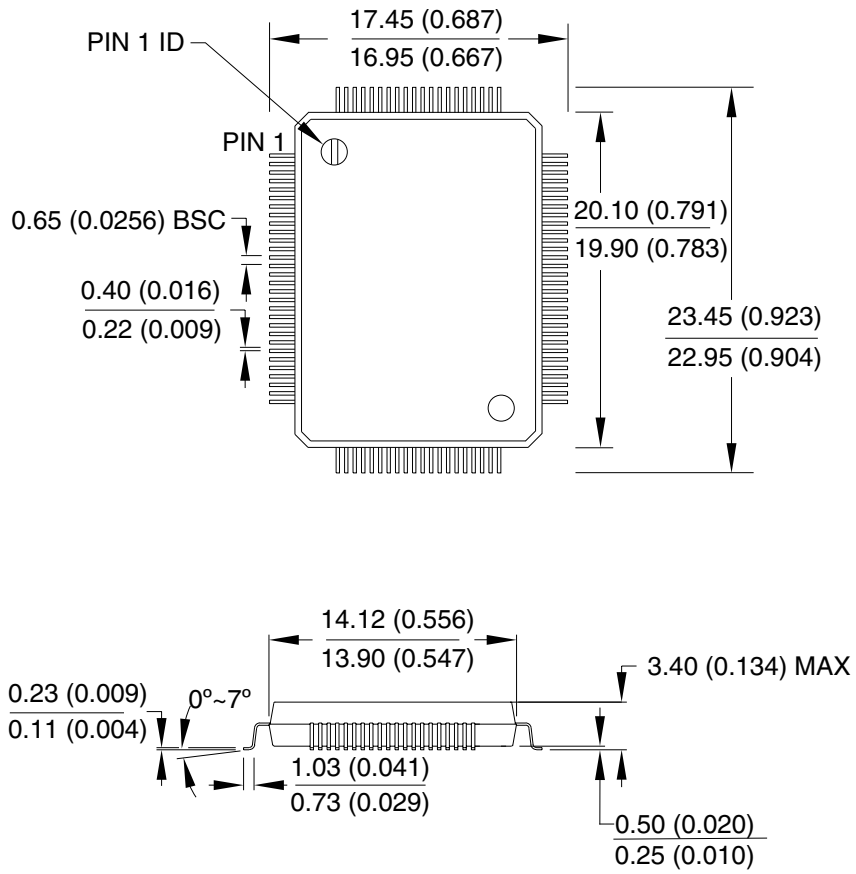
Notes:
1. This package conforms to JEDEC reference MS-018, Variation AF.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
3. Lead coplanarity is 0.004" (0.102 mm) maximum.

10/04/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**84J**, 84-lead, Plastic J-leaded Chip Carrier (PLCC)	84J	B

100Q1 – PQFP

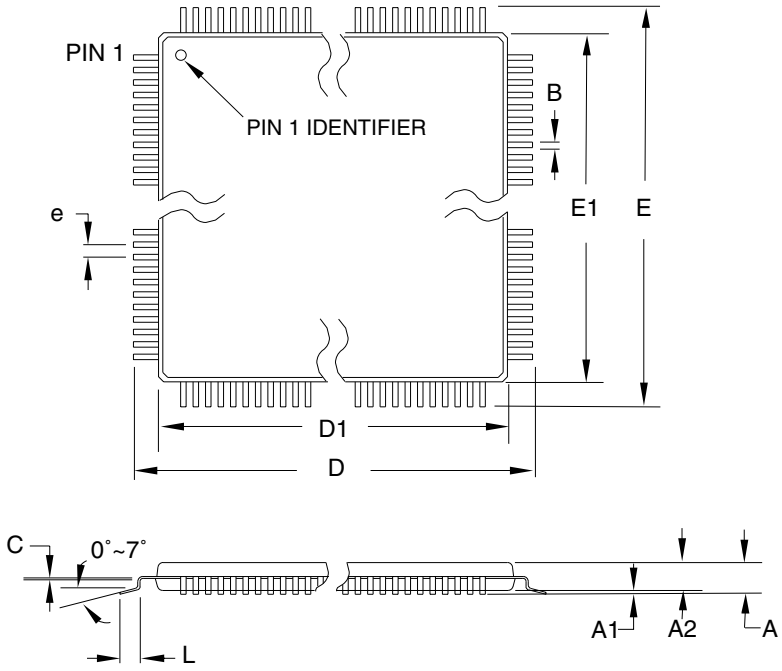
Dimensions in Millimeters and (Inches)*
*Controlling dimensions: millimeters
JEDEC STANDARD MS-022, GC-1



04/11/2001

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**100Q1**, 100-lead, 14 x 20 mm Body, 3.2 mm Footprint, 0.65 mm Pitch, Plastic Quad Flat Package (PQFP)	100Q1	A

100A – TQFP



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	15.75	16.00	16.25	
D1	13.90	14.00	14.10	Note 2
E	15.75	16.00	16.25	
E1	13.90	14.00	14.10	Note 2
B	0.17	–	0.27	
C	0.09	–	0.20	
L	0.45	–	0.75	
e	0.50 TYP			

Notes:
1. This package conforms to JEDEC reference MS-026, Variation AED.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.08 mm maximum.

10/5/2001

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**100A,** 100-lead, 14 x 14 mm Body Size, 1.0 mm Body Thickness, 0.5 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)	100A	C

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1409I–PLD–2/03 xM

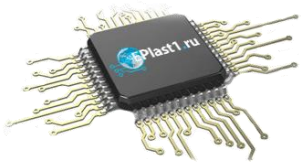
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