

100 mA Low Noise, High Ripple Rejection, Negative-voltage LDO Regulator

No. EA-379-181207

OVERVIEW

The RP117x is a negative voltage LDO regulator that provides high ripple rejection and low output noise. Adding only one capacitor to each input and output pin can make a simple structure and high performance LDO regulator.

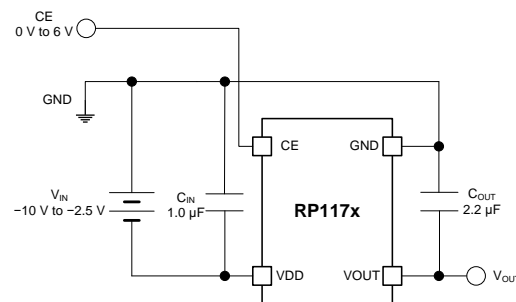
KEY BENEFITS

- Provides high ripple rejection rate and low output noise, which is ideal for noise-sensitive devices.
- Requires only one capacitor for each input and output pin, and is available in small DFN(PLP)1212-6 and SC-88A packages, both of which can utilize the space on board.

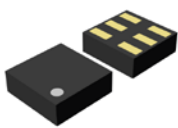
KEY SPECIFICATIONS

- Input Voltage Range: -10.0 V to -2.5 V
- Output Voltage Range: -5.5 V to -1.0 V
- Output Current: 100 mA
- Supply Current: Typ. 75 μA
- Ripple Rejection Rate: Typ. 80 dB, $f = 1\text{ kHz}$
- Output Noise: Typ. 16 μVrms
($V_{\text{SET}} = -5.5\text{ V}$ to -2.0 V)
- Protection Features: Thermal Shutdown Protection
Short-circuit Protection
- Auto-discharge Function

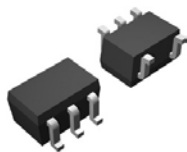
TYPICAL APPLICATIONS



PACKAGE



DFN(PLP)1212-6
1.20 x 1.20 x 0.4⁽¹⁾ (mm)
⁽¹⁾ maximum dimension



SC-88A
2.0 x 2.1 x 0.9 (mm)

SELECTION GUIDE

The set output voltage and the package type are user-selectable options.

Product Name	Package
RP117Kxx1D-TR	DFN(PLP)1212-6
RP117Qxx2D-TR-FE	SC-88A

xx: Specify the set output voltage (V_{SET}) within the range of -5.5 V to -1.0 V in 0.1 V steps.

APPLICATIONS

- Noise-sensitive Devices: Sensors, DACs, ADCs, Amplifiers
- Audio Devices, DSLRs
- Measuring Instruments
- Liquid Crystal Panels, Bias Power Supply for CCDs

RP117x

No. EA-379-181207

SELECTION GUIDE

The RP117x includes an auto-discharge function⁽¹⁾. A set output voltage and a package type are user-selectable options.

Selection Guide

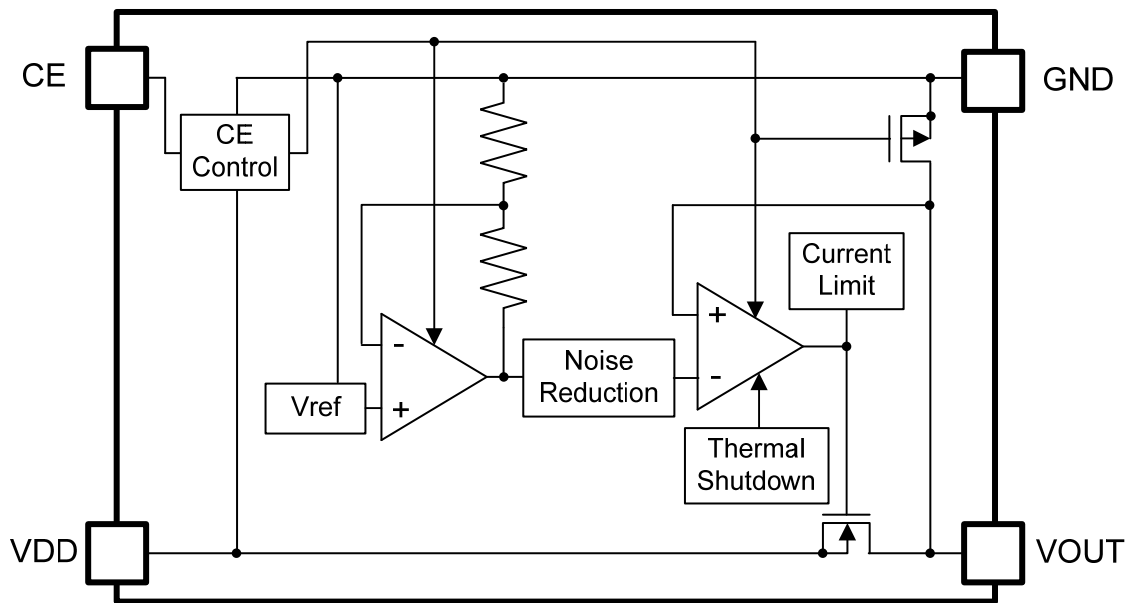
Product Name	Package	Quantity per Real	Pb Free	Halogen Free
RP117Kxx1D-TR	DFN(PLP)1212-6	5,000 pcs	Yes	Yes
RP117Qxx2D-TR-FE	SC-88A	3,000 pcs	Yes	Yes

xx: Specify the set output voltage (V_{SET}) within the range of -5.5 V to -1.0 V in 0.1 V steps.

The voltage in 0.05 V step is shown as follows:

Ex. -1.35 V : RP117x13xx5

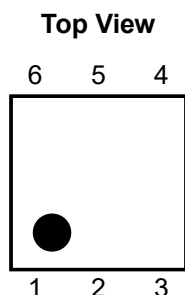
BLOCK DIAGRAM



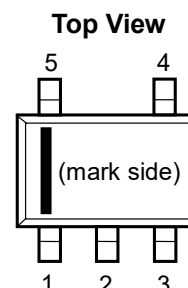
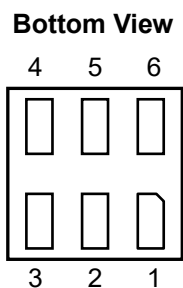
RP117x Block Diagram

⁽¹⁾ Auto-discharge function quickly lowers the output voltage to 0 V , when the chip enable signal is switched from the active mode to the standby mode, by releasing the electrical charge accumulated in the external capacitor.

PIN DESCRIPTIONS



DFN(PLP)1212-6 Pin Configuration



SC-88A Pin Configuration

DFN(PLP)1212-6 Pin Description

Pin No.	Symbol	Description
1	CE	Chip Enable Pin, Active-high
2	NC	No Connection
3	VDD	Input Pin
4	VOUT	Output Pin
5	NC	No Connection
6	GND	Ground Pin

SC-88A Pin Description

Pin No.	Symbol	Description
1	GND	Ground Pin
2	VDD	Input Pin
3	VOUT	Output Pin
4	CE	Chip Enable Pin, Active-high
5	NC	No Connection

ABSOLUTE MAXIMUM RATINGS**Absolute Maximum Ratings**

Symbol	Parameter		Rating	Unit
V _{IN}	Input Voltage		-11.0 to 0.3	V
V _{CE}	CE Pin Voltage		-0.3 to 7.0	V
V _{OUT}	VOUT Pin Voltage		V _{IN} - 0.3 to 0.3	V
I _{OUT}	Output Current		220	mA
P _D	Power Dissipation ⁽¹⁾	DFN(PLP)1212-6 (JEDEC STD.51)	450	mW
		SC-88A (Standard Test Land Pattern)	380	mW
T _j	Junction Temperature		-40 to 125	°C
T _{stg}	Storage Temperature Range		-55 to 125	°C

ABSOLUTE MAXIMUM RATINGS

Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause the permanent damages and may degrade the life time and safety for both device and system using the device in the field. The functional operation at or over these absolute maximum ratings is not assured.

RECOMMENDED OPERATING TEMPERATURE**Recommended Operating Conditions**

Symbol	Parameter	Rating	Unit
V _{IN}	Input Voltage	-10.0 to -2.5	V
V _{CE}	CE Pin Voltage	0 to 6.0	V
T _a	Operating Temperature	-40 to 85	°C

RECOMMENDED OPERATING CONDITIONS

All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if when they are used over such conditions by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

⁽¹⁾ Please refer to *POWER DISSIPATION* for detailed information.

ELECTRICAL CHARACTERISTICS

$V_{IN} = V_{SET} - 1.0\text{ V}$ ($V_{SET} > -1.5\text{ V}$, $V_{IN} = -2.5\text{ V}$), $I_{OUT} = 1\text{ mA}$, $C_{IN} = 1.0\text{ }\mu\text{F}$, $C_{OUT} = 2.2\text{ }\mu\text{F}$, unless otherwise noted.

The specifications surrounded by are guaranteed by design engineering at $-40^{\circ}\text{C} \leq T_a \leq 85^{\circ}\text{C}$.

RP117x Electrical Characteristics

($T_a = 25^{\circ}\text{C}$)

Symbol	Parameter	Test Conditions/Comments	Min.	Typ.	Max.	Unit
V_{OUT}	Output Voltage	$T_a = 25^{\circ}\text{C}$	x 1.020		x 0.980	V
		$-40^{\circ}\text{C} \leq T_a \leq 85^{\circ}\text{C}$	x 1.050		x 0.950	V
I_{OUT}	Output Current		100			mA
$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	Load Regulation	$1\text{ mA} \leq I_{OUT} \leq 100\text{ mA}$		10	30	mV
V_{DIF}	Dropout Voltage	$I_{OUT} = 100\text{ mA}$	Refer to <i>PRODUCT-SPECIFIC ELECTRICAL CHARACTERISTICS</i>			
I_{SS}	Supply Current	$I_{OUT} = 0\text{ mA}$		75	150	μA
$I_{STANDBY}$	Standby Current	$V_{CE} = 0\text{ V}$		0.01	0.15	μA
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation	$-10.0\text{ V} \leq V_{IN} \leq V_{SET} - 0.5\text{ V}$ (Up to -2.5 V)	-0.30		0.30	%/V
RR	Ripple Rejection	$f = 1\text{ kHz}$, Ripple 0.2 V_{p-p} , $V_{IN} = V_{SET} - 1.0\text{ V}$, $I_{OUT} = 30\text{ mA}$ ($V_{SET} \geq -2.5\text{ V}$, $V_{IN} = -3.5\text{ V}$)		80		dB
V_{IN}	Input Voltage		-10.0		-2.5	V
$\frac{\Delta V_{OUT}}{\Delta T_a}$	Output Voltage Temperature Coefficient	$-40^{\circ}\text{C} \leq T_a \leq 85^{\circ}\text{C}$		± 100		ppm/ $^{\circ}\text{C}$
I_{SC}	Short Current Limit	$V_{OUT} = 0\text{ V}$		150		mA
R_{CE}	CE Pull-down Resistance	$V_{IN} = -5\text{ V}$, $V_{CE} = 3\text{ V}$		5		M Ω
V_{CEH}	CE Pin Input Voltage, high		1.5			V
V_{CEL}	CE Pin Input Voltage, low				0.5	V
en	Output Noise	BW = 10 Hz to 100 kHz, $I_{OUT} = 30\text{ mA}$	$V_{SET} > -2.0\text{ V}$	$44 - 13 \times V_{SET} $		μV_{rms}
			$V_{SET} \leq -2.0\text{ V}$			
T_{TSD}	Thermal Shutdown Temperature Threshold, rising	Junction Temperature		165		$^{\circ}\text{C}$
T_{TSR}	Thermal Shutdown Temperature Threshold, falling	Junction Temperature		110		$^{\circ}\text{C}$
R_{LOW}	Auto-discharge PMOS On Resistance	$V_{IN} = -4.0\text{ V}$, $V_{CE} = 0\text{ V}$		250		Ω

All test items listed under *Electrical Characteristics* are done under the pulse load condition ($T_j \approx T_a = 25^{\circ}\text{C}$) except Output Voltage Temperature Coefficient, Output Noise and Ripple Rejection.

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ELECTRICAL CHARACTERISTICS (continued)

The specifications surrounded by are guaranteed by design engineering at $-40^{\circ}\text{C} \leq T_a \leq 85^{\circ}\text{C}$.

RP117x Product-specific Electrical Characteristics

Product Name	V _{OUT} [V]						V _{DIF} [V]	
	T _a = 25°C			-40°C ≤ T _a ≤ 85°C			Typ.	Max.
	Min.	Typ.	Max.	Min.	Typ.	Max.		
RP117x10xx	-1.020	-1.000	-0.980	-1.050	-1.000	-0.950	(1)	(1)
RP117x11xx	-1.122	-1.100	-1.078	-1.155	-1.100	-1.045		
RP117x12xx	-1.224	-1.200	-1.176	-1.260	-1.200	-1.140		
RP117x13xx	-1.326	-1.300	-1.274	-1.365	-1.300	-1.235		
RP117x13xx5	-1.377	-1.350	-1.323	-1.417	-1.350	-1.283		
RP117x14xx	-1.428	-1.400	-1.372	-1.470	-1.400	-1.330		
RP117x15xx	-1.530	-1.500	-1.470	-1.575	-1.500	-1.425	0.66 ⁽¹⁾	0.7
RP117x16xx	-1.632	-1.600	-1.568	-1.680	-1.600	-1.520		
RP117x17xx	-1.734	-1.700	-1.666	-1.785	-1.700	-1.615		
RP117x18xx	-1.836	-1.800	-1.764	-1.890	-1.800	-1.710		
RP117x19xx	-1.938	-1.900	-1.862	-1.995	-1.900	-1.805		
RP117x20xx	-2.040	-2.000	-1.960	-2.100	-2.000	-1.900		
RP117x21xx	-2.142	-2.100	-2.058	-2.205	-2.100	-1.995	0.31 ⁽¹⁾	0.45
RP117x22xx	-2.244	-2.200	-2.156	-2.310	-2.200	-2.090		
RP117x23xx	-2.346	-2.300	-2.254	-2.415	-2.300	-2.185		
RP117x24xx	-2.448	-2.400	-2.352	-2.520	-2.400	-2.280		
RP117x25xx	-2.550	-2.500	-2.450	-2.625	-2.500	-2.375		
RP117x26xx	-2.652	-2.600	-2.548	-2.730	-2.600	-2.470		
RP117x27xx	-2.754	-2.700	-2.646	-2.835	-2.700	-2.565		
RP117x28xx	-2.856	-2.800	-2.744	-2.940	-2.800	-2.660		
RP117x29xx	-2.958	-2.900	-2.842	-3.045	-2.900	-2.755		
RP117x30xx	-3.060	-3.000	-2.940	-3.150	-3.000	-2.850		
RP117x31xx	-3.162	-3.100	-3.038	-3.255	-3.100	-2.945	0.23	0.30
RP117x32xx	-3.264	-3.200	-3.136	-3.360	-3.200	-3.040		
RP117x33xx	-3.366	-3.300	-3.234	-3.465	-3.300	-3.135		
RP117x34xx	-3.468	-3.400	-3.332	-3.570	-3.400	-3.230		
RP117x35xx	-3.570	-3.500	-3.430	-3.675	-3.500	-3.325		
RP117x36xx	-3.672	-3.600	-3.528	-3.780	-3.600	-3.420		
RP117x37xx	-3.774	-3.700	-3.626	-3.885	-3.700	-3.515		
RP117x38xx	-3.876	-3.800	-3.724	-3.990	-3.800	-3.610		
RP117x39xx	-3.978	-3.900	-3.822	-4.095	-3.900	-3.705		
RP117x40xx	-4.080	-4.000	-3.920	-4.200	-4.000	-3.800		
RP117x41xx	-4.182	-4.100	-4.018	-4.305	-4.100	-3.895	0.13	0.21
RP117x42xx	-4.284	-4.200	-4.116	-4.410	-4.200	-3.990		
RP117x43xx	-4.386	-4.300	-4.214	-4.515	-4.300	-4.085		
RP117x44xx	-4.488	-4.400	-4.312	-4.620	-4.400	-4.180		
RP117x45xx	-4.590	-4.500	-4.410	-4.725	-4.500	-4.275		
RP117x46xx	-4.692	-4.600	-4.508	-4.830	-4.600	-4.370		
RP117x47xx	-4.794	-4.700	-4.606	-4.935	-4.700	-4.465		
RP117x48xx	-4.896	-4.800	-4.704	-5.040	-4.800	-4.560		
RP117x49xx	-4.998	-4.900	-4.802	-5.145	-4.900	-4.655		
RP117x50xx	-5.100	-5.000	-4.900	-5.250	-5.000	-4.750		
RP117x51xx	-5.202	-5.100	-4.998	-5.355	-5.100	-4.845		
RP117x52xx	-5.304	-5.200	-5.096	-5.460	-5.200	-4.940		
RP117x53xx	-5.406	-5.300	-5.194	-5.565	-5.300	-5.035		
RP117x54xx	-5.508	-5.400	-5.292	-5.670	-5.400	-5.130		
RP117x55xx	-5.610	-5.500	-5.390	-5.775	-5.500	-5.225		

⁽¹⁾ Input voltage should be equal or less than the maximum operating voltage (-2.5 V).

THEORY OF OPERATION

CE Pin Input Current

The CE pin input current is determined by the VDD pin input voltage and the CE pin input voltage as shown in the table below.

		CE Voltage[V]				
		1.5	2	3	4	5
V _{in} [V]	-2.5	0.3	0.3	0.4	0.5	0.6
	-3	0.3	0.4	0.5	0.5	0.6
	-4	0.4	0.4	0.5	0.6	0.7
	-5	0.5	0.5	0.6	0.7	0.8
	-6	0.5	0.6	0.7	0.7	0.8
	-7	0.6	0.6	0.7	0.8	0.9
	-8	0.7	0.7	0.8	0.9	1.0
	-9	0.7	0.8	0.9	1.0	1.0
	-10	0.8	0.8	0.9	1.0	1.1

(uA)

RP117x CE Pin Input Current

Minimum Operating Voltage

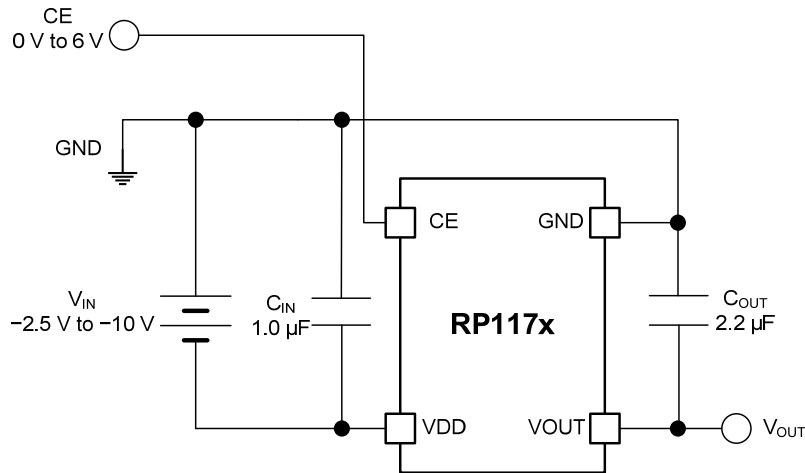
The RP 117x does not include an UVLO circuit. To make the internal circuit operate normally and to ensure good output regulation, V_{IN} has to be: $V_{IN} \leq V_{SET} - V_{DIF}$ (Max. -2.5 V). To bring out the best characteristics of the output noise voltage, the ripple rejection and the load transient response, V_{IN} has to be $V_{IN} = V_{SET} - 1.0$ V.

Thermal Shutdown

Thermal shutdown deactivates a circuit when the junction temperature exceeds the thermal shutdown threshold (T_{TSD}) of Typ. 165°C, and reactivates it when the junction temperature falls below the thermal shutdown release threshold (T_{TSR}) of Typ. 110°C. During the reactivation, the inrush current limit is in operation. Note that deactivation and activation cycle can be repeated due to load, heat dissipation and ambient temperature conditions. Thermal shutdown cannot be used for the purpose of heat sink, so the repetitive cycles of deactivation and activation may affect the reliability of the device.

RP117x

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APPLICATION INFORMATION**RP117x Typical Application Circuit****External Components**

Symbol	Description
C _{IN}	Ceramic Capacitor, 1.0 μF, TDK, CGA3E1X7R1C105K
C _{OUT}	Ceramic Capacitor, 2.2 μF, TDK, CGA5L2X7R1E225K

Technical Notes on the Selection of External Components

- Phase compensation is provided to secure stable operation even when the load current is varied. For this purpose, use a 2.2-μF or more output capacitor (C_{OUT}) with good frequency characteristics and proper ESR (Equivalent Series Resistance). In case of using a tantalum type capacitor with a large ESR, the output might become unstable. Evaluate your circuit including consideration of frequency characteristics.
- The high impedance of the wirings may result in noise pickup and unstable operation of the device. Reduce the impedance of the VDD and GND wirings. Connect a 1.0-μF or more input capacitor (C_{IN}) between the VDD and GND pins with shortest-distance wiring. Also, connect a 2.2-μF or more output capacitor (C_{OUT}) between the VOUT and GND pins with shortest-distance wiring

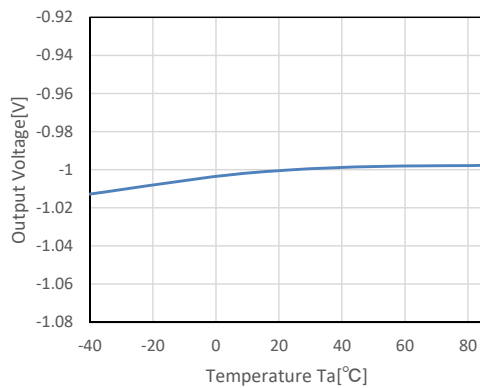
TYPICAL CHARACTERISTICS

Note: Typical Characteristics are intended to be used as reference data; they are not guaranteed.

1) Output Voltage vs. Ambient Temperature (C_{IN} = Ceramic 1.0 μ F, C_{OUT} = Ceramic 2.2 μ F)

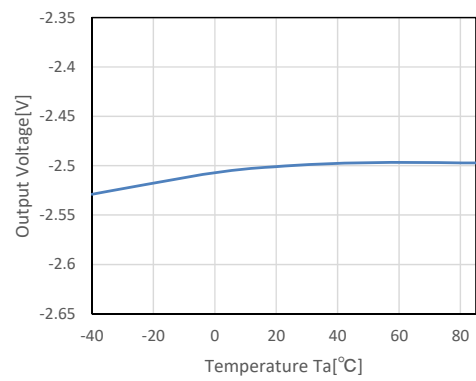
RP117x101x

$V_{IN} = -2.5$ V, $I_{OUT} = 1$ mA



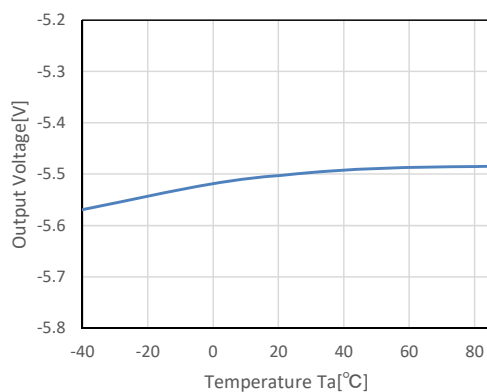
RP117x251x

$V_{IN} = -3.5$ V, $I_{OUT} = 1$ mA



RP117x551x

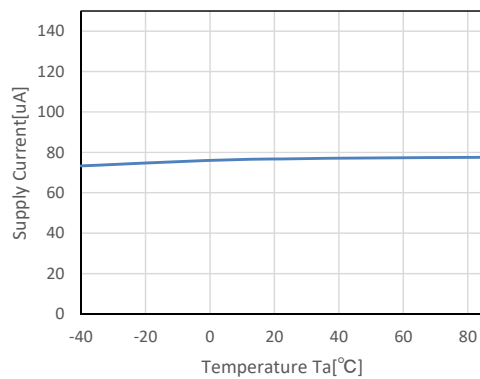
$V_{IN} = -6.5$ V, $I_{OUT} = 1$ mA



2) Supply Current vs. Ambient Temperature (C_{IN} = Ceramic 1.0 μ F, C_{OUT} = Ceramic 2.2 μ F)

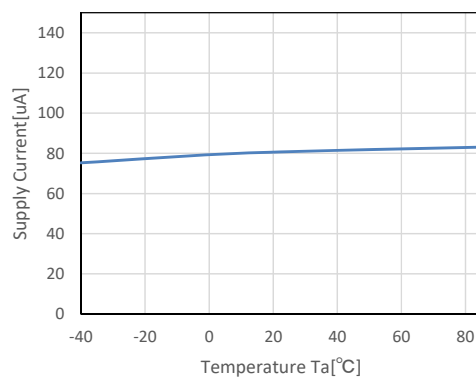
RP117x101x

$V_{IN} = -2.5$ V



RP117x251x

$V_{IN} = -3.5$ V

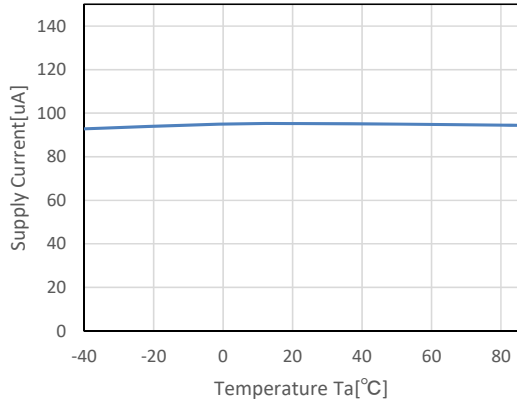


RP117x

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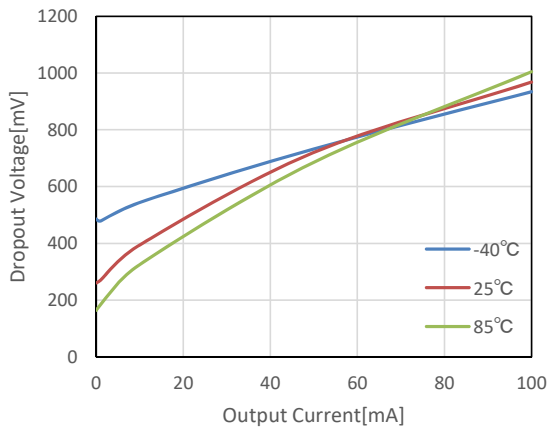
RP117x551x

$V_{IN} = -6.5\text{ V}$

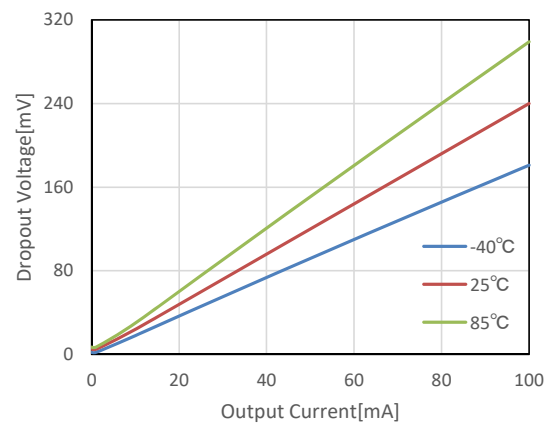


3) Dropout Voltage vs. Output Current ($C_{IN} = \text{Ceramic } 1.0\ \mu\text{F}$, $C_{OUT} = \text{Ceramic } 2.2\ \mu\text{F}$)

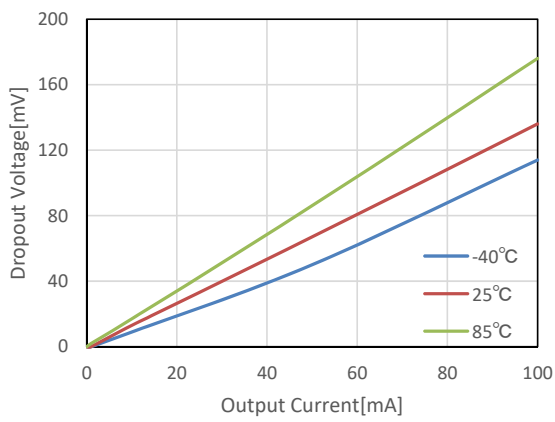
RP117x101x



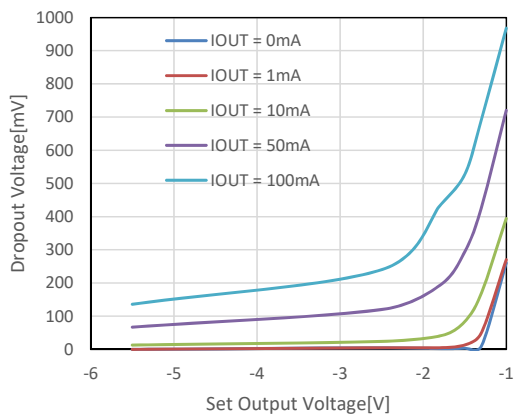
RP117x251x



RP117x551x

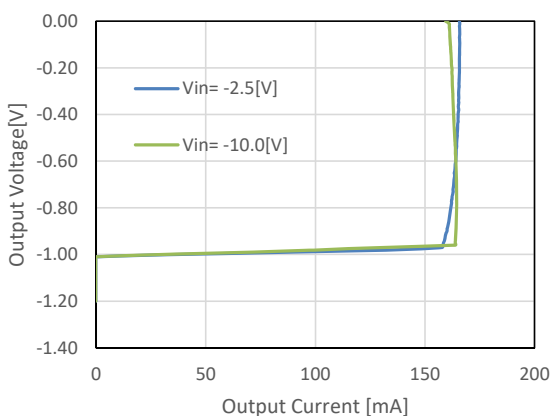


4) Dropout Voltage vs. Set Output Voltage (C_{IN} = Ceramic 1.0 μ F, C_{OUT} = Ceramic 2.2 μ F, T_a = 25°C)

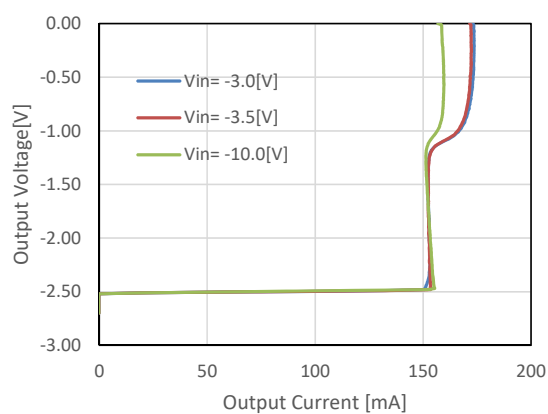


5) Output Voltage vs. Output Current (C_{IN} = Ceramic 1.0 μ F, C_{OUT} = Ceramic 2.2 μ F, T_a = 25°C)

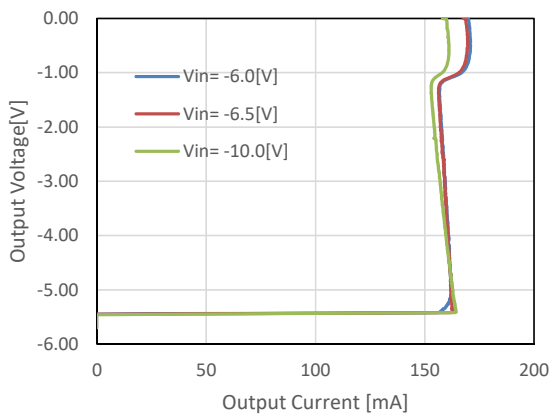
RP117x101x



RP117x251x



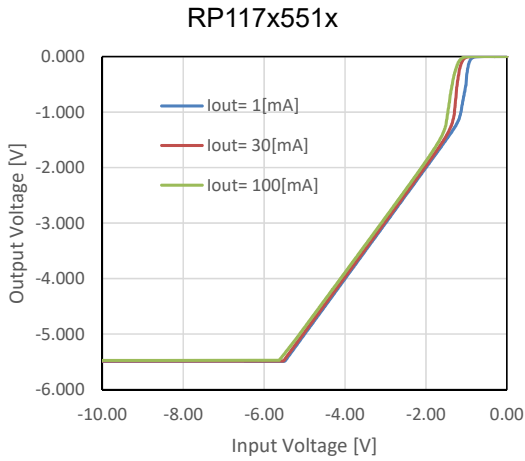
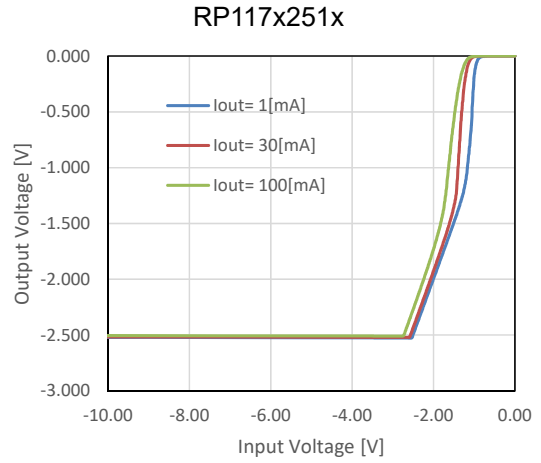
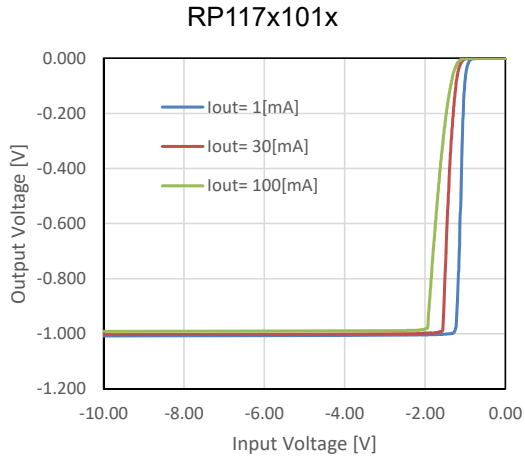
RP117x551x



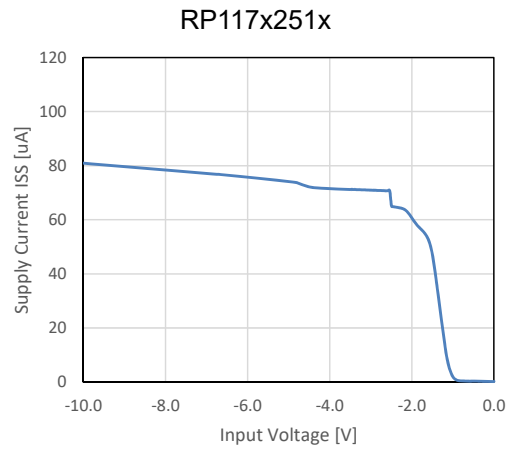
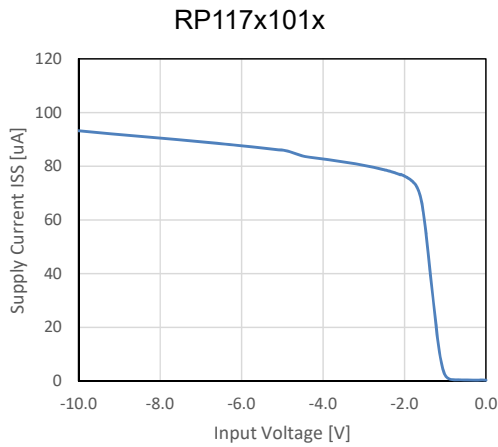
RP117x

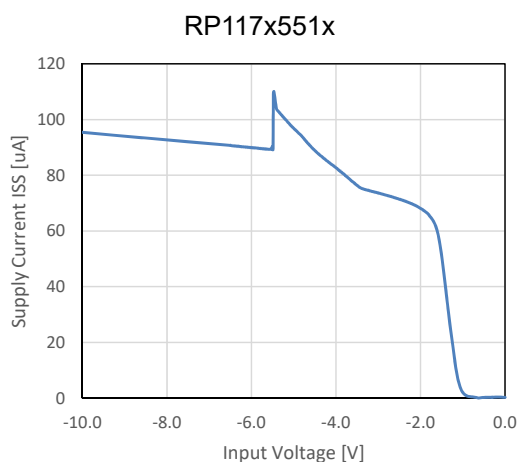
No. EA-379-181207

6) Output Voltage vs. Input Voltage (C_{IN} = Ceramic 1.0 μ F, C_{OUT} = Ceramic 2.2 μ F, T_a = 25°C)



7) Supply Current vs. Input Voltage (C_{IN} = Ceramic 1.0 μ F, C_{OUT} = Ceramic 2.2 μ F, T_a = 25°C)

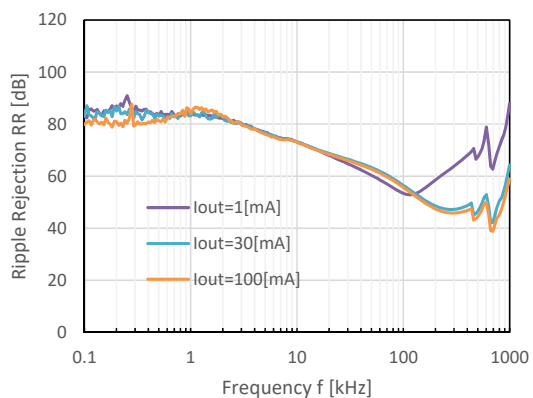




8) Ripple Rejection vs. Frequency (C_{IN} = none, C_{OUT} = Ceramic 2.2 μ F, Ripple = 0.2 Vp-p, T_a = 25°C)

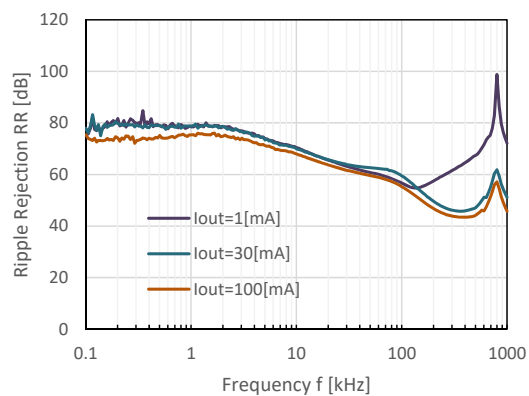
RP117x101x

$V_{IN} = -3.5$ V



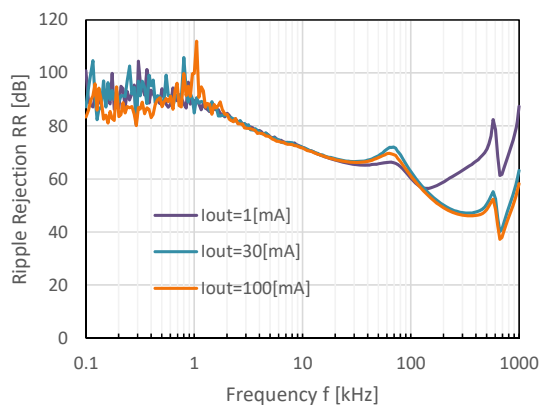
RP117x251x

$V_{IN} = -3.5$ V



RP117x551x

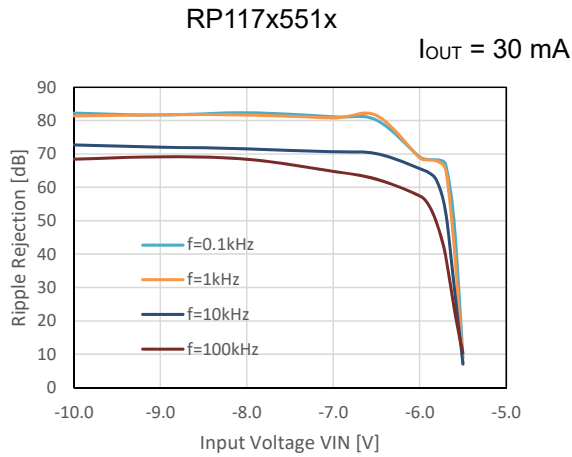
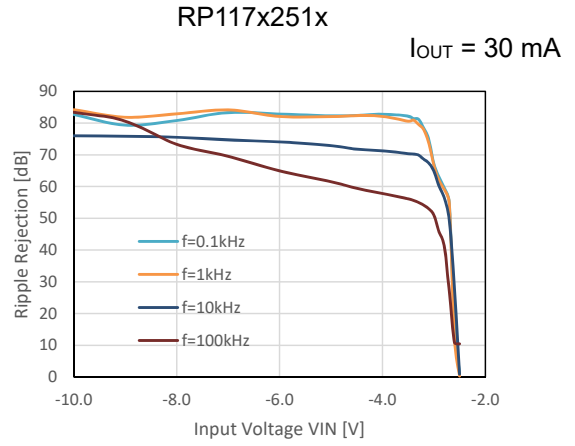
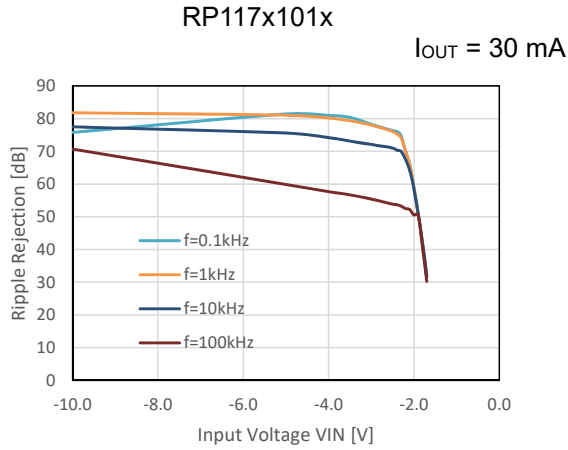
$V_{IN} = -6.5$ V



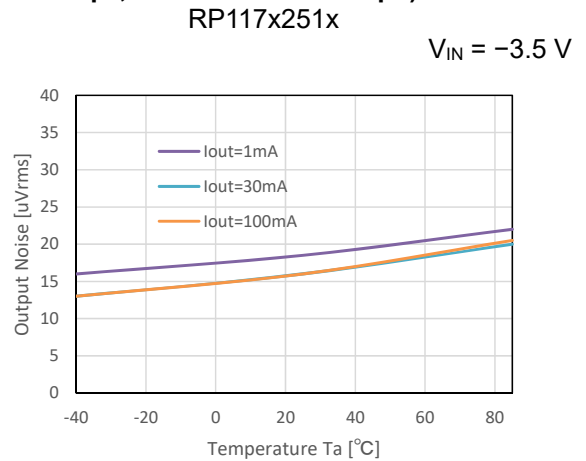
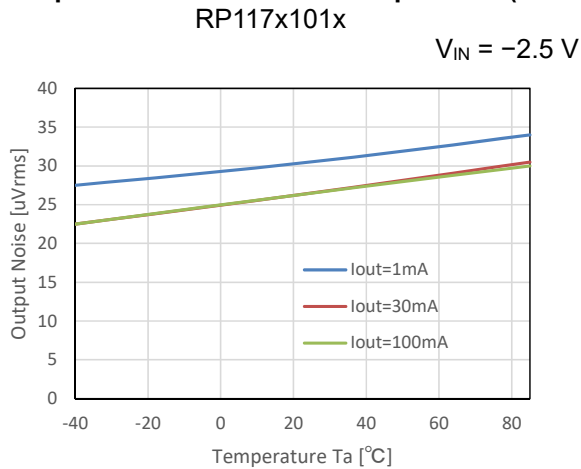
RP117x

No. EA-379-181207

9) Ripple Rejection vs. Input Voltage (C_{IN} = none, C_{OUT} = Ceramic 2.2 μ F, Ripple = 0.2 Vp-p, T_a = 25°C)

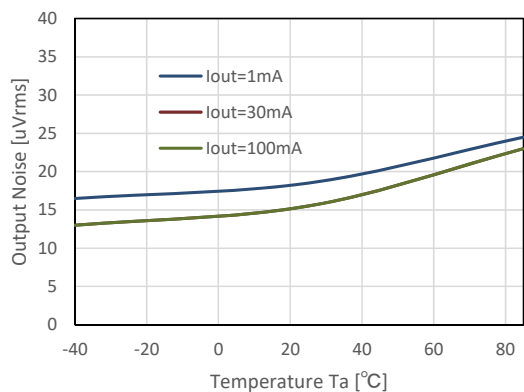


10) Output Noise vs. Ambient Temperature (C_{IN} = Ceramic 1.0 μ F, C_{OUT} = Ceramic 2.2 μ F)



RP117x551x

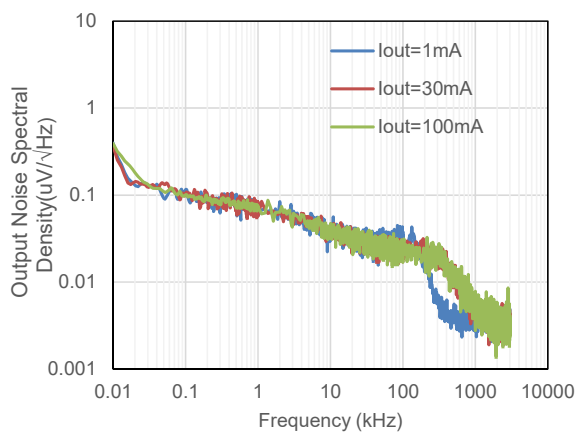
$V_{IN} = -6.5\text{ V}$



11) Output Noise vs. Frequency ($C_{IN} = \text{Ceramic } 1.0\ \mu\text{F}$, $C_{OUT} = \text{Ceramic } 2.2\ \mu\text{F}$, $T_a = 25^\circ\text{C}$)

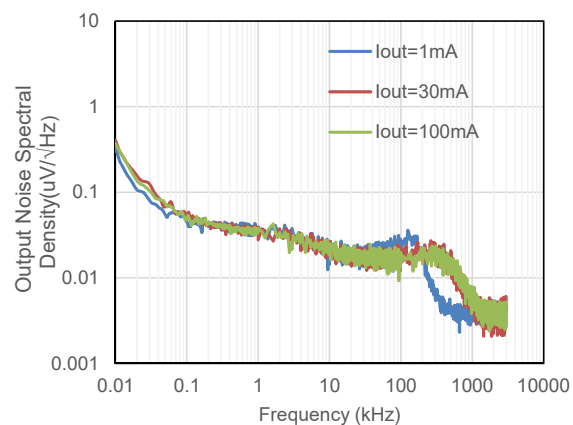
RP117x101x

$V_{IN} = -2.5\text{ V}$



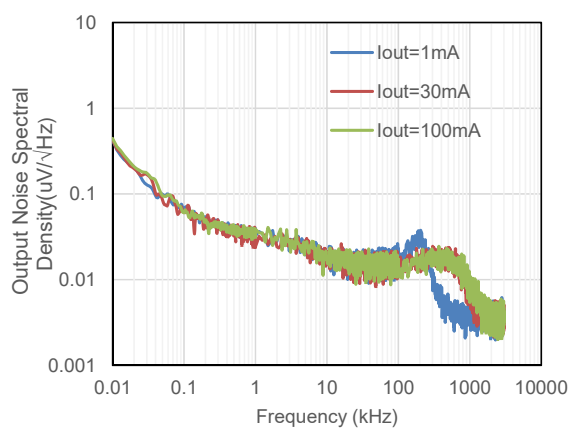
RP117x251x

$V_{IN} = -3.5\text{ V}$



RP117x551x

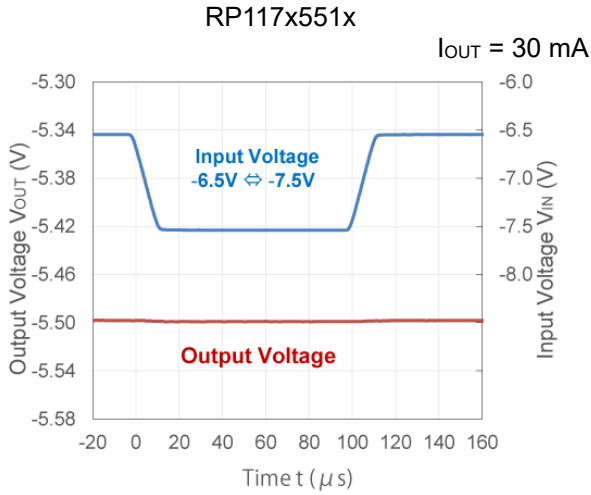
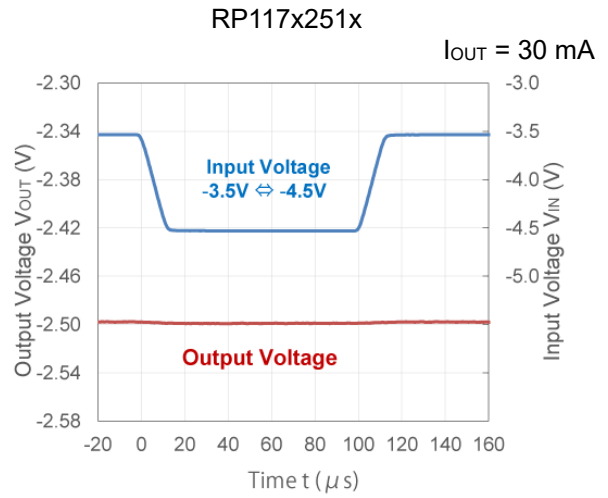
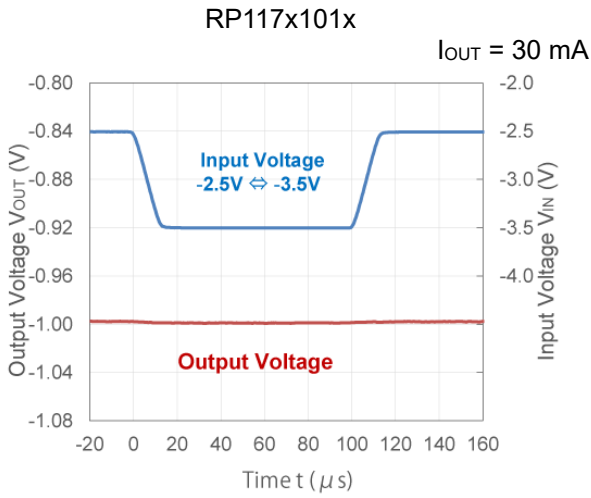
$V_{IN} = -6.5\text{ V}$



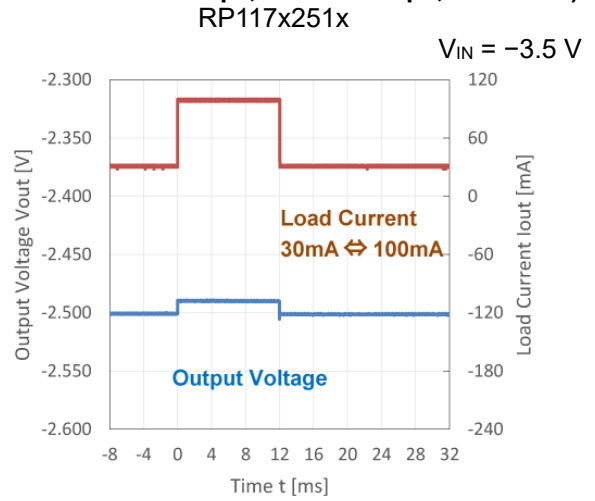
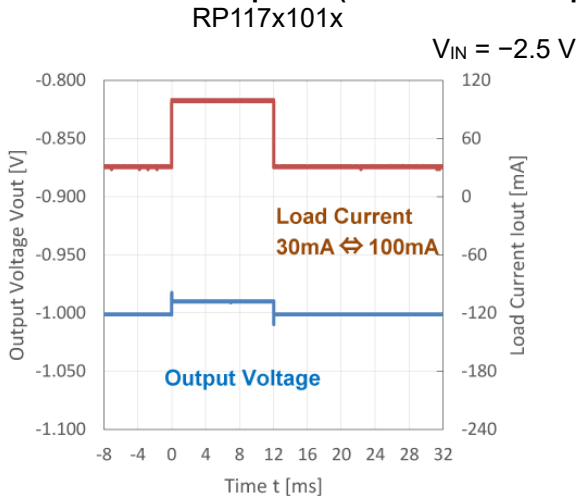
RP117x

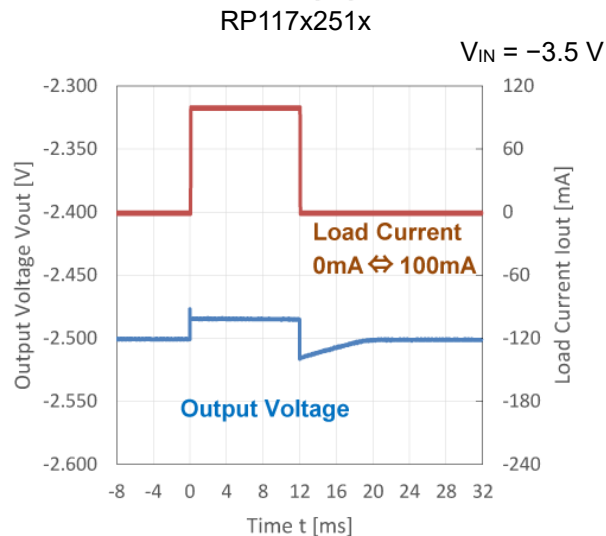
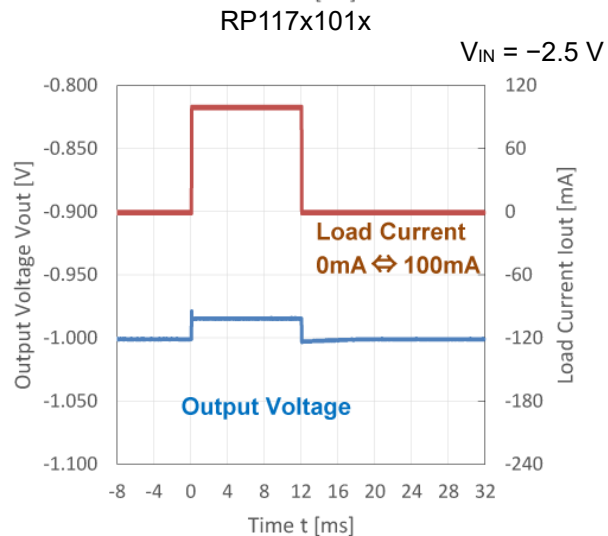
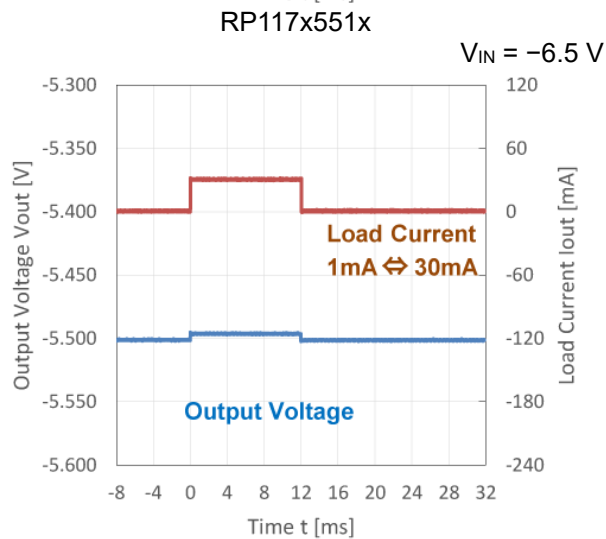
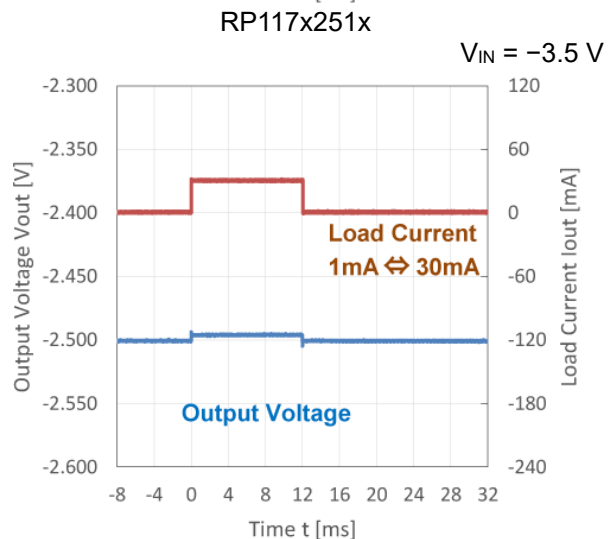
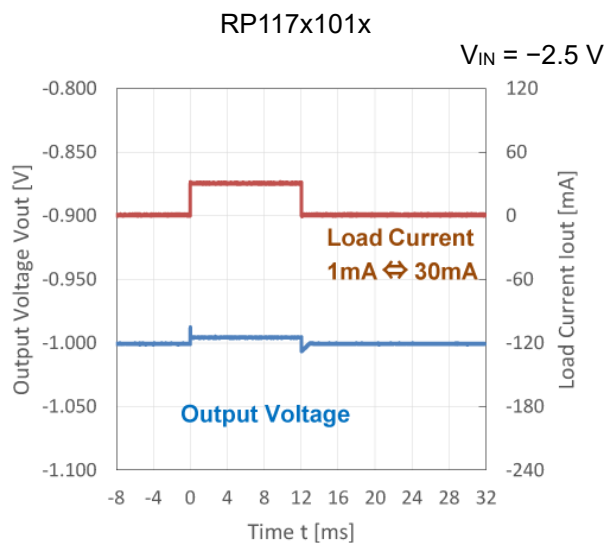
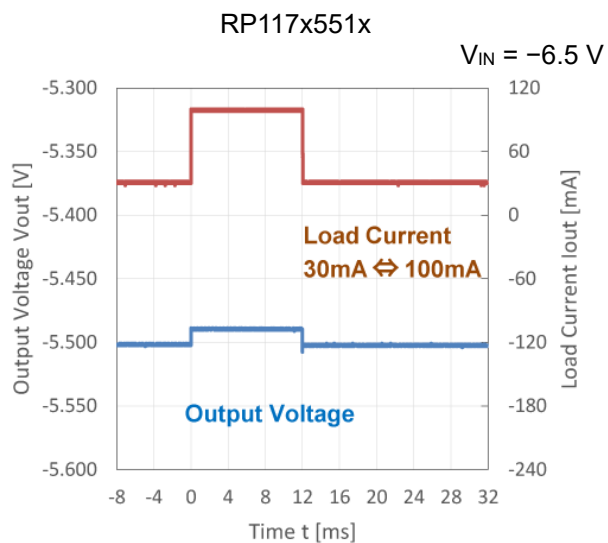
No. EA-379-181207

12) Input Transient Response ($C_{IN} = \text{Ceramic } 1.0 \mu\text{F}$, $C_{OUT} = \text{Ceramic } 2.2 \mu\text{F}$, $t_r = t_f = 10 \mu\text{s}$, $T_a = 25^\circ\text{C}$)



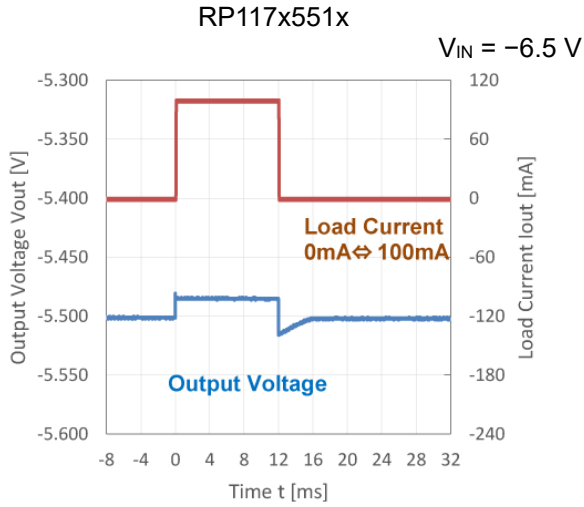
13) Load Transient Response ($C_{IN} = \text{Ceramic } 1.0 \mu\text{F}$, $C_{OUT} = \text{Ceramic } 2.2 \mu\text{F}$, $t_r = t_f = 0.5 \mu\text{s}$, $T_a = 25^\circ\text{C}$)



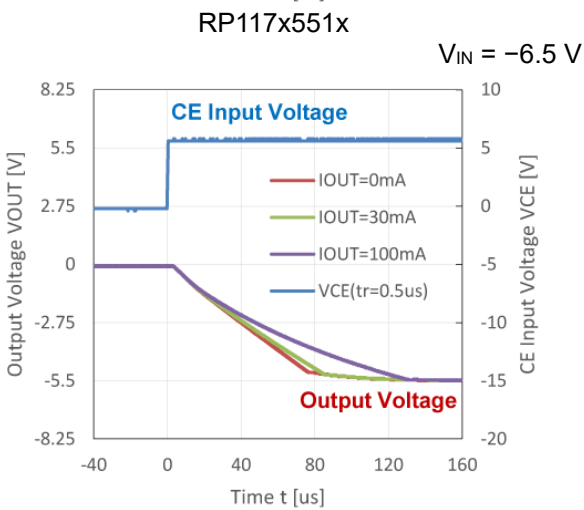
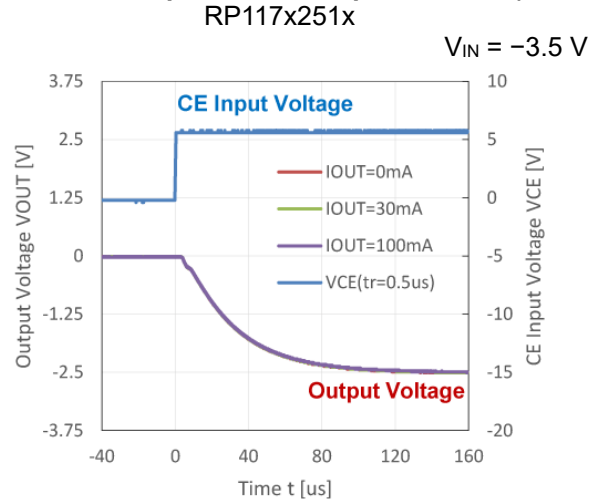
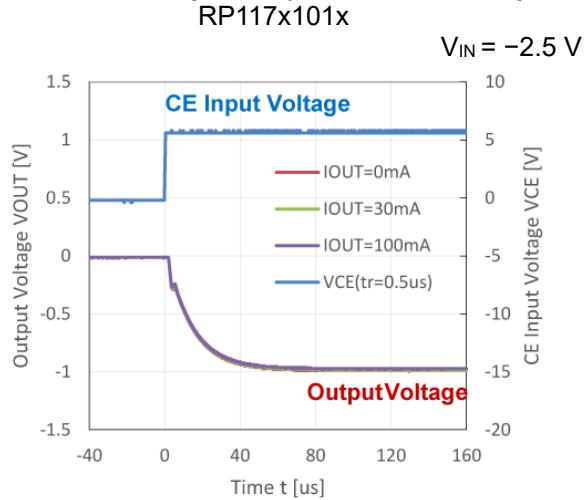


RP117x

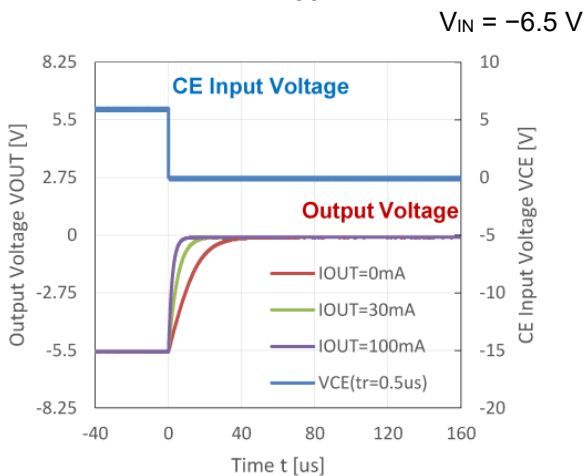
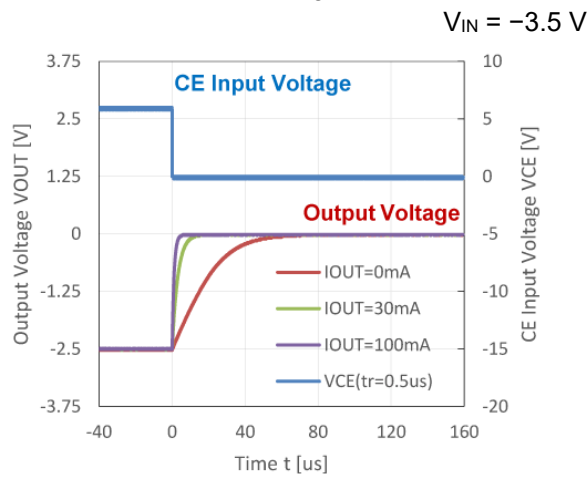
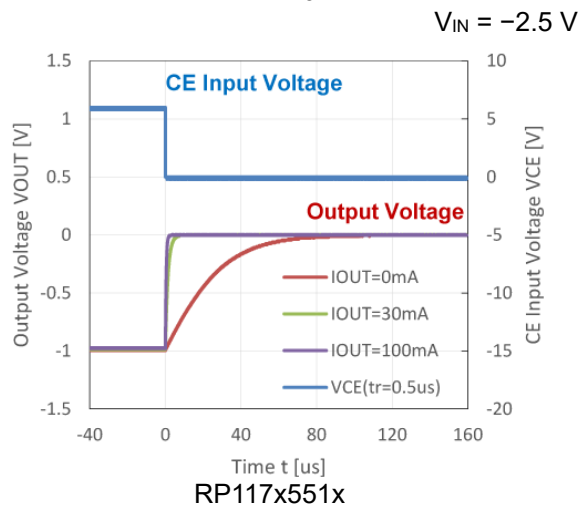
No. EA-379-181207



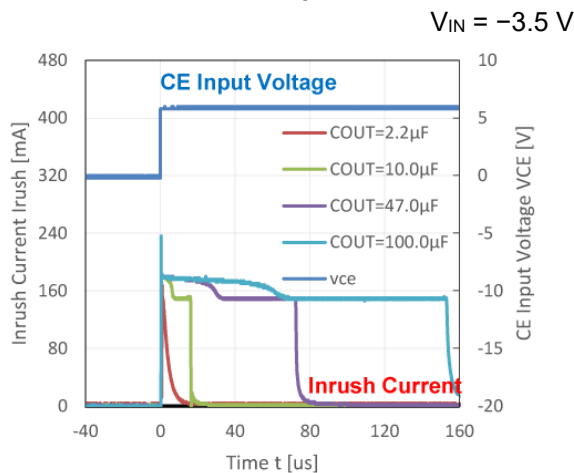
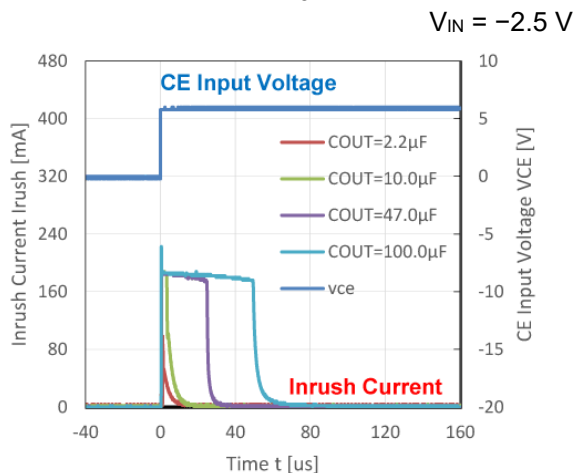
14) CE Pin Start-up Time ($C_{IN} = \text{Ceramic } 1.0\ \mu\text{F}$, $C_{OUT} = \text{Ceramic } 2.2\ \mu\text{F}$, $t_r = t_f = 0.5\ \mu\text{s}$, $T_a = 25^\circ\text{C}$)



15) CE Pin Shutdown Time (C_{IN} = Ceramic 1.0 μ F, C_{OUT} = Ceramic 2.2 μ F, $t_r = t_f = 0.5 \mu$ s, $T_a = 25^\circ$ C)

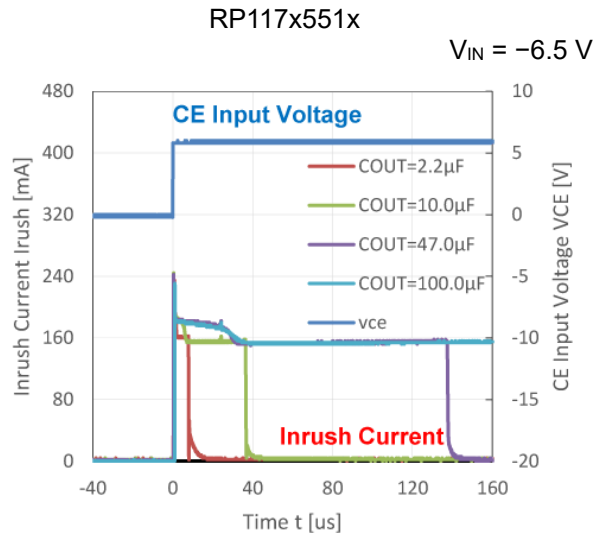


16) Inrush Current (C_{IN} = Ceramic 1.0 μ F, C_{OUT} = Ceramic 2.2 μ F, $t_r = t_f = 0.5 \mu$ s, $T_a = 25^\circ$ C)



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Equivalent Series Resistance (ESR) vs. Output Current

It is recommended that a ceramic type capacitor be used for this device. However, other types of capacitors having lower ESR can also be used. The relation between the output current (I_{OUT}) and the ESR of output capacitor is shown below.

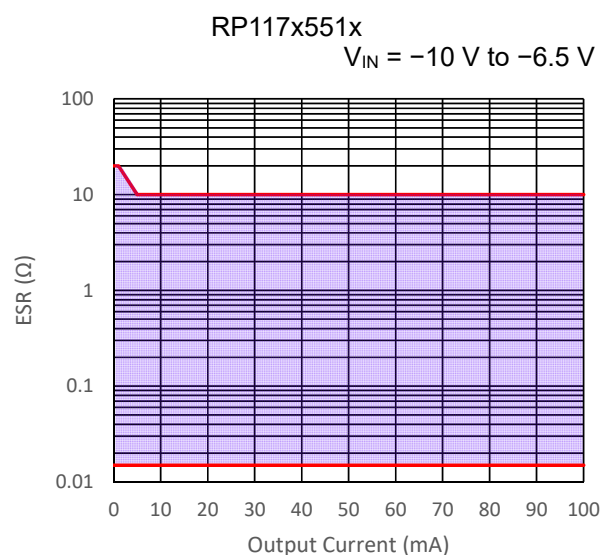
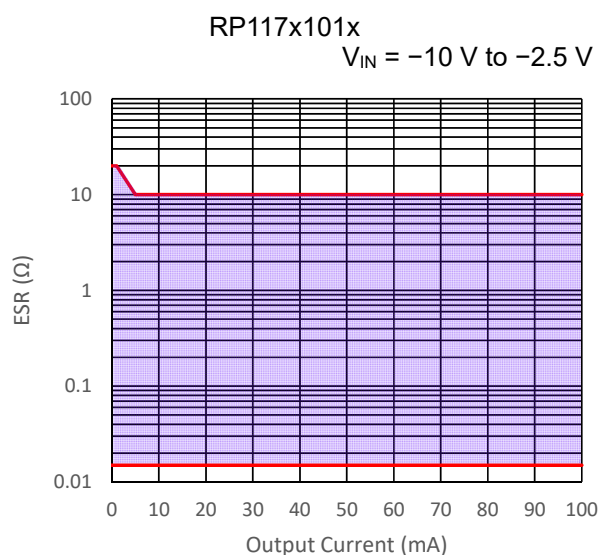
Measurement Conditions

Frequency Band: 10 Hz to 2 MHz

Ambient Temperature: -40°C to 85°C

Input Capacitor (C_{IN}): Ceramic, $1.0\ \mu\text{F}$

Output Capacitor (C_{OUT}): Ceramic, $2.2\ \mu\text{F}$



The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following measurement conditions are based on JEDEC STD. 51-7.

Measurement Conditions

Item	Measurement Conditions
Environment	Mounting on Board (Wind Velocity = 0 m/s)
Board Material	Glass Cloth Epoxy Plastic (Four-Layer Board)
Board Dimensions	76.2 mm × 114.3 mm × 0.8 mm
Copper Ratio	Outer Layer (First Layer): Less than 95% of 50 mm Square Inner Layers (Second and Third Layers): Approx. 100% of 50 mm Square Outer Layer (Fourth Layer): Approx. 100% of 50 mm Square
Through-holes	φ 0.2 mm × 14 pcs

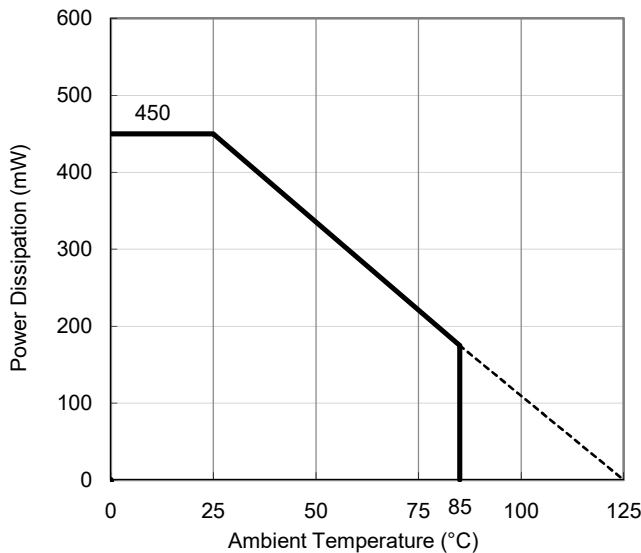
Measurement Result

(Ta = 25°C, Tjmax = 125°C)

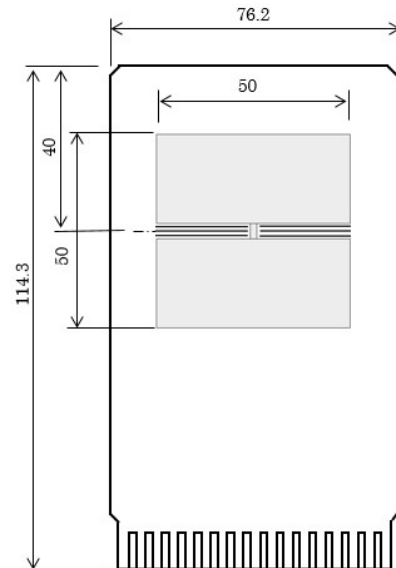
Item	Measurement Result
Power Dissipation	450 mW
Thermal Resistance (θ_{ja})	$\theta_{ja} = 218^{\circ}\text{C/W}$
Thermal Characterization Parameter (ψ_{jt})	$\psi_{jt} = 105^{\circ}\text{C/W}$

θ_{ja} : Junction-to-Ambient Thermal Resistance

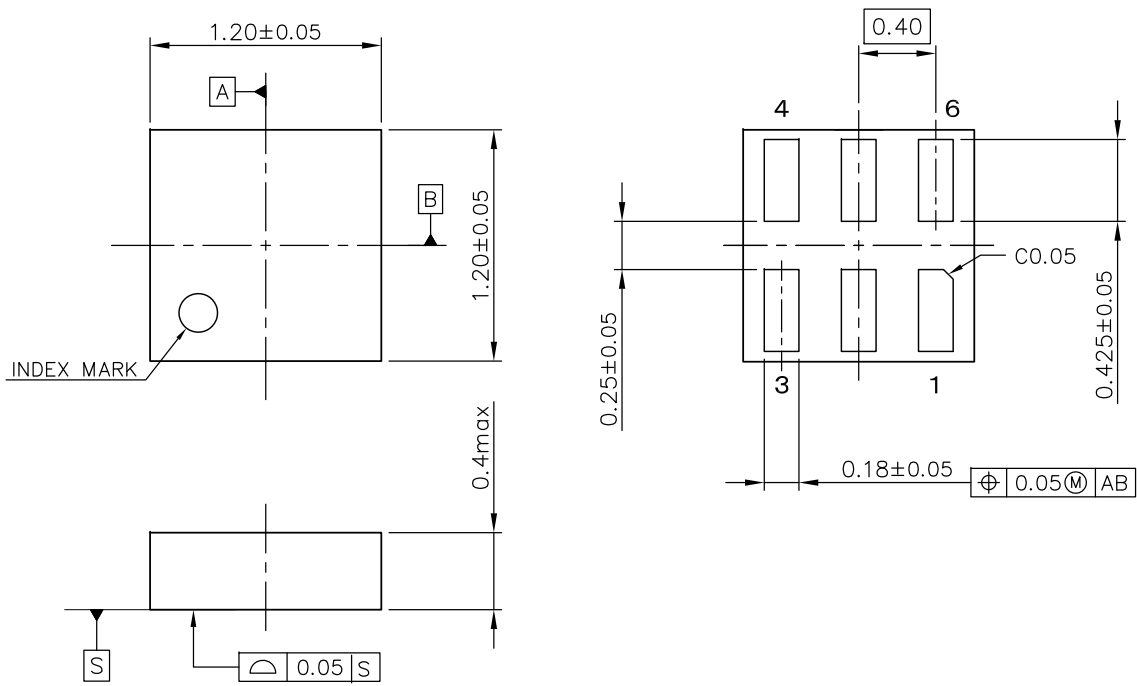
ψ_{jt} : Junction-to-Top Thermal Characterization Parameter



Power Dissipation vs. Ambient Temperature



Measurement Board Pattern



UNIT: mm

DFN(PLP)1212-6 Package Dimensions

The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following conditions are used in this measurement.

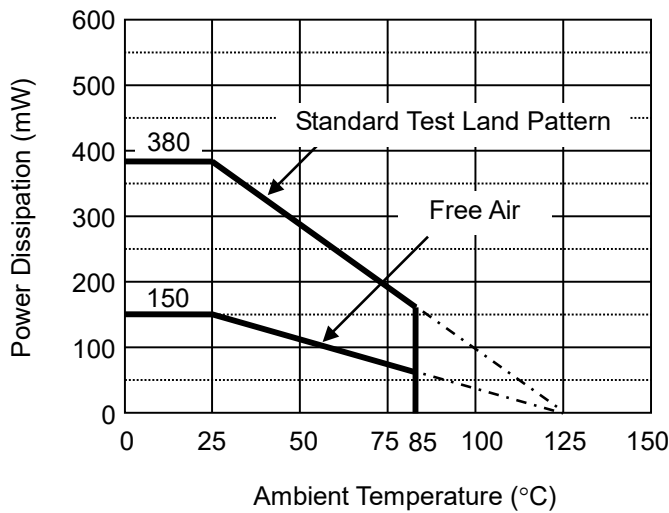
Measurement Conditions

	Standard Test Land Pattern
Environment	Mounting on Board (Wind Velocity = 0 m/s)
Board Material	Glass Cloth Epoxy Plastic (Double-Sided Board)
Board Dimensions	40 mm × 40 mm × 1.6 mm
Copper Ratio	Top Side: Approx. 50% Bottom Side: Approx. 50%
Through-holes	φ 0.5 mm × 44 pcs

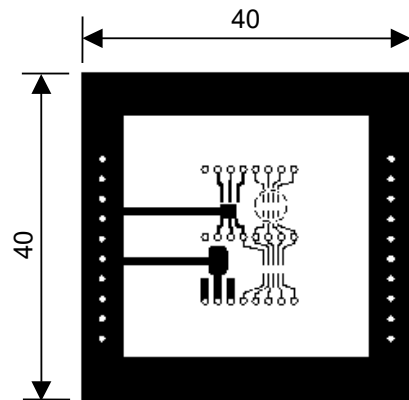
Measurement Result

(Ta = 25°C, Tjmax = 125°C)

	Standard Test Land Pattern	Free Air
Power Dissipation	380 mW	150 mW
Thermal Resistance	$\theta_{ja} = (125 - 25^\circ\text{C}) / 0.38\text{W} = 263^\circ\text{C/W}$ $\theta_{ja} = 75^\circ\text{C/W}$	$\theta_{ja} = (125 - 25^\circ\text{C}) / 0.15\text{W} = 667^\circ\text{C/W}$ -

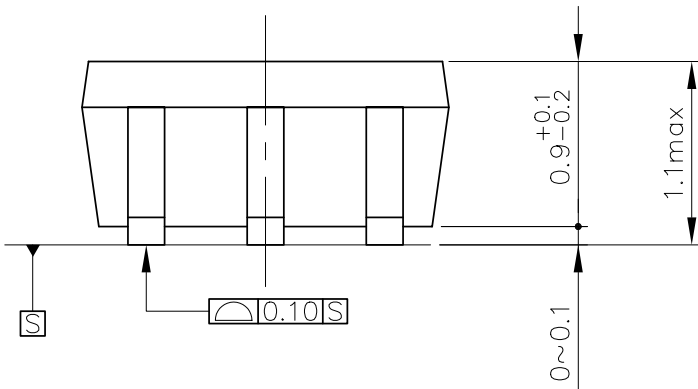
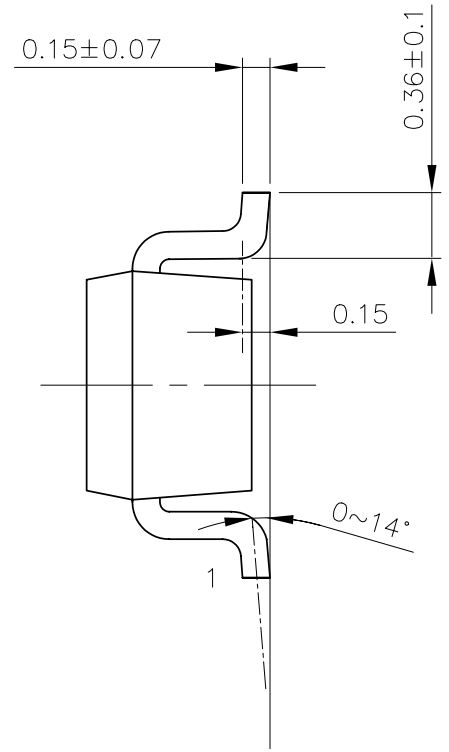
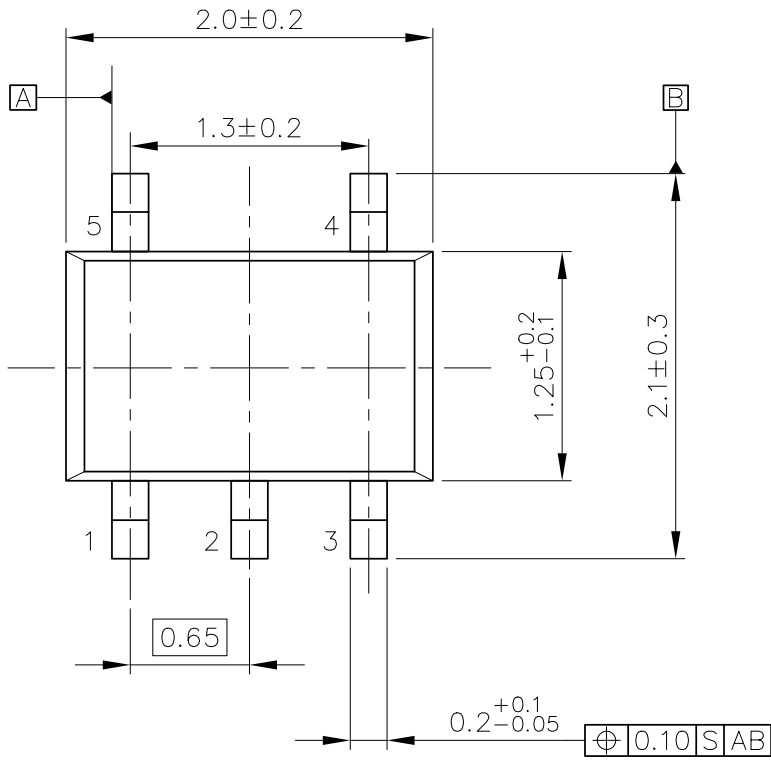


Power Dissipation vs. Ambient Temperature



○ IC Mount Area (mm)

Measurement Board Pattern



UNIT: mm

SC-88A Package Dimensions



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