NCD9830

8-Bit, 8-Channel ADC with I^2C Serial Interface

The NCD9830 is a two−wire serially programmable analog to digital converter. It can monitor 8 analog inputs to 8−bit resolution. Each channel is selected using the I^2C interface and can also be configured to be a single ended or differential type measurement.

Communication with the NCD9830 is accomplished via the I^2C interface which is compatible with industry standard protocols. Through this interface configuration of the NCD9830 is achieved. This allows the user to read the current measurement for the selected channel, change to an external reference and modify the measurement type (single ended or differential).

The NCD9830 is available in a 16−lead TSSOP package and operates over a wide supply range of 2.7 to 5.5 V.

Features

- 8−bit ADC
- 8 Single−ended Inputs/4 Differential Inputs
- 2.7 V to 5.5 V Operation
- Built in 2.5 V Reference
- 2 Address Selection Pins
- Low Power Consumption
- I^2C Compliant Interface − Standard, Fast and High Speed Modes
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

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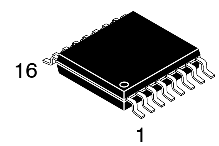
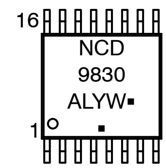
MARKING DIAGRAM



TSSOP−16
DT SUFFIX
CASE 948F



A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(*Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 15 of this data sheet.

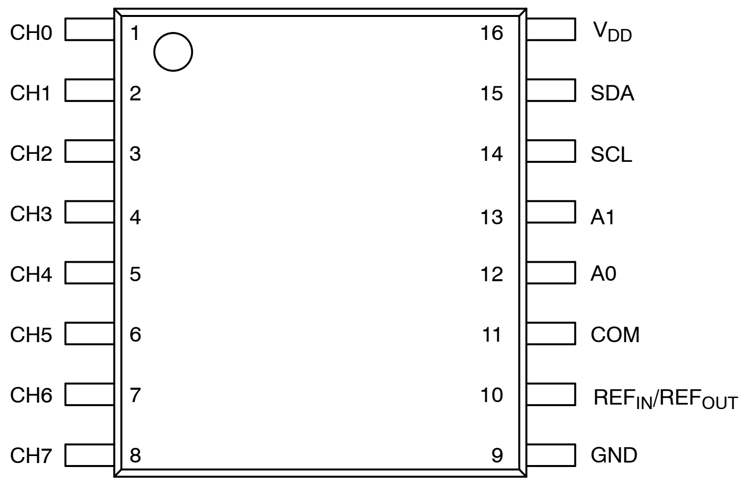


Figure 1. Pin Configuration (Top View)

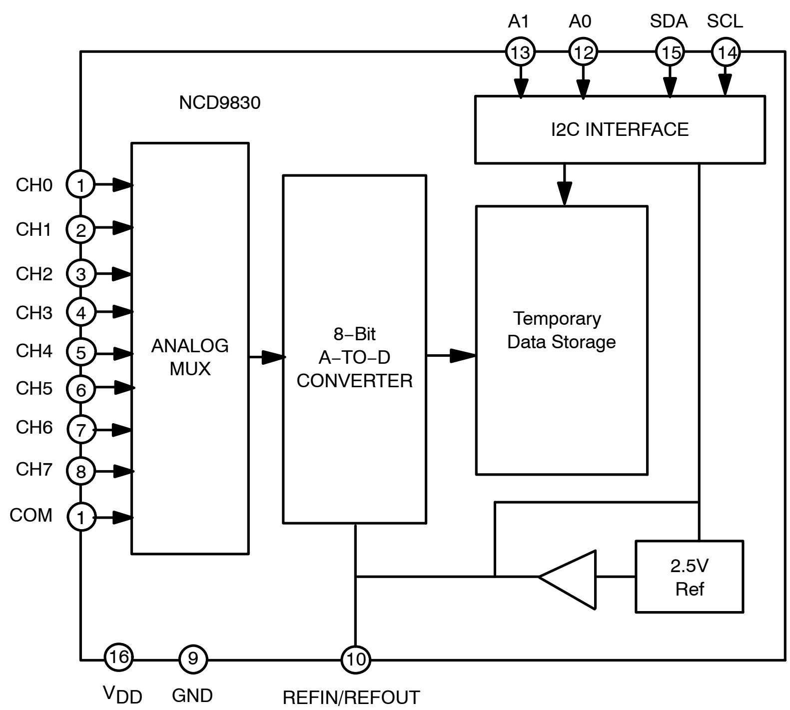


Figure 2. Functional Block Diagram of NCD9830

Table 1. PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Description
1	CH0	Analog Input.
2	CH1	Analog Input.
3	CH2	Analog Input.
4	CH3	Analog Input.
5	CH4	Analog Input.
6	CH5	Analog Input.
7	CH6	Analog Input.
8	CH7	Analog Input.
9	GND	Power Supply Ground.
10	REF_{IN} / REF_{OUT}	Internal 2.5 V reference or external reference input.
11	COM	Common to analog input channel (typically connected to GND).
12	A0	Functions as an I^2C address selection bit.
13	A1	Functions as an I^2C address selection bit.
14	SCL	Serial Clock Input. Open−drain pin; needs a pull−up resistor.
15	SDA	I^2C Serial Bi−directional Data Input/Output. Open−drain pin; needs a pull−up resistor.
16	V_{DD}	Positive Supply Voltage. Bypass to ground with a 0.1 μF bypass capacitor.

Table 2. ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (V_{DD})	V_{DD}	−0.3 to +6.5	V
Analog input voltage to GND		−0.3 to V_{DD} +0.3	V
Voltage on any pin (not analog inputs)		V_{DD}	V
Maximum Junction Temperature	$T_{J(max)}$	150.7	°C
Storage Temperature Range	T_{STG}	−65 to 160	°C
ESD Capability, Human Body Model (Note 1)	ESD_{HBM}	3	kV
ESD Capability, Machine Model (Note 1)	ESD_{MM}	150	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.

Table 3. OPERATING RANGES

Rating	Symbol	Min	Max	Unit
Operating Supply Voltage	V_{DD}	2.7	5.5	V
Operating Ambient Temperature Range	T_A	−40	125	°C

2. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.

Table 4. ELECTRICAL CHARACTERISTICS ±2.7 V

T_A = −40°C to +125°C, V_{DD} = 2.7 V, V_{REF} = 2.5 V, SCL Freq = 3.4 MHz, unless otherwise noted.

Parameter	Test Conditions	Min	Typ	Max	Unit
ANALOG INPUT					
Full scale input range	Positive and negative input	0		V_{REF}	V
Max input range	Positive input	−0.2		V_{DD} + 0.2	V
	Negative input	−0.2		0.2	V
Capacitance			25		pF
Leakage Current			±1		μA
SYSTEM PERFORMANCE					
No Missing Codes		8			Bits
Integral Linearity Error			±0.1	±0.5	LSB
Differential Linearity Error			±0.1	±0.5	LSB
Offset Error			+0.5	+1	LSB
Offset Error Match			±0.05	±0.25	LSB
Gain Error			±0.1	±0.5	LSB
Gain Error Match			±0.05	±0.25	LSB
Noise			100		μVRMS
Power Supply Rejection			72		dB
SAMPLING DYNAMICS					
Throughput Frequency	High speed mode: SCL = 3.4 MHz			70	kSPS
	Fast mode: SCL = 400 kHz			10	kSPS
	Standard mode: SCL = 100 kHz			2.5	kSPS
Conversion Time			5		μs
AC ACCURACY					
Total Harmonic Distortion	V_{IN} = 2.5 Vpp at 1 kHz		−72		dB
Signal−to−Ratio	V_{IN} = 2.5 Vpp at 1 kHz		50		dB
Signal−to−(Noise+Distortion) Ratio	V_{IN} = 2.5 Vpp at 1 kHz		49		dB
Spurious Free Dynamic Range	V_{IN} = 2.5 Vpp at 1 kHz		68		dB
Channel to channel isolation			90		dB
VOLTAGE REFERENCE OUTPUT					
Range		2.475	2.5	2.525	V
Internal Reference Drift			15		ppm/°C
Output Impedance	Internal reference ON		700		Ω
	Internal reference OFF		1		GΩ
Quiescent Current	Internal Reference ON, SCL and SDA pulled HIGH		850		μA
VOLTAGE REFERENCE INPUT					
Range		0.05		V_{DD}	V
Resistance			1		GΩ
Current Drain	High Speed Mode: SCL = 3.4 MHz		20		μA
DIGITAL INPUT/OUTPUT					

Table 4. ELECTRICAL CHARACTERISTICS ±2.7 V

T_A = −40°C to +125°C, V_{DD} = 2.7 V, V_{REF} = 2.5 V, SCL Freq = 3.4 MHz, unless otherwise noted.

Parameter		Test Conditions	Min	Typ	Max	Unit
DIGITAL INPUT/OUTPUT						
Logic Levels:	V_{IH}		0.7 x V_{DD}		V_{DD} + 0.5	V
	V_{IL}		0		0.3 x V_{DD}	V
	V_{OL}	Minimum 3 mA sink current			0.4	V
Input Leakage:	I_{IH}	$V_{IH} = V_{DD} + 0.5$			10	μA
	I_{IL}	V_{IL} = 0 V	−10			μA
POWER SUPPLY REQUIREMENTS						
V_{DD}			2.7		3.6	V
Quiescent Current		High speed mode: SCL = 3.4 MHz		225	320	μA
		Fast mode: SCL = 400 kHz		100		μA
		Standard mode: SCL = 100 kHz		60		μA
Power Dissipation		High speed mode: SCL = 3.4 MHz		675	1000	μW
		Fast mode: SCL = 400 kHz		300		μW
		Standard mode: SCL = 100 kHz		180		μW
Power Down Mode (Wrong address selected)		High speed mode: SCL = 3.4 MHz		70		μA
		Fast mode: SCL = 400 kHz		25		μA
		Standard mode: SCL = 100 kHz		6		μA
Full Power Down		SCL, SDA pulled HIGH		400	3000	nA

Table 5. ELECTRICAL CHARACTERISTICS ±5 V

T_A = −40°C to +125°C, V_{DD} = 5 V, V_{REF} = 5 V (external), SCL Freq = 3.4 MHz, unless otherwise noted.

Parameter	Test Conditions	Min	Typ	Max	Unit
ANALOG INPUT					
Full scale input range	Positive and negative input	0		V_{REF}	V
Max input range	Positive input	−0.2		V_{DD} + 0.2	V
	Negative input	−0.2		0.2	V
Capacitance			25		pF
Leakage Current			±1		μA
SYSTEM PERFORMANCE					
No Missing Codes		8			Bits
Integral Linearity Error			±0.1	±0.5	LSB
Differential Linearity Error			±0.1	±0.5	LSB
Offset Error			+0.5	+1	LSB
Offset Error Match			±0.05	±0.25	LSB
Gain Error			±0.1	±0.5	LSB
Gain Error Match			±0.05	±0.25	LSB
Noise			100		μVRMS
Power Supply Rejection			72		dB

Table 5. ELECTRICAL CHARACTERISTICS ±5 V

T_A = −40°C to +125°C, V_{DD} = 5 V, V_{REF} = 5 V (external), SCL Freq = 3.4 MHz, unless otherwise noted.

Parameter		Test Conditions	Min	Typ	Max	Unit
SAMPLING DYNAMICS						
Throughput Frequency		High speed mode: SCL = 3.4 MHz			70	kSPS
		Fast mode: SCL = 400 kHz			10	kSPS
		Standard mode: SCL = 100 kHz			2.5	kSPS
Conversion Time				5		μs
AC ACCURACY						
Total Harmonic Distortion		V_{IN} = 2.5 Vpp at 1 kHz		−72		dB
Signal−to−Ratio		V_{IN} = 2.5 Vpp at 1 kHz		50		dB
Signal−to−(Noise+Distortion) Ratio		V_{IN} = 2.5 Vpp at 1 kHz		49		dB
Spurious Free Dynamic Range		V_{IN} = 2.5 Vpp at 1 kHz		68		dB
Channel to channel isolation				90		dB
VOLTAGE REFERENCE OUTPUT						
Range			2.475	2.5	2.525	V
Internal Reference Drift				15		ppm/°C
Output Impedance		Internal reference ON		700		Ω
		Internal reference OFF		1		GΩ
Quiescent Current		Internal Reference ON, SCL and SDA pulled HIGH		1300		μA
VOLTAGE REFERENCE INPUT						
Range			0.05		V_{DD}	V
Resistance				1		GΩ
Current Drain		High Speed Mode: SCL = 3.4 MHz		20		μA
DIGITAL INPUT/OUTPUT						
Logic Levels:	V_{IH}		0.7 x V_{DD}		V_{DD} + 0.5	V
	V_{IL}		0		0.3 x V_{DD}	V
	V_{OL}	Minimum 3 mA sink current			0.4	V
Input Leakage:	I_{IH}	V_{IH} = V_{DD} + 0.5			10	μA
	I_{IL}	V_{IL} = 0 V	−10			μA
POWER SUPPLY REQUIREMENTS						
V_{DD}			4.75		5.25	V
Quiescent Current		High speed mode: SCL = 3.4 MHz		750	1000	μA
		Fast mode: SCL = 400 kHz		300		μA
		Standard mode: SCL = 100 kHz		150		μA
Power Dissipation		High speed mode: SCL = 3.4 MHz		3.75	5	mW
		Fast mode: SCL = 400 kHz		1.5		mW
		Standard mode: SCL = 100 kHz		0.75		mW
Power Down Mode (Wrong address selected)		High speed mode: SCL = 3.4 MHz		400		μA
		Fast mode: SCL = 400 kHz		150		μA
		Standard mode: SCL = 100 kHz		35		μA
Full Power Down		SCL, SDA pulled HIGH TA = −40°C to 85°C TA = −40°C to 125°C		 400 400	 3000 3500	nA

TIMING CHARACTERISTICS

Table 6. I^{2}C TIMING

Parameter (Note 3)	Symbol	Conditions	Min	Max	Unit
Clock Frequency	f_{SCL}	Standard Mode Fast Mode High speed Mode (100 pF) High speed Mode (400 pF)	10	100 400 3.4 1.7	kHz kHz MHz MHz
Bus Free Time	t_{BUF}	Standard Mode Fast Mode	4.7 1.3		μs μs
Start Hold Time (Note 4)	$t_{HD;STA}$	Standard Mode Fast Mode High speed Mode	4.0 600 160		μs ns ns
SCL Low Time	t_{LOW}	Standard Mode Fast Mode High speed Mode (100 pF) High speed Mode (400 pF)	4.7 1.3 160 320		μs μs ns ns
SCL High Time	t_{HIGH}	Standard Mode Fast Mode High speed Mode (100 pF) High speed Mode (400 pF)	4.0 600 60 120		μs ns ns ns
Start Setup Time	$t_{SU;STA}$	Standard Mode Fast Mode High speed Mode	4.7 600 160		μs ns ns
Data Setup Time (Note 5)	$t_{SU;DAT}$	Standard Mode Fast Mode High speed Mode	250 100 10		ns
Data Hold Time (Note 6)	$t_{HD;DAT}$	Standard Mode Fast Mode High speed Mode (100 pF) High speed Mode (400 pF)	0 0 0 0	3.45 0.9 70 150	μs μs ns ns
SCL Rise Time	t_{RCL}	Standard Mode Fast Mode High speed Mode (100 pF) High speed Mode (400 pF)	 $20+0.1C_B$ 10 20	1000 300 40 80	ns ns ns ns
SCL Rise Time (after repeated start)	t_{RCL1}	Standard Mode Fast Mode High speed Mode (100 pF) High speed Mode (400 pF)	 $20+0.1C_B$ 10 20	1000 300 80 160	ns ns ns ns
SCL Fall Time	t_{FCL}	Standard Mode Fast Mode High speed Mode (100 pF) High speed Mode (400 pF)	 $20+0.1C_B$ 10 20	300 300 40 80	ns ns ns ns
SDA Rise Time	t_{RDA}	Standard Mode Fast Mode High speed Mode (100 pF) High speed Mode (400 pF)	 $20+0.1C_B$ 10 20	1000 300 80 160	ns ns ns ns
SDA Fall Time	t_{FDA}	Standard Mode Fast Mode High speed Mode (100 pF) High speed Mode (400 pF)	 $20+0.1C_B$ 10 20	300 300 80 160	ns ns ns ns
Stop Setup Time	$t_{SU;STO}$	Standard Mode Fast Mode High speed Mode	0.4 600 160		μs ns ns
Capacitive load	C_B			400	pF

3. Guaranteed by design, but not production tested.
4. Time from 10% of SDA to 90% of SCL.
5. Time for 10%or 90% of SDA to 10% of SCL.
6. A device must internally provide a hold time of at least 300 ns for the SDA signal to bridge the undefined region of the falling edge of SCL.

Table 6. I²C TIMING

Parameter (Note 3)	Symbol	Conditions	Min	Max	Unit
Glitch Immunity	t_{SP}	Fast Mode High−speed Mode		50 10	ns ns
Noise margin at high level	V_{NH}	Standard Mode Fast Mode High speed Mode	0.2 V_{DD}		V
Noise margin at low level	V_{NL}	Standard Mode Fast Mode High speed Mode	0.1 V_{DD}		V

3. Guaranteed by design, but not production tested.
4. Time from 10% of SDA to 90% of SCL.
5. Time for 10%or 90% of SDA to 10% of SCL.
6. A device must internally provide a hold time of at least 300 ns for the SDA signal to bridge the undefined region of the falling edge of SCL.

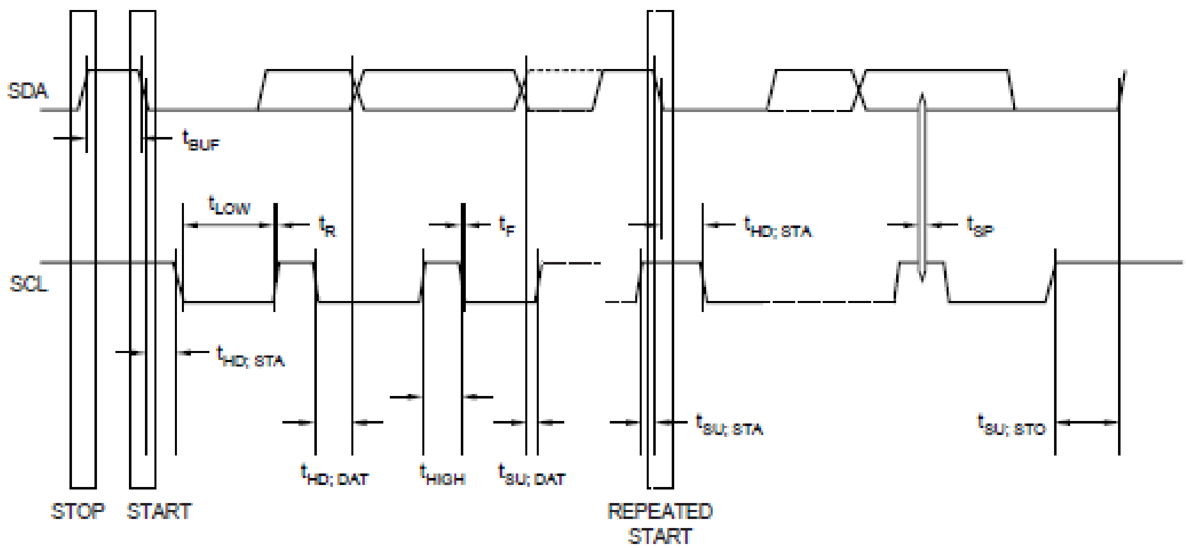


Figure 3. Serial Interface Timing

TYPICAL CHARACTERISTICS

T_A = +25°C, V_{DD} = +2.7 V, V_{REF} = External 2.5 V, f_{SAMPLE} = 50 kHz, unless otherwise stated.

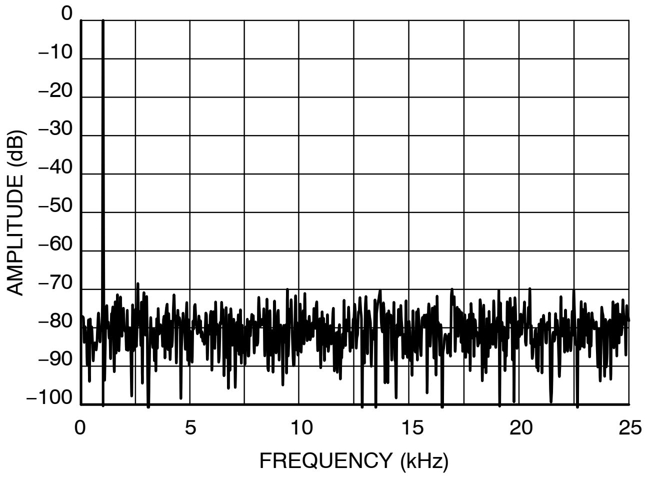


Figure 4. FFT vs. Frequency

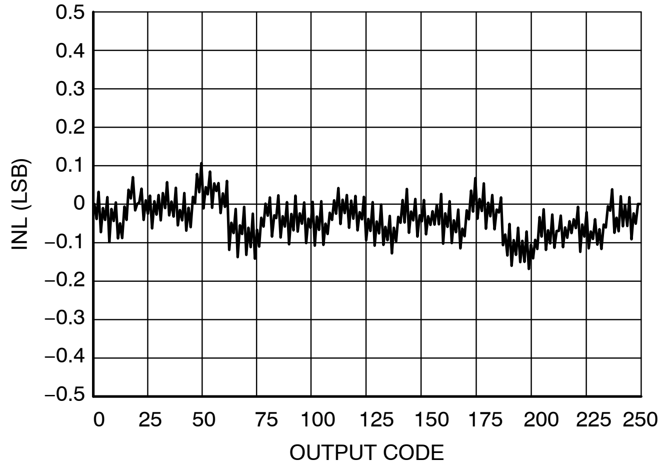


Figure 5. INL vs. Code (EXT REF)

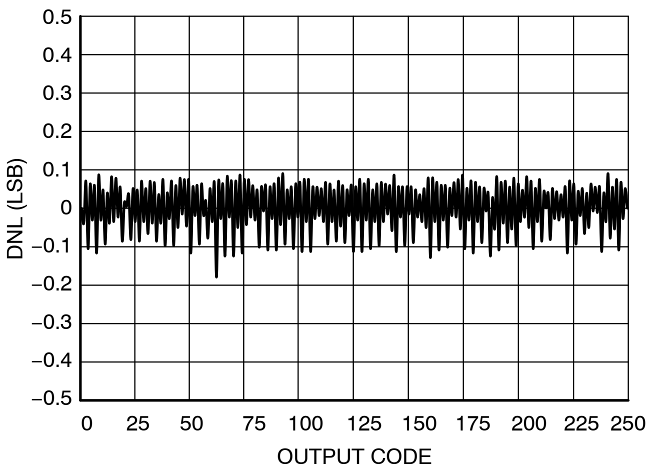


Figure 6. DNL vs. Code (EXT REF)

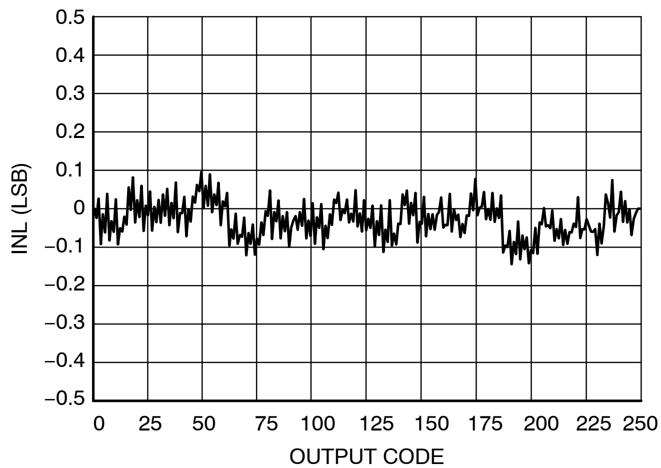


Figure 7. INL vs. Code (INT REF)

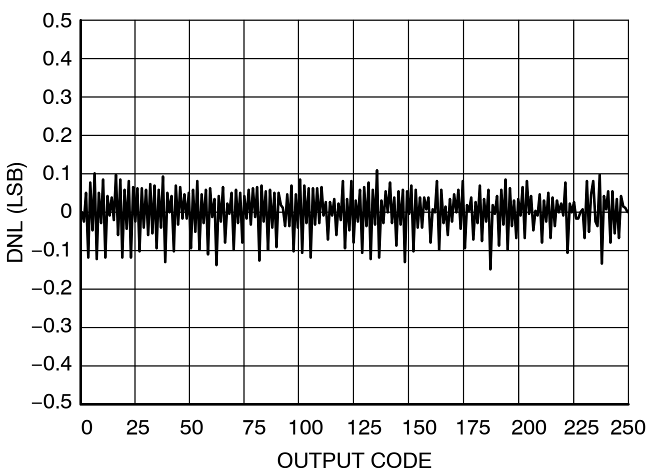


Figure 8. DNL vs. Code (INT REF)

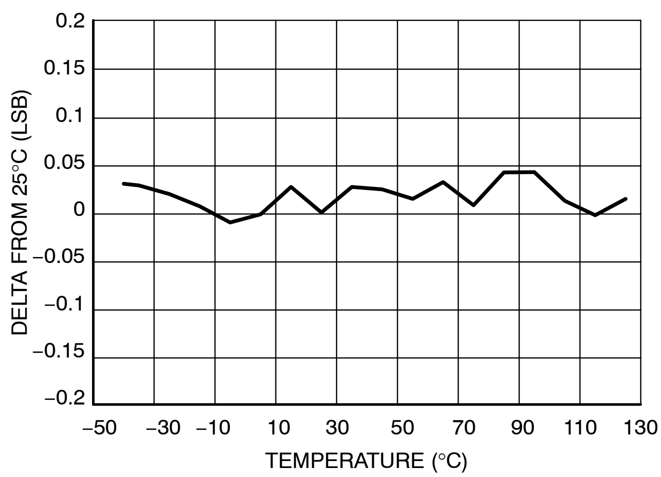


Figure 9. Change in Offset vs. Temperature

TYPICAL CHARACTERISTICS

T_A = +25°C, V_{DD} = +2.7 V, V_{REF} = External 2.5 V, f_{SAMPLE} = 50 kHz, unless otherwise stated.

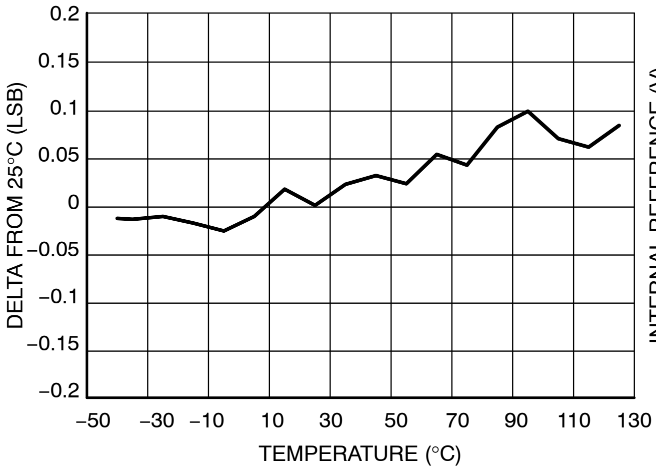


Figure 10. Change in Gain vs. Temperature

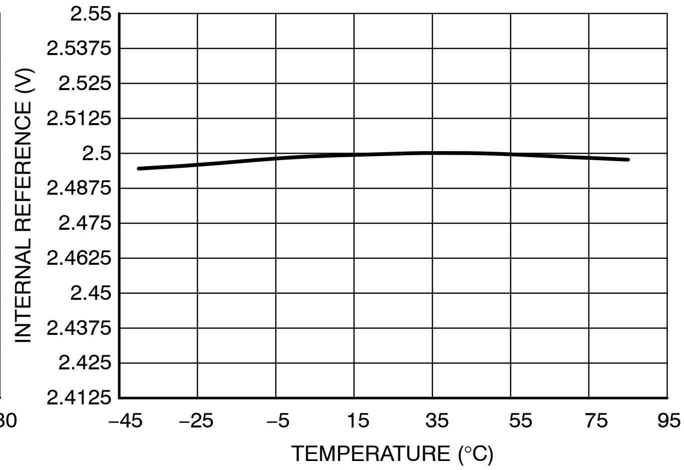


Figure 11. Internal V_{REF} vs. Temperature

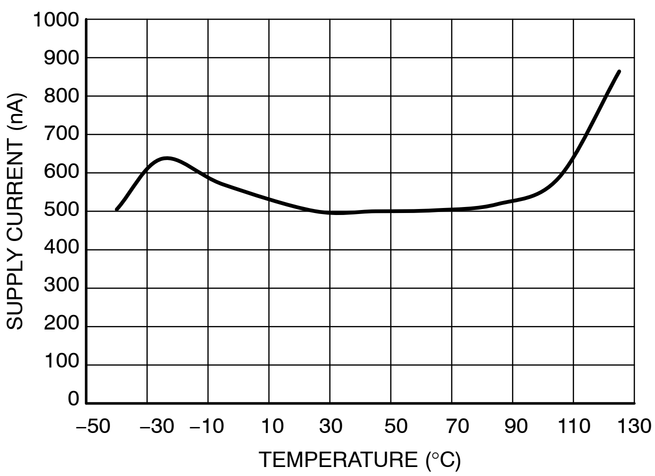


Figure 12. Power−Down Supply Current vs. Temperature

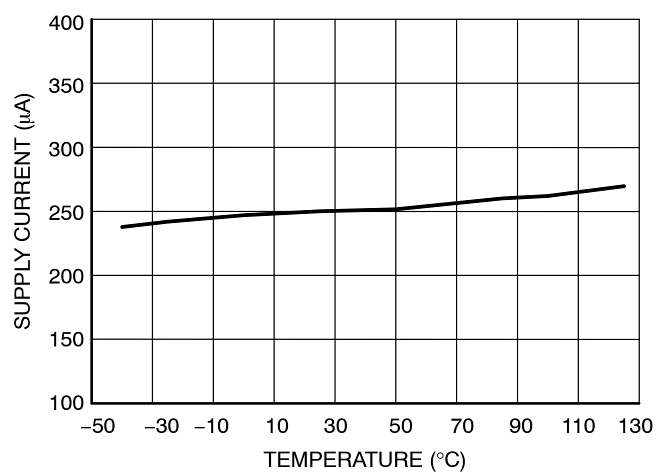


Figure 13. Supply Current vs. Temperature

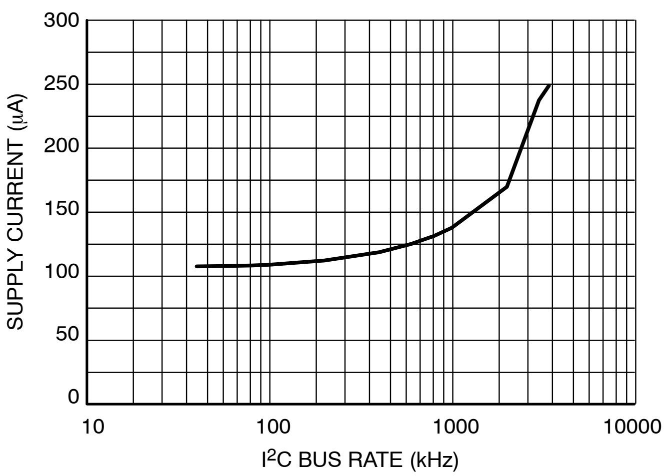


Figure 14. Supply Current vs. I^2C Bus Rate

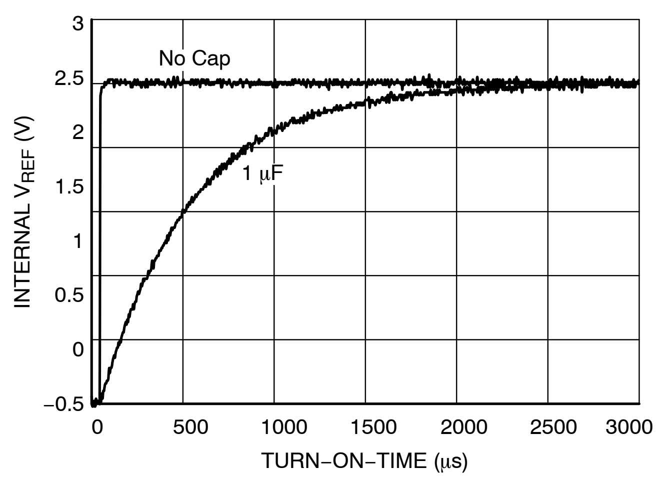


Figure 15. Internal V_{REF} vs. Turn−ON Time

CIRCUIT INFORMATION

OPERATION

The NCD9830 is a low power successive approximation ADC with a built in 8 channel multiplexer and 8 bit resolution. The 8 bit resolution assures high noise immunity and fast digitization that makes this device suitable for medium to high speed applications. The device internal circuitry operates at speed higher than the conversion time of the device because of the binary algorithm used. The algorithm is based on approximating the input signal by comparing with successive analog signal generated from the built in DAC.

The device can be operated at supply voltages of 2.7 V and 5 V. The liberty of supply voltage variation must be used with appropriate reference voltage selection. The NCD9830 internal DAC can be configured with an externally (50 mV −5 V) supplied or an internally internally generated reference voltage of 2.5 V. However, to avail full dynamic range an external reference of 5 V must be used while operating the device at 5 V supply voltage. The internal 2.5 V reference voltage is sufficient for full dynamic range while operating the device at 2.7 V.

The value of each output bit is evaluated on the basis of output of the comparator. The converter requires N conversion periods to give N bit digital output of the input analog signal. The SAR register stores the digital equivalent bits of the input analog signal and can be read by the master device using an I^{2}C interface. The main building block of the device are

i. Digital to Analog Converter

ii. Comparator

iii. Digital Logic

Digital to Analog Converter

A charge scaling DAC is used due to its compatibility with the switch capacitor circuits. The DAC operation consists of two phases called acquisition phase and the conversion phase. The acquisition phase is analogous to sample and hold circuit while the conversion phase is the process of conversion of the internal digital word in to an analog output.

Acquisition phase: The top plates of all the capacitors on the array are connected to the ground and the bottom plates are connected to the applied voltage Vin. Thus there is a charge proportional to input voltage on the capacitor array. After acquisition the top and bottom plates are disconnected from their respective connections.

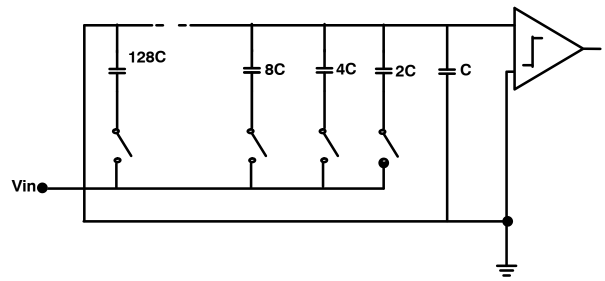


Figure 16. The Acquisition Phase of a Typical ADC

Conversion Phase: The conversion phase is administered by a two phase non overlapping clock with phases ϕ_1 and ϕ_2 respectively.

During ϕ_1 the bottom plates of all the capacitors are grounded i.e the top plates of all the capacitors are now Vin times higher than the ground. As the conversion process starts the digital control sets all the bits zero except the MSB in the SAR register. During the ϕ_2 the capacitors associated with MSB is connected to VREF while others are connected to ground. In this way the DAC generates analog voltage of magnitude VREF/2. The analog output of DAC is compared with the input analog signal. The digital control logic sets the MSB to 1 if comparator output is high and 0 otherwise. Thus the first step of SAR algorithm decides whether the input signal is greater or less than VREF/2. The approximation process is then run again with the MSB in its proven value and the next lower bit is set to 1. This gives a general direction path and the remaining approximations will converge the output in this direction.

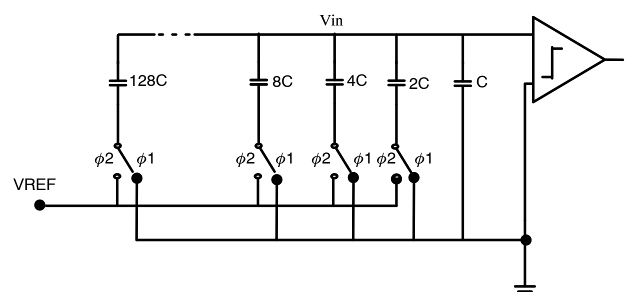


Figure 17. The Conversion Phase of a Typical ADC

Comparator

A switch capacitor comparator is used to alleviate the effects of input offset voltage. The issue of charge injection is controlled by using fully differential topology.

Digital Logic

The function of the digital logic is to generate the binary word to be compared with the input analog signal in each approximation cycle. The result of each approximation cycle is stored in the SAR register. In short the digital logic determines the value of each output bit in a sequential manner base don the output of the comparator.

ANALOG CHANNELS

The analog inputs (CH0−CH7) are multiplexed into the on−chip successive approximation, analog−digital converter. This has a resolution of 8 bits. The basic input range is 0 V to V_{DD}. When not performing a conversion or being addressed, the ADC core is powered off to preserve power. The internal clock is also powered off.

REFERENCE

The NCD9830 can operate with either its own internal 2.5 V reference or an externally supplied reference. If using a 5 V supply then an external 5 V reference needs to be used in order to provide the full range for the 0 to V_{DD} analog input channels. The internal 2.5 V reference will still be sufficient to provide full dynamic range for the 0 to V_{DD} analog input channels.

SERIAL BUS INTERFACE

Control of the NCD9830 is carried out via the I^2C bus. The NCD9830 is connected to this bus as a slave device, under the control of a master device. The NCD9830 has a 7−bit serial bus address. The upper 5 bits of the device address are 10010. The lower 2 bits are set by pins 12 and 13. Table 7 shows the 7−bit address for each of the pin states. The address pins can be connected to V_{DD} or GND and the address is set by the state of these pins on power up.

The logic of this address pin is monitored on power up on the first I^2C transaction, more precisely, on the low−to−high transition at the beginning of the eighth SCL pulse.

The ability to make hardwired changes to the I^2C slave address allows the user to avoid conflicts with other devices sharing the same I^2C address, for example, if more than one NCD9830 is used in a system. NCD9830 is compatible to all three operating modes of I^2C interface i.e Standard (100 kHz), Fast (400 kHz) and high speed (3.4 MHz) modes.

Table 7. I^2C ADDRESS OPTIONS

A1	A0	Address
0	0	0x48
0	1	0x49
1	0	0x4A
1	1	0x4B

The serial bus protocol operates as follows:

1. The master initiates data transfer by establishing a START condition, defined as a high−to−low transition on the serial data line SDA while the serial clock line, SCL, remains high. This indicates that an address/data stream will follow. All slave peripherals connected to the serial bus respond to the START condition, and shift in the next eight bits, consisting of a 7−bit address (MSB first) plus an R/W bit, which determines the direction of the data transfer, i.e., whether data will be written to or read from the slave device. The peripheral whose address corresponds to the transmitted address responds by pulling the data line low during the low period before the ninth clock pulse, known as the Acknowledge Bit. All other devices on the bus now remain idle while the selected device waits for data to be read from or written to it. If the R/W bit is a 0, the master will write to the slave device. If the R/W bit is a 1, the master will read from the slave device.
2. Data is sent over the serial bus in sequences of nine clock pulses, eight bits of data followed by an Acknowledge Bit from the slave device. Transitions on the data line must occur during the low period of the clock signal and remain stable during the high period, as a low−to−high transition when the clock is high may be interpreted as a STOP signal. The number of data bytes that can be transmitted over the serial bus in a single READ or WRITE operation is limited only by what the master and slave devices can handle.
3. When all data bytes have been read or written, stop conditions are established. In WRITE mode, the master will pull the data line high during the 10th clock pulse to assert a STOP condition. In READ mode, the master device will override the acknowledge bit by pulling the data line high during the low period before the ninth clock pulse. This is known as No Acknowledge. The master will then take the data line low during the low period before the tenth clock pulse, then high during the tenth clock pulse to assert a STOP condition.

COMMAND BYTE

NCD9830 can be operated in different modes depending on the internal power state of different circuit sections and input configuration (single ended or differential). Command byte also contains three channel select C_x bits of the internal eight channel multiplexer. The format of the command byte is as follows

The 8 bit command code is used to configure:

- Either a single ended or differential measurement
- Channel to be selected
- Power down/reference options

MSB	6	5	4	3	2	1	0
SD	C2	C1	C0	PD1	PD0	x	x

Bit 7: SD − this configures the type of input to be used. If set to 0 then the device performs a differential measurement. If set to 1 then a single ended measurement is made.

Bit 6−4: C2−C0 − these are the channel selection bits. See Channel Selector table below for more detail.

Bit 3−2: PD1−PD0 − these bits let the use select whether the ADC is powered on, off and whether the internal reference is to be used or the external one. See Power Down Selection Table 8 for more detail.

Table 8. POWER DOWN SELECTION

PD1	PD0	Description
0	0	Power down between ADC conversions
0	1	Internal reference OFF, ADC ON
1	0	Internal reference ON, ADC OFF
1	1	Internal reference ON. ADC ON

Table 9. CHANNEL SELECTOR

CHANNEL SELECTION CONTROL												
SD	C2	C1	C0	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7	COM
0	0	0	0	+IN	−IN	–	–	–	–	–	–	–
0	0	0	1	–	–	+IN	−IN	–	–	–	–	–
0	0	1	0	–	–	–	–	+IN	−IN	–	–	–
0	0	1	1	–	–	–	–	–	–	+IN	−IN	–
0	1	0	0	−IN	+IN	–	–	–	–	–	–	–
0	1	0	1	–	–	−IN	+IN	–	–	–	–	–
0	1	1	0	–	–	–	–	−IN	+IN	–	–	–
0	1	1	1	–	–	–	–	–	–	−IN	+IN	–
1	0	0	0	+IN	–	–	–	–	–	–	–	−IN
1	0	0	1	–	–	+IN	–	–	–	–	–	−IN
1	0	1	0	–	–	–	–	+IN	–	–	–	−IN
1	0	1	1	–	–	–	–	–	–	+IN	–	−IN
1	1	0	0		+IN	–	–	–	–	–	–	−IN
1	1	0	1	–	–	–	+IN	–	–	–	–	−IN
1	1	1	0	–	–	–	–	–	+IN	–	–	−IN
1	1	1	1	–	–	–	–	–	–	–	+IN	−IN

INITIATING CONVERSIONS

Communication in Standard/Fast Mode

Communication in standard/fast mode corresponds to a clock speed of 100/400 kHz. The device address is sent over the bus followed by R/W set to 0. This is followed by the Command byte. If the Command byte is correct the device initiates the conversion cycle by turning on the converter circuit after it receives the channel selection bits (SD, C_2-C_0) of the Command byte. After receiving the Command byte the NCD 9830 sends an acknowledge bit. The device is now ready to be read by the master.

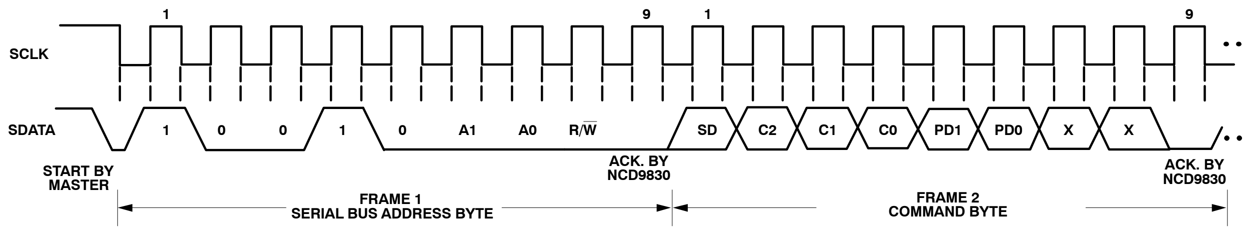


Figure 18. Write Addressing the Device to Write the Command Byte

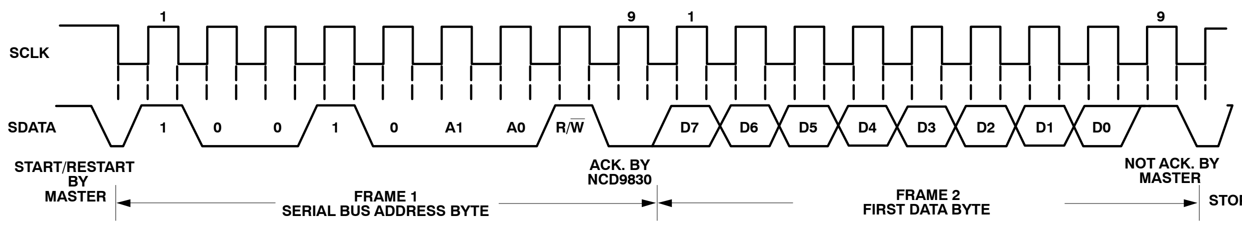


Figure 19. Conversation between Master and NCD9830 in Standard/Fast Mode

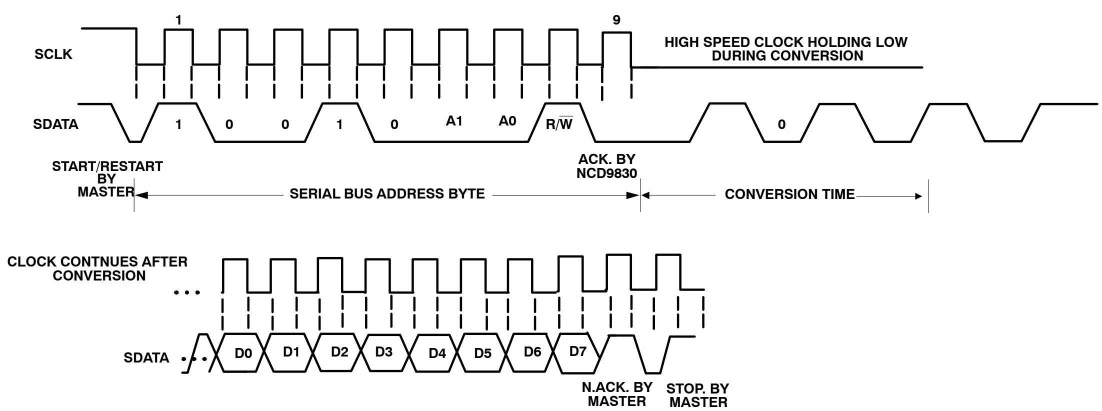


Figure 20. Conversation Between Master and NCD9830 in High Speed Mode

During read operation the device address is sent over the bus followed by R/W set to 1 followed by the acknowledge bit from the slave .Data can be read from the device in the form of a 8 bit byte. The MSB of the data word is D_7 and LSB is D_0.

Communication in High Speed Mode

Communication in high speed mode corresponds to a clock speed of 3.4 MHz. Master initiates a high speed master code that change the mode from standard/fast to high speed. The high speed master code format is as follows:

START	0	0	0	0	1	X	X	X	N.ACK

The START condition bit is initiated by master and N.ACK is initiated by NCD9830. The master code must be run in fast mode to enter in the high speed mode.

High speed operation does not give enough time span for a conversion to be completed between the start condition initiated by the master and the read cycle. Therefore, in high speed mode NCD9830 stretches the clock at low level after the read cycle is initiated by the master until the conversion is complete. Master can decide to remain in high speed mode by initiating a RESTART condition instead of STOP at the end of read sequence. A STOP bit at the end of read cycle changes the mode back to the standard/fast. A typical high speed read operation is shown in Figure 20.

Reference Voltage Selection

The internal reference can be turned ON or OFF depending on the Command byte bit PD_1 status.

When the device turns on for the first time the internal reference is OFF. Proper settling time must be allowed while switching any reference (external or internal) ON or OFF before any conversion is initiated. Depending on the I^2C operation mode (standard, fast or high speed) the settling time would vary.

LAYOUT CONSIDERATIONS

Digital boards are electrically noisy environments, and the NCD9830 SAR architecture is sensitive to power supply transients, reference voltage variation and other noise sources in the circuit. Any sudden transient spike can affect the accuracy of over all conversion result. So care must be taken to minimize noise induced at the device inputs. Take the following precautions:

- Place a 0.1 μF bypass capacitor close to the V_{DD} pin. In extremely noisy environments, where the impedance between the V_{DD} and the power supply is high a bigger capacitor with capacitance value from 1−10 μF must be used.
- Extra care must be taken while using external reference voltage for the device. Using a 5 V external reference voltage may require to connect the I/O REF pin directly to V_{DD}. Any transient glitches and spikes will induce a lot of noise in the reference voltage that would compromise the overall performance of the ADC. Appropriate measures must be taken to avoid pollution of reference voltage. Place the component far from the microprocessor or any other digital circuitry to avoid high frequency noise injection in the analog portions of ADC. A clean analog ground must be used with a dedicated analog ground plane

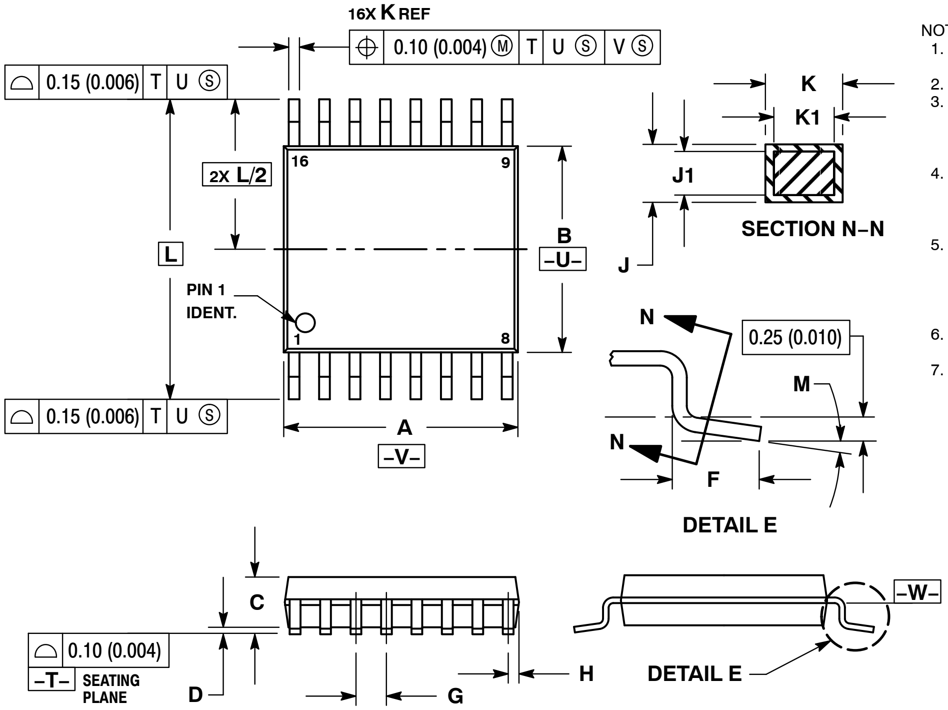
ORDERING INFORMATION

Device	Package	Shipping†
NCD9830DBR2G	TSSOP−16 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

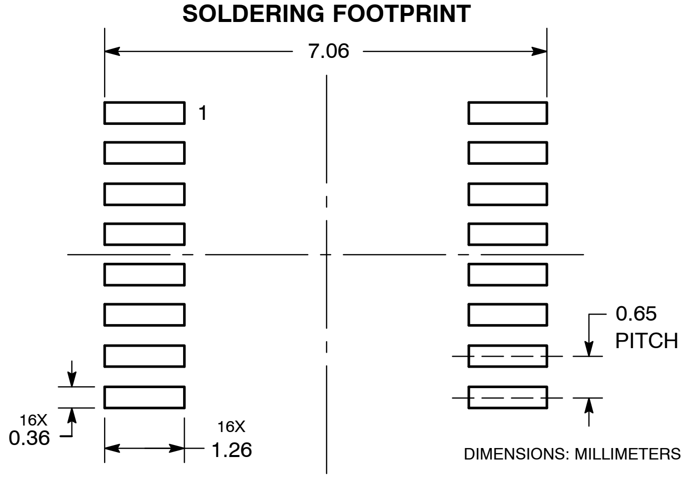
TSSOP−16
CASE 948F
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

SOLDERING FOOTPRINT



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