

NB3N1200K, NB3W1200L

3.3 V 100/133 MHz Differential 1:12 HCSL or Push-Pull Clock ZDB/Fanout Buffer for PCIe

Description

The NB3N1200K and NB3W1200L differential clock buffers are DB1200Z and DB1200ZL compliant and are designed to work in conjunction with a PCIe compliant source clock synthesizer to provide point-to-point clocks to multiple agents. The device is capable of distributing the reference clocks for Intel® QuickPath Interconnect (Intel QPI), PCIe Gen1/Gen2/Gen3, SAS, SATA, and Intel Scalable Memory Interconnect (Intel SMI) applications. The VCO of the device is optimized to support 100 MHz and 133 MHz frequency operation. The NB3N1200K and NB3W1200L utilize pseudo-external feedback topology to achieve low input-to output delay variation. The NB3N1200K is configured with the HCSL buffer type, while the NB3W1200L is configured with the low-power NMOS Push-Pull buffer type.

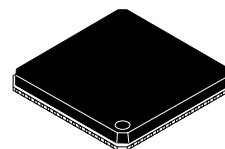
Features

- 12 Differential Clock Output Pairs @ 0.7 V
- HCSL Compatible Outputs for NB3N1200K
- Low-Power NMOS Push-Pull Compatible Outputs for NB3W1200L
- Optimized 100 MHz and 133 MHz Operating Frequencies to Meet The Next Generation PCIe Gen 2/Gen 3 and Intel QPI Phase Jitter
- DB1200Z and DB1200ZL Compliant
- 3.3 V $\pm 5\%$ Supply Voltage Operation
- Fixed-Feedback for Lowest Input-To-Output Delay Variation
- SMBus Programmable Configurations to Allow Multiple Buffers in a Single Control Network
- PLL Bypass Configurable for PLL or Fanout Operation
- Programmable PLL Bandwidth
- 2 Tri-level Addresses Selection (9 SMBUS Addresses)
- Individual OE Control Pin for Each of 12 Outputs
- Low Phase Jitter (Intel QPI, PCIe Gen 2/Gen 3 Phase Jitter Compliant)
- 50 ps Max Output-to-Output Skew Performance
- 50 ps Max Cycle-to-Cycle Jitter (PLL mode)
- 100 ps Input to Output Delay Variation Performance
- QFN 64-pin Package, 9 mm x 9 mm
- Spread Spectrum Compatible: Tracks Input Clock Spreading for Low EMI
- 0°C to +70°C Ambient Operating Temperature
- These Devices are Pb-Free and are RoHS Compliant



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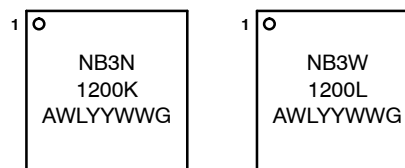
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QFN64
MN SUFFIX
CASE 485DH

MARKING DIAGRAMS



NB3x1200x= Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb-Free Package

ORDERING INFORMATION

| Device | Package | Shipping† |
|----------------|---------------------|-----------------------|
| NB3N1200KMNG | QFN-64 (Pb-Free) | 260 Units / Tray |
| NB3N1200KMNTXG | QFN-64 (Pb-Free) | 1000 / Tape & Reel |
| NB3W1200LMNG | QFN-64 (Pb-Free) | 260 Units / Tray |
| NB3W1200LMNTXG | QFN-64 (Pb-Free) | 1000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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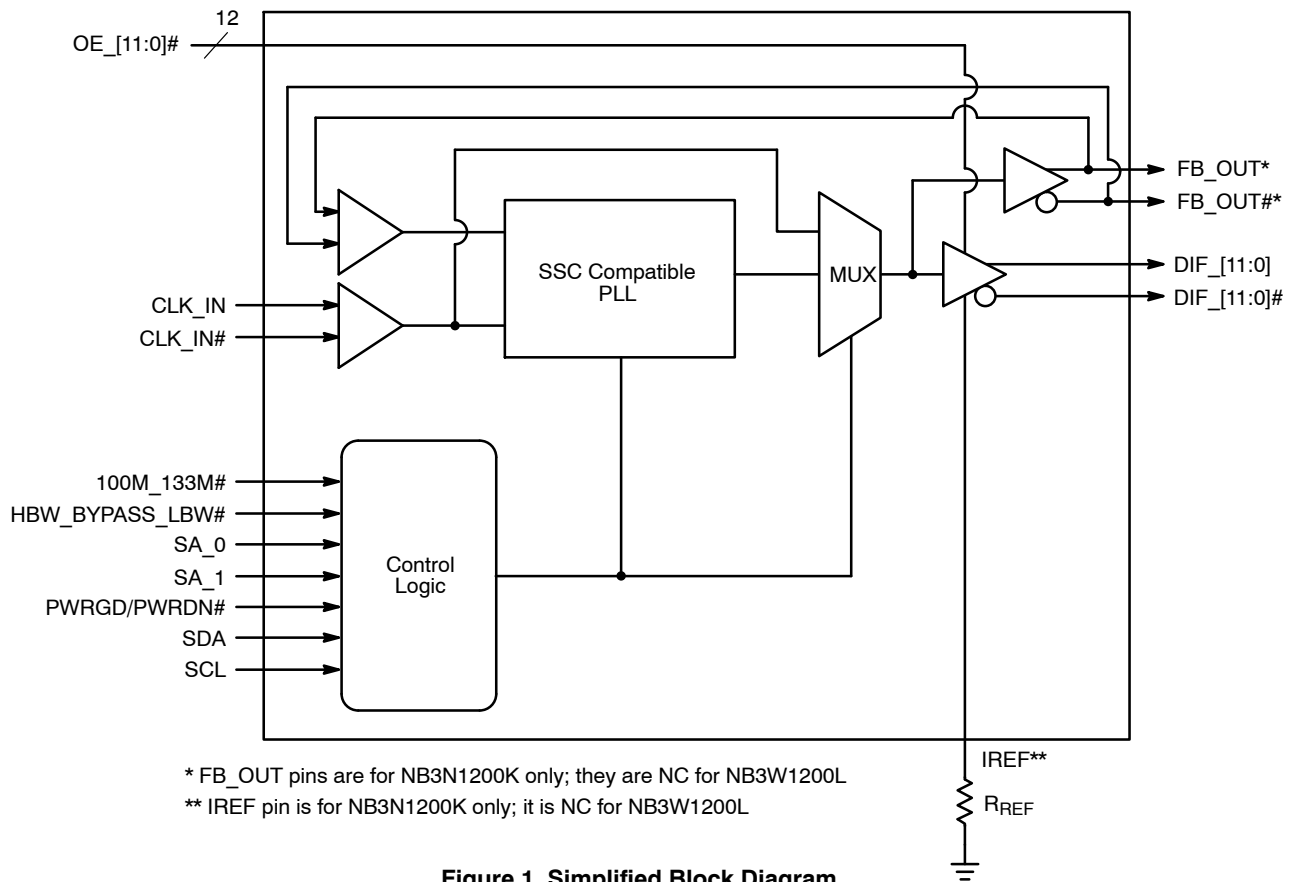


Figure 1. Simplified Block Diagram

NB3N1200K, NB3W1200L

PIN CONNECTIONS

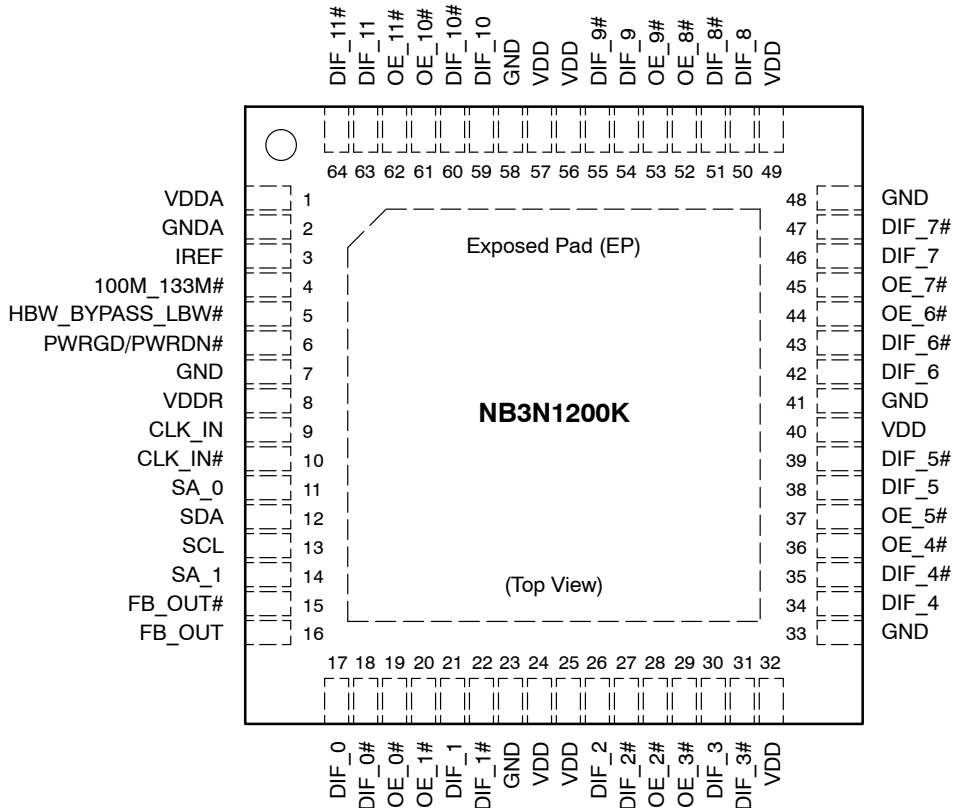


Figure 2. NB3N1200K Pinout: QFN-64 (Top View)

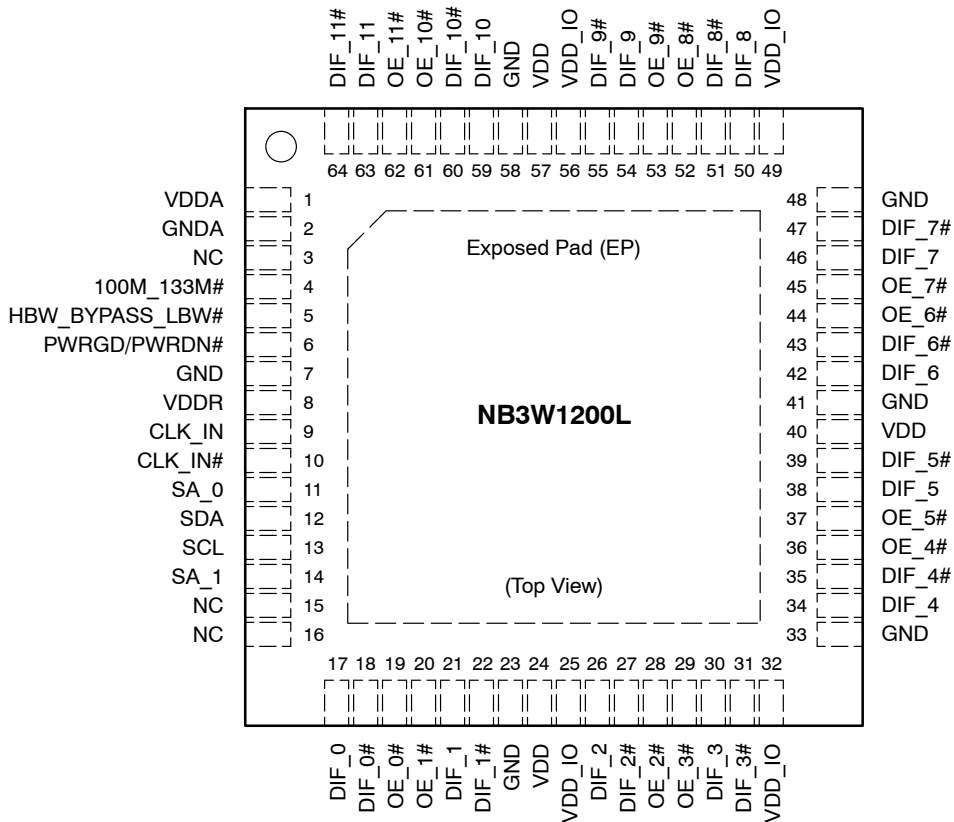


Figure 3. NB3W1200L Pinout: QFN-64 (Top View)

NB3N1200K, NB3W1200L

Table 1. NB3N1200K PIN DESCRIPTIONS

| Pin Number | Pin Name | Type | Description |
|------------|-----------------|--------|---|
| 1 | VDDA | 3.3 V | 3.3 V Power Supply for PLL. |
| 2 | GND A | GND | Ground for PLL. |
| 3 | IREF | I | A precision resistor is attached to this pin to set the differential output current. Use $R_{REF} = 475 \Omega$, 1% for 100 Ohms trace. Use $R_{REF} = 412 \Omega$, 1% for 85 Ohms trace. |
| 4 | 100M_133M# | I, SE | Input/output Frequency Selection (FS). An external pull-up or pull-down resistor is attached to this pin to select the input/output frequency. High = 100 MHz Output Low = 133 MHz Output |
| 5 | HBW_BYPASS_LBW# | I, SE | Tri-Level input for selecting the PLL bandwidth or bypass mode (refer to tri-level threshold in Table 4). High = High BW mode Med = Bypass mode Low = Low BW mode |
| 6 | PWRGD / PWRDN# | I, SE | 3.3 V LVTTTL input to power up or power down the device. |
| 7 | GND | GND | Ground for outputs. |
| 8 | VDDR | VDD | 3.3 V power supply for receiver. |
| 9 | CLK_IN | I, DIF | 0.7 V Differential True input |
| 10 | CLK_IN# | I, DIF | 0.7 V Differential Complementary input |
| 11 | SA_0 | I, SE | 3.3 V LVTTTL input selecting the address. Tri-level input (refer to tri-level threshold in Table 4.) |
| 12 | SDA | I/O | Open collector SMBus data. |
| 13 | SCL | I/O | SMBus slave clock input. |
| 14 | SA_1 | I, SE | 3.3 V LVTTTL input selecting the address. Tri-level input (refer to tri-level threshold in Table 4.) |
| 15 | FB_OUT# | O, DIF | Complementary Feedback out pin, termination required. See External Feedback Termination section. |
| 16 | FB_OUT | O, DIF | True Feedback out pin, termination required. See External Feedback Termination section. |
| 17 | DIF_0 | O, DIF | 0.7 V Differential True clock output |
| 18 | DIF_0# | O, DIF | 0.7 V Differential Complementary clock output |
| 19 | OE_0# | I, SE | 3.3 V LVTTTL active low input for enabling DIF output pair 0. 0 enables outputs, 1 disables outputs. Internal pull down. |
| 20 | OE_1# | I, SE | 3.3 V LVTTTL active low input for enabling DIF output pair 1. 0 enables outputs, 1 disables outputs. Internal pull down. |
| 21 | DIF_1 | O, DIF | 0.7 V Differential True clock output |
| 22 | DIF_1# | O, DIF | 0.7 V Differential Complementary clock output |
| 23 | GND | GND | Ground for outputs. |
| 24 | VDD | 3.3 V | 3.3 V power supply for outputs. |
| 25 | VDD | 3.3 V | 3.3 V power supply for outputs. |
| 26 | DIF_2 | O, DIF | 0.7 V Differential True clock output |
| 27 | DIF_2# | O, DIF | 0.7 V Differential Complementary clock output |
| 28 | OE_2# | I, SE | 3.3 V LVTTTL active low input for enabling DIF output pair 2. 0 enables outputs, 1 disables outputs. Internal pull down. |
| 29 | OE_3# | I, SE | 3.3 V LVTTTL active low input for enabling DIF output pair 3. 0 enables outputs, 1 disables outputs. Internal pull down. |
| 30 | DIF_3 | O, DIF | 0.7 V Differential True clock output |
| 31 | DIF_3# | O, DIF | 0.7 V Differential Complementary clock output |
| 32 | VDD | 3.3 V | 3.3 V power supply for outputs. |
| 33 | GND | GND | Ground for outputs. |

NB3N1200K, NB3W1200L

Table 1. NB3N1200K PIN DESCRIPTIONS

| Pin Number | Pin Name | Type | Description |
|------------|-------------|---------|---|
| 34 | DIF_4 | O, DIF | 0.7 V Differential True clock output |
| 35 | DIF_4# | O, DIF | 0.7 V Differential Complementary clock output |
| 36 | OE_4# | I, SE | 3.3 V LVTTTL active low input for enabling DIF output pair 4. 0 enables outputs, 1 disables outputs. Internal pull down. |
| 37 | OE_5# | I, SE | 3.3 V LVTTTL active low input for enabling DIF output pair 5. 0 enables outputs, 1 disables outputs. Internal pull down. |
| 38 | DIF_5 | O, DIF | 0.7 V Differential True clock output |
| 39 | DIF_5# | O, DIF | 0.7 V Differential Complementary clock output |
| 40 | VDD | 3.3 V | 3.3 V power supply for outputs. |
| 41 | GND | GND | Ground for outputs. |
| 42 | DIF_6 | O, DIF | 0.7 V Differential True clock output |
| 43 | DIF_6# | O, DIF | 0.7 V Differential Complementary clock output |
| 44 | OE_6# | I, SE | 3.3 V LVTTTL active low input for enabling DIF output pair 6. 0 enables outputs, 1 disables outputs. Internal pull down. |
| 45 | OE_7# | I, SE | 3.3 V LVTTTL active low input for enabling DIF output pair 7. 0 enables outputs, 1 disables outputs. Internal pull down. |
| 46 | DIF_7 | O, DIF | 0.7 V Differential True clock output |
| 47 | DIF_7# | O, DIF | 0.7 V Differential Complementary clock output |
| 48 | GND | GND | Ground for outputs. |
| 49 | VDD | 3.3 V | 3.3 V power supply for outputs. |
| 50 | DIF_8 | O, DIF | 0.7 V Differential True clock output |
| 51 | DIF_8# | O, DIF | 0.7 V Differential Complementary clock output |
| 52 | OE_8# | I, SE | 3.3 V LVTTTL active low input for enabling DIF output pair 8. 0 enables outputs, 1 disables outputs. Internal pull down. |
| 53 | OE_9# | I, SE | 3.3 V LVTTTL active low input for enabling DIF output pair 9. 0 enables outputs, 1 disables outputs. Internal pull down. |
| 54 | DIF_9 | O, DIF | 0.7 V Differential True clock output |
| 55 | DIF_9# | O, DIF | 0.7 V Differential Complementary clock output |
| 56 | VDD | 3.3 V | 3.3 V power supply for outputs. |
| 57 | VDD | 3.3 V | 3.3 V power supply for outputs. |
| 58 | GND | GND | Ground for outputs. |
| 59 | DIF_10 | O, DIF | 0.7 V Differential True clock output |
| 60 | DIF_10# | O, DIF | 0.7 V Differential Complementary clock output |
| 61 | OE_10# | I, SE | 3.3 V LVTTTL active low input for enabling DIF output pair 10. 0 enables outputs, 1 disables outputs. Internal pull down. |
| 62 | OE_11# | I, SE | 3.3 V LVTTTL active low input for enabling DIF output pair 11. 0 enables outputs, 1 disables outputs. Internal pull down. |
| 63 | DIF_11 | O, DIF | 0.7 V Differential True clock output |
| 64 | DIF_11# | O, DIF | 0.7 V Differential Complementary clock output |
| EP | Exposed Pad | Thermal | The Exposed Pad (EP) on the QFN-64 package bottom is thermally connected to the die for improved heat transfer out of package. The exposed pad must be attached to a heat-sinking conduit. The pad is electrically connected to the die, and must be electrically and thermally connected to GND on the PC board. |

NB3N1200K, NB3W1200L

Table 2. NB3W1200L PIN DESCRIPTIONS

| Pin Number | Pin Name | Type | Description |
|------------|-----------------|--------|---|
| 1 | VDDA | 3.3 V | 3.3 V Power Supply for PLL. |
| 2 | GND A | GND | Ground for PLL. |
| 3 | NC | I/O | No Connect |
| 4 | 100M_133M# | I, SE | 3.3 V tolerant inputs for input/output Frequency Selection (FS). An external pull-up or pull-down resistor is attached to this pin to select the input/output frequency. High = 100 MHz Output Low = 133 MHz Output |
| 5 | HBW_BYPASS_LBW# | I, SE | Tri-Level input for selecting the PLL bandwidth or bypass mode (refer to tri-level threshold in Table 4). High = High BW mode, Med = Bypass mode, Low = Low BW mode |
| 6 | PWRGD / PWRDN# | I | 3.3 V LVTTTL input to power up or power down the device. |
| 7 | GND | GND | Ground for outputs. |
| 8 | VDDR | VDD | 3.3 V power supply for receiver. |
| 9 | CLK_IN | I, DIF | 0.7 V Differential True input |
| 10 | CLK_IN# | I, DIF | 0.7 V Differential Complementary input |
| 11 | SA_0 | I | 3.3 V LVTTTL input selecting the address. Tri-level input (refer to tri-level threshold in Table 4.) |
| 12 | SDA | I/O | Open collector SMBus data. |
| 13 | SCL | I/O | SMBus slave clock input. |
| 14 | SA_1 | I | 3.3 V LVTTTL input selecting the address. Tri-level input (refer to tri-level threshold in Table 4.) |
| 15 | NC | I/O | No Connect. There are active signals on pin 15; do not connect anything to this pin. |
| 16 | NC | I/O | No Connect. There are active signals on pin 16; do not connect anything to this pin. |
| 17 | DIF_0 | O, DIF | 0.7 V Differential True clock output |
| 18 | DIF_0# | O, DIF | 0.7 V Differential Complementary clock output |
| 19 | OE_0# | I, SE | 3.3 V LVTTTL active low input for enabling DIF output pair 0. 0 enables outputs, 1 disables outputs. Internal pull down. |
| 20 | OE_1# | I, SE | 3.3 V LVTTTL active low input for enabling DIF output pair 1. 0 enables outputs, 1 disables outputs. Internal pull down. |
| 21 | DIF_1 | O, DIF | 0.7 V Differential True clock output |
| 22 | DIF_1# | O, DIF | 0.7 V Differential Complementary clock output |
| 23 | GND | GND | Ground for outputs. |
| 24 | VDD | 3.3 V | 3.3 V power supply for core. |
| 25 | VDD_IO | VDD | Power supply for differential outputs. |
| 26 | DIF_2 | O, DIF | 0.7 V Differential True clock output |
| 27 | DIF_2# | O, DIF | 0.7 V Differential Complementary clock output |
| 28 | OE_2# | I, SE | 3.3 V LVTTTL active low input for enabling DIF output pair 2. 0 enables outputs, 1 disables outputs. Internal pull down. |
| 29 | OE_3# | I, SE | 3.3 V LVTTTL active low input for enabling DIF output pair 3. 0 enables outputs, 1 disables outputs. Internal pull down. |
| 30 | DIF_3 | O, DIF | 0.7 V Differential True clock output |
| 31 | DIF_3# | O, DIF | 0.7 V Differential Complementary clock output |
| 32 | VDD_IO | VDD | Power supply for differential outputs. |
| 33 | GND | GND | Ground for outputs. |

NB3N1200K, NB3W1200L

Table 2. NB3W1200L PIN DESCRIPTIONS

| Pin Number | Pin Name | Type | Description |
|------------|-------------|---------|---|
| 34 | DIF_4 | O, DIF | 0.7 V Differential True clock output |
| 35 | DIF_4# | O, DIF | 0.7 V Differential Complementary clock output |
| 36 | OE_4# | I, SE | 3.3 V LVTTTL active low input for enabling DIF output pair 4. 0 enables outputs, 1 disables outputs. Internal pull down. |
| 37 | OE_5# | I, SE | 3.3 V LVTTTL active low input for enabling DIF output pair 5. 0 enables outputs, 1 disables outputs. Internal pull down. |
| 38 | DIF_5 | O, DIF | 0.7 V Differential True clock output |
| 39 | DIF_5# | O, DIF | 0.7 V Differential Complementary clock output |
| 40 | VDD | 3.3 V | 3.3 V power supply for core. |
| 41 | GND | GND | Ground for outputs. |
| 42 | DIF_6 | O, DIF | 0.7 V Differential True clock output |
| 43 | DIF_6# | O, DIF | 0.7 V Differential Complementary clock output |
| 44 | OE_6# | I, SE | 3.3 V LVTTTL active low input for enabling DIF output pair 6. 0 enables outputs, 1 disables outputs. Internal pull down. |
| 45 | OE_7# | I, SE | 3.3 V LVTTTL active low input for enabling DIF output pair 7. 0 enables outputs, 1 disables outputs. Internal pull down. |
| 46 | DIF_7 | O, DIF | 0.7 V Differential True clock output |
| 47 | DIF_7# | O, DIF | 0.7 V Differential Complementary clock output |
| 48 | GND | GND | Ground for outputs. |
| 49 | VDD_IO | VDD | Power supply for differential outputs. |
| 50 | DIF_8 | O, DIF | 0.7 V Differential True clock output |
| 51 | DIF_8# | O, DIF | 0.7 V Differential Complementary clock output |
| 52 | OE_8# | I, SE | 3.3 V LVTTTL active low input for enabling DIF output pair 8. 0 enables outputs, 1 disables outputs. Internal pull down. |
| 53 | OE_9# | I, SE | 3.3 V LVTTTL active low input for enabling DIF output pair 9. 0 enables outputs, 1 disables outputs. Internal pull down. |
| 54 | DIF_9 | O, DIF | 0.7 V Differential True clock output |
| 55 | DIF_9# | O, DIF | 0.7 V Differential Complementary clock output |
| 56 | VDD_IO | VDD | Power supply for differential outputs. |
| 57 | VDD | 3.3 V | 3.3 V power supply for core. |
| 58 | GND | GND | Ground for outputs. |
| 59 | DIF_10 | O, DIF | 0.7 V Differential True clock output |
| 60 | DIF_10# | O, DIF | 0.7 V Differential Complementary clock output |
| 61 | OE_10# | I, SE | 3.3 V LVTTTL active low input for enabling DIF output pair 10. 0 enables outputs, 1 disables outputs. Internal pull down. |
| 62 | OE_11# | I, SE | 3.3 V LVTTTL active low input for enabling DIF output pair 11. 0 enables outputs, 1 disables outputs. Internal pull down. |
| 63 | DIF_11 | O, DIF | 0.7 V Differential True clock output |
| 64 | DIF_11# | O, DIF | 0.7 V Differential Complementary clock output |
| EP | Exposed Pad | Thermal | The Exposed Pad (EP) on the QFN-64 package bottom is thermally connected to the die for improved heat transfer out of package. The exposed pad must be attached to a heat-sinking conduit. The pad is electrically connected to the die, and must be electrically and thermally connected to GND on the PC board. |

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Table 3. MAXIMUM RATINGS

| Symbol | Parameter | Condition | Min | Max | Units |
|--------------------------|-------------------------|---|------|----------|-------|
| $V_{DD}/V_{DDA}/V_{DDR}$ | Core Supply Voltage | | | 4.6 | V |
| V_{DD_IO} | I/O Supply Voltage | | | 4.6 | V |
| V_{IH} (Note 1) | Input High Voltage | | | 4.6 | V |
| V_{IHSMB} | SMB Input High Voltage | SDA, SCL Pins | | 5.5 | V |
| V_{IL} | 3.3 V Input Low Voltage | | -0.5 | | V |
| t_s | Storage Temperature | | -65 | 150 | °C |
| ESD prot. | Input ESD protection | Human Body Model | 2000 | | V |
| I_{OUTmax} | Maximum Output Current | Powerdown Mode (PWRGD/PWRDN# = 0) | | | |
| | NB3N1200K NB3W1200L | All Pairs Tri-stated All Pairs Tri-state Low/Low | | 24 12 | mA |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

- Maximum V_{IH} is not to exceed maximum V_{DD} .

Table 4. DC OPERATING CHARACTERISTICS ($V_{DD} = V_{DDA} = V_{DDR} = 3.3\text{ V} \pm 5\%$, $T_A = 0^\circ\text{C} - 70^\circ\text{C}$)

| Symbol | Parameter | Condition | Min | Max | Units |
|--------------------------|---|---------------------------------|---------|--------------|---------------|
| $V_{DD}/V_{DDA}/V_{DDR}$ | 3.3 V Core Supply Voltage | 3.3 V $\pm 5\%$ | 3.135 | 3.465 | V |
| V_{DD_IO} (Note 2) | I/O Supply Voltage | 1.05 V to 3.3 V $\pm 5\%$ | 0.975 | 3.465 | V |
| I_{DD} | Power Supply Current | At 133 MHz, $C_L = 2\text{ pF}$ | | | |
| | NB3N1200K NB3W1200L | | | 330 180 | mA |
| I_{DDPD} | Power Down Current | | | | |
| | NB3N1200K NB3W1200L | | | 6 6 | mA |
| V_{IH} (Note 3) | Input High Voltage, Single-Ended Inputs | | 2.0 | 5.5 | V |
| V_{IL} (Note 3) | Input Low Voltage, Single-Ended Inputs | | GND-0.3 | 0.8 | V |
| V_{IHCLK_IN} | CLK_IN/CLK_IN# High | | 600 | 1150 | mV |
| V_{ILCLK_IN} | CLK_IN/CLK_IN# Low | | -300 | 300 | mV |
| I_{IL} (Note 4) | Input Leakage Current | $0 < V_{IN} < V_{DD}$ | -5 | +5 | μA |
| V_{IH_FS} (Note 5) | Input High Voltage | | 0.7 | $V_{DD}+0.3$ | V |
| V_{IL_FS} (Note 5) | Input Low Voltage | | GND-0.3 | 0.35 | V |
| V_{IL_Tri} (Note 6) | Tri-Level Input Low Voltage | | 0 | 0.8 | V |
| V_{IM_Tri} (Note 6) | Tri-Level Input Med Voltage | | 1.2 | 1.8 | V |
| V_{IH_Tri} (Note 6) | Tri-Level Input High Voltage | | 2.2 | V_{DD} | V |
| V_{OH} (Note 7) | Output High Voltage SCL, SDA | $I_{OH} = -1\text{ mA}$ | 2.4 | | V |
| V_{OL} (Note 7) | Output Low Voltage SCL, SDA | $I_{OL} = 1\text{ mA}$ | | 0.4 | V |
| C_{in} (Note 8) | Input Capacitance | | 2.5 | 4.5 | pF |
| C_{out} (Note 8) | Output Capacitance | | 2.5 | 4.5 | pF |
| L_{pin} | Pin Inductance | | | 7 | nH |
| t_a | Ambient Temperature | No Airflow | 0 | 70 | °C |

- V_{DD_IO} applies to the low power NMOS push-pull NB3W1200L only.
- SDA, SCL, OEn#, PWRGD/PWRDN#.
- Input Leakage Current does not include inputs with pull-up or pull-down resistors.
- 100M_133M# Frequency Select (FS).
- SA_0, SA_1, HBW_BYPASS_LBW#.
- Signal edge is required to be monotonic when transitioning through this region.
- Ccomp capacitance based on pad metallization and silicon device capacitance. Not including package pin capacitance.

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NB3N1200K / NB3W1200L Output Relational Timing Parameters

Table 5. ELECTRICAL CHARACTERISTICS – Skew and Differential Jitter Parameters

($V_{DD} = V_{DDA} = V_{DDR} = 3.3\text{ V} \pm 5\%$, $T_A = 0 - 70^\circ\text{C}$)

| Group | Description | Min | Typ | Max | Units |
|---|---|------|-----|-----|-------|
| CLK_IN, DIF[x:0] (Notes 9, 10, 12, 13) | Input-to-Output Delay in PLL mode, nominal value | -100 | | 100 | ps |
| CLK_IN, DIF[x:0] (Notes 10, 11, 13) | Input-to-Output Delay in Bypass mode, nominal value | 2.5 | | 4.5 | ns |
| CLK_IN, DIF[x:0] (Notes 10, 11, 13) | Input-to-Output Delay variation in PLL mode (over voltage and temperature), nominal value | | | 100 | ps |
| CLK_IN, DIF[x:0] (Notes 10, 11, 13) | Input-to-Output Delay variation in Bypass mode (over voltage and temperature), nominal value | | | 250 | ps |
| DIF[11:0] (Notes 9, 10, 11, 13) | Output-to-Output Skew across all 12 outputs (Common to Bypass and PLL mode) | 0 | | 50 | ps |

9. Measured into fixed 2 pF load capacitance. Input to output skew is measured at the first output edge following the corresponding input.
 10. Measured from differential cross-point to differential cross-point.
 11. All Bypass Mode Input-to-Output specs refer to the timing between an input edge and the specific output edge created by it.
 12. This parameter is deterministic for a given device.
 13. Measured with scope averaging on to find mean value.

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Table 6. LOW BAND PHASE JITTER – PLL MODE

| Group | Parameter | Min | Typ | Max | Units |
|-------------------------------|--|-----|-----|-----|-------------|
| DIF (Notes 14, 16, 17) | Output PCIe Gen1 | | 13 | 86 | ps (p-p) |
| DIF (Notes 14, 15, 17, 19) | Output PCIe Gen2 Low Band, 10 kHz < f < 1.5 MHz | | 0.1 | 3.0 | ps RMS |
| DIF (Notes 14, 15, 17, 19) | Output PCIe Gen2 High Band, 1.5 MHz < f < 50 MHz | | 0.8 | 3.1 | ps RMS |

HIGH BAND, 1.5 MHz < F < Nyquist

| | | | | | |
|-------------------------------|---|--|------|-----|-----------|
| DIF (Notes 14, 15, 17, 19) | Output phase jitter impact – PCIe* Gen3 (including PLL BW 2 – 4 MHz, CDR = 10 MHz) | | 0.18 | 1.0 | ps RMS |
| DIF (Notes 14, 18, 20) | Output Intel QPI & Intel SMI REFCLK accumulated jitter (4.8 Gb/s or 6.4 Gb/s, 100 MHz or 133 MHz, 12 UI) | | 0.14 | 0.5 | ps RMS |
| DIF (Notes 14, 18) | Output Intel QPI & Intel SMI REFCLK accumulated jitter (8 Gb/s, 100 MHz, 12 UI) | | 0.07 | 0.3 | ps RMS |
| DIF (Notes 14, 18) | Output Intel QPI & Intel SMI REFCLK accumulated jitter (9.6 Gb/s, 100 MHz, 12 UI) | | 0.06 | 0.2 | ps RMS |

Table 7. ADDITIVE PHASE JITTER – BYPASS MODE

| Group | Parameter | Min | Typ | Max | Units |
|-------------------------------|---|-----|-------|-----|-------------|
| DIF (Notes 14, 16, 17) | Output PCIe Gen1 | | 0.04 | 10 | ps (p-p) |
| DIF (Notes 14, 15, 17, 19) | Output PCIe Gen2 Low Band, 10 kHz < f < 1.5 MHz | | 0.001 | 0.3 | ps RMS |
| DIF (Notes 14, 15, 17, 19) | Output PCIe Gen2 High Band, 1.5 MHz < f < 50 MHz | | 0.002 | 0.7 | ps RMS |
| DIF (Notes 14, 15, 17, 19) | Output phase jitter impact – PCIe* Gen3 | | 0.001 | 0.3 | ps RMS |
| DIF (Notes 14, 18, 20) | Output Intel QPI & Intel SMI REFCLK accumulated jitter (4.8 Gb/s or 6.4 Gb/s, 100 MHz or 133 MHz, 12 UI) | | 0.001 | 0.3 | ps RMS |
| DIF (Notes 14, 18) | Output Intel QPI & Intel SMI REFCLK accumulated jitter (8 Gb/s, 100 MHz, 12 UI) | | 0.001 | 0.1 | ps RMS |
| DIF (Notes 14, 18) | Output Intel QPI & Intel SMI REFCLK accumulated jitter (9.6 Gb/s, 100 MHz, 12 UI) | | 0.001 | 0.1 | ps RMS |

14. Post processed evaluation through Intel supplied Matlab scripts. Tested with NB3N1200K/NB3W1200L driven by a CK420BQ or equivalent.
 15. PCIe Gen3 filter characteristics are subject to final ratification by PCISIG. Please check the PCI SIG for the latest specification.
 16. These jitter numbers are defined for a BER of 1E-12. Measured numbers at a smaller sample size have to be extrapolated to this BER target.
 17. (= 0.54 is implying a jitter peaking of 3 dB.
 18. Measuring on 100 MHz output using Intel supplied clock template jitter tool.
 19. Measuring on 100 MHz PCIe SRC output using Intel supplied clock jitter tool.
 20. Measuring on 100 MHz, 133 MHz output using Intel supplied clock jitter tool.

Table 8. PLL BANDWIDTH AND PEAKING

| Group | Parameter | Min | Typ | Max | Units |
|---------------|--|-----|-----|-----|-------|
| DIF (Note 21) | PLL Jitter Peaking (HBW_BYPASS_LBW# = 0) | - | 0.7 | 2.0 | dB |
| DIF (Note 21) | PLL Jitter Peaking (HBW_BYPASS_LBW# = 1) | - | 0.4 | 2.5 | dB |
| DIF (Note 22) | PLL Bandwidth (HBW_BYPASS_LBW# = 1) | 2.0 | 2.7 | 4.0 | MHz |
| DIF (Note 22) | PLL Bandwidth (HBW_BYPASS_LBW# = 0) | 0.7 | 0.9 | 1.4 | MHz |

21. Measured as maximum pass band gain. At frequencies within the loop BW, highest point of magnification is called PLL jitter peaking.
 22. Measured at 3 db down or half power point.

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Table 9. DIF 0.7 V AC TIMING CHARACTERISTICS (Non-Spread or -0.5% Spread Spectrum Mode)

($V_{DD} = V_{DDA} = V_{DDR} = 3.3 \text{ V} \pm 5\%$)

| Symbol | Parameter | | CLK = 100 MHz, 133.33 MHz | | Unit |
|--|---|--------------|---------------------------|----------------------|--------|
| | | | Min | Max | |
| Tstab (Note 44) | Clock Stabilization Time | | | 1.8 | ms |
| Laccuracy (Notes 26, 30, 38, 45) | Long Accuracy | | | 100 | ppm |
| Tabs (Notes 26, 27, 30) | Absolute Min/Max Host CLK Period | No Spread | 9.94900 for 100 MHz | 10.05100 for 100 MHz | ns |
| | | | 7.44925 for 133 MHz | 7.55075 for 133 MHz | |
| | | -0.5% Spread | 9.49900 for 100 MHz | 10.10126 for 100 MHz | |
| | | | 7.44925 for 133 MHz | 7.58845 for 133 MHz | |
| Slew_rate (Notes 24, 26, 30) | DIFF OUT Slew_rate (see Figure 4) | | 1.0 | 4.0 | V/ns |
| Δ Trise / Δ Tfall (Notes 26, 29, 40) | Rise and Fall Time Variation | | | 125 | ps |
| Rise/Fall Matching (Notes 26, 30, 41, 43) | | | | 20 | % |
| VHigh (Notes 26, 29, 32) | Voltage High (typ 0.70 Volts) | | 660 | 850 | mV |
| VLow (Notes 26, 29, 33) | Voltage Low (typ 0.0 Volts) | | -150 | 150 | mV |
| Vmax (Note 29) | Maximum Voltage | | | 1150 | mV |
| Vcross absolute (Notes 23, 25, 26, 29, 36) | Absolute Crossing Point Voltages | | 250 | 550 | mV |
| Vcross relative (Notes 26, 28, 29, 36) | Relative Crossing Point Voltages | | Calc | Calc | |
| Total Δ Vcross (Notes 26, 29, 37) | Total Variation of Vcross Over All Edges | | | 140 | mV |
| Tccjitter (Notes 26, 30, 42) | Cycle-to-Cycle Jitter | | | 50 | ps |
| Duty Cycle (Notes 26, 30) | PLL and Bypass Modes | | 45 | 55 | % |
| tOE# Latency | OE# Latency – DIFF start after OE# Assertion – DIFF stop after OE# Deassertion | | 4 | 12 | Clocks |
| Vovs (Notes 26, 29, 34) | Maximum Voltage (Overshoot) | | | Vhigh + 0.3 | V |
| Vuds (Notes 26, 29, 35) | Maximum Voltage (Undershoot) | | | Vlow – 0.3 | V |
| Vrb (Notes 26, 29) | Ringback Voltage | | 0.2 | N/A | V |

23. Measured at crossing point where the instantaneous voltage value of the rising edge of CLK equals the falling edge of CLK#.
24. Measurement taken from differential waveform on a component test board. The slew rate is measured from -150 mV to +150 mV on the differential waveform. Scope is set to average because the scope sample clock is making most of the dynamic wiggles along the clock edge. Only valid for Rising CLK_IN and Falling CLK_IN#. Signal must be monotonic through the Vol to Voh region for Trise and Tfall.
25. This measurement refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing.
26. Test configuration is $R_s = 33.2 \Omega$, $R_p = 49.9 \Omega$, 2 pF for 100 Ω transmission line; $R_s = 27 \Omega$, $R_p = 42.2 \Omega$, 2 pF for 85 Ω transmission line.
27. The average period over any 1 μ s period of time must be greater than the minimum and less than the maximum specified period.
28. Vcross(rel) Min and Max are derived using the following, Vcross(rel) Min = $0.250 + 0.5 (V_{avg} - 0.700)$, Vcross(rel) Max = $0.550 - 0.5 (0.700 - V_{avg})$, (see Figure 7).
29. Measurement taken from Single Ended waveform.
30. Measurement taken from differential waveform. Bypass mode, input duty cycle = 50%.
31. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
32. VHigh is defined as the statistical average High value as obtained by using the Oscilloscope VHigh Math function.
33. VLow is defined as the statistical average Low value as obtained by using the Oscilloscope VLow Math function.
34. Overshoot is defined as the absolute value of the maximum voltage.
35. Undershoot is defined as the absolute value of the minimum voltage.
36. The crossing point must meet the absolute and relative crossing point specifications simultaneously.
37. Δ Vcross is defined as the total variation of all crossing voltages of Rising DIFF and Falling DIFF#. This is the maximum allowed variance in Vcross for any particular system.
38. Using frequency counter with the measurement interval equal or greater than 0.15 s, target frequencies are 100,000,000 Hz, 133,333,333 Hz.
39. Using frequency counter with the measurement interval equal or greater than 0.15 s, target frequencies are 99,750,00 Hz, 133,000,000 Hz.
40. Measured with oscilloscope, averaging off, using min max statistics. Variation is the delta between min and max.
41. Measured with oscilloscope, averaging on, The difference between the rising edge rate (average) of DIFF versus the falling edge rate (average) of DIFF#. Measured in a ± 75 mV window around the crosspoint of DIFF and DIFF#.
42. Measured with device in PLL mode, in BYPASS mode jitter is additive.
43. Rise/Fall matching is derived using the following, $2 * (Trise - Tfall) / (Trise + Tfall)$.
44. This is the time from the valid CLK_IN input clocks and the assertion of the PWRGD signal level at 1.8 V – 2.0 V to the time that stable clocks are output from the buffer chip (PLL locked).
45. All Long Term Accuracy specifications are guaranteed with the assumption that the input clock complies with CK410B+/CK420BQ accuracy requirements. The NB3N1200K and NB3W1200L itself do not contribute to ppm error.

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Table 10. CLOCK PERIOD SSC DISABLED

| SSC OFF Center Freq. MHz | Measurement Window | | | | | | | Units |
|-----------------------------------|-----------------------------|------------------------|-----------------------|-----------------|-----------------------|------------------------|-----------------------------|-------|
| | 1 Clock | 1 μ s | 0.1 s | 0.1 s | 0.1 s | 1 μ s | 1 Clock | |
| | - Jitter c-c Abs Per Min | - SSC Short Avg Min | - ppm Long Avg Min | 0 ppm Period | + ppm Long Avg Max | + SSC Short Avg Max | + Jitter c-c Abs Per Max | |
| 100.00 | 9.94900 | | 9.99900 | 10.00000 | 10.00100 | | 10.05100 | ns |
| 133.33 | 7.44925 | | 7.49925 | 7.50000 | 7.50075 | | 7.55075 | ns |

Table 11. CLOCK PERIOD SSC ENABLED

| SSC ON Center Freq. MHz | Measurement Window | | | | | | | Units |
|----------------------------------|-----------------------------|------------------------|-----------------------|-----------------|-----------------------|------------------------|-----------------------------|-------|
| | 1 Clock | 1 μ s | 0.1 s | 0.1 s | 0.1 s | 1 μ s | 1 Clock | |
| | - Jitter c-c Abs Per Min | - SSC Short Avg Min | - ppm Long Avg Min | 0 ppm Period | + ppm Long Avg Max | + SSC Short Avg Max | + Jitter c-c Abs Per Max | |
| 99.75 | 9.94900 | 9.99900 | 10.02406 | 10.02506 | 10.02607 | 10.05126 | 10.10126 | ns |
| 133.00 | 7.44925 | 7.49925 | 7.51805 | 7.51880 | 7.51955 | 7.53845 | 7.58845 | ns |

Table 12. INPUT EDGE RATE (Note 46)

| Frequency Select (FS) | Min | Max | Unit |
|-----------------------|------|-----|------|
| 100 MHz | 0.35 | N/A | V/ns |
| 133 MHz | 0.35 | N/A | V/ns |

46. Input edge rate is based on single ended measurement. This is the minimum input edge rate at which the NB3N1200K / NB3W1200L devices are guaranteed to meet all performance specifications.

Measurement Points for Differential

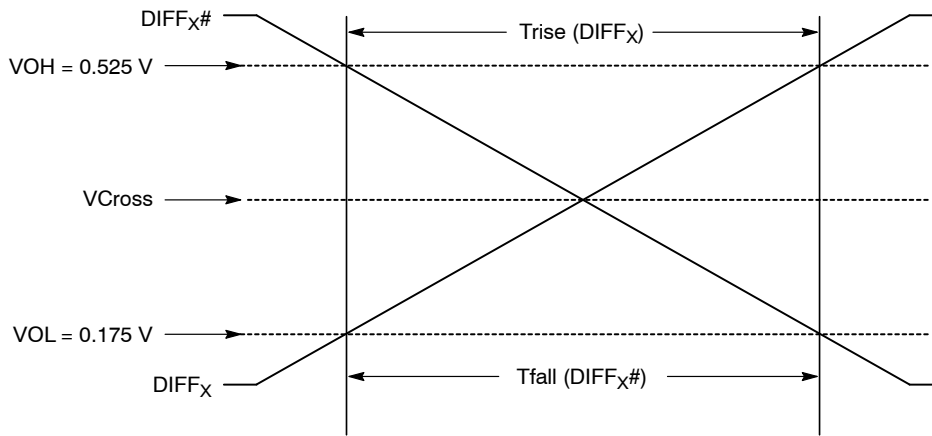


Figure 4. Single-Ended Measurement Points for Trise, Tfall

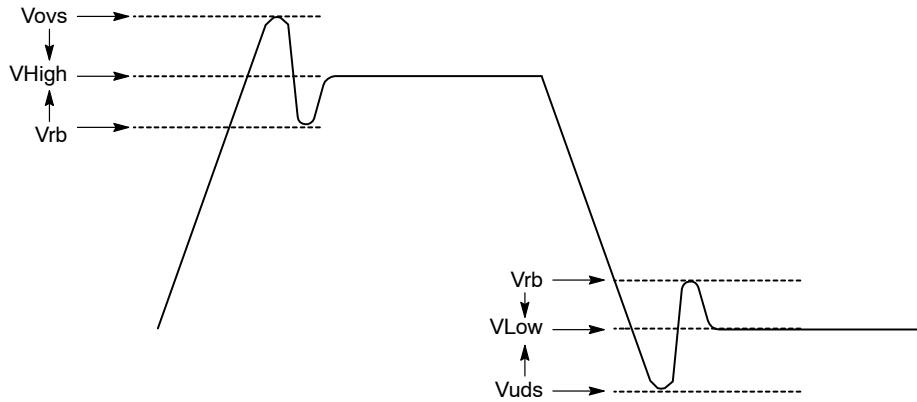


Figure 5. Single-Ended Measurement Points for Vovs, Vuds, Vrb

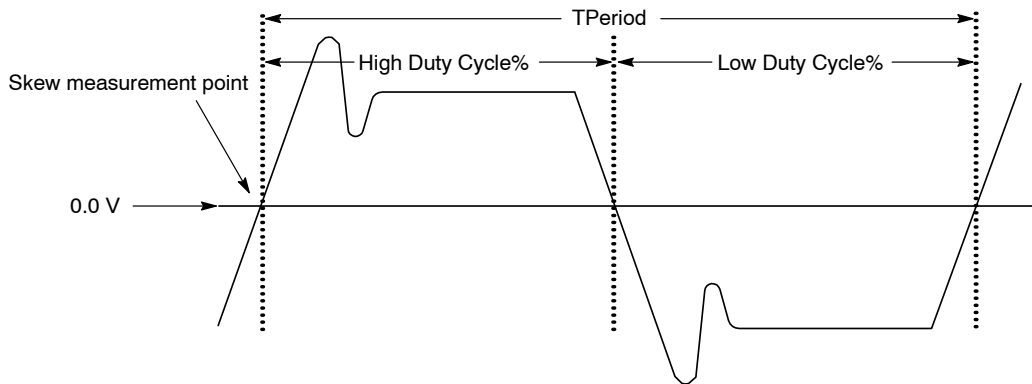
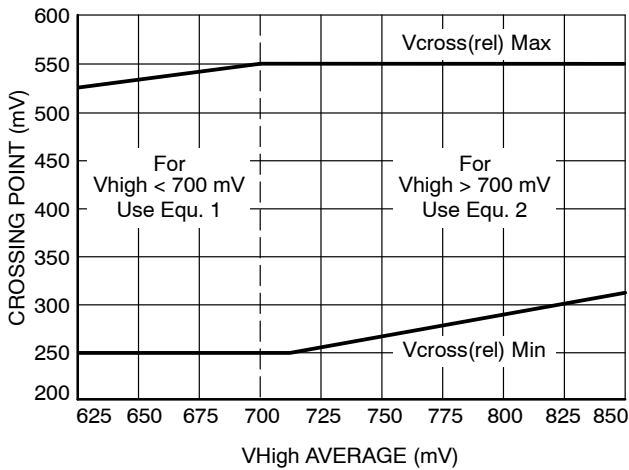


Figure 6. Differential ($DIFF_x - DIFF_{x\#}$) Measurement Points (Tperiod, Duty Cycle, Jitter)

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Equ 1: $V_{cross(rel) Max} = 0.550 - 0.5(0.7 - V_{havg})$

Equ 2: $V_{cross(rel) Min} = 0.250 + 0.5(V_{havg} - 0.7)$

Figure 7. Vcross Range Clarification

The picture above illustrates the effect of V_{high} above and below 700 mV on the V_{cross} range. The purpose of this is to prevent a 250 mV V_{cross} with an 850 mV V_{high} . In addition, this prevents the case of a 550 mV V_{cross} with a 660 mV V_{high} . The actual specification for V_{cross} is dependent upon the measured amplitude of V_{high} .

CLK_IN, CLK_IN#

The differential input clock is expected to be sourced from a clock synthesizer.

OE# and Output Enables (Control Registers)

Each output can be individually enabled or disabled by SMBus control register bits. Additionally, each output of the DIF[11:0] has a dedicated OE# pin. The OE# pins are asynchronous asserted-low signals. The Output Enable bits in the SMBus registers are active high and are set to enable by default.

The disabled state for the NB3N1200K HCSL outputs is Hi-Z, with the termination network pulling the outputs Low/Low. The disabled state for the NB3W1200L low power NMOS Push-Pull outputs is Low/Low. In the following text, if the NB3N1200K HCSL output is referred to as Hi-Z or Tri- state, the equivalent state of the NB3W1200L NMOS Push-pull output is Low/Low.

Please note that the logic level for assertion or deassertion is different in software than it is on hardware. This follows hardware default nomenclature for communication channels (e.g., output is enabled if OE# pin is pulled low) and still maintains software programming logic (e.g., output is enabled if OE register is true).

Please refer to Table 13 for the truth table for enabling and disabling outputs via hardware and software. Note that both the control register bit must be a '1' AND the OE# pin must be a '0' for the output to be active.

NOTE: The assertion and de-assertion of this signal is absolutely asynchronous.

Table 13. NB3N1200K OE AND POWER MANAGEMENT

| Inputs | | OE# Hardware Pins & Control Register Bits | | | Outputs | PLL State |
|------------------|--------------------|---|---------|-----------------|--------------------|-----------|
| PWRGD/ PWRDN# | CLK_IN/ CLK_IN# | SMBUS Enable Bit | OE# Pin | DIF/DIF# [11:0] | FB_OUT/ FB_OUT# | |
| 0 | X | X | X | Hi-Z | Hi-Z | OFF |
| 1 | Running | 0 | X | Hi-Z | Running | ON |
| | | 1 | 0 | Running | Running | ON |
| | | 1 | 1 | Hi-Z | Running | ON |

Table 14. NB3W1200L POWER MANAGEMENT

| Inputs | | OE# Hardware Pins & Control Register Bits | | | Outputs | PLL State |
|------------------|--------------------|---|---------|-----------------|--------------------------|-----------|
| PWRGD/ PWRDN# | CLK_IN/ CLK_IN# | SMBUS Enable Bit | OE# Pin | DIF/DIF# [11:0] | NC pins (Pins 15, 16) | |
| 0 | X | X | X | Low/Low | Low/Low | OFF |
| 1 | Running | 0 | X | Low/Low | Running | ON |
| | | 1 | 0 | Running | Running | ON |
| | | 1 | 1 | Low/Low | Running | ON |

NB3N1200K, NB3W1200L

OE# Assertion (Transition from '1' to '0')

All differential outputs that were tri-stated are to resume normal operation in a glitch free manner. The latency from the assertion to active outputs is 4 – 12 DIF clock periods.

OE# De-Assertion (Transition from '0' to '1')

The impact of de-asserting OE# is each corresponding output will transition from normal operation to tri-state in a glitch free manner. A minimum of 4 valid clocks will be provided after the de-assertion of OE#. The maximum latency from the de-assertion to tri-stated outputs is 12 DIF clock periods.

100M_133M# – Frequency Selection (FS)

The NB3N1200K / NB3W1200L is optimized for lowest phase jitter performance at 100 MHz and 133 MHz operating frequencies. The 100M_133M# is a hardware pin, which programs the appropriate output frequency of the DIF pairs. Note that the CLK_IN frequency is equal to CLK_OUT frequency; this means that the NB3N1200K / NB3W1200L is operated in the 1:1 mode only. The Frequency Selection can be enabled by the 100M_133M# hardware pin. An external pull-up or pull-down resistor is attached to this pin to select the input/output frequency. The functionality is summarized in Table 15.

Table 15. FREQUENCY SELECT (FS) PROGRAM

| 100M_133M# | Optimized Frequency (CLK_IN = CLK_OUT) |
|------------|--|
| 0 | 133.33 MHz |
| 1 | 100.00 MHz |

NOTE: All differential outputs transition from 100 MHz to 133 MHz or from 133 MHz to 100 MHz in a glitch free manner.

SA_0, SA_1 – Address Selection

SA_0 and SA_1 are tri-level hardware pins, which program the appropriate address for the NB3N1200K / NB3W1200L. The two tri-level input pins that can configure the NB3N1200K / NB3W1200L to nine different addresses (refer to Table 4 for VIL_Tri, VIM_Tri, VIH_Tri signal level).

Table 16. SMBUS ADDRESS TABLE

| SA_1 | SA_0 | SMBUS Address |
|------|------|---------------|
| L | L | D8 |
| L | M | DA |
| L | H | DE |
| M | L | C2 |
| M | M | C4 |
| M | H | C6 |
| H | L | CA |
| H | M | CC |
| H | H | CE |

PWRGD/PWRDN#

PWRGD is asserted high and de-asserted low. De-assertion of PWRGD (pulling the signal low) is equivalent to indicating a powerdown condition. PWRGD (assertion) is used by the NB3N1200K / NB3W1200L to sample initial configurations such as frequency select condition and SA selections.

After PWRGD has been asserted high for the first time, the pin becomes a PWRDN# (Power Down) pin that can be used to shut off all clocks cleanly and instruct the device to invoke power savings mode. PWRDN# is a completely asynchronous active low input. When entering power savings mode, PWRDN# should be asserted low **prior to shutting off the input clock or power** to ensure all clocks shut down in a glitch free manner. When PWRDN# is asserted low, all clocks will be tri-stated prior to turning off the VCO. When PWRDN# is de-asserted high, all clocks will start and stop without any abnormal behavior and will meet all AC and DC parameters.

NOTE: The assertion and de-assertion of PWRDN# is absolutely asynchronous.

WARNING: Disabling of the CLK_IN input clock prior to assertion of PWRDN# is an undefined mode and not recommended. Operation in this mode may result in glitches, excessive frequency shifting, etc.

Table 17. PWRGD/PWRDN# FUNCTIONALITY

| PWRGD/PWRDN# | DIF | DIF# |
|--------------|-----------|-----------|
| 0 | Tri-state | Tri-state |
| 1 | Normal | Normal |

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PWRDN# Assertion

When PWRDN# is sampled low by two consecutive rising edges of DIF#, all differential outputs must held tri-stated on the next DIF# high to low transition.

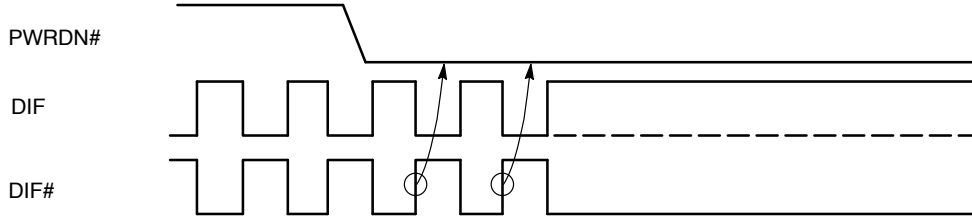


Figure 8. PWRDN#—Assertion

PWRGD Assertion

The power-up latency is to be less than 1.8 ms. This is the time from the valid CLK_IN input clocks and the assertion of the PWRGD signal to the time that stable clocks are output from the buffer chip (PLL locked). All differential

outputs stopped in a tri-state condition resulting from power down must be driven high in less than 300 μs of PWRDN# de-assertion to a voltage greater than 200 mV.

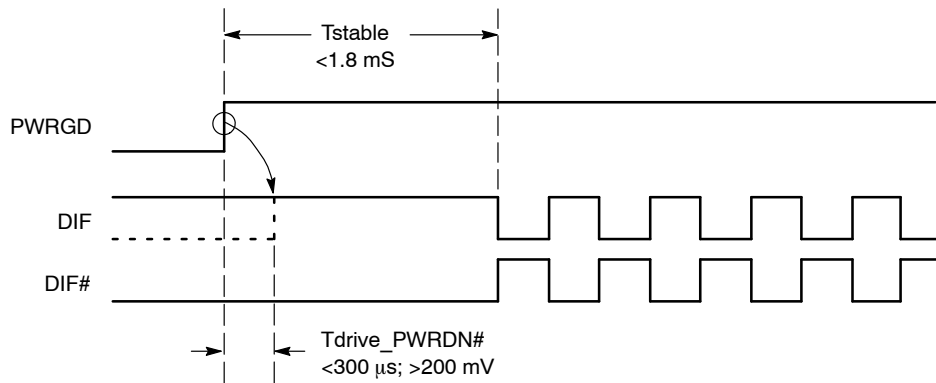


Figure 9. PWRGD Assertion (Pwrdown - De-assertion)

HBW_BYPASS_LBW#

The HBW_BYPASS_LBW# is a tri level function input pin (refer to Table 13 for VIL_Tri, VIM_Tri, VIH_Tri—signal level). It is used to select between PLL high bandwidth, bypass mode and PLL low bandwidth mode. In the bypass mode, the input clock is passed directly to the output stage which may result in up to 50 ps of additive

cycle-to-cycle jitter (50 ps + input jitter) on DIF outputs. In the case of PLL mode, the input clock is passed through a PLL to reduce high frequency jitter. The PLL HBW, BYPASS, and PLL LBW mode may be selected by asserting the HBW_BYPASS_LBW# input pin to the appropriate level per the following table:

Table 18. PLL BANDWIDTH AND READBACK TABLE

| HBW_BYPASS_LBW# Pin | Mode | Byte 0, Bit 7 | Byte 0, Bit 6 |
|---------------------|--------|---------------|---------------|
| L | LBW | 0 | 0 |
| M | BYPASS | 0 | 1 |
| H | HBW | 1 | 1 |

Additionally, the NB3N1200K/NB3W1200L has the ability to override the Latch value of the PLL operating mode from hardware strap pin 5 via use of Byte 0, bits 2 and 1. Byte 0 Bit 3 must be set to 1 to allow user to change Bits

2 and 1 to affect the PLL. Bits 7 and 6 will always read back the original latched value. A warm reset of the system will have to be accomplished if the user changes these bits.

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External Feedback Termination

NB3N1200K External Feedback Termination

The NB3N1200K utilizes fixed external feedback topology to achieve low input-to-output delay variation. A normal HCSL termination will be needed on the FB_OUT/FB_OUT# pin 15 and pin 16. A combined shunt and series resistors value can be used to form a single termination resistor for the R_{FB_term} .

The termination resistor value is the sum of the R_s and R_p values.

For 100 Ω trace impedance line:

$$R_s = 33 \Omega; R_p = 49.9 \Omega$$

$$\text{Therefore, } R_{FB_term} = 82.9 \Omega$$

NOTE: Use the standard 82.5 Ω , 1% resistor value.

For 85 Ω trace impedance line:

$$R_s = 27 \Omega; R_p = 43.2 \Omega$$

$$\text{Therefore, } R_{FB_term} = 70.2 \Omega$$

NOTE: Use the standard 69.8 Ω , 1% resistor value.

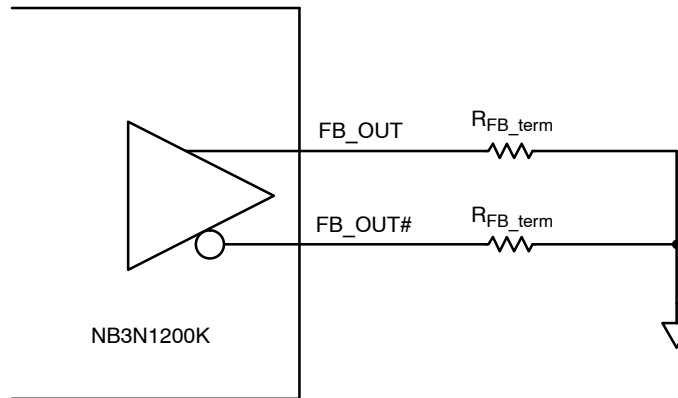


Figure 10. External Feedback Example Schematic

Table 19. FEEDBACK TERMINATION RESISTORS

| Board Trace Impedance | R_{FB_term} | Units |
|-----------------------|----------------|----------|
| 100 | 82.5 1% | Ω |
| 85 | 69.8 1% | Ω |

NB3W1200L Feedback Termination

There is no termination resistor needed at pin 15 and pin 16 of the NB3W1200L NMOS push-pull low power buffer. Pin 15 and pin 16 of the NB3W1200L are no connect (NC) pins. These pins have an active signal on them, so they MUST be left unconnected.

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Byte Read/Write

Reading or writing a register in a SMBus slave device in byte mode always involves specifying the register number.

Read. The standard byte read is as shown in the following figure. It is an extension of the byte write. The write start condition is repeated then the slave device starts sending

data and the master acknowledges it until the last byte is sent. The master terminates the transfer with a NAK, then a stop condition. For byte operation, the 2*7th bit of the command byte must be set. For block operations, the 2*7th bit must be reset. If the bit is not set, the next byte must be the byte transfer count.

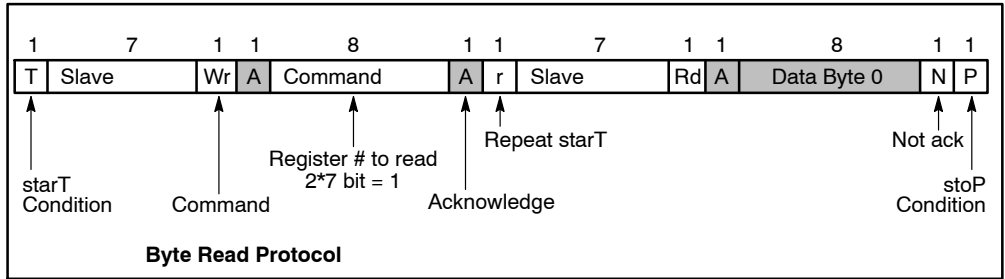


Figure 11. Byte Read Protocol

Write. The following figure illustrates a simple typical byte write. For byte operation the 2*7th bit of the command byte must be set. For block operations, the 2*7th bit must be reset.

If the bit is not set, the next byte must be the byte transfer count. The count can be between 1 and 32. It is not allowed to be zero or exceed 32.

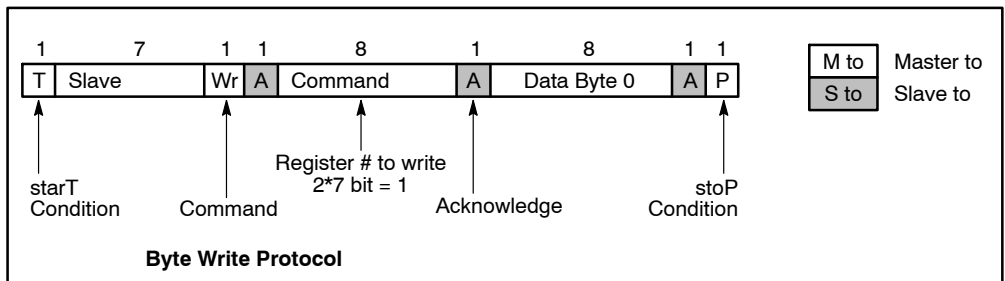


Figure 12. Byte Write Protocol

Block Read/Write

Read. After the slave address is sent with the r/w condition bit *set*, the command byte is sent with the MSB = 0. The slave Ack's the register index in the command byte. The master sends a repeat start function. After the slave Ack's this, the

slave sends the number of bytes it wants to transfer (>0 and <33). The master Ack's each byte except the last and sends a stop function.

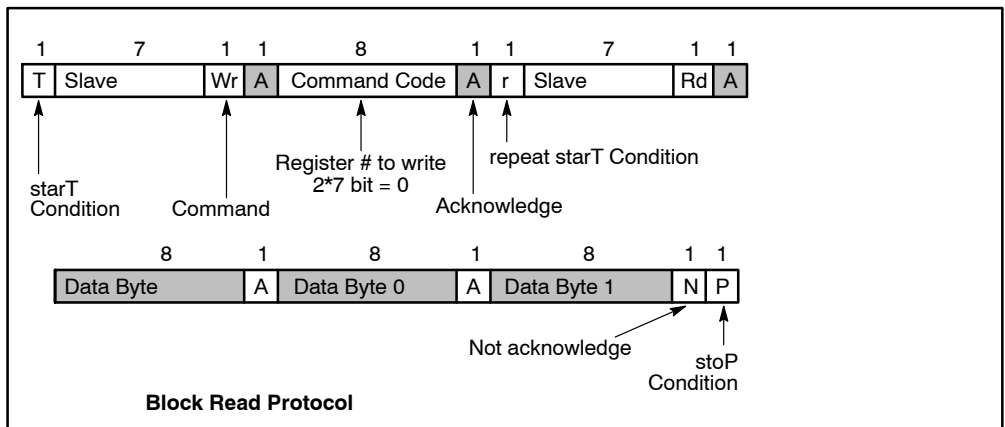


Figure 13. Block Read Protocol

NB3N1200K, NB3W1200L

Write. After the slave address is sent with the r/w condition bit not set, the command byte is sent with the MSB = 0. The lower seven bits indicate what register to start the transfer at. If the command byte is 00h, the slave device will be compatible with existing block mode slave devices. The next byte of a write must be the count of bytes that the master

will transfer to the slave device. The byte count must be greater than zero and less than 33. Following this byte are the data bytes to be transferred to the slave device. The slave device always acknowledges each byte received. The transfer is terminated after the slave sends the Ack and the master sends a stop function.

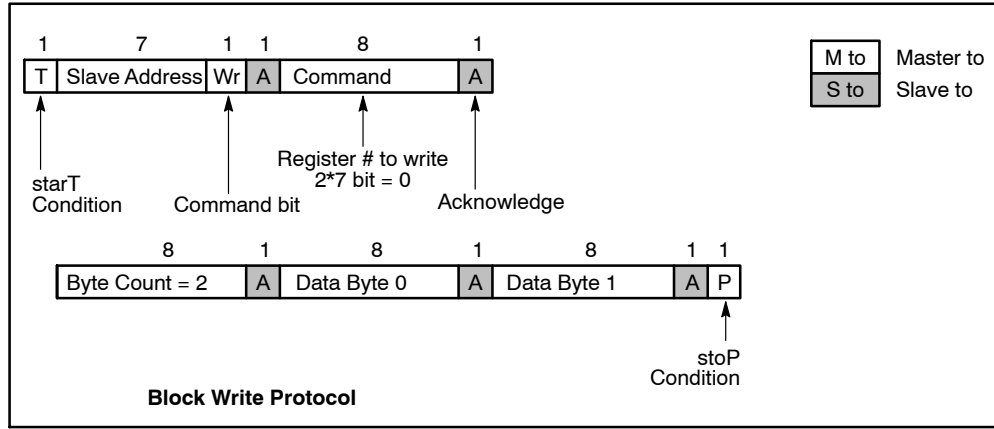


Figure 14. Block Write Protocol

NB3N1200K/NB3W1200L Control Register

Table 20. BYTE 0: FREQUENCY SELECT, OUTPUT ENABLE, PLL MODE CONTROL REGISTER

| Bit | Description | If Bit = 0 | If Bit = 1 | Type | Default | Output(s) Affected |
|-----|----------------------------------|---------------------------------------|---------------|------|---------------------|--------------------|
| 0 | 100M_133M# Frequency Select (FS) | 133 MHz | 100 MHz | R | Latched at power up | DIF[11:0] |
| 1 | PLL Mode 0 | See PLL Operating Mode Readback Table | | RW | 1 | |
| 2 | PLL Mode 1 | | | RW | 1 | |
| 3 | PLL Software Enable | HW Latch | SMBUS Control | RW | 0 | |
| 4 | Reserved | | | | 0 | |
| 5 | Reserved | | | | 0 | |
| 6 | PLL Mode 0 | See PLL Operating Mode Readback Table | | R | Latched at power up | |
| 7 | PLL Mode 1 | See PLL Operating Mode Readback Table | | R | Latched at power up | |

NOTE: Byte 0, bit [3:1] are BW PLL SW enable for the NB3W1200L and NB3N1200K. Setting bit 3 to '1' allows the user to override the Latch value from pin 5 via use of bits 2 and 1. Use the values from the PLL Operating Mode Readback Table. Note that Bits 7 and 6 will keep the value originally latched on pin 5. A warm reset of the system will have to be accomplished if the user changes these bits.

NB3N1200K, NB3W1200L

Table 21. BYTE 1: OUTPUT ENABLE CONTROL REGISTER

| Bit | Description | If Bit = 0 | If Bit = 1 | Type | Default | Output(s) Affected |
|-----|---------------------|-----------------------|------------|------|---------|--------------------|
| 0 | Output Enable DIF 0 | Hi-Z for NB3N1200K | Enabled | RW | 1 | DIF_0, DIF_0# |
| | | Low/Low for NB3W1200L | | | | |
| 1 | Output Enable DIF 1 | Hi-Z for NB3N1200K | Enabled | RW | 1 | DIF_1, DIF_1# |
| | | Low/Low for NB3W1200L | | | | |
| 2 | Output Enable DIF 2 | Hi-Z for NB3N1200K | Enabled | RW | 1 | DIF_2, DIF_2# |
| | | Low/Low for NB3W1200L | | | | |
| 3 | Output Enable DIF 3 | Hi-Z for NB3N1200K | Enabled | RW | 1 | DIF_3, DIF_3# |
| | | Low/Low for NB3W1200L | | | | |
| 4 | Output Enable DIF 4 | Hi-Z for NB3N1200K | Enabled | RW | 1 | DIF_4, DIF_4# |
| | | Low/Low for NB3W1200L | | | | |
| 5 | Output Enable DIF 5 | Hi-Z for NB3N1200K | Enabled | RW | 1 | DIF_5, DIF_5# |
| | | Low/Low for NB3W1200L | | | | |
| 6 | Output Enable DIF 6 | Hi-Z for NB3N1200K | Enabled | RW | 1 | DIF_6, DIF_6# |
| | | Low/Low for NB3W1200L | | | | |
| 7 | Output Enable DIF 7 | Hi-Z for NB3N1200K | Enabled | RW | 1 | DIF_7, DIF_7# |
| | | Low/Low for NB3W1200L | | | | |

Table 22. BYTE 2: OUTPUT ENABLE CONTROL REGISTER

| Bit | Description | If Bit = 0 | If Bit = 1 | Type | Default | Output(s) Affected |
|-----|----------------------|-----------------------|------------|------|---------|--------------------|
| 0 | Output Enable DIF 8 | Hi-Z for NB3N1200K | Enabled | RW | 1 | DIF_8, DIF_8# |
| | | Low/Low for NB3W1200L | | | | |
| 1 | Output Enable DIF 9 | Hi-Z for NB3N1200K | Enabled | RW | 1 | DIF_9, DIF_9# |
| | | Low/Low for NB3W1200L | | | | |
| 2 | Output Enable DIF 10 | Hi-Z for NB3N1200K | Enabled | RW | 1 | DIF_10, DIF_10# |
| | | Low/Low for NB3W1200L | | | | |
| 3 | Output Enable DIF 11 | Hi-Z for NB3N1200K | Enabled | RW | 1 | DIF_11, DIF_11# |
| | | Low/Low for NB3W1200L | | | | |
| 4 | Reserved | | | | | |
| 5 | Reserved | | | | | |
| 6 | Reserved | | | | | |
| 7 | Reserved | | | | | |

NB3N1200K, NB3W1200L

Table 23. BYTE 3: OE_[7:0]# PINS REALTIME READBACK CONTROL REGISTER

| Bit | Description | If Bit = 0 | If Bit = 1 | Type | Default | Output(s) Affected |
|-----|-------------|------------|------------|------|---------|--------------------|
| 0 | Reserved | | | | 0 | |
| 1 | Reserved | | | | 0 | |
| 2 | Reserved | | | | 0 | |
| 3 | Reserved | | | | 0 | |
| 4 | Reserved | | | | 0 | |
| 5 | Reserved | | | | 0 | |
| 6 | Reserved | | | | 0 | |
| 7 | Reserved | | | | 0 | |

Table 24. BYTE 4: OE_[11:8]# PINS REALTIME READBACK CONTROL REGISTER

| Bit | Description | If Bit = 0 | If Bit = 1 | Type | Default | Output(s) Affected |
|-----|-------------|------------|------------|------|---------|--------------------|
| 0 | Reserved | | | | 0 | |
| 1 | Reserved | | | | 0 | |
| 2 | Reserved | | | | 0 | |
| 3 | Reserved | | | | 0 | |
| 4 | Reserved | | | | 0 | |
| 5 | Reserved | | | | 0 | |
| 6 | Reserved | | | | 0 | |
| 7 | Reserved | | | | 0 | |

Table 25. BYTE 5: VENDOR/REVISION IDENTIFICATION CONTROL REGISTER

| Bit | Description | If Bit = 0 | If Bit = 1 | Type | Default | |
|-----|---------------------|-------------------------|------------|------|---------|---------------|
| 0 | Vendor ID Bit 0 | 1111 = ON Semiconductor | | R | 1 | Vendor ID |
| 1 | Vendor ID Bit 1 | | | R | 1 | |
| 2 | Vendor ID Bit 2 | | | R | 1 | |
| 3 | Vendor ID Bit 3 | | | R | 1 | |
| 4 | Revision Code Bit 0 | 0011 | | R | X | Revision Code |
| 5 | Revision Code Bit 1 | | | R | X | |
| 6 | Revision Code Bit 2 | | | R | X | |
| 7 | Revision Code Bit 3 | | | R | X | |

NB3N1200K, NB3W1200L

Table 26. BYTE 6: DEVICE ID CONTROL REGISTER

| Bit | Description | If Bit = 0 | If Bit = 1 | Type | 1200K | 1200L |
|-----|-------------------|--|------------|------|-------|-------|
| 0 | Device ID 0 | 1200K = 120d = 78hex 1200L = 130d = 82hex | | R | 0 | 0 |
| 1 | Device ID 1 | | | R | 0 | 1 |
| 2 | Device ID 2 | | | R | 0 | 0 |
| 3 | Device ID 3 | | | R | 1 | 0 |
| 4 | Device ID 4 | | | R | 1 | 0 |
| 5 | Device ID 5 | | | R | 1 | 0 |
| 6 | Device ID 6 | | | R | 1 | 0 |
| 7 | Device ID 7 (MSB) | | | R | 0 | 1 |

Table 27. BYTE 7: BYTE COUNT REGISTER

| Bit | Description | If Bit = 0 | If Bit = 1 | Type | Default | |
|-----|--|------------|------------|------|---------|---|
| 0 | BC0 – Writing to this register configures how many bytes will be read back | | | RW | 0 | |
| 1 | BC1 – Writing to this register configures how many bytes will be read back | | | RW | 0 | |
| 2 | BC2 – Writing to this register configures how many bytes will be read back | | | RW | 0 | |
| 3 | BC3 – Writing to this register configures how many bytes will be read back | | | RW | 1 | |
| 4 | BC4 – Writing to this register configures how many bytes will be read back | | | RW | 0 | |
| 5 | Reserved | | | | | 0 |
| 6 | Reserved | | | | | 0 |
| 7 | Reserved | | | | | 0 |

Table 28. BYTE 8 AND BEYOND: VENDOR SPECIFIC

| Bit | Description | If Bit = 0 | If Bit = 1 | Type | Default | |
|-----|-------------|------------|------------|------|---------|---|
| 0 | Reserved | | | | | 0 |
| 1 | Reserved | | | | | 0 |
| 2 | Reserved | | | | | 0 |
| 3 | Reserved | | | | | 0 |
| 4 | Reserved | | | | | 0 |
| 5 | Reserved | | | | | 0 |
| 6 | Reserved | | | | | 0 |
| 7 | Reserved | | | | | 0 |

Buffer Power-Up State Machine

Table 29. BUFFER POWER-UP STATE MACHINE

| State | Description |
|-------|---|
| 0 | 3.3 V Buffer power off |
| 1 | After 3.3 V supply is detected to rise above 1.8 V–2.0 V, the buffer enters State 1 and initiates a 0.1 ms–0.3 ms delay. |
| 2 | Buffer waits for a valid clock on the CLK input and PWRDN# de-assertion |
| 3 | Once the PLL is locked to the CLK_IN input clock, the buffer enters state 3 and enables outputs for normal operation. (Notes 47, 48) |

47. The total power up latency from power on to all outputs active must be less than 1.8 ms (assuming a valid clock is present on CLK_IN input).
 48. If power is valid and powerdown is de-asserted but no input clocks are present on the CLK_IN input, DIF clocks must remain disabled. Only after valid input clocks are detected, valid power, PWRDN# de-asserted with the PLL locked/stable and the DIF outputs enabled.

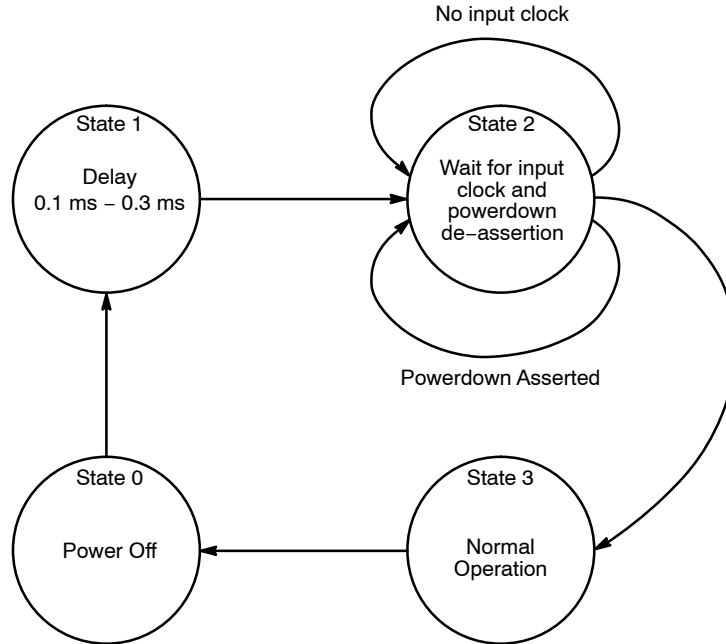


Figure 15. Buffer Power-Up State Diagram

NB3N1200K, NB3W1200L

Table 30. DIF CLOCK OUTPUT CURRENT

| Board Target Trace/Term Z | Reference R, $I_{ref} = V_{DD}/(3 \cdot R_r)$ | Output Current | $V_{OH} @ Z$ |
|---------------------------|--|----------------------------|-----------------------|
| 100 Ω | $R_{REF} = 475 \Omega$ 1%, $I_{ref} = 2.32 \text{ mA}$ | $I_{OH} = 6 \cdot I_{ref}$ | 0.7 V @ 50 Ω |
| 85 Ω | $R_{REF} = 412 \Omega$, 1%, $I_{ref} = 2.67 \text{ mA}$ | $I_{OH} = 6 \cdot I_{ref}$ | 0.7 V @ 43.2 Ω |

NMOS Push-Pull Buffer Specifications for NB3W1200L

Low Power NMOS Push-Pull Differential Buffer

The NB3W1200L utilizes the low-power output buffer for all differential clocks. This buffer uses efficient NMOS

push-pull drivers powered off a low voltage rail, offering a reduction in power consumption, improved edge rate performance, and cross point voltage control.

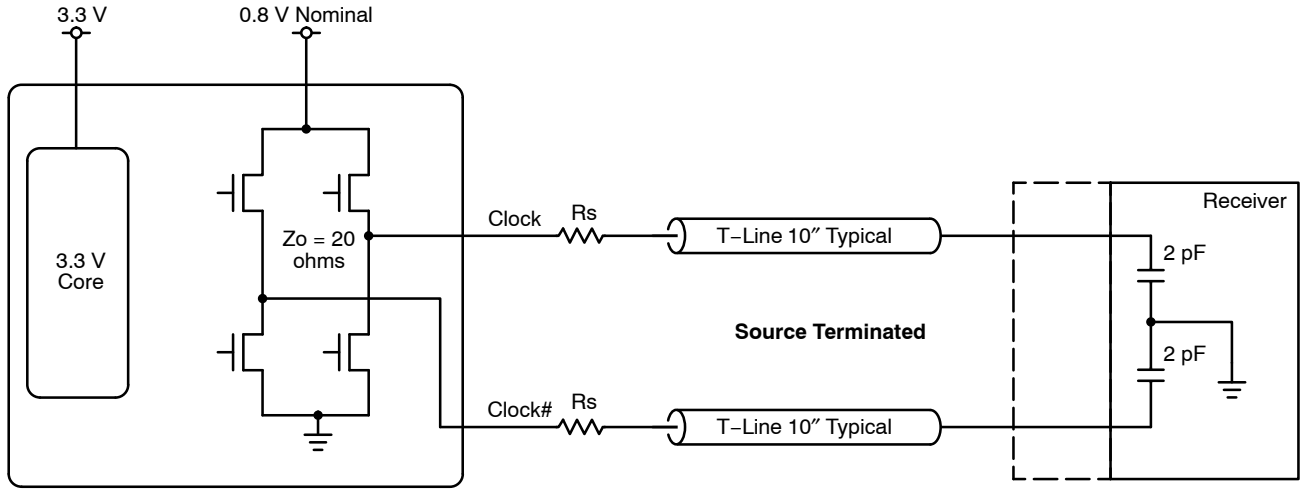


Figure 16. NMOS Push-Pull Buffer Diagram

Power Filtering Example

Ferrite Bead Power Filtering

Recommended ferrite bead filtering equivalent to the following:

600 Ω impedance at 100 MHz, $\leq 0.1 \Omega$ DCR max., $\geq 400 \text{ mA}$ current rating.

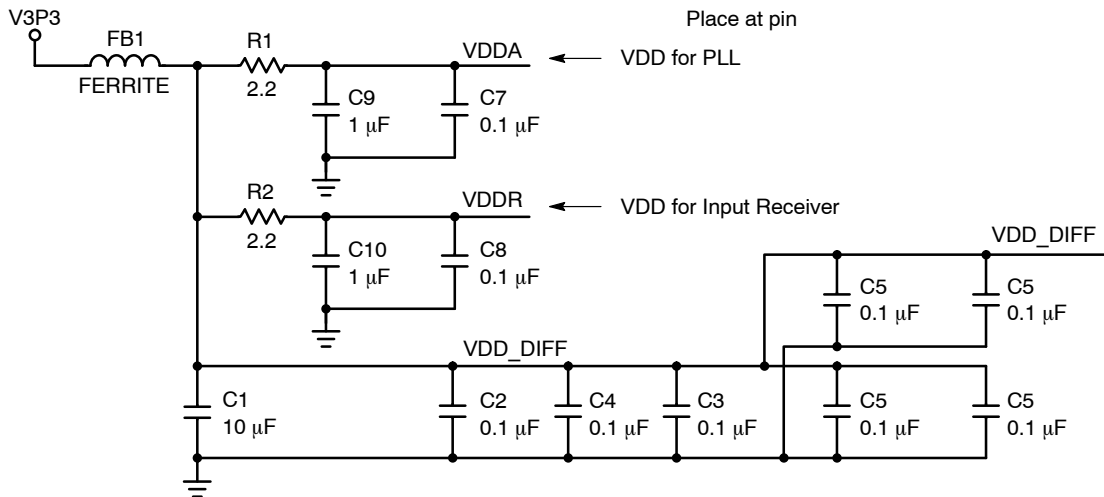


Figure 17. Schematic Example of the NB3N1200K / NB3W1200L Power Filtering

NB3N1200K, NB3W1200L

Termination of Differential Outputs

Table 31. NB3N1200K RESISTIVE LUMPED TEST LOADS FOR DIFFERENTIAL CLOCKS

| Clock | Board Trace Impedance | R_s | R_p | $R_{I_{ref}}$ | Units |
|--|-----------------------|----------|------------|---------------|----------|
| DIFF Clocks – 50 Ω configuration | 100 | 33 5% | 49.9 1% | 475 1% | Ω |
| DIFF Clocks – 43 Ω configuration | 85 | 27 5% | 42.2 1% | 412 1% | Ω |

Table 32. NB3W1200L RESISTIVE LUMPED TEST LOADS FOR DIFFERENTIAL CLOCKS

| Clock | Board Trace Impedance | R_s | R_p | $R_{I_{ref}}$ | Units |
|--|-----------------------|----------|-------|---------------|----------|
| DIFF Clocks – 50 Ω configuration | 100 | 33 5% | N/A | N/A | Ω |
| DIFF Clocks – 43 Ω configuration | 85 | 27 5% | N/A | N/A | Ω |

Termination of Differential HCSL Type Outputs (NB3N1200K)

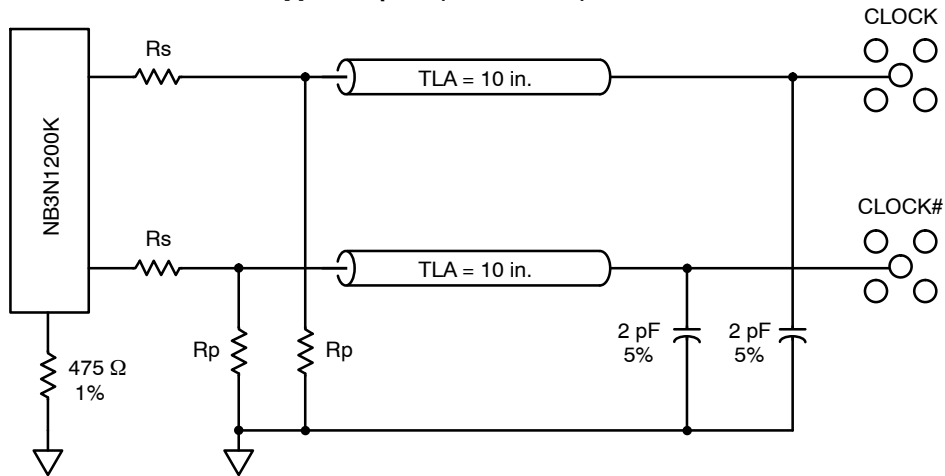


Figure 18. 0.7 V Configuration Test Load Board Termination for HCSL NB3N1200K

Termination of Differential NMOS Push– Pull Type Outputs (NB3W1200L)

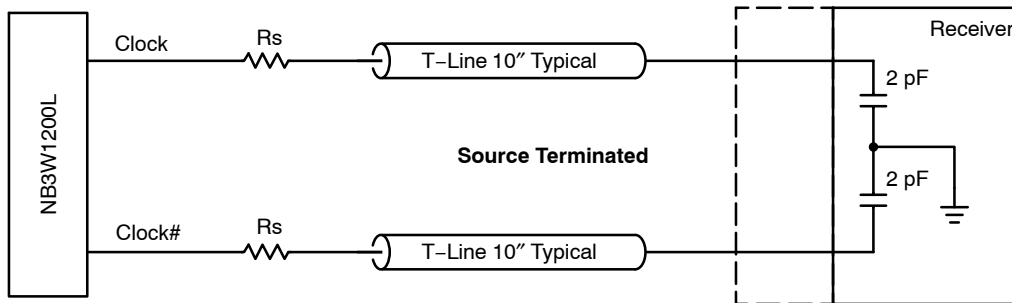


Figure 19. 0.7 V Configuration Test Load Board Termination for NMOS Push–Pull NB3W1200L

NB3N1200K, NB3W1200L

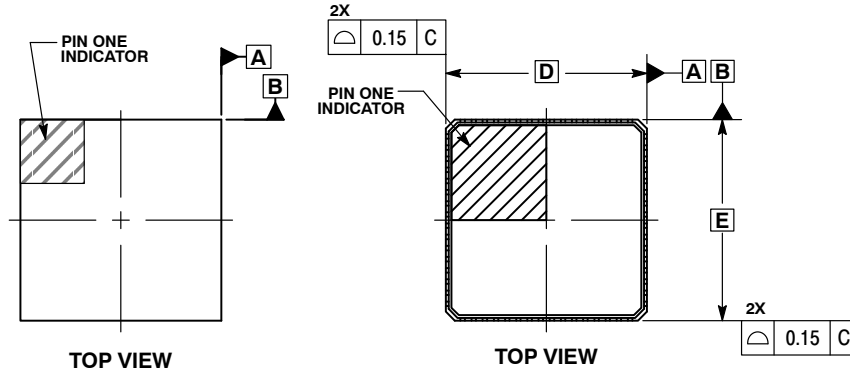
PACKAGE DIMENSIONS

QFN64 9x9, 0.5P (PUNCH & SAWN)
CASE 485DH
ISSUE O

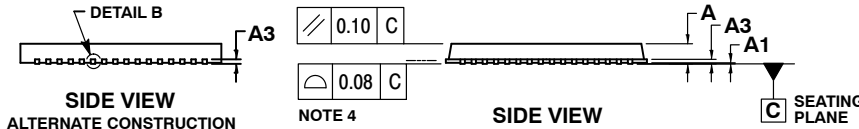
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25mm FROM THE TERMINAL TIP
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. ALL DIMENSIONS APPLY TO BOTH THE SAWN AND PUNCH PACKAGES.

| MILLIMETERS | | |
|-------------|------|------|
| DIM | MIN | MAX |
| A | 0.80 | 1.00 |
| A1 | 0.00 | 0.05 |
| A3 | 0.20 | REF |
| b | 0.18 | 0.30 |
| D | 9.00 | BSC |
| D2 | 5.90 | 6.25 |
| E | 9.00 | BSC |
| E2 | 5.90 | 6.25 |
| e | 0.50 | BSC |
| L | 0.30 | 0.50 |
| L1 | 0.00 | 0.15 |

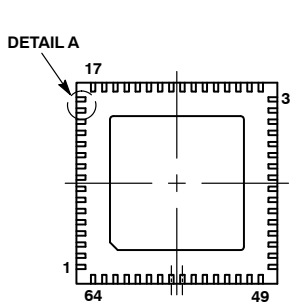


TOP VIEW
ALTERNATE CONSTRUCTION

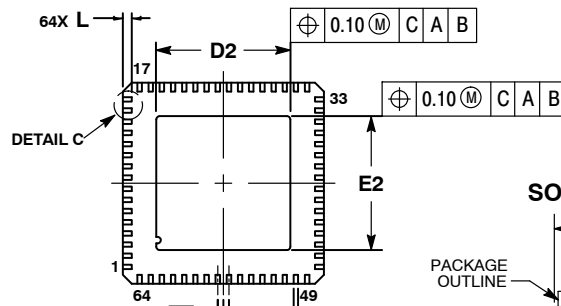


SIDE VIEW
ALTERNATE CONSTRUCTION

SIDE VIEW

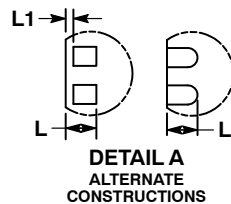
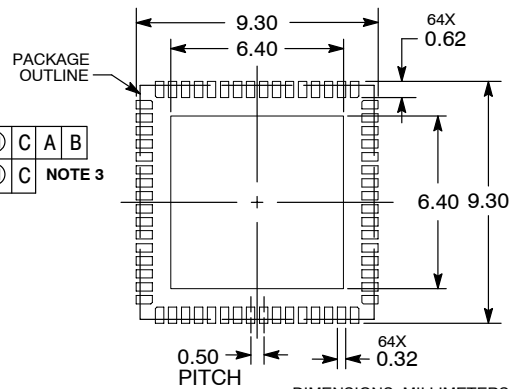


BOTTOM VIEW
ALTERNATE CONSTRUCTION

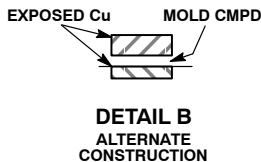


BOTTOM VIEW

RECOMMENDED SOLDERING FOOTPRINT



DETAIL A
ALTERNATE CONSTRUCTIONS



DETAIL B
ALTERNATE CONSTRUCTION



DETAIL C
ALTERNATE CONSTRUCTION

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