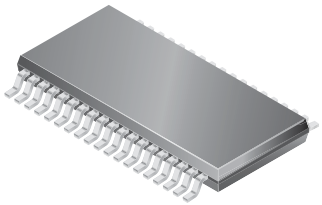
Quad High-Side Gate Driver for Automotive Applications

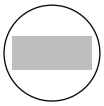
Features and Benefits

- Drives four N-channel high-side MOSFETS
- Charge pump for 100% duty cycle operation
- Serial and discrete inputs
- SPI port for control and fault diagnostics
- 4.5 to 60 V input voltage range
- Sleep function for minimum power drain
- Thin profile 38-lead TSSOP with internally fused leads for enhanced thermal dissipation
- Lead (Pb) free
- Device protection features:
  - Short-to-ground detection (latched)
  - Short-to-battery protection (latched)
  - Open load detection (latched)
  - V_{DD} undervoltage lockout
  - V_{CP} undervoltage lockout
  - Thermal monitor

Package: 38 pin TSSOP (suffix LG)



Approximate Scale 1:1



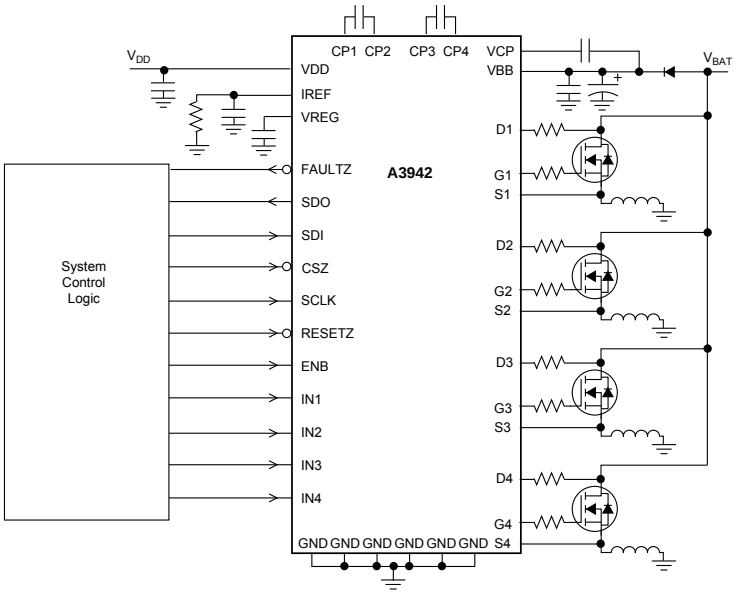
Description

The A3942 is a highly-integrated gate driver IC that can drive up to four N-Channel MOSFETs in a high-side configuration. The device is designed to withstand the harsh environmental conditions and high reliability standards of automotive applications.

Serial Peripheral Interface (SPI) compatibility makes the device easily integrated into existing applications. The MOSFETs in such applications are typically used to drive gasoline or diesel engine management actuators, transmission actuators, body control actuators and other general-purpose automotive or industrial loads. In particular, the A3942 is suited for driving glow plugs, valves, solenoids, and other inductive loads in engine management and transmission systems.

The device is available in a 38-lead thin (1.20 mm maximum overall height) TSSOP package with six pins that are fused internally to provide enhanced thermal dissipation (package LG). It is lead (Pb) free with 100% matte tin leadframe plating.

Typical Application



Selection Guide

Part Number	Packing
A3942KLGTR-T	4000 pieces per reel

Absolute Maximum Ratings*

Characteristic	Symbol	Notes	Rating	Units
VBB, CP1, CP3 Pins Voltage			–0.3 to 60	V
Dx (Drain Detect) Pins Voltage	V_{Dx}		V_{BB} – 6 V to V_{BB} + 0.5 V	V
Sx (Output Source) Pins Voltage	V_{Sx}		–10 to 60	V
VCP, CP2, CP4, Gx Pins Voltage			–0.3 to 74	V
All Other Pins			–0.3 to 7	V
Operating Ambient Temperature	T_A	Range K	–40 to 125	ºC
Maximum Junction Temperature	T_J(max)		150	ºC
Storage Temperature	T_{stg}		–55 to 150	ºC
ESD Rating, Human Body Model		AEC-Q100-002, all pins	2500	V
ESD Rating, Charged Device Model		AEC-Q100-011, all pins	1050	V

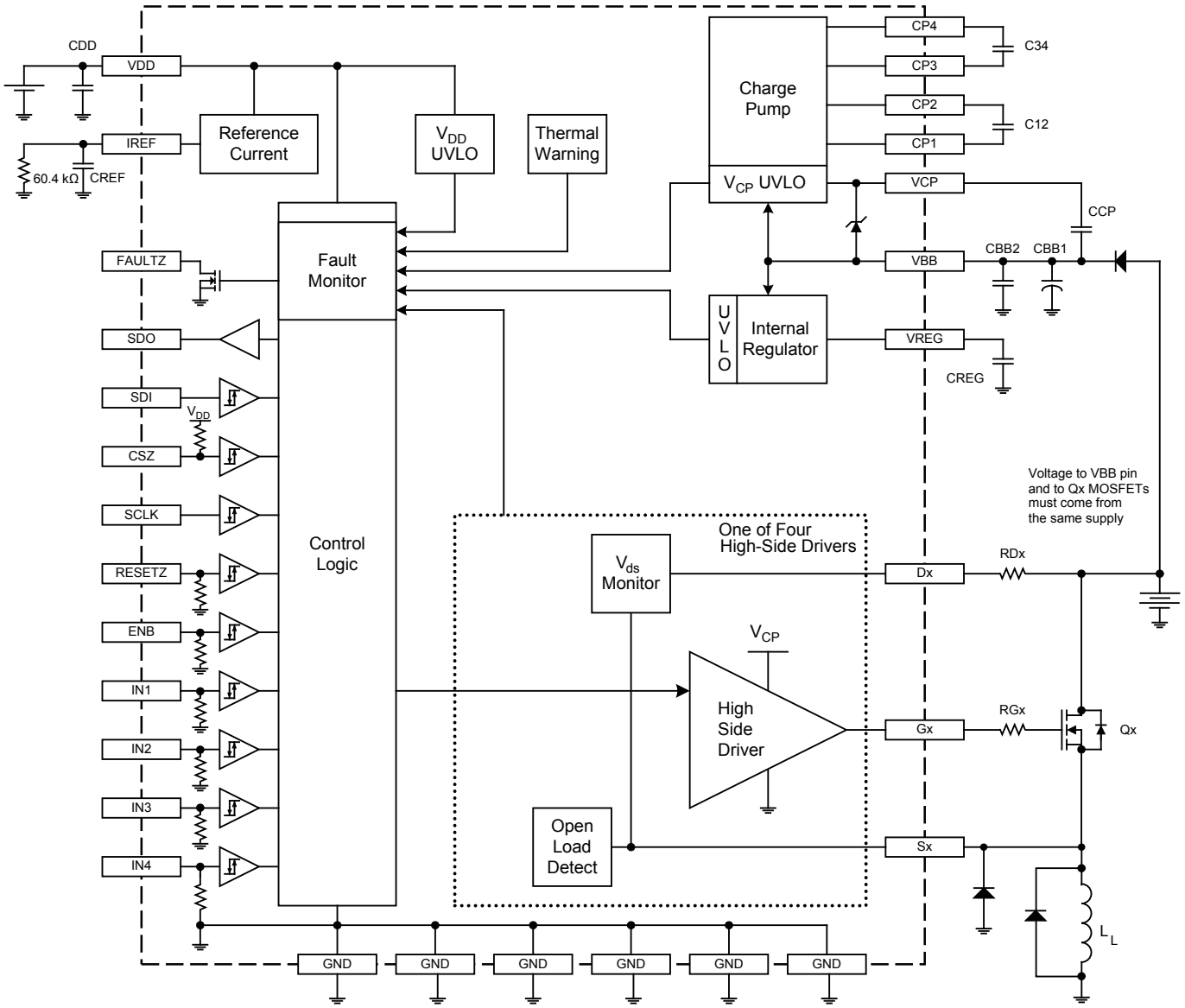
*With respect to ground. Exceeding maximum ratings may cause permanent damage. Correct operation is not guaranteed when absolute maximum conditions are applied.

Thermal Characteristics

Characteristic	Symbol	Test Conditions*	Rating	Units
Package Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	4-layer PCB based on JEDEC standard, with no thermal vias	47	ºC/W

*For additional information, refer to the Allegro website.

Functional Block Diagram



Name	Suitable Characteristics	Representative Device
C12, C34	0.33 µF or 0.47 µF, 25 V, X7R ceramic	
CBB1	47 µF, 63 V, electrolytic	EGXE630ELL470MJC5S
CBB2	0.22 µF, 100 V, X7R ceramic	
CCP	1 µF, 16V, X7R ceramic	
CDD	0.47 µF, 16 V, X7R ceramic	
CREF	47 pF, 16 V, X7R ceramic	
CREG	0.22 µF, 16 V, X7R ceramic	

ELECTRICAL CHARACTERISTICS Valid at –40°C ≤ T_J ≤ 150°C, C12 = C34 = 0.47 µF, CCP = 1 µF, R_{REF} = 60.4 kΩ, and V_{BB} within limits, unless otherwise noted

Characteristics	Symbol	Test Conditions		Min.	Typ.	Max.	Units
Supplies and Regulators							
Operating Voltage	V_{BB}			4.5	–	60	V
Quiescent Current	$I_{BB(Q)}$	Charge pump on, outputs disabled	V_{BB} = 60 V	–	–	10	mA
			V_{BB} = 36 V	–	–	8	mA
		Sleep mode	V_{BB} = 36 V	–	–	15	µA
			V_{BB} = 36 V, T_J = 25°C	–	–	1	µA
Logic Supply (voltage supplied to logic circuits)	V_{DD}			3	–	5.5	V
Logic Supply Current	I_{DD}	V_{DD} = 5.5 V, serial port switching		–	–	3	mA
		V_{DD} = 5.5 V, device quiescent or in sleep mode		–	–	0.5	mA
Logic Supply UVLO Threshold	$V_{DD(UV)}$	V_{DD} falling, FAULTZ pin held active (low) for 1.5 V ≤ V_{DD} ≤ V_{DDUV}		2.6	–	2.9	V
Logic Supply UVLO Hysteresis	$V_{DD(hys)}$			100	150	200	mV
Charge Pump Switching Frequency	f_{CP}			–	100	–	kHz
Charge Pump Output Voltage	V_{CP}	Measured relative to VBB pin	V_{BB} = 12 V, I_{CP} = 10 mA	10	–	13	V
			V_{BB} = 6.0 V, I_{CP} = 5 mA	10	–	13	V
			V_{BB} = 4.5 V, I_{CP} = 5 mA	7	–	11	V
Charge Pump UVLO	$V_{CP(UV)}$	Relative to VBB pin, V_{CP} falling		5.1	–	5.8	V
Internal Regulator Voltage	V_{REG}	CREG = 0.22 µF		–	4	–	V
Regulator Voltage UVLO	$V_{REG(UV)}$	V_{REG} falling		3	–	3.8	V
Regulator Voltage UVLO Hysteresis	$V_{REG(hys)}$			100	–	400	mV
Control Circuits							
Current Reference Source Voltage	V_{REF}			1.14	1.2	1.26	V
Master Reset Pulse	t_{RESET}	RESETZ pin pulsed low		0.3	–	5	µs
Sleep Command	t_{SLEEP}	RESETZ pin held low		20	–	–	µs
Wake-Up Delay	t_{WAKE}	RESETZ pin held high; CCP = 1 µF		–	–	2	ms
Logic I/O							
Logic Input Voltage, High	V_{IH}			0.7 × V_{DD}	–	V_{DD}	V
Logic Input Voltage, Low	V_{IL}			0	–	0.3 × V_{DD}	V

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ELECTRICAL CHARACTERISTICS (continued) Valid at –40°C ≤ T_J ≤ 150°C, C12 = C34 = 0.47 µF, CCP = 1 µF, R_{REF} = 60.4 kΩ, and V_{BB} within limits, unless otherwise noted

Characteristics	Symbol	Test Conditions		Min.	Typ.	Max.	Units
Logic Input Hysteresis	V_{hys}			0.1 × V_{DD}	–	–	V
Logic Input Current[1]	$I_{I(HI)}$	CSZ pin	$V_I = V_{DD}$ = 5.5 V	–	–	10	µA
		SDI and SCLK Pins		–	–	5	µA
		All other pins		–	–	100	µA
	$I_{I(LO)}$	CSZ pin	V_I = 0 V	–	–	–100	µA
		SDI and SCLK Pins		–	–	–5	µA
		All other pins		–	–	–10	µA
Logic Output Voltage, SDO Pin (CMOS push-pull circuit)	$V_{OUT(HI)}$	I_{OUT} = –1 mA		V_{DD} – 0.5	–	V_{DD}	V
	$V_{OUT(LO)}$	I_{OUT} = 1 mA		–	–	0.4	V
FAULTZ Pin Active (Low) Voltage	$V_{FAULTZ(LO)}$	I_{FAULTZ} = 1 mA, V_{DD} = 1.5 V, V_{BB} = 4.5 V		–	–	0.4	V
FAULTZ Pin Inactive (High) Current	$I_{FAULTZ(HI)}$	V_{FAULTZ} = 5 V		–	–	10	µA
Drivers							
Gate Voltage, High	$V_{G(HI)}$	Measured relative to Sx pin, capacitive load–fully charged		V_{CP} – 1	–	V_{CP}	V
Gate Voltage, Low	$V_{G(LO)}$	Measured relative to Sx pin, capacitive load–fully discharged		–	–	0.1	V
Peak Gate Current[1,2]	$I_{G(HI)}$	R_G = 0 Ω, 1 V ≤ V_{GS} ≤ 4 V, V_{Sx} = V_{BB}	V_{BB} = 4.5 V, V_{CP} = 9 V	–10	–	–	mA
			V_{BB} ≥ 9 V, V_{CP} = 13 V	–15	–	–	mA
	$I_{G(LO)}$	R_G = 0 Ω, V_{GS} = 1 V, V_{Sx} = 0 V		10	–	–	mA
		R_G = 0 Ω, 2 V ≤ V_{GS} ≤ 4 V, V_{Sx} = 0 V		25	–	–	mA
Propagation Delay	$t_{p(on)}$	From 90% V_{INx} to V_{Gx} – V_{Sx} = 200 mV		–	0.6	–	µs
	$t_{p(off)}$	From 10% V_{INx} to V_{CP} – V_{Gx} = 200 mV		–	0.6	–	µs
Gate-to-Source Resistance	R_{GS}	RESETZ pin held low; V_{GSZ} = 10 V		300	500	800	kΩ
Gate-to-Source Zener Diode Voltage	$V_{GS(Z)}$	I_G = 2 mA		15	–	18	V
Drain Leakage Current	I_{Dlkg}	RESETZ pin held low, V_{BB} = V_{Dx} = 60 V		–	–	10	µA
		RESETZ pin held low, V_{BB} = V_{Dx} = 36 V	T_J = 150°C	–	–	5	µA
			T_J = 25°C	–	–	1	µA

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ELECTRICAL CHARACTERISTICS (continued) Valid at –40°C ≤ T_J ≤ 150°C, C12 = C34 = 0.47 µF, CCP = 1 µF, R_{REF} = 60.4 kΩ, and V_{BB} within limits, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Driver Fault Detection						
Drain Fault Detect Current	I_{Dx}	V_{BB} = 60 V	75	100	125	µA
		V_{BB} = 36 V	85	100	120	µA
Drain Fault Detect Voltage[3]	V_{Dx}	V_{BB} ≥ 9 V	V_{BB} – 3	–	V_{BB} + 0.2	V
		V_{BB} = 6 V	5	–	V_{BB} + 0.2	V
		V_{BB} = 4.5 V	4	–	V_{BB} + 0.2	V
Open Load Detect Source Current[1]	I_{OL}	V_{Sx} = 1.35 V; 4.5 V ≤ V_{BB} ≤ 36 V	–48	–	–82	µA
Open Load Detect Voltage	V_{OL}		1.4	1.5	1.6	V
Open Load V_{Sx} Clamp	V_{CLAMP}	Active (when an open load fault is active), V_{BB} ≤ 36 V	–	–	5	V
	I_{CLAMP}	Current limit in short-to-battery; V_{Sx} =V_{BB} = 36 V	–	–	200	µA
Turn-On Blank Time	$t_{ON(00)}$	$t_{ON(00)}$ is the default, T_J = 150°C	2.5	–	3.4	µs
	$t_{ON(01)}$		3.7	–	5.9	µs
	$t_{ON(10)}$		5.6	–	11.2	µs
	$t_{ON(11)}$		8.9	–	22.3	µs
Turn-Off Blank Time	t_{OFF}		–	t_{ON}	–	µs
Short-to-Ground Fault Detect Filter Delay	t_{STG}	From V_{Sx} < V_{Dx} to 90% V_{FAULTZ}	–	1	1.2	µs
STB Comparator Offset Voltage	$V_{OS(STB)}$		–	–	60	mV
STG Comparator Offset Voltage	$V_{OS(STG)}$		–	–	45	mV
Temperature Monitor						
Thermal Warning Threshold[4]	T_{WARN}	Temperature rising	155	165	175	°C
Thermal Warning Hysteresis	$T_{WARN(hys)}$		–	15	–	°C

[1]For input and output current specifications, negative current is defined as coming out of (sourcing) the specified device pin.

[2]For $I_{G(HI)}$, V_{CP} relative to V_{BB}.

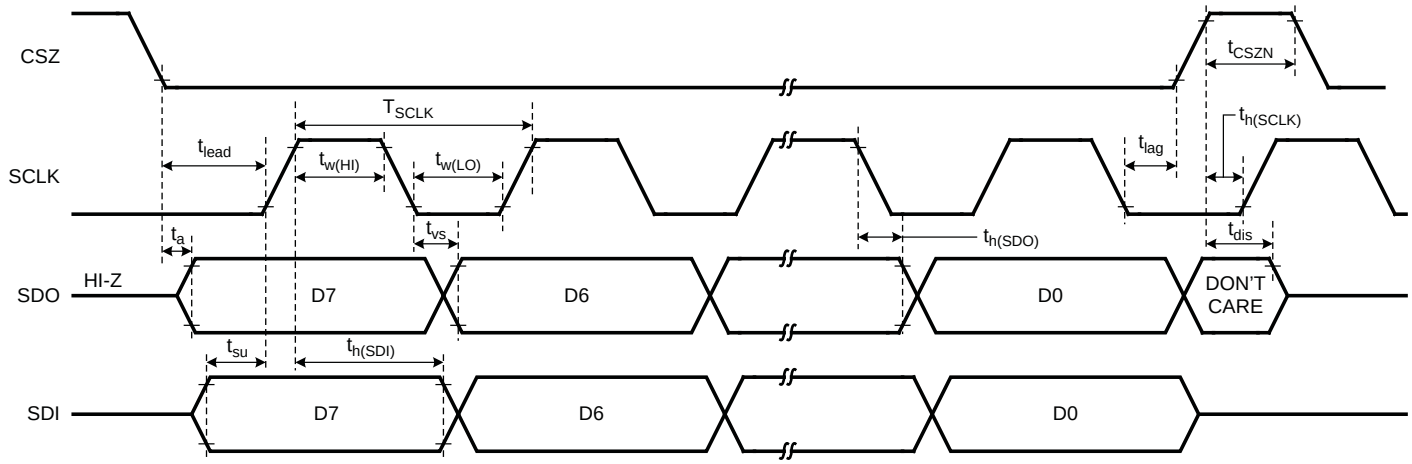
[3]Minimum values of V_{Dx} are specified only to avoid short-to-battery nuisance faults. For more information, refer to the Open Load Fault Level topic in the Applications Information section.

[4]Minimum and maximum not tested; guaranteed by design.

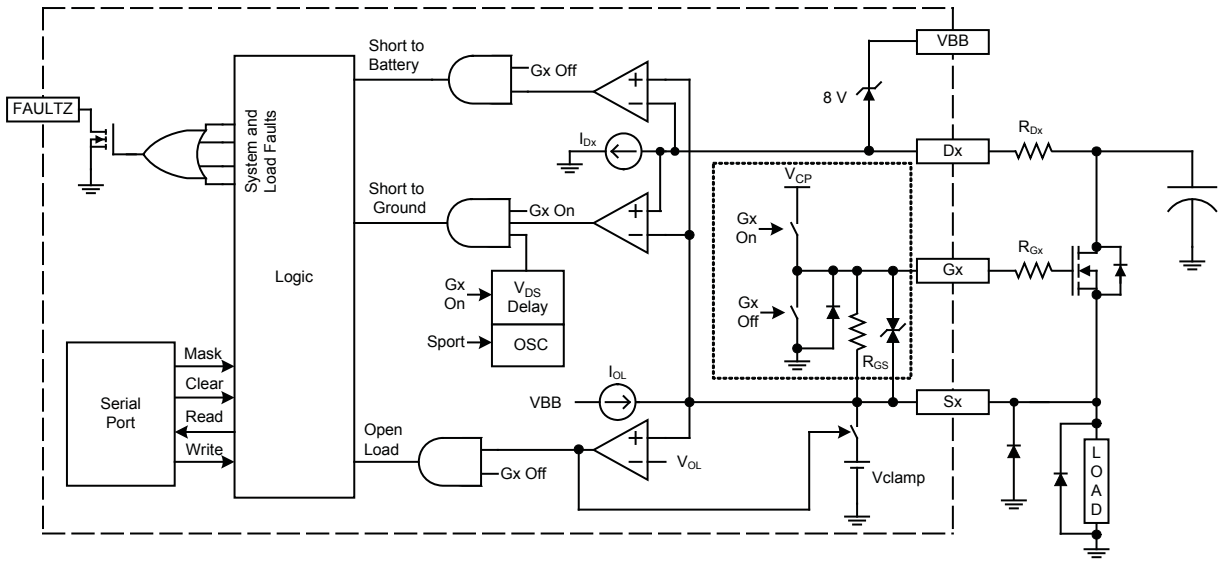
SERIAL PERIPHERAL INTERFACE (SPI) TIMING CHARACTERISTICS Valid at –40°C ≤ T_J ≤ 150°C and V_{BB} and V_{DD} within limits, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Transfer Frequency	f		–	–	8	MHz
Setup Lead Time	t_{lead}		375	–	–	ns
Setup Lag Time	t_{lag}		50	–	–	ns
Setup Time Before Read	t_{su}		15	–	–	ns
Access Time Before Write	t_a	C_{SDO} = 100 pF	–	–	340	ns
Chip Selection Inactive Time	t_{CSZN}		2	–	–	µs
Delay Before Output Disabled	t_{dis}	C_{SDO} = 0 pF	–	–	100	ns
Serial Clock Period	T_{SCLK}		125	–	–	ns
Serial Clock Pulse Width, High	$t_{w(HI)}$		50	–	–	ns
Serial Clock Pulse Width, Low	$t_{w(LO)}$		50	–	–	ns
Serial Clock Hold Time	$t_{h(SCLK)}$		300	–	–	ns
Serial Data In Hold Time	$t_{h(SDI)}$		20	–	–	ns
Serial Data Out Hold Time	$t_{h(SDO)}$	C_{SDO} = 0 pF	0	–	–	ns
Serial Data Out Time Before Valid State	t_{vs}	C_{SDO} = 100 pF, V_{DD} = 3 V	–	–	120	ns
		C_{SDO} = 100 pF, V_{DD} = 4.75 V	–	–	80	ns

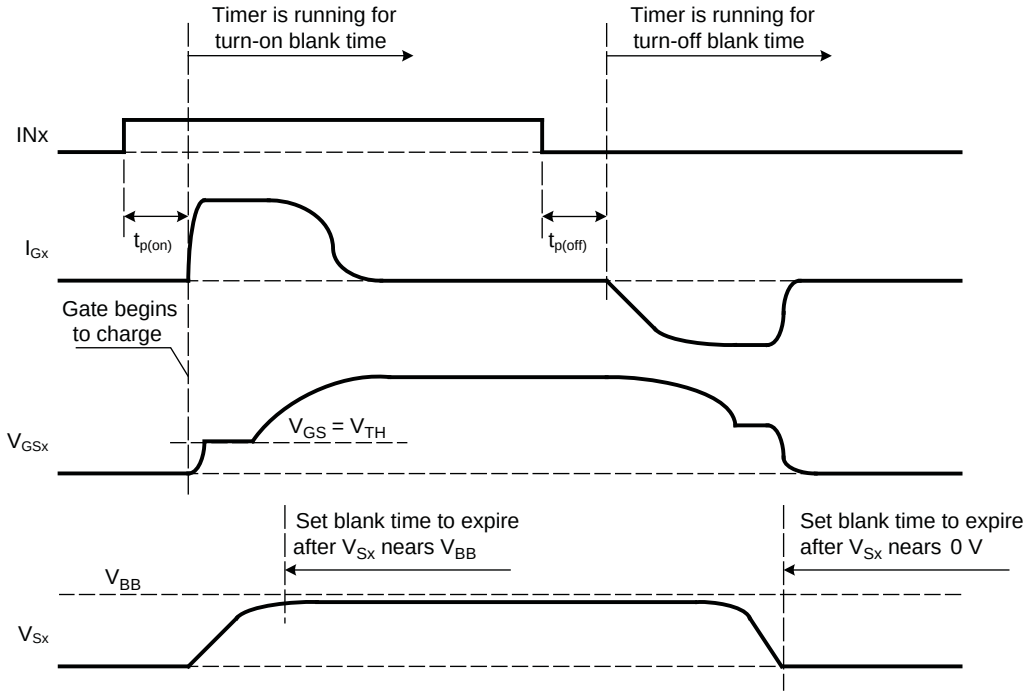
Serial Peripheral Interface (SPI) Timing Diagram



Fault System Block Diagram



Input SettingsTiming Chart



Fault Logic Table

Circled data cells indicate default settings, X indicates “don’t care”, Z indicates high impedance state

Causes									Effects				
				Channel-Specific									
RESETZ	ENB	VDD UVLO	VCP UVLO	Open Load	Short-to-Battery	Short-to-Ground	Off-State Faults Masked	Thermal Warning	FAULTZ	Gx	VCP	VREG	Mode of Operation
1	(0)	0	0	0	0	0	X	0	1	0	1	1	Gates actively pulled low
1	1	0	0	0	0	0	X	0	1	INx	1	1	Normal operation
1	1	0	0	0	0	0	X	(1)	0	INx	1	1	FAULTZ issued but A3942 fully operational
1	1	0	0	X	X	0	(1)	0	1	INx	1	1	Normal operation, OL and STB masked
1	X	0	0	0	0	(1)	X	X	0	0	1	1	STG cannot be masked
1	X	0	0	0	(1)	0	0	X	0	0	1	1	STB
1	X	0	0	(1)	0	0	0	X	0	0	1	1	OL
1	X	0	(1)	X	X	X	X	X	0	0	UV	1	VCP UVLO disables outputs only
1	X	(1)	0	X	X	X	X	X	0	0	1	1	VDD UVLO disables outputs only
(0)	X	X	X	X	X	X	X	X	0	Z	0	0	Sleep mode

Serial Port Registers Description

There are two 8-bit registers served by the serial port, the Input register and the Output Fault register. The structure of the registers is shown in the table at the bottom of this page. The function of each bit in the registers is described in this section.

Input Register

D0 Gate On/Off Bit This bit is used to control the gate drive output. It is logically ORed with the signal on the discrete input pin, INx, corresponding to each of the four channels, according to the following table:

ORed Settings		Result on Gx Pin
Bit D0	Pin INx	
0	0	Off
0	1	On
1	0	On
1	1	On

D1, D2 Short-to-Ground (STG) Turn-On Blank Time MSB and LSB Bits The blank time, $t_{on(xx)}$, delay allows switching transients to settle before the A3942 STG function checks for a short. For each individual channel, the combination of these bits sets the wait time for the V_{DS} monitor, according to the following table:

D2	D1	t_{ON} Selected
0	0	$t_{ON(00)}$*
0	1	$t_{ON(01)}$
1	0	$t_{ON(10)}$
1	1	$t_{ON(11)}$

*default state at device power-on

D3 Clear Faults Bit This bit is used to clear a latched fault. After the fault is cleared, the gate output can again follow the input logic to determine if the fault is still present. Faults are cleared on a channel specific basis.

D4 Mask Off-State Faults Bit [See asterisks (*) in the table below.] When the application requires that Short-to-Battery (STB) and Open Load (OL) faults be checked primarily before output is enabled for the first time, this bit can be used to allow STB and Open Load faults to be ignored during normal operation (Short-to-Ground faults can not be masked). This bit is applied

Serial Port Bit Definition All bits active high, except WriteZ

Register	Bits							
	D7	D6	D5	D4	D3	D2	D1	D0
Input	Address MSB	Address LSB	Input Read Enable	Mask Off-State Faults (*)	Clear Faults	STG Blank Time MSB	STG Blank Time LSB	Gate On/Off
Output Fault	Address MSB	Address LSB	WriteZ	Charge Pump UVLO	Thermal Warning	Open Load Fault (*)	STB Fault (*)	STG Fault

on a channel-specific basis, according to the following table:

D4 Setting	Handling of Off-State Faults
0	Registered
1	Ignored

D5 Read Enable Bit This bit enables or disables reading on the serial inputs, according to the following table:

D5 Setting	Handling of Serial Input
0	Ignored
1	Registered

D6, D7 Address MSB and LSB Bits (Input and Output Fault registers) For channel-specific bits, these bits are used to specify which channel is indicated. The channel-specific bits are:

Register	Channel-Specific Bits
Input	D0, D1, D2, D3, D4
Output	D0, D1, D2

These bits determine the channel, according to the following table:

D7	D6	Channel Selected
0	0	1
0	1	2
1	0	3
1	1	4

Output FAULT Register

D0 Short-to-Ground (STG) Fault Bit The voltage from drain to source for each MOSFET is monitored. An internal current source sinks I_{Dx} from the Dx pins to set the V_{DS} threshold for each channel, the level at which an STG fault condition is evaluated.

The A3942 enables monitoring for an STG fault after the MOSFET is turned on and the turn-on blank time, t_{ON}, expires. (The MOSFET is turned on via the Input register D0 bit, ORed with the INx discrete input pin for the channel of the MOSFET, and t_{ON} is set by Input register D1 and D2 bits). If the MOSFET gate-to-source voltage exceeds the V_{DS} threshold, then an STG fault will be registered for that channel, the MOSFET gate will be discharged, and the FAULTZ pin will be set low (active).

An STG fault is latched until cleared (using the Input register D3 bit). In the meantime, the other channels can continue to operate normally.

D1 Short to Battery (STB) Fault Bit When a channel turns off, STB fault detection is blanked for t_{OFF}. Subsequently, if the Sx pin voltage exceeds the V_{DS} threshold voltage for that channel, an STB fault is latched. The output for that channel is disabled until the fault is either cleared (via the Input register D3 bit) or the off-state fault diagnostics are masked (via the Input register D4 bit).

Because the output is disabled, there is no active pull-down during an STB event. Note that, in general, when the voltage on SX is high enough to trip the STB comparator, it also trips the OL comparator, and both the STB and the OL faults are latched.

D2 Open Load (OL) Fault Bit When a channel turns off, the OL fault is blanked for t_{OFF}. A small bias current, I_{OL}, is sourced to the Sx pin of the channel. There it divides between RSx and the load. If the load is open, the Sx voltage will rise above the OL fault detection threshold. In that case, the output is disabled until the fault is cleared (via the Input register D3 bit) or the off-state fault diagnostics are masked (via the Input register D4 bit).

D3 Thermal Warning Bit A die temperature monitor is integrated on the A3942 chip. If the die temperature

approaches the maximum allowable level, a thermal warning signal will be triggered.

Note that this fault sets the FAULTZ pin low (active), but does not disable the outputs or operation of the chip.

D4 Charge Pump UVLO Bit The charge pump must maintain a voltage guard band above V_{BB}, in order to charge the gates when commanded to turn on the MOSFETs. If an undervoltage (UVLO) condition is detected on the charge pump, the FAULTZ pin will be set low (active), and all outputs will be disabled.

D5 WriteZ (Not Write) Bit In a written byte, D5 = 0.

D6, D7 Address Bits See description, above.

Pin Descriptions

In this section, the functions of the individual terminals of the A3942 are described.

VBB Supply Voltage (Power) The A3942 is fully operational over the specified range of V_{BB}. The external MOSFETs must be supplied by the same voltage source as the A3942. A bypass capacitor should be placed as close as practicable to the A3942.

VDD Supply Voltage (Logic) Logic voltage must be supplied to the A3942. The wide allowable range of input voltages allows both 3.3 V and 5 V supplies. A bypass capacitor should be placed as close as practicable to the A3942.

VCP Charge Pump The integrated charge pump is used to generate a supply above V_{BB} to drive the gates of the external power MOSFETs. This tripler keeps the part functional over a wide range of V_{BB}.

CP1 through CP4 Charge Pump Capacitor Connections These are the connections for the two external capacitors that level-shift the charge up to V_{CP}.

VREG Internal Linear Voltage Regulator This provides a connection for an external capacitor that sets the regulation value for voltage supplied to internal logic circuits.

IN1 through IN4 Discrete Inputs For each output channel, the gate pin, Gx, sources voltage when the corresponding INx pin is set high. Gx sinks voltage to ground when the corresponding INx pin is set low. The INx setting is logically ORed with the Gate On/Off bit (Input register bit D0) for the respective output.

D1 through D4 Output Drains For each output channel, the voltage on the corresponding Dx pin is used to evaluate STB and STG fault conditions. The A3942 compares the Dx voltage level to the V_{DS} threshold of the MOSFET to determine if a fault condition exists. The trip voltage level is set by selecting an appropriate value for the resistor, RDx, connected to the corresponding current sink. Because both the Dx pins and RDx are high impedance, each RDx must be placed as close to the corresponding A3942 Dx pin as practicable.

G1 through G4 Output Gates These pins drive the gates of the high-side external MOSFETs. They source voltage from VCP and sink to GND. The corresponding external gate resistors, RGx, should be $\geq 2\ k\Omega$ for consistent switching times between A3942s when applicable (see $I_{G(HI)}$ and $I_{G(LO)}$ in the Electrical Characteristics table).

If negative voltages are applied, Gx is clamped to GND by internal diodes. Back-to-back Zener diodes are internally connected between Gx and Sx.

Sx Output Sources These are used to measure the source terminal of the external MOSFET. The pins may be tied directly to the MOSFET. Although the Sx pins can survive large negative transients, it is recommended to connect a clamp diode between the Sx pin and ground to limit any negative transients at the Sx pin when a load is switched off. This helps to avoid false fault detection caused by transient noise coupling into adjacent channels which may not be switching and therefore have no fault blanking during the transient. This is especially recommended when there is significant wiring between the load and the Sx pin even if the load incorporates a recirculation diode.

RESETZ Master Reset and Sleep Mode Pulsing this pin low clears all latched faults in the channel-specific fault registers. It also clears the serial port registers (they return to their default values). When RESETZ is held low long enough ($t > t_{SLEEP}$) the A3942 goes to sleep, as described in the Sleep topic in the Functional Description section.

ENB Enable Set low to actively pull low all outputs.

FAULTZ Fault Active low open drain output. Signals a fault. Allows parallel connection with FAULTZ signals from other devices when required.

SCLK SPI Clock See Serial Port Operation topic in Functional Description section.

CSZ SPI Chip Select input.

SDO SPI Data Output connection.

SDI SPI Data Input connection.

IREF Current Reference Defines the current used as a reference to set gate drive currents, diagnostic currents and internal timers. A resistor, RREF, connected between the IREF pin and the adjacent GND pin is selected to set the reference current to 20µA. The IREF pin is a voltage source at a voltage, V_{REF}, of typically 1.2V. The resistor required is therefore 60.4kOhm, which is the standard resistor value that provides a typical current closest to the 20µA target. Any variation in RREF will affect the internal settings as described in the section below on RREF selection. Being a high impedance node, the IREF pin is susceptible to external sources of noise and transients and should be decoupled with a capacitor across RREF between the IREF pin and the adjacent GND pin. The capacitor value should be less than 100pF to avoid any delay when power is first applied to the A3942 or when coming out of sleep mode. When controlling large load currents a larger capacitor may be required to suppress any transient noise. At power-on or when coming out of sleep mode this capacitor will be charged at typically 240µA until it reaches V_{REF}. The time taken to charge the capacitor will be approximately:

$$t_{CHARGE} = 5 \times C$$

where t_{CHARGE} is in µs and C is the capacitor value in nF. At least twice this time should be allowed, after power-on or after coming out of sleep mode, before the A3942 is used to switch any loads.

GND Ground All GND pins are internally fused to the metal die pad to which the chip is soldered. This allows for high thermal conductance through the GND pins. Connecting to these pins to a PCB ground plane improves thermal performance.

Functional Description

Power On When power is applied to either VDD or VBB, the Output Fault register is initially loaded with default values, all zeros (0). However, as individual internal circuits are initially powered on, they may latch spurious faults in the fault registers for each channel. Therefore, before operating the A3942 all fault registers must be cleared by pulsing the RESETZ pin.

Sleep Mode This mode disables various internal circuits including the charge pump, VREG, and the logic circuits. The serial port also is disabled. All Input and Output Fault register bits are cleared.

To leave sleep mode, pull RESETZ high and then allow a delay for the charge pump to stabilize. Before sending commands, clear any spurious faults as described in the Power On topic.

Faults Faults are categorized either as *system faults* or *load faults*. All faults are ORed to the FAULTZ pin.

System faults are VREG UVLO, CP UVLO, VDD UVLO, and Thermal Warning. They are not latched in the channel-specific self-protection circuit fault registers, however, the flags in the Output Fault register

bits D3, D4, and D5, are latched. If the fault condition is resolved, these flags are latched until they are read, at which time they are cleared.

Load faults are OL, STB, and STG. They are latched into the channel-specific self-protection circuit fault registers, and shifted into Output Fault register bits D0, D1, and D2 when called. Thus, load faults may be masked or cleared on a channel-specific basis.

Serial Port Operation

The serial port is compatible with the full duplex Serial Peripheral Interface (SPI) conventions. The inputs to the SPI port are logically ORed with the discrete input pins, INx, settings. This allows independent operation using only the discrete inputs, only the serial inputs, or both. Timing is clocked by an on-board 4 MHz oscillator.

When a Chip Select event occurs, the Output Fault register loads one eight-bit byte into the shift register, and the byte is then shifted out through the SDO pin. Simultaneously, bits at the SDI pin are shifted into the shift register (full duplex). At the end of a Chip Select event, the shift register contents are latched into the Input register.

Alternative Configurations Multiple A3942s can be configured together.

- *Standalone Connection* In this configuration, the master simultaneously shifts eight bits in through the SDI pin and shifts eight bits out of the SDO pin. First, the CSZ pin is set low. Then, the Output Fault register is loaded with the relevant fault byte (see the Output Fault Register topic below). Eight clock cycles are used to perform the shifts.
- *Parallel Connection* Because each slave has a CSZ pin, operation is identical to the Standalone configuration. When CSZ is inactive, SDI is “don’t care” and SDO is high impedance.
- *Daisy Chain Connection* The master shifts *n* bytes (eight bits each) during $n \times 8$ clock cycles. Regardless of the position of an individual A3942 slave in the daisy chain, the slaves shift the output byte during the first eight clock cycles after CSZ goes low. When CSZ goes high, the eight bits in the Shift register are latched into the Input register.

Serial Port Disabling Disable the serial port by setting the CSZ pin high while in sleep mode. This loads the Input register with default values, all zeroes (0).

Serial Port Error Handling Input data is discarded if the number of bits in an input stream are not a multiple of eight. Furthermore, unless the number of clock cycles is a multiple of eight while CSZ is active, any bits shifted in from the SDI pin are discarded.

Input Register Operation After a valid byte is latched into the Input register from the shift register, bit D5 is evaluated to determine if the byte is to be read. An inactive (0) bit value causes all other bits to be ignored.

If bit D5 is active (1) the other bits are read and decoded. Bits D6 and D7 are used to determine which output channel is updated. Bits D0 through D4 set the channel-specific operation, including clearing and masking of faults.

Output Fault Register Operation This register is loaded with fault data to be shifted out through the SDO pin. No handshaking is required.

The Output Fault register contains data on active faults. Four internal channel-specific fault registers contain any latched fault data for each respective channel. The following describes how the A3942 determines which channel-specific fault register to transfer into the Output Fault register.

- *No Faults* If there are no current faults, the Output Fault register is loaded with all zeros:

  0 0 0 0 0 0 0 0

- *Single Fault* If there is only one fault detected, the Output Fault register is filled to indicate that fault.

  For a load fault, the Address bits are set to indicate the affected channel; for example, a short-to-battery on channel 3 would be written:

  1 0 0 0 0 0 1 0

  On the other hand, for system faults, the Address bits are irrelevant, and a CP UVLO fault would be loaded as:

  0 0 0 1 0 0 0 0

  with the Address bits defaulting to *0 0*.

- *Multiple System Faults* If there are multiple system faults, the Output Fault register is loaded with the setting for each system fault (the Address bits remain irrelevant, as in the case of a single fault). For example, when CP UVLO and Thermal Warning faults both have occurred, the Output Fault register is loaded with:

  0 0 0 1 1 0 0 0

- *Multiple System Faults and Single Channel Load Fault* If one or more system faults and one or more load faults from a single channel have occurred, all faults are loaded into the Output Fault register, with the channel of the load faults indicated in the Address bits. For example, a CP UVLO system fault and an STG load fault on Channel 2 would be written as:

  0 1 0 1 0 0 0 1

- *Multiple Channel Load Faults* When load faults occur on more than one channel, the data cannot be signalled in a single SDO byte. However, the data can still be retrieved. The A3942 polls each channel-specific fault register, in ascending order by channel number.

  Each output is delimited by the appropriate CSZ event. For example, assume an OL on channel 2 and an STG on Channel 4. The first CSZ event writes:

  0 1 0 0 0 1 0 0

  and the second CSZ writes:

  1 1 0 0 0 0 0 1

In summary, all faults are retrieved by issuing consecutive CSZ events until the channel number stops increasing.

- If there are no faults, this byte will be shifted out each time:

  0 0 0 0 0 0 0 0

- If there are only system faults, this byte will be shifted out each time:

  0 0 [1|0] [1|0] [1|0] 0 0 0

- If there are system faults and only one load fault, one byte contains all of the fault data.
- If there are load faults on more than one channel, these bytes would be shifted out in succession, and any existing system faults will be indicated. For example, if there were no system faults and load faults on channels 2, 3, and 4, the following series of bytes would be shifted out:

  0 1 0 0 0 [1|0] [1|0] [1|0]

  1 0 0 0 0 [1|0] [1|0] [1|0]

  1 1 0 0 0 [1|0] [1|0] [1|0]

  0 1 0 0 0 [1|0] [1|0] [1|0]

  . . .

Applications

Unused Outputs When any of the four output channels are not used, the related pins should be connected as follows:

Unused Channel Pin	Connection
INx	GND
Sx	GND
Dx	VBB
Gx	Floating

RREF Selection The tolerance on RREF can be as high as ±4%. Depending on how a specific part

changes over temperature changes and lifetime, the ±4% range generally covers nominal 1% resistors.

The parameters which are affected by changes in RREF are listed in the following table:

Parameter	Change as RREF Tolerance	
	Increases	Decreases
I_{REF}	–	+
t_{RESET}	+	–
t_{SLEEP}	+	–
t_{WAKE}	+	–
$I_{G(HI)}$ and $I_{G(LO)}$	–	+
I_{OL}	–	+
t_{ON} and t_{OFF}	+	–

Setting Fault Circuit Trip Levels The load faults, Short-to-Battery (STB), Short-to-Ground (STG), and Open Load (OL), are all latched. The thresholds for STG and OL faults can be set by the value for the RDx resistor.

Open Load Fault Level When the gate is commanded off, a commanded current, I_{OL}, is sourced to Sx to detect if the load is still in the circuit. V_{OL} is compared to

$$I_{OL} \times [R_L \,//\, R_{GS}]$$

to evaluate an OL fault.

If the load has been removed, V_{Sx} exceeds V_{OL} and a fault is registered. V_{Sx} would drift to V_{BB} when an open load exists and thereby inadvertantly trip a nuisance STB fault. To prevent this, the Sx pin is clamped to V_{CLAMP}.

The operating limits specified in the Electrical Characteristics table allow the fault circuitry to distinguish all faults within the operating range of V_{BB}. If, however, the specified limits on V_{Dx} are too restrictive at low V_{BB} levels, the only repercussion is a nuisance STB fault, and this only occurs when an OL condition exists. The limit on V_{Dx} can be ignored either if the off-state faults are masked or if it is acceptable to latch the nuisance fault and clear it when the OL fault is cleared.

Because $V_{OS} << V_{OL}$, a fault is registered if

$$I_{OL} \times R_L \,//\, R_{GS} > V_{OL} \ .$$

Hence, the trip level, R_L(trip) is:

$$R_L(\text{trip}) = \left(\frac{I_{OL}}{V_{OL}} - \frac{1}{R_{GS}} \right)^{-1}$$

The OL circuit and its tolerances are designed to ensure that external loads above 50 kΩ are identified as open load and that loads below 10 kΩ are identified as valid. Note that these numbers are valid in steady state. As a result, blanking times must be set appropriately for a given load.

Under normal conditions, when the external MOSFET is off, and the load is in circuit,

$$I_{OL} \times R_L < V_{OL}.$$

Short-to-Battery Fault Level The STB comparator compares the load voltage

$$I_{OL} \times R_L \,//\, R_{GS}]$$

to the voltage set by RDx,

$$V_{BB} - I_D \times R_D \ .$$

The comparator is active only when the gate is commanded off.

During an STB condition, $I_{OL} = 0$ because the current source has run out of headroom. A fault is registered when

$$V_L > V_{BB} - I_D \times R_D \pm V_{OS}.$$

That is, the load voltage is within $\Delta V = I_D \times R_D$ volts of V_{BB}.

Using $V_{DS} = V_{BB} - V_L$ and rearranging, we find that

$$V_{DS} < I_D \times R_D \pm V_{OS} .$$

Therefore,

$$R_D = (V_{DS}(trip) \pm V_{OS}) / I_D ,$$

which is also the case for STG faults, described below. Note that an STB condition generally latches the OL flag as well.

Under normal conditions R_L << RGS and I_{OL} flows through the load, given

$$I_{OL} \times (R_D + R_L) < V_{BB} - I_D \times R_D \pm V_{OS} .$$

Because $I_{OL} \times (R_D + R_L) \approx 0$ when the external MOSFET is off, no fault is registered.

Short-to-Ground Fault Level The effect of the STG comparator is to compare the external MOSFET V_{DS} (V_L) to the set trip voltage $V_{BB} - I_D \times R_D$.

The comparator is active only when the gate is commanded on. Also, the sourced current I_{OL} is deactivated.

If V_{DS} is too large, an STG fault is registered when

$$V_L < V_{BB} - I_D \times R_D \pm V_{OS} ,$$

or, because the external MOSFET $V_{DS} = V_{BB} - V_L$,

$$V_{DS} > I_D \times R_D \pm V_{OS} .$$

Therefore, the STG trip level in the on state is the same as the STB level in the off state:

$$R_D = (V_{DS}(trip) \pm V_{OS}) / I_D .$$

Converse to the preceding, in normal operation

$$V_L > V_{BB} - I_D \times R_D \pm V_{OS},$$

or

$$V_{DS} < I_D \times R_D \pm V_{OS} .$$

Power Limits

Power dissipation, P_D, is limited by thermal constraints. The maximum junction temperature, T_J(max), and the thermal resistance, $R_{\theta JA}$, are given in this datasheet. The maximum allowed power is then found for a given ambient, T_A, from this equation:

$$T_J = P_D \times R_{\theta JA} + T_A , \text{ or}$$
$$P_D = (T_J - T_A) / R_{\theta JA} .$$

The three main contributions to power dissipation are:

- quiescent supply, $P_{BB(Q)}$
- driver outputs, P_{DRV}, and
- logic level supply, P_{DD}.

These three terms appear in the following equation:

$$P_D = P_{BB(Q)} + P_{DRV} + P_{DD} .$$

The quiescent supply current leads to a baseline power loss:

$$P_{BB(Q)} = V_{BB} \times I_{BB(Q)} .$$

In general, the losses in a driver can be quantified as follows. Given that the driver current leaves Gx to charge a gate, and assuming that the external circuit is approximately lossless, then the same charge is sunk back into Gx. Therefore, all driver current can be treated as going to heat the chip.

Total current into V_{BB} includes the quiescent current, $I_{BB(Q)}$, plus additional current, ΔI_{BB}, to energize the gates. The latter is three times the average gate current:

$$\Delta I_{BB} = 3 \times I_{Gx}(av) .$$

The average load current is calculated using the gate charge, Q_G, from the external MOSFET datasheet and the switching frequency:

$$I_{Gx}(av) = f_{sw} \times Q_G .$$

If all four outputs are supplying this current,

$$\Delta I_{BB} = 4\ (3 \times I_{Gx}) = 12 \times f_{SW} \times Q_G,$$

and

$$P_{DRV} = V_{BB} \times \Delta I_{BB} = 12 \times f_{SW} \times Q_G \times V_{BB}\ .$$

Finally, loss in the logic circuits is

$$P_{DD} = V_{DD} \times I_{DD}.$$

Example:

Find the junction temperature with one IRFZ44ES MOSFET at each output, being switched at 5 kHz, and given V_{BB} = 14 V and V_{DD} = 5.5 V.

Answer: The IRFZ44ES datasheet gives Q_G(max) = 60 nC (note that this parameter depends on circuit design constraints, such as V_{DS}). The Electrical Characteristics table gives the following maximum values for the A3942: $I_{BB(Q)}$ = 10 mA, V_{DD} = 5.5 V, and I_{DD} = 3 mA.

First, calculate total power loss:

$$\begin{aligned} P_D &= V_{BB}\, I_{BB(Q)} + 12\, f_{sw} Q_G V_{BB} + V_{DD} I_{DD} \\ &= 14\ \text{V} \times 11\ \text{mA} \\ &\quad + 4 \times 3 \times 5\ \text{kHz} \times 60\ \text{nC} \times 14\ \text{V} \\ &\quad + 5.5\ \text{V} \times 3\ \text{mA} \\ &= 221\ \text{mW}\ . \end{aligned}$$

Then, the junction temperature can be found for a given ambient temperature; T_A = 125°C is assumed here. Thermal resistance depends significantly on the board design; $R_{\theta JA}$ = 100 °C/W is assumed here. Substituting these values:

$$\begin{aligned} T_J &= P_D \times R_{\theta JA} + T_A \\ &= 221\ \text{mW} \times 100\ \text{°C/W} + 125\text{°C} \\ &= 147\text{°C}\ . \end{aligned}$$

LAYOUT AND COMPONENTS

General good practices should be followed. In addition, the following are recommended:

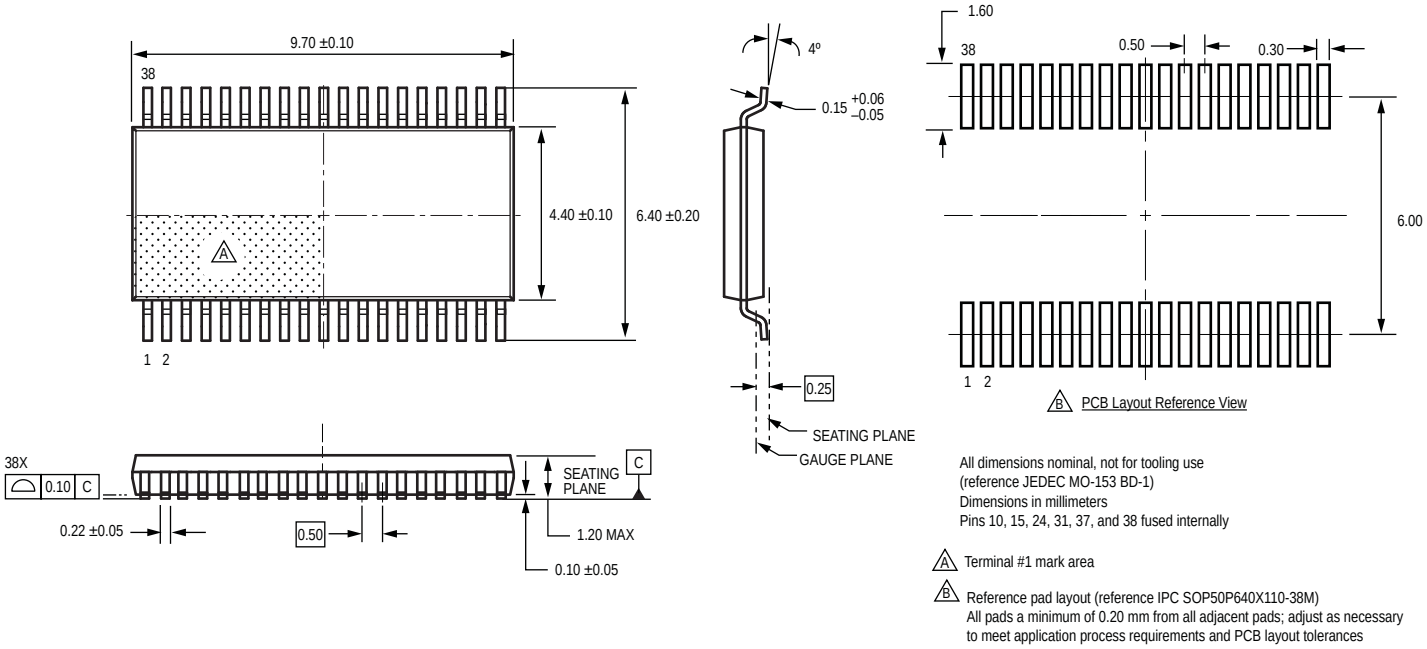
- Locate bypass capacitors (VBB, VDD, VREG, and IREF) as close to the A3942 as practicable.
- Traces to bypass capacitors should be as wide as practicable; minimize the number of vias.
- Use both bulk storage capacitors (for example, electrolytic) and low impedance bypass capacitors (for example, ceramic) on all supply pins. See the Functional Block Diagram for recommended values.
- Input and output lines should not be in close proximity. If they do overlap, it should be at right angles.
- Use ample copper in the ground and power paths. Use planes or fills where possible.
- The A3942 ground and VBB supply should be star-connected to the power ground and supply.
- The trace connecting the RDx resistors to the A3942 Dx pins should be as short as possible.
- The trace leaving the other side of the RDx resistors can be long because it has a low impedance path to ground; however, it must run independently to the respective external MOSFET in order to make a Kelvin connection.
- All support capacitors are to be referenced to the A3942 ground plane or ground fill. Minimize loop area of traces.
- These traces should be as wide as practicable: VBB, VDD, VREG, VCP, and Gx. Secondarily, it is also preferred that the traces to the charge pump caps be as wide as practicable. In both cases, the number of vias should be minimized.
- Minimize the distance connecting to ground pins in order to minimize ground loops.

Finally, a note about thermals. Because the A3942 ground pins are internally fused to the die mounting pad, they are the main path for heat dissipation. In applications producing high junction temperatures, care must be given to designing the thermal path. For example, multiple thermal vias should be run from ground pins down to the ground plane. If space allows, wide traces from ground pins to exposed copper fills on the top layer efficiently release heat through convection cooling.

Terminal List

No.	Name	Pin Description
1	SDO	Serial Data Out
2	SDI	Serial Data In
3	SCLK	Serial Clock
4	CSZ	Chip Select – NOT
5	FAULTZ	Fault – NOT (Open Drain)
6	RESETZ	Reset – NOT (Discrete)
7	ENB	Enable (Discrete)
8	VDD	Logic Supply
9	IREF	Current Reference Pin
10	GND	
11	IN2	Discrete Input Channel 2
12	IN1	Discrete Input Channel 1
13	D2	Channel 2: Drain
14	D1	Channel 1: Drain
15	GND	
16	S1	Channel 1: Source
17	G1	Channel 1: Gate
18	G2	Channel 2: Gate
19	S2	Channel 2: Source
20	S3	Channel 3: Source
21	G3	Channel 3: Gate
22	G4	Channel 4: Gate
23	S4	Channel 4: Source
24	GND	
25	D3	Channel 3: Drain
26	D4	Channel 4: Drain
27	IN3	Discrete Input Channel 3
28	IN4	Discrete Input Channel 4
29	VREG	Internal Regulator
30	VBB	Power Supply
31	GND	
32	VCP	Reservoir Capacitor Terminal
33	CP1	Charge Pump Capacitor Terminal
34	CP3	Charge Pump Capacitor Terminal
35	CP2	Charge Pump Capacitor Terminal
36	CP4	Charge Pump Capacitor Terminal
37	GND	
38	GND	

LG Package, 38-Pin TSSOP



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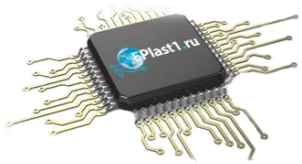

Как с нами связаться

Телефон: 8 (812) 309 58 32 (многоканальный)
Факс: 8 (812) 320-02-42
Электронная почта: org@eplast1.ru
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.