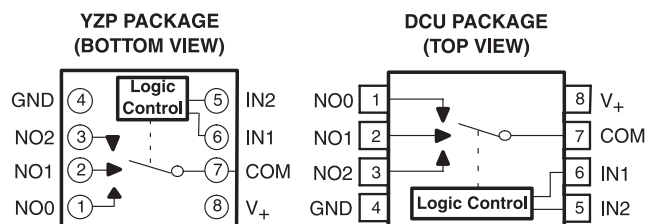


FEATURES

- Isolation in Power-Down Mode, $V_+ = 0$
- Specified Break-Before-Make Switching
- Low ON-State Resistance (1 Ω)
- Control Inputs Are 5.5-V Tolerant
- Low Charge Injection
- Excellent ON-State Resistance Matching
- Low Total Harmonic Distortion (THD)
- 1.65-V to 5.5-V Single-Supply Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
 - 2000-V Human-Body Model (A114-B, Class II)
 - 1000-V Charged-Device Model (C101)

APPLICATIONS

- Cell Phones
- PDAs
- Portable Instrumentation
- Audio and Video Signal Routing
- Low-Voltage Data Acquisition Systems
- Communication Circuits
- Modems
- Hard Drives
- Computer Peripherals
- Wireless Terminals and Peripherals



FUNCTION TABLE

IN2	IN1	COM TO NO, NO TO COM
L	L	OFF
L	H	COM = NO0
H	L	COM = NO1
H	H	COM = NO2

DESCRIPTION/ORDERING INFORMATION

The TS5A3359 is a single-pole triple-throw (SP3T) analog switch that is designed to operate from 1.65 V to 5.5 V. The device offers a low ON-state resistance and excellent ON-state resistance matching with the break-before-make feature, to prevent signal distortion during the transferring of a signal from one channel to another. The device has an excellent total harmonic distortion (THD) performance and consumes very low power. These features make this device suitable for portable audio applications.

ORDERING INFORMATION

T_A	PACKAGE ⁽¹⁾⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING ⁽³⁾
–40°C to 85°C	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)	Tape and reel	TS5A3359YZPR	__ _J9_
	VSSOP – DCU	Tape and reel	TS5A3359DCUR	JAL_

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

(3) DCU: The actual top-side marking has one additional character that designates the assembly/test site.
YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NanoFree is a trademark of Texas Instruments.

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1-Ω SP3T ANALOG SWITCH
5-V/3.3-V SINGLE-CHANNEL 3:1 MULTIPLEXER/DEMULTIPLEXER

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Summary of Characteristics⁽¹⁾

Configuration	Triple 3:1 Multiplexer/ Demultiplexer (1 × SP3T)
Number of channels	1
ON-state resistance (r_{on})	1.1 Ω
ON-state resistance match (Δr_{on})	0.1 Ω
ON-state resistance flatness ($r_{on(flat)}$)	0.15 Ω
Turn-on/turn-off time (t_{ON}/t_{OFF})	40 ns/35 ns
Break-before-make time (t_{BBM})	1 ns
Charge injection (Q_C)	40 pC
Bandwidth (BW)	100 MHz
OFF isolation (O_{ISO})	–65 dB at 10 MHz
Crosstalk (X_{TALK})	–66 dB at 10 MHz
Total harmonic distortion (THD)	0.01%
Leakage current ($I_{COM(OFF)}/I_{NO(OFF)}$)	±20 μA
Power supply current (I_+)	0.1 μA
Package options	8-pin DCU or YZP

(1) $V_+ = 5\text{ V}$, $T_A = 25^\circ\text{C}$

ABSOLUTE MINIMUM AND MAXIMUM RATINGS⁽¹⁾⁽²⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_+	Supply voltage range ⁽³⁾	–0.5	6.5	V
V_{NO} V_{COM}	Analog voltage range ⁽³⁾⁽⁴⁾⁽⁵⁾	–0.5	$V_+ + 0.5$	V
I_K	Analog port diode current $V_{NO}, V_{COM} < 0$	–50		mA
I_{NO} I_{COM}	On-state switch current $V_{NO}, V_{COM} = 0$ to V_+	–200 –400	200 400	mA
V_I	Digital input voltage range ⁽³⁾⁽⁴⁾	–0.5	6.5	V
I_{IK}	Digital input clamp current $V_I < 0$	–50		mA
I_+	Continuous current through V_+		100	mA
I_{GND}	Continuous current through GND	–100	100	mA
T_{stg}	Storage temperature range	–65	150	°C

- (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
- (2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
- (3) All voltages are with respect to ground, unless otherwise specified.
- (4) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (5) This value is limited to 5.5 V maximum.

PACKAGE THERMAL IMPEDANCE

		UNIT
θ_{JA}	Package thermal impedance ⁽¹⁾	
	DCU package	227
	YZP package	140
		°C/W

- (1) The package thermal impedance is calculated in accordance with JESD 51-7.

ELECTRICAL CHARACTERISTICS FOR 5-V SUPPLY⁽¹⁾

$V_+ = 4.5 \text{ V to } 5.5 \text{ V}$, $T_A = -40^\circ\text{C to } 85^\circ\text{C}$ (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch								
Analog signal range	$V_{\text{COM}}, V_{\text{NO}}$				0		V_+	V
Peak ON resistance	r_{peak}	$0 \leq (V_{\text{NO}}) \leq V_+$, $I_{\text{COM}} = -100 \text{ mA}$, Switch ON, See Figure 19	25°C Full	4.5 V		0.8 1.1	1.5	Ω
ON-state resistance	r_{on}	$V_{\text{NO}} = 2.5 \text{ V}$, $I_{\text{COM}} = -100 \text{ mA}$, Switch ON, See Figure 19	25°C Full	4.5 V		0.7 1.1	0.9	Ω
ON-state resistance match between channels	Δr_{on}	$V_{\text{NO}} = 2.5 \text{ V}$, $I_{\text{COM}} = -100 \text{ mA}$, Switch ON, See Figure 19	25°C Full	4.5 V		0.1 0.1	0.1	Ω
ON-state resistance flatness	$r_{\text{on(flat)}}$	$0 \leq (V_{\text{NO}}) \leq V_+$, $I_{\text{COM}} = -100 \text{ mA}$, Switch ON, See Figure 19	25°C Full	4.5 V		0.15 0.1	0.25	Ω
NO OFF leakage current	$I_{\text{NO(OFF)}}$	$V_{\text{NO}} = 1 \text{ V or } 4.5 \text{ V}$, $V_{\text{COM}} = 1 \text{ V to } 4.5 \text{ V}$, Switch OFF, See Figure 20	25°C Full	5.5 V	-20 -150	5	20 150	nA
	$I_{\text{NO(PWROFF)}}$	$V_{\text{NO}} = 0 \text{ to } 5.5 \text{ V}$, $V_{\text{COM}} = 5.5 \text{ V to } 0$, Switch OFF, See Figure 20	25°C Full	0 V	-1 -25	0.8	1 25	μA
NO ON leakage current	$I_{\text{NO(ON)}}$	$V_{\text{NO}} = 1 \text{ V or } 4.5 \text{ V}$, $V_{\text{COM}} = \text{Open}$, Switch ON, See Figure 20	25°C Full	5.5 V	-30 -220	5	30 220	nA
COM OFF leakage current	$I_{\text{COM(OFF)}}$	$V_{\text{NO}} = 4.5 \text{ V or } 1 \text{ V}$, $V_{\text{COM}} = 1 \text{ V or } 4.5 \text{ V}$, Switch OFF, See Figure 20	25°C Full	5.5 V	-25 -250	8	25 250	nA
	$I_{\text{COM(PWROFF)}}$	$V_{\text{COM}} = 0 \text{ to } 5.5 \text{ V}$, $V_{\text{NO}} = 5.5 \text{ V to } 0$, Switch OFF, See Figure 20	25°C Full	0 V	-8 -50	0.1	8 50	μA
COM ON leakage current	$I_{\text{COM(ON)}}$	$V_{\text{NO}} = \text{Open}$, $V_{\text{COM}} = 1 \text{ V or } 4.5 \text{ V}$, Switch ON, See Figure 20	25°C Full	5.5 V	-30 -220	5	30 220	nA
Digital Control Inputs (IN1, IN2)⁽²⁾								
Input logic high	V_{IH}		Full		2.4		5.5	V
Input logic low	V_{IL}		Full		0		0.8	V
Input leakage current	$I_{\text{IH}}, I_{\text{IL}}$	$V_{\text{I}} = 5.5 \text{ V or } 0$	25°C Full	5.5 V	-2 -20		2 20	μA

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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ELECTRICAL CHARACTERISTICS FOR 5-V SUPPLY (continued)

$V_+ = 4.5\text{ V to }5.5\text{ V}$, $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T _A	V ₊	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t _{ON}	V _{COM} = V ₊ , R _L = 50 Ω,	C _L = 35 pF, See Figure 23	25°C	5 V	1	2.5	21	ns
				Full	4.5 V to 5.5 V	1		23.5	
Turn-off time	t _{OFF}	V _{COM} = V ₊ , R _L = 50 Ω,	C _L = 35 pF, See Figure 23	25°C	5 V	1	6	10.5	ns
				Full	4.5 V to 5.5 V	1		12	
Break-before-make time	t _{BBM}	V _{NO} = V ₊ , R _L = 50 Ω,	C _L = 35 pF, See Figure 24	25°C	5 V	0.5	8.5	18	ns
				Full	4.5 V to 5.5 V	0.5		23	
Charge injection	Q _C	V _{GEN} = 0, R _{GEN} = 0,	C _L = 1 nF, See Figure 28	25°C	5 V		20		pC
NO OFF capacitance	C _{NO(OFF)}	V _{NO} = V ₊ or GND, Switch OFF,	See Figure 22	25°C	5 V		18		pF
COM OFF capacitance	C _{COM(OFF)}	V _{COM} = V ₊ or GND, Switch OFF,	See Figure 22	25°C	2.5 V		54		pF
NO ON capacitance	C _{NO(ON)}	V _{NO} = V ₊ or GND, Switch ON,	See Figure 22	25°C	5 V		78		pF
COM ON capacitance	C _{COM(ON)}	V _{COM} = V ₊ or GND, Switch ON,	See Figure 22	25°C	5 V		78		pF
Digital input capacitance	C _I	V _I = V ₊ or GND,	See Figure 22	25°C	5 V		2.5		pF
Bandwidth	BW	R _L = 50 Ω, Switch ON,	See Figure 25	25°C	5 V		75		MHz
OFF isolation	O _{ISO}	R _L = 50 Ω, f = 1 MHz ,	Switch OFF, See Figure 26	25°C	5 V		–64		dB
Crosstalk	X _{TALK}	R _L = 50 Ω, f = 1 MHz ,	Switch ON, See Figure 27	25°C	5 V		–64		dB
Total harmonic distortion	THD	R _L = 600 Ω, C _L = 50 pF,	f = 20 Hz to 20 kHz, See Figure 29	25°C	5 V		0.005		%
Supply									
Positive supply current	I ₊	V _I = V ₊ or GND,	Switch ON or OFF	25°C	5.5 V		16	50	nA
				Full				1200	

ELECTRICAL CHARACTERISTICS FOR 3.3-V SUPPLY⁽¹⁾

$V_+ = 3\text{ V to }3.6\text{ V}$, $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T _A	V ₊	MIN	TYP	MAX	UNIT
Analog Switch									
Analog signal range	V _{COM} , V _{NO}					0		V ₊	V
Peak ON resistance	r _{peak}	0 ≤ (V _{NO}) ≤ V ₊ , I _{COM} = −100 mA,	Switch ON, See Figure 19	25°C	3 V		1.3	1.6	Ω
				Full				2	
ON-state resistance	r _{on}	V _{NO} = 2 V, I _{COM} = −100 mA,	Switch ON, See Figure 19	25°C	3 V		1.2	1.6	Ω
				Full				1.8	
ON-state resistance match between channels	Δr _{on}	V _{NO} = 2 V, 0.8 V, I _{COM} = −100 mA,	Switch ON, See Figure 19	25°C	3 V		0.1	0.15	Ω
				Full				0.15	
ON-state resistance flatness	r _{on(flat)}	0 ≤ (V _{NO}) ≤ V ₊ , I _{COM} = −100 mA,	Switch ON, See Figure 19	25°C	3 V		0.2		Ω
		V _{NO} = 2 V, 0.8 V, I _{COM} = −100 mA,	Switch ON, See Figure 19	25°C			0.2	0.35	
				Full				0.35	
NO OFF leakage current	I _{NO(OFF)}	V _{NO} = 1 V or 3 V, V _{COM} = 1 V to 3 V,	Switch OFF, See Figure 20	25°C	3.6 V	−15	3	15	nA
				Full			−30	30	
		I _{NO(PWROFF)}	V _{NO} = 0 to 3.6 V, V _{COM} = 3.6 V to 0,	Switch OFF, See Figure 20	25°C	0 V	−1	0.2	1
				Full			−10	10	
NO ON leakage current	I _{NO(ON)}	V _{NO} = 1 V or 3 V, V _{COM} = Open,	Switch ON, See Figure 20	25°C	3.6 V	−15	3	15	nA
				Full			−40	40	
COM OFF leakage current	I _{COM(OFF)}	V _{NO} = 0 V to 3.6 V, V _{COM} = 1 V or V _{NO} = 3.6 V to 0, V _{COM} = 3 V,	Switch OFF, See Figure 20	25°C	3.6 V	−15	3	15	nA
				Full			−75	75	
	I _{COM(PWROFF)}	V _{COM} = 0 to 3.6 V, V _{NO} = 3.6 V to 0,	Switch OFF, See Figure 20	25°C	0 V	−1	0.2	1	μA
				Full			−20	20	
COM ON leakage current	I _{COM(ON)}	V _{NO} = Open, V _{COM} = 1 V or 3 V,	Switch ON, See Figure 20	25°C	3.6 V	−15	4	15	nA
				Full			−40	40	
Digital Control Inputs (IN1, IN2) ⁽²⁾									
Input logic high	V _{IH}			Full		2		5.5	V
Input logic low	V _{IL}			Full		0		0.8	V
Input leakage current	I _{IH} , I _{IL}	V _I = 5.5 V or 0		25°C	3.6 V	−2		2	nA
				Full			−20	20	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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ELECTRICAL CHARACTERISTICS FOR 3.3-V SUPPLY (continued)

$V_+ = 3\text{ V}$ to 3.6 V , $T_A = -40^\circ\text{C}$ to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T _A	V ₊	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t _{ON}	V _{COM} = V ₊ , R _L = 50 Ω,	C _L = 35 pF, See Figure 23	25°C	3.3 V	1	16	30.5	ns
				Full	3 V to 3.6 V	1		34	
Turn-off time	t _{OFF}	V _{COM} = V ₊ , R _L = 50 Ω,	C _L = 35 pF, See Figure 23	25°C	3.3 V	1	6	11.5	ns
				Full	3 V to 3.6 V	1		12.5	
Break-before-make time	t _{BBM}	V _{NO} = V ₊ , R _L = 50 Ω,	C _L = 35 pF, See Figure 24	25°C	3.3 V	0.5	13	26	ns
				Full	3 V to 3.6 V	0.5		30	
Charge injection	Q _C	V _{GEN} = 0, R _{GEN} = 0,	C _L = 1 nF, See Figure 28	25°C	3.3 V		12		pC
NO OFF capacitance	C _{NO(OFF)}	V _{NO} = V ₊ or GND, Switch OFF,	See Figure 22	25°C	3.3 V		18		pF
COM OFF capacitance	C _{COM(OFF)}	V _{COM} = V ₊ or GND, Switch OFF,	See Figure 22	25°C	3.3 V		55		pF
NO ON capacitance	C _{NO(ON)}	V _{NO} = V ₊ or GND, Switch ON,	See Figure 22	25°C	3.3 V		78		pF
COM ON capacitance	C _{COM(ON)}	V _{COM} = V ₊ or GND, Switch ON,	See Figure 22	25°C	3.3 V		78		pF
Digital input capacitance	C _I	V _I = V ₊ or GND,	See Figure 22	25°C	3.3 V		2.5		pF
Bandwidth	BW	R _L = 50 Ω, Switch ON,	See Figure 25	25°C	3.3 V		73		MHz
OFF isolation	O _{ISO}	R _L = 50 Ω, f = 1 MHz,	Switch OFF, See Figure 26	25°C	3.3 V		−64		dB
Crosstalk	X _{TALK}	R _L = 50 Ω, f = 1 MHz,	Switch ON, See Figure 27	25°C	3.3 V		−64		dB
Total harmonic distortion	THD	R _L = 600 Ω, C _L = 50 pF,	f = 20 Hz to 20 kHz, See Figure 29	25°C	3.3 V		0.010		%
Supply									
Positive supply current	I ₊	V _I = V ₊ or GND,	Switch ON or OFF	25°C	3.6 V		2	20	nA
				Full				350	

ELECTRICAL CHARACTERISTICS FOR 2.5-V SUPPLY⁽¹⁾

$V_+ = 2.3 \text{ V to } 2.7 \text{ V}$, $T_A = -40^\circ\text{C to } 85^\circ\text{C}$ (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T _A	V ₊	MIN	TYP	MAX	UNIT
Analog Switch									
Analog signal range	V _{COM} , V _{NO}					0		V ₊	V
Peak ON resistance	r _{peak}	0 ≤ (V _{NO}) ≤ V ₊ , I _{COM} = −8 mA,	Switch ON, See Figure 19	25°C	2.3 V	1.8		2.5	Ω
				Full		2.7			
ON-state resistance	r _{on}	V _{NO} = 1.8 V, I _{COM} = −8 mA,	Switch ON, See Figure 19	25°C	2.3 V	1.5		2	Ω
				Full		2.4			
ON-state resistance match between channels	Δr _{on}	V _{NO} = 1.8 V, I _{COM} = −8 mA,	Switch ON, See Figure 19	25°C	2.3 V			0.2	Ω
				Full				0.2	
ON-state resistance flatness	r _{on(flat)}	0 ≤ (V _{NO}) ≤ V ₊ , I _{COM} = −8 mA,	Switch ON, See Figure 19	25°C	2.3 V	0.6			Ω
		V _{NO} = 0.8 V, 1.8 V I _{COM} = −8 mA,	Switch ON, See Figure 19	25°C		0.6		1	
				Full				1	
NO OFF leakage current	I _{NO(OFF)}	V _{NO} = 0.5 V or 2.3 V, V _{COM} = 0.5 V to 2.3 V,	Switch OFF, See Figure 20	25°C	2.7 V	−15	3	15	nA
				Full		−30		30	
		I _{NO(PWROFF)}	V _{NO} = 0 to 2.7 V, V _{COM} = 2.7 V to 0,	Switch OFF, See Figure 20	25°C	0 V	−1	0.1	1
			Full	−10			10		
NO ON leakage current	I _{NO(ON)}	V _{NO} = 0.5 V or 2.3 V, V _{COM} = Open,	Switch ON, See Figure 20	25°C	2.7 V	−15	3	15	nA
				Full		−35		35	
COM OFF leakage current	I _{COM(OFF)}	V _{NO} = 0.3 V to 2.3 V, V _{COM} = 0.5 V or 2.3 V,	Switch OFF, See Figure 20	25°C	2.7 V	−15	3	15	nA
				Full		−60		60	
		I _{COM(PWROFF)}	V _{COM} = 0 to 2.7 V, V _{NO} = 2.7 V to 0,	Switch OFF, See Figure 20	25°C	0 V	−1	0.1	1
			Full	−10			10		
COM ON leakage current	I _{COM(ON)}	V _{NO} = Open, V _{COM} = 0.5 V or 2.2 V,	Switch ON, See Figure 20	25°C	2.7 V	−15	3.5	15	nA
				Full		−40		40	
Digital Control Inputs (IN1, IN2) ⁽²⁾									
Input logic high	V _{IH}			Full		1.8		5.5	V
Input logic low	V _{IL}			Full		0		0.6	V
Input leakage current	I _{IH} , I _{IL}	V _I = 5.5 V or 0		25°C	2.7 V	1		1	nA
				Full		10		10	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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ELECTRICAL CHARACTERISTICS FOR 2.5-V SUPPLY (continued)

$V_+ = 2.3 \text{ V to } 2.7 \text{ V}$, $T_A = -40^\circ\text{C to } 85^\circ\text{C}$ (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T _A	V ₊	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t _{ON}	V _{COM} = V ₊ , R _L = 50 Ω,	C _L = 35 pF, See Figure 23	25°C	2.5 V	2	4.5	43	ns
				Full	2.3 V to 2.7 V	2		47.5	
Turn-off time	t _{OFF}	V _{COM} = V ₊ , R _L = 50 Ω,	C _L = 35 pF, See Figure 23	25°C	2.5 V	2	8.5	11	ns
				Full	2.3 V to 2.7 V	2		12.5	
Break-before-make time	t _{BBM}	V _{NO} = V ₊ , R _L = 50 Ω,	C _L = 35 pF, See Figure 24	25°C	2.5 V	0.5	18.5	38.5	ns
				Full	2.3 V to 2.7 V	0.5		43	
Charge injection	Q _C	V _{GEN} = 0, R _{GEN} = 0,	C _L = 1 nF, See Figure 28	25°C	2.5 V		8		pC
NO OFF capacitance	C _{NO(OFF)}	V _{NO} = V ₊ or GND, Switch OFF,	See Figure 22	25°C	2.5 V		18.5		pF
COM OFF capacitance	C _{COM(OFF)}	V _{COM} = V ₊ or GND, Switch OFF,	See Figure 22	25°C	2.5 V		55		pF
NO ON capacitance	C _{NO(ON)}	V _{NO} = V ₊ or GND, Switch ON,	See Figure 22	25°C	2.5 V		78		pF
COM ON capacitance	C _{COM(ON)}	V _{COM} = V ₊ or GND, Switch ON,	See Figure 22	25°C	2.5 V		78		pF
Digital input capacitance	C _I	V _I = V ₊ or GND,	See Figure 22	25°C	2.5 V		3		pF
Bandwidth	BW	R _L = 50 Ω, Switch ON,	See Figure 25	25°C	2.5 V		73		MHz
OFF isolation	O _{ISO}	R _L = 50 Ω, f = 1 MHz,	Switch OFF, See Figure 26	25°C	2.5 V		−64		dB
Crosstalk	X _{TALK}	R _L = 50 Ω, f = 1 MHz,	Switch ON, See Figure 27	25°C	2.5 V		−64		dB
Total harmonic distortion	THD	R _L = 600 Ω, C _L = 50 pF,	f = 20 Hz to 20 kHz, See Figure 29	25°C	2.5 V		0.030		%
Supply									
Positive supply current	I ₊	V _I = V ₊ or GND,	Switch ON or OFF	25°C	2.7 V		1	10	nA
				Full				250	

ELECTRICAL CHARACTERISTICS FOR 1.8-V SUPPLY⁽¹⁾

$V_+ = 1.65 \text{ V to } 1.95 \text{ V}$, $T_A = -40^\circ\text{C to } 85^\circ\text{C}$ (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T _A	V ₊	MIN	TYP	MAX	UNIT
Analog Switch									
Analog signal range	V _{COM} , V _{NO}					0		V ₊	V
Peak ON resistance	r _{peak}	0 ≤ (V _{NO}) ≤ V ₊ , I _{COM} = −2 mA,	Switch ON, See Figure 19	25°C	1.65 V	5		30	Ω
				Full					
ON-state resistance	r _{on}	V _{NO} = 1.5 V, I _{COM} = −2 mA,	Switch ON, See Figure 19	25°C	1.65 V	2		2.5	Ω
				Full		3.5			
ON-state resistance match between channels	Δr _{on}	V _{NO} = 1.5 V, I _{COM} = −2 mA,	Switch ON, See Figure 19	25°C	1.65 V	0.15		0.4	Ω
				Full		0.4			
ON-state resistance flatness	r _{on(flat)}	0 ≤ (V _{NO}) ≤ V ₊ , I _{COM} = −2 mA,	Switch ON, See Figure 19	25°C	1.65 V	5			Ω
				25°C		4.5			
				Full		5			
NO OFF leakage current	I _{NO(OFF)}	V _{NO} =0.3 V or 1.65 V, V _{COM} = 0.3 V to 1.65 V,	Switch OFF, See Figure 20	25°C	1.95 V	−15	3	15	nA
				Full		−30 30			
		I _{NO(PWROFF)}	V _{NO} = 0 to 1.95 V, V _{COM} = 1.95 V to 0,	Switch OFF, See Figure 20	25°C	0 V	−1	0.1	1
			Full	−15 15					
NO ON leakage current	I _{NO(ON)}	V _{NO} =0.3 V or 1.65 V, V _{COM} = Open,	Switch ON, See Figure 20	25°C	1.95 V	−15	3	15	nA
				Full		−30 30			
COM OFF leakage current	I _{COM(OFF)}	V _{NO} = 0.3 V to 1.65 V, V _{COM} =0.3 V or 1.65 V,	Switch OFF, See Figure 20	25°C	1.95 V	−15	3	15	nA
				Full		−50 50			
		I _{COM(PWROFF)}	V _{COM} = 0 to 1.95 V, V _{NO} = 1.95 V to 0,	Switch OFF, See Figure 20	25°C	0 V	−1	0.1	1
			Full	−10 10					
COM ON leakage current	I _{COM(ON)}	V _{NO} = Open, V _{COM} = 0.3 V or 1.65 V,	Switch ON, See Figure 20	25°C	1.95 V	−15	3	15	nA
				Full		−30 30			
Digital Control Inputs (IN1, IN2) ⁽²⁾									
Input logic high	V _{IH}			Full		1.5		5.5	V
Input logic low	V _{IL}			Full		0		0.6	V
Input leakage current	I _{IH} , I _{IL}	V _I = 5.5 V or 0		25°C	1.95 V	−2		2	nA
				Full		−20 20			

- (1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
 (2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

TS5A3359
1-Ω SP3T ANALOG SWITCH
5-V/3.3-V SINGLE-CHANNEL 3:1 MULTIPLEXER/DEMULTIPLEXER

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ELECTRICAL CHARACTERISTICS FOR 1.8-V SUPPLY (continued)

$V_+ = 1.65 \text{ V to } 1.95 \text{ V}$, $T_A = -40^\circ\text{C to } 85^\circ\text{C}$ (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T _A	V ₊	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t _{ON}	V _{COM} = V ₊ , R _L = 50 Ω,	C _L = 35 pF, See Figure 23	25°C	1.8 V	3	38.5	85	ns
				Full	1.65 V to 1.95 V	3		90	
Turn-off time	t _{OFF}	V _{COM} = V ₊ , R _L = 50 Ω,	C _L = 35 pF, See Figure 23	25°C	1.8 V	2	8.5	16	ns
				Full	1.65 V to 1.95 V	2		18	
Break-before-make time	t _{BBM}	V _{NO} = V ₊ , R _L = 50 Ω,	C _L = 35 pF, See Figure 24	25°C	1.8 V	1	33	75	ns
				Full	1.65 V to 1.95 V	1		80	
Charge injection	Q _C	V _{GEN} = 0, R _{GEN} = 0,	C _L = 1 nF, See Figure 28	25°C	1.8 V		5		pC
NO OFF capacitance	C _{NO(OFF)}	V _{NO} = V ₊ or GND, Switch OFF,	See Figure 22	25°C	1.8 V		18.5		pF
COM OFF capacitance	C _{COM(OFF)}	V _{COM} = V ₊ or GND, Switch OFF,	See Figure 22	25°C	1.8 V		55		pF
NO ON capacitance	C _{NO(ON)}	V _{NO} = V ₊ or GND, Switch ON,	See Figure 22	25°C	1.8 V		78		pF
COM ON capacitance	C _{COM(ON)}	V _{COM} = V ₊ or GND, Switch ON,	See Figure 22	25°C	1.8 V		78		pF
Digital input capacitance	C _I	V _I = V ₊ or GND,	See Figure 22	25°C	1.8 V		3		pF
Bandwidth	BW	R _L = 50 Ω, Switch ON,	See Figure 25	25°C	1.8 V		73		MHz
OFF isolation	O _{ISO}	R _L = 50 Ω, f = 1 M Hz ,	Switch OFF, See Figure 26	25°C	1.8 V		−64		dB
Crosstalk	X _{TALK}	R _L = 50 Ω, f = 1 MHz,	Switch ON, See Figure 27	25°C	1.8 V		−64		dB
Total harmonic distortion	THD	R _L = 600 Ω, C _L = 50 pF,	f = 20 Hz to 20 kHz, See Figure 29	25°C	1.8 V		0.080		%
Supply									
Positive supply current	I ₊	V _I = V ₊ or GND,	Switch ON or OFF	25°C	1.95 V	1			nA
				Full		200			

TYPICAL PERFORMANCE

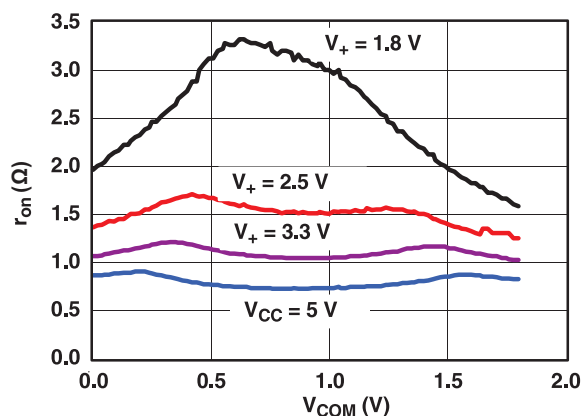


Figure 1. r_{on} vs V_{COM}

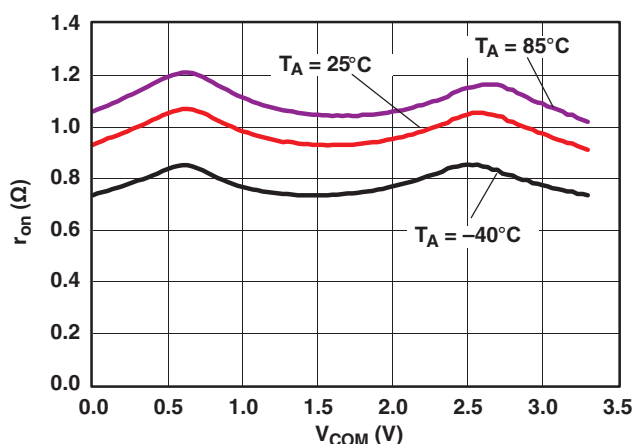


Figure 2. r_{on} vs V_{COM} ($V_+ = 3.3$ V)

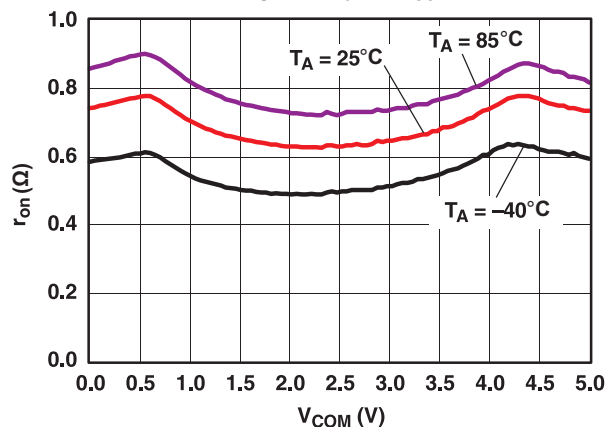


Figure 3. r_{on} vs V_{COM} ($V_+ = 5$ V)

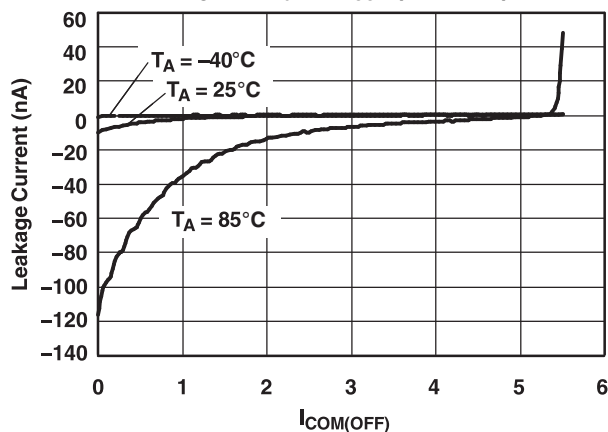


Figure 4. Leakage Current vs Temperature

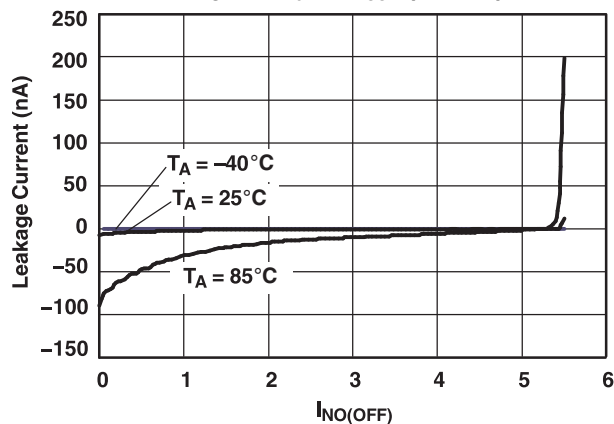


Figure 5. Leakage Current vs Temperature

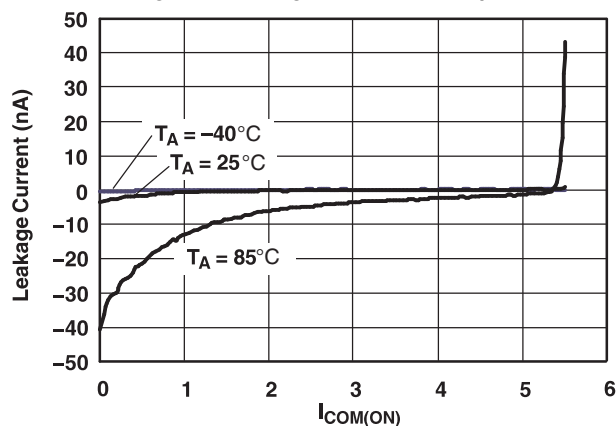


Figure 6. Leakage Current vs Temperature

TYPICAL PERFORMANCE (continued)

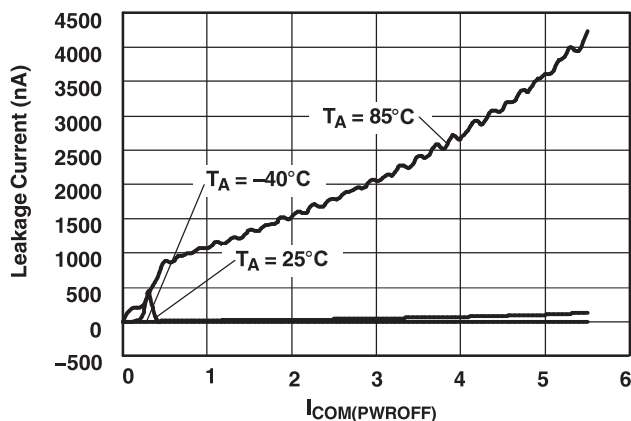


Figure 7. Leakage Current vs Temperature

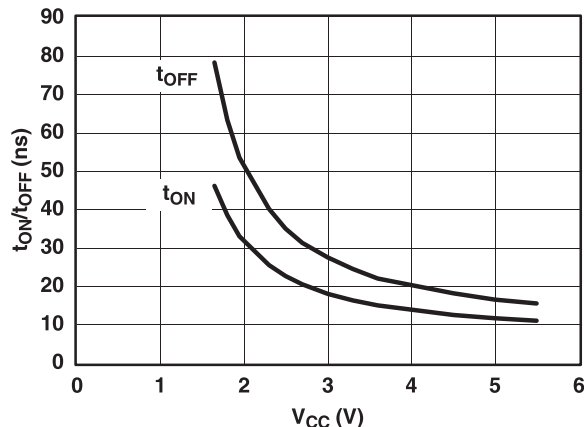


Figure 9. t_{ON} and t_{OFF} vs Supply Voltage

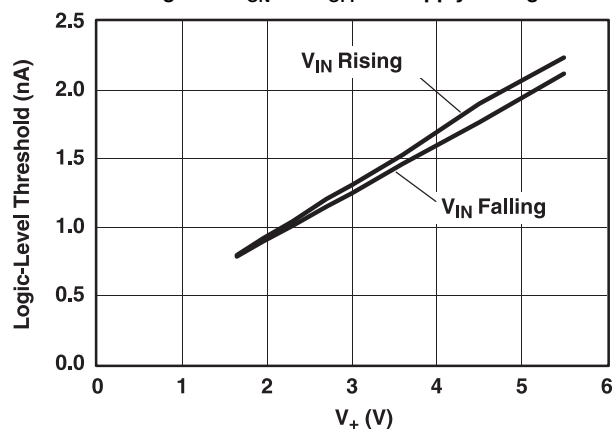


Figure 11. Logic-Level Threshold vs V_+

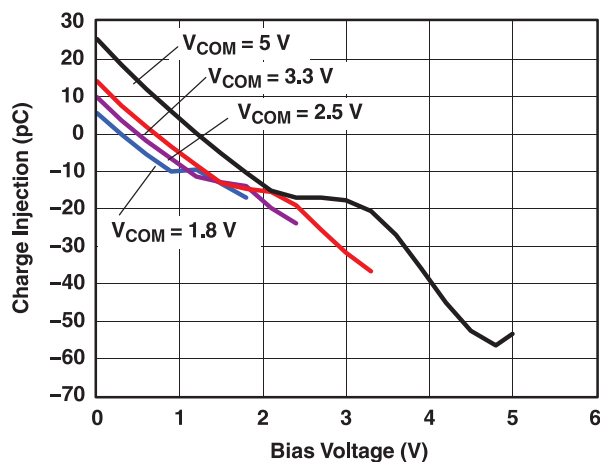


Figure 8. Charge Injection (Q_C) vs V_{COM}

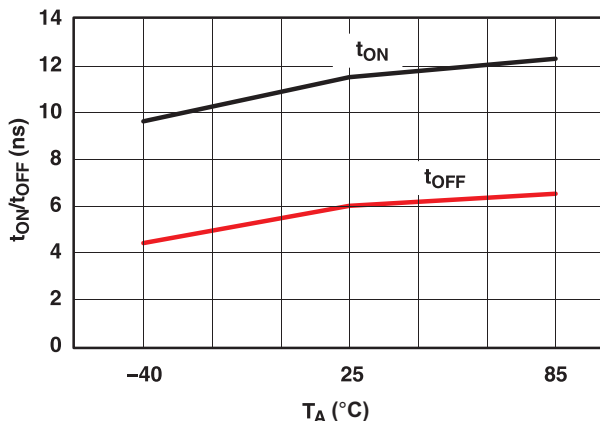


Figure 10. t_{ON} and t_{OFF} vs Temperature

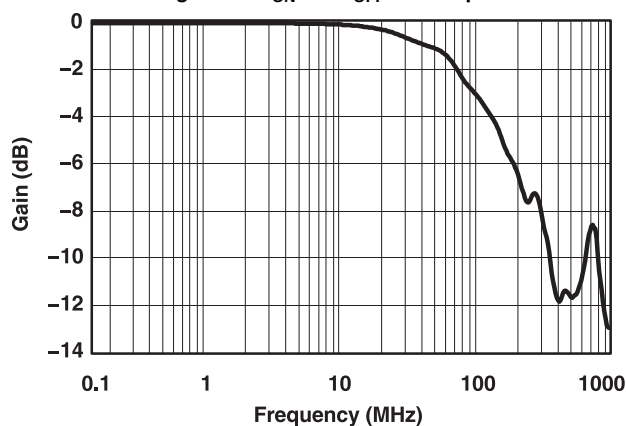


Figure 12. Bandwidth ($V_+ = 5\text{ V}$)

TYPICAL PERFORMANCE (continued)

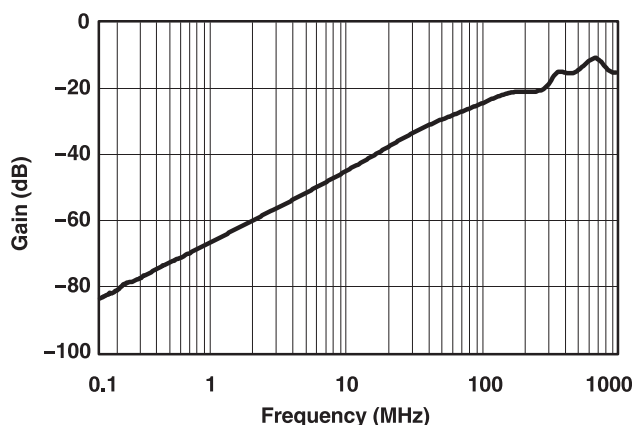


Figure 13. OFF Isolation vs Crosstalk

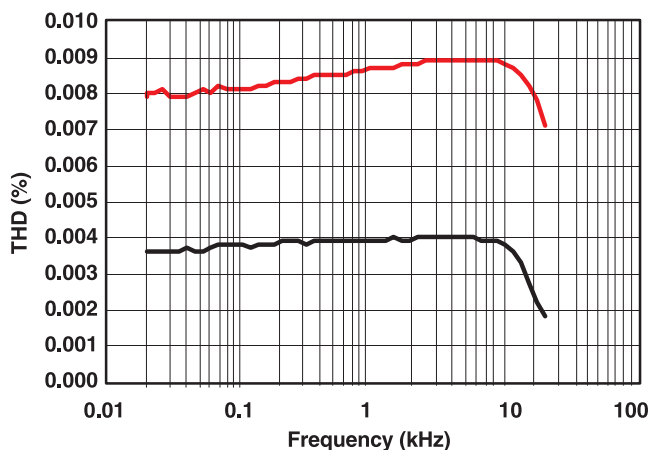


Figure 14. Total Harmonic Distortion vs Frequency

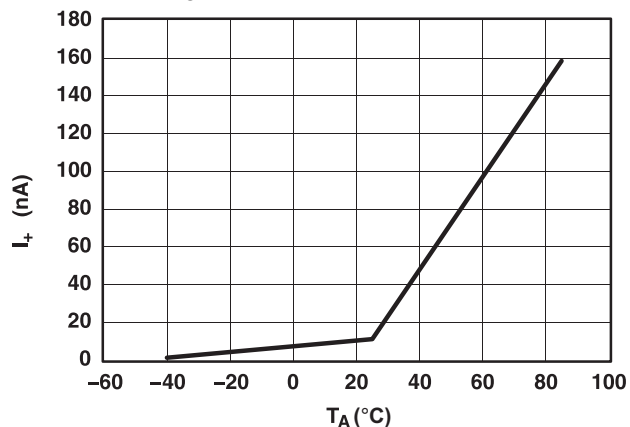


Figure 15. Power-Supply Current vs Temperature ($V_+ = 5$)

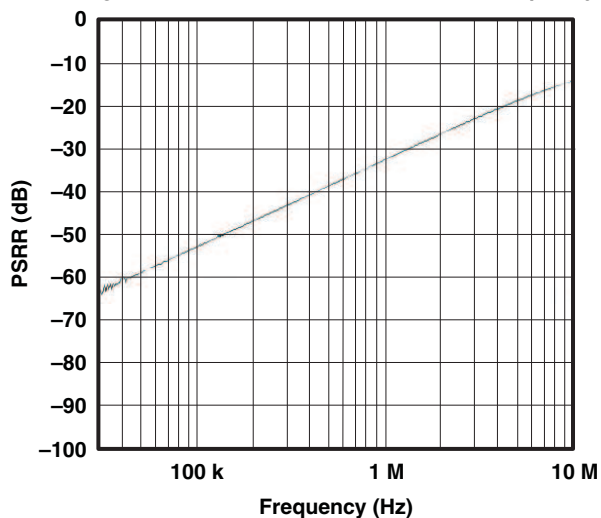


Figure 16. COM Port to NO2 PSRR,
 $IN1 = V_{CC}$, $IN2 = V_{CC}$ ($V_{CC} = 5$ V)

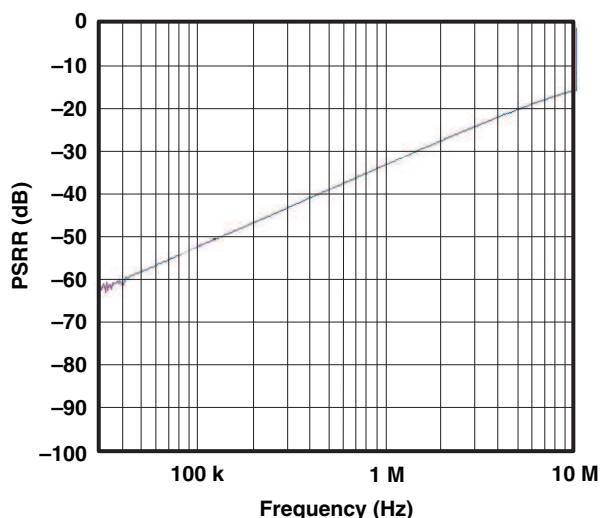


Figure 17. COM Port to NO0 PSRR,
 $IN1 = V_{CC}$, $IN2 = V_{CC}$ ($V_{CC} = 5$ V)

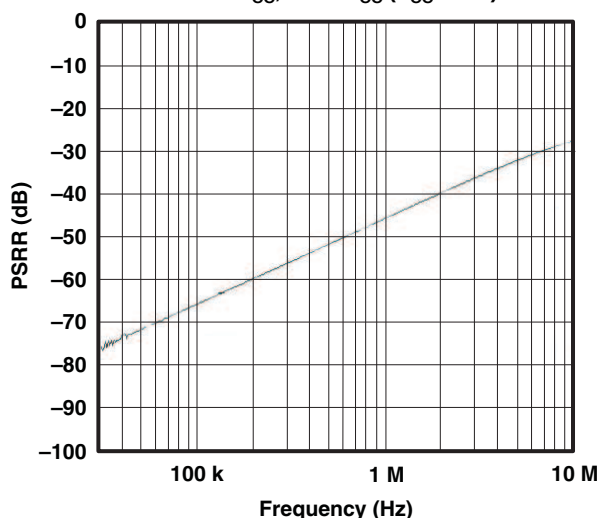


Figure 18. COM Port Hi-Z PSRR,
 $IN1 = 0$ V, $IN2 = 0$ V ($V_{CC} = 5$ V)

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PIN DESCRIPTION

PIN NO.	NAME	DESCRIPTION
1	NO0	Normally open
2	NO1	Normally open
3	NO2	Normally open
4	GND	Digital ground
5	IN2	Digital control to connect COM to NO
6	IN1	Digital control to connect COM to NO
7	COM	Common
8	V ₊	Power supply

PARAMETER DESCRIPTION

SYMBOL	DESCRIPTION
V _{COM}	Voltage at COM
V _{NO}	Voltage at NO
r _{on}	Resistance between COM and NC or COM and NO ports when the channel is ON
r _{peak}	Peak on-state resistance over a specified voltage range
Δr _{on}	Difference of r _{on} between channels in a specific device
r _{on(flat)}	Difference between the maximum and minimum value of r _{on} in a channel over the specified range of conditions
I _{NO(OFF)}	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the OFF state
I _{NO(PWROFF)}	Leakage current measured at the NO port during the power-down condition, V ₊ = 0.
I _{NO(ON)}	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the ON state and the output (COM) open
I _{COM(ON)}	Leakage current measured at the COM port, with the corresponding channel (COM to NO or COM to NC) in the ON state and the output (NC or NO) open
I _{COM(OFF)}	Leakage current measured at the COM port during the power-down condition, V ₊ = 0
I _{COM(PWROFF)}	Leakage current measured at the COM port during the power-down condition, V ₊ = 0.
V _{IH}	Minimum input voltage for logic high for the control input (IN)
V _{IL}	Maximum input voltage for logic low for the control input (IN)
V _I	Voltage at the control input (IN)
I _{IH} , I _{IL}	Leakage current measured at the control input (IN)
t _{ON}	Turn-on time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM or NO) signal when the switch is turning ON.
t _{OFF}	Turn-off time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM or NO) signal when the switch is turning OFF.
t _{BBM}	Break-before-make time. This parameter is measured under the specified range of conditions and by the propagation delay between the output of two adjacent analog channels (NC and NO) when the control signal changes state.
Q _C	Charge injection is a measurement of unwanted signal coupling from the control (IN) input to the analog (NO or COM) output. This is measured in coulomb (C) and measured by the total charge induced due to switching of the control input. Charge injection, Q _C = C _L × ΔV _{COM} , C _L is the load capacitance and ΔV _{COM} is the change in analog output voltage.
C _{NO(OFF)}	Capacitance at the NO port when the corresponding channel (NO to COM) is OFF
C _{NO(ON)}	Capacitance at the NO port when the corresponding channel (NO to COM) is ON
C _{COM(ON)}	Capacitance at the COM port when the corresponding channel (COM to NO) is ON
C _{COM(OFF)}	Capacitance at the COM port when the corresponding channel (COM to NO) is OFF
C _I	Capacitance of control input (IN)
O _{ISO}	OFF isolation of the switch is a measurement of OFF-state switch impedance. This is measured in dB in a specific frequency, with the corresponding channel (NC to COM or NO to COM) in the OFF state.
X _{TALK}	Crosstalk is a measurement of unwanted signal coupling from an ON channel to an OFF channel (NC to NO or NO to NC). This is measured in a specific frequency and in dB.
BW	Bandwidth of the switch. This is the frequency in which the gain of an ON channel is –3 dB below the DC gain.

PARAMETER DESCRIPTION (continued)

SYMBOL	DESCRIPTION
THD	Total harmonic distortion describes the signal distortion caused by the analog switch. This is defined as the ratio of root mean square (RMS) value of the second, third, and higher harmonic to the absolute magnitude of the fundamental harmonic.
I_+	Static power-supply current with the control (IN) pin at V_+ or GND

PARAMETER MEASUREMENT INFORMATION

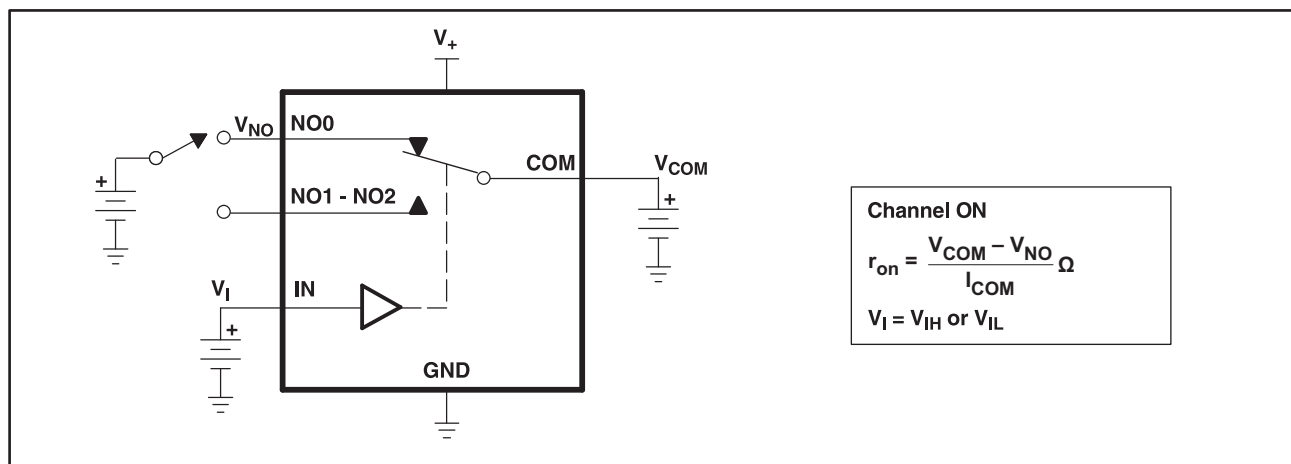


Figure 19. ON-State Resistance (r_{on})

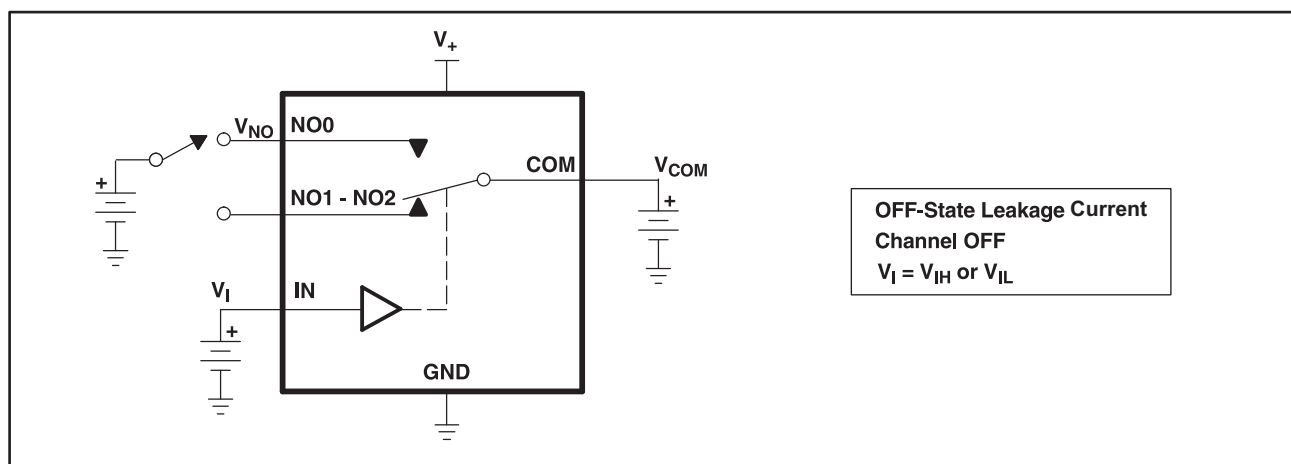


Figure 20. OFF-State Leakage Current ($I_{NC(OFF)}$, $I_{NO(OFF)}$, $I_{NO(PWROFF)}$, $I_{COM(OFF)}$, $I_{COM(PWROFF)}$)

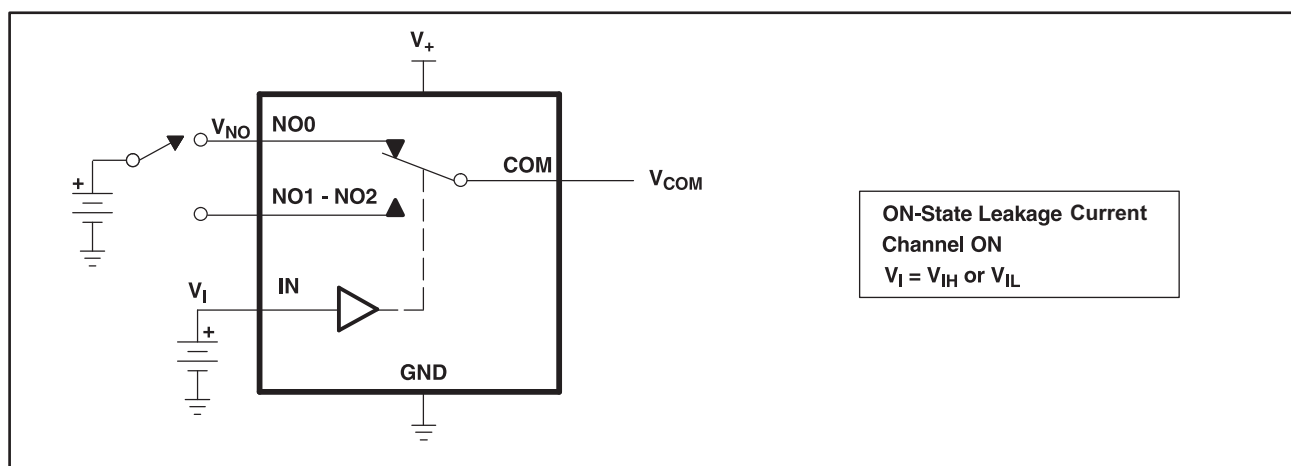


Figure 21. ON-State Leakage Current ($I_{COM(ON)}$, $I_{NO(ON)}$)

PARAMETER MEASUREMENT INFORMATION (continued)

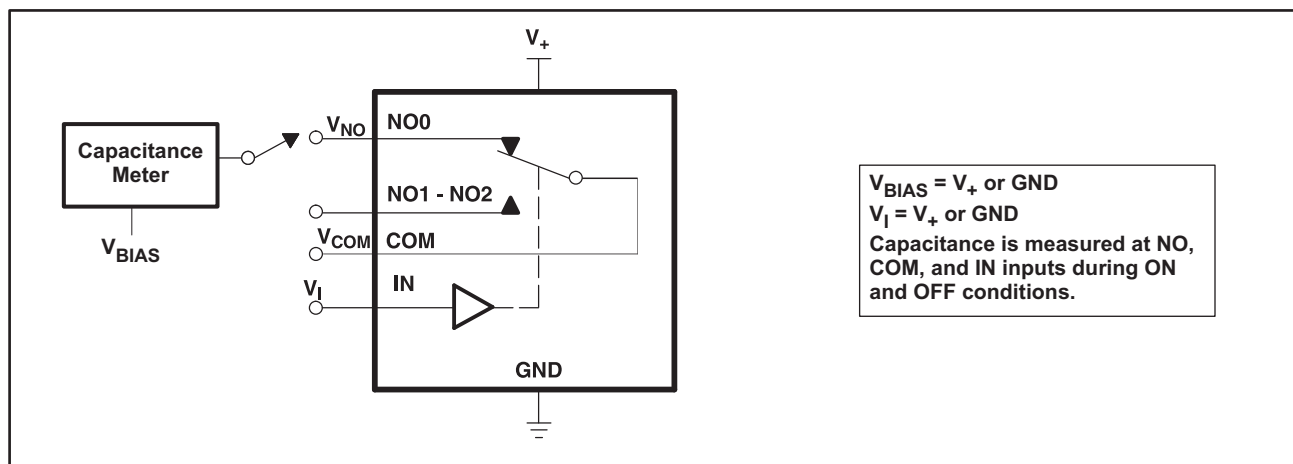
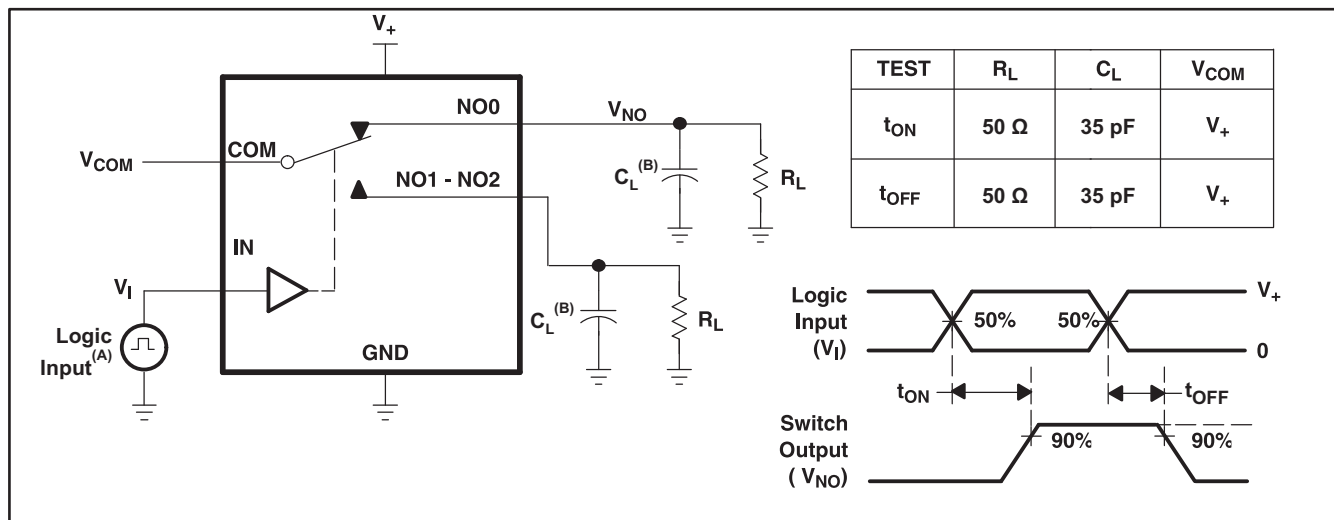


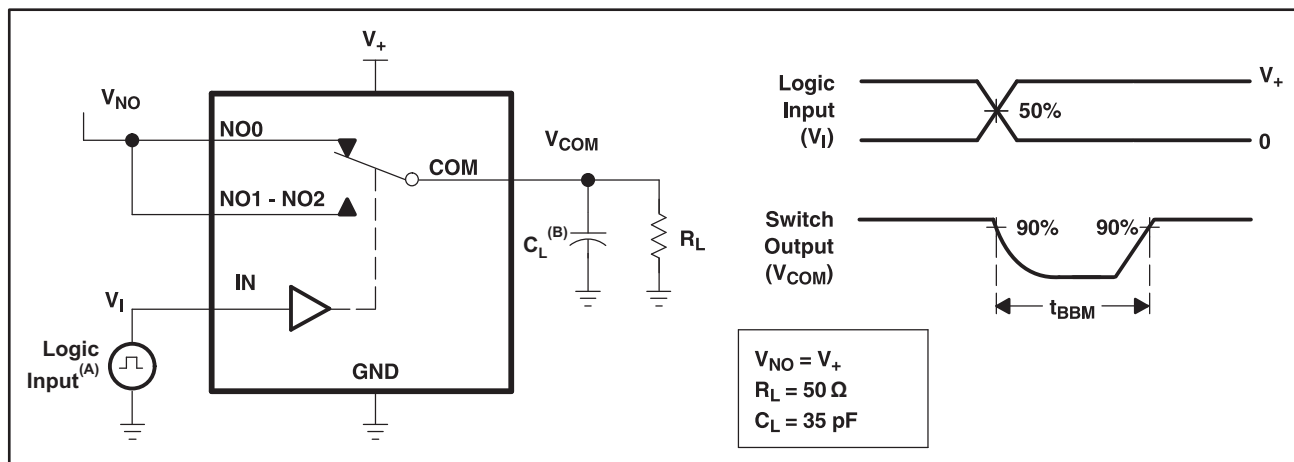
Figure 22. Capacitance (C_I , $C_{COM(ON)}$, $C_{NO(OFF)}$, $C_{COM(OFF)}$, $C_{NO(ON)}$)



- A. All input pulses are supplied by generators having the following characteristics: PRR $\leq$ 10 MHz, $Z_O = 50 \Omega$, $t_r < 5$ ns, $t_f < 5$ ns.
- B. C_L includes probe and jig capacitance.

Figure 23. Turn-On (t_{ON}) and Turn-Off Time (t_{OFF})

PARAMETER MEASUREMENT INFORMATION (continued)



- All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.
- C_L includes probe and jig capacitance.

Figure 24. Break-Before-Make Time (t_{BBM})

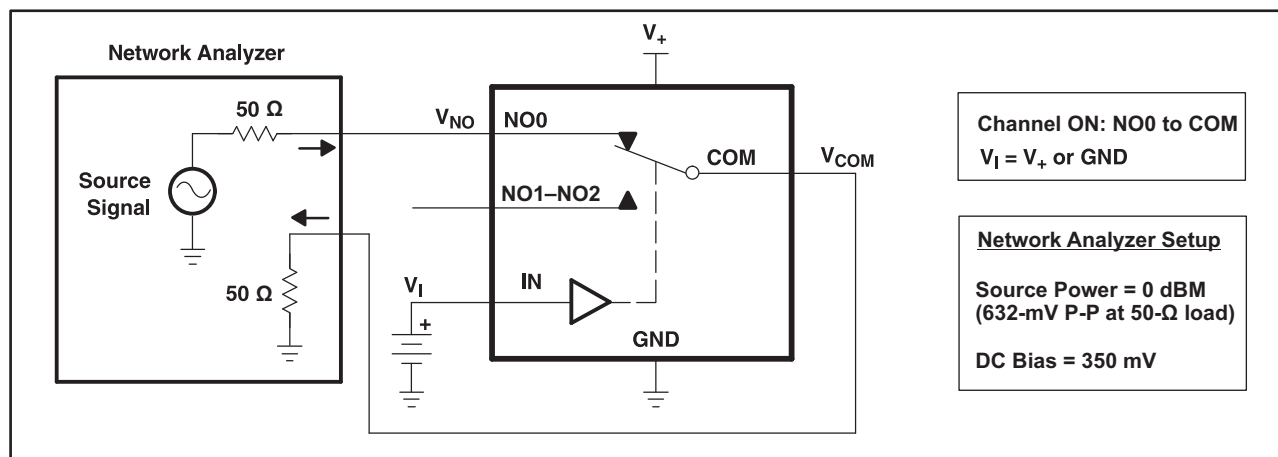


Figure 25. Bandwidth (BW)

PARAMETER MEASUREMENT INFORMATION (continued)

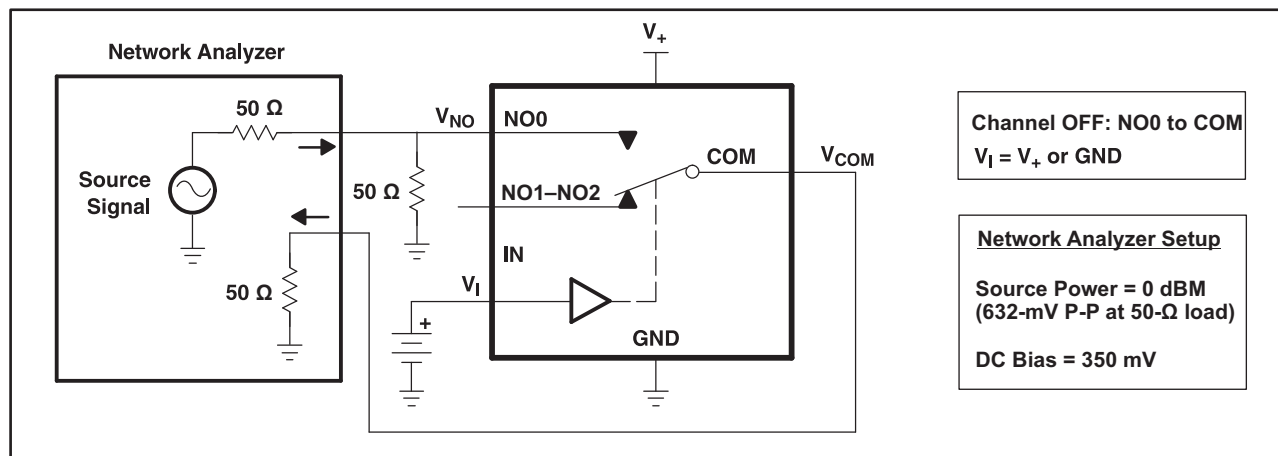


Figure 26. OFF Isolation (O_{ISO})

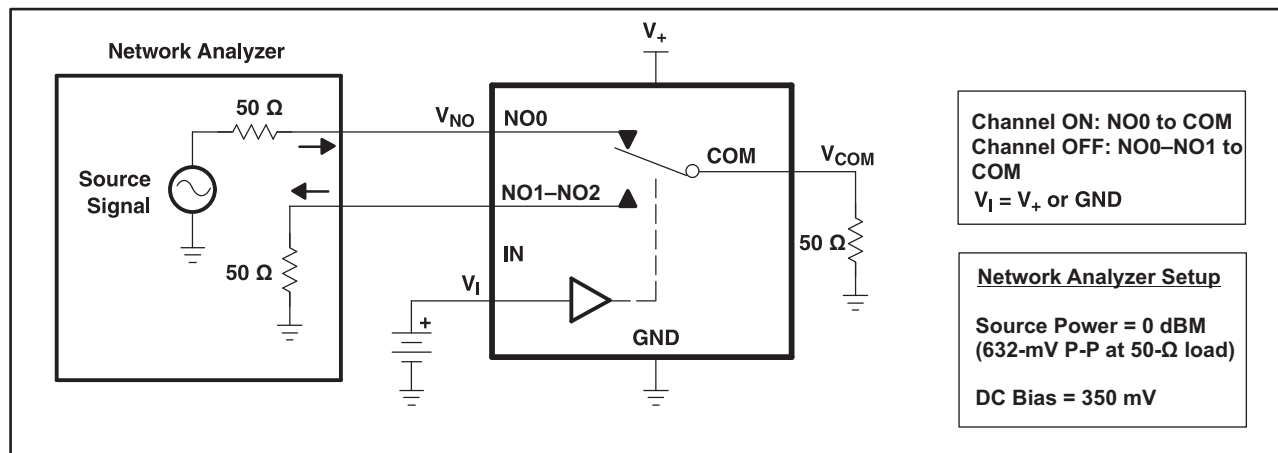
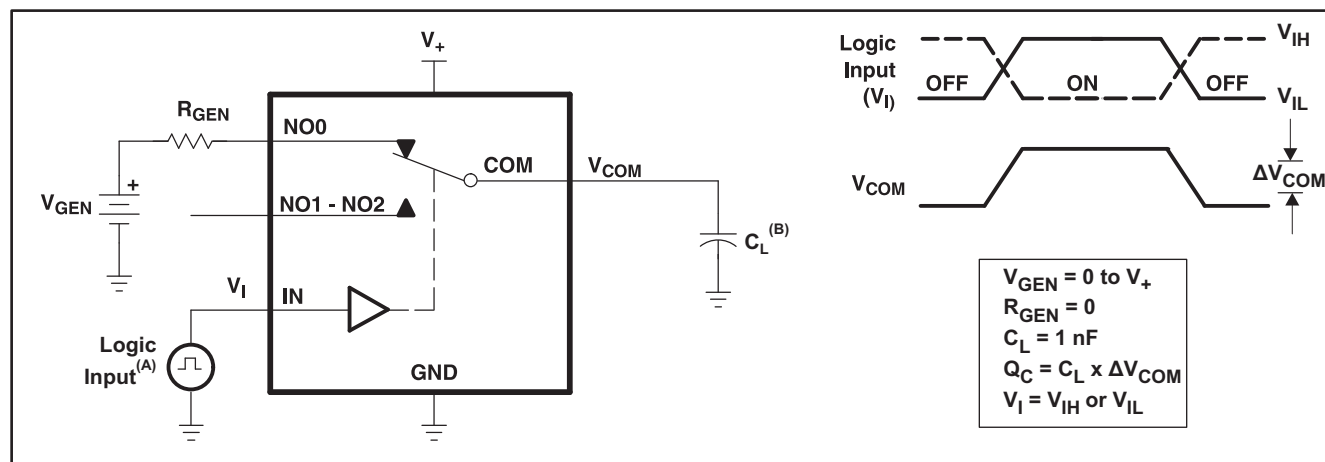


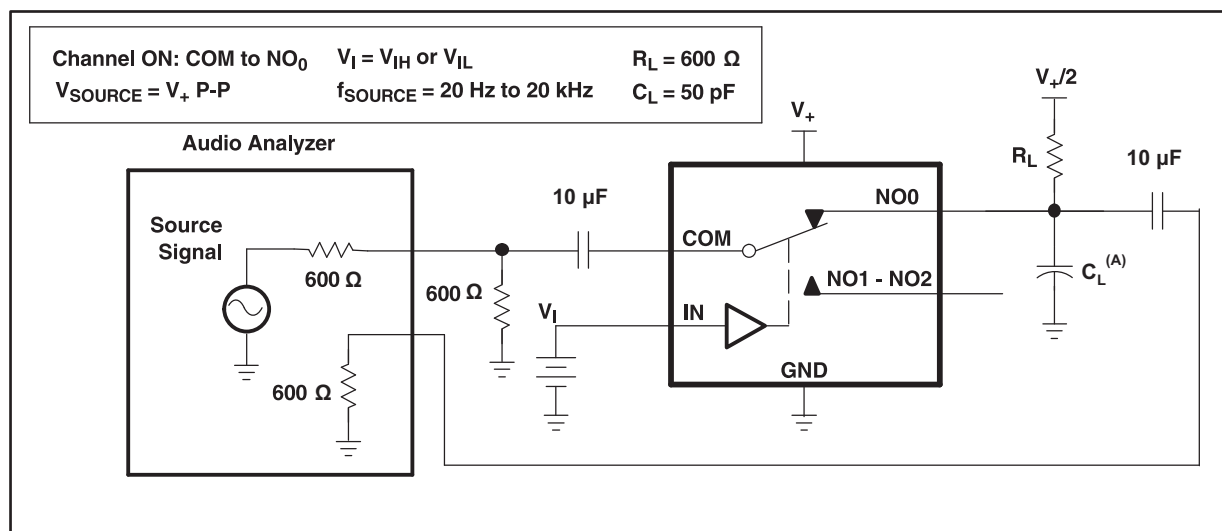
Figure 27. Crosstalk (X_{TALK})

PARAMETER MEASUREMENT INFORMATION (continued)



- A. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r < 5 \text{ ns}$, $t_f < 5 \text{ ns}$.
- B. C_L includes probe and jig capacitance.

Figure 28. Charge Injection (Q_C)



- A. C_L includes probe and jig capacitance.

Figure 29. Total Harmonic Distortion (THD)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TS5A3359DCUR	ACTIVE	US8	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(AL ~ JALR) JZ	Samples
TS5A3359DCURE4	ACTIVE	US8	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(AL ~ JALR) JZ	Samples
TS5A3359DCURG4	ACTIVE	US8	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(AL ~ JALR) JZ	Samples
TS5A3359DCUT	ACTIVE	US8	DCU	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(AL ~ JALR) JZ	Samples
TS5A3359DCUTE4	ACTIVE	US8	DCU	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(AL ~ JALR) JZ	Samples
TS5A3359DCUTG4	ACTIVE	US8	DCU	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(AL ~ JALR) JZ	Samples
TS5A3359YZPR	ACTIVE	DSBGA	YZP	8	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	J97	Samples
TS5A3359YZPRB	LIFEBUY	DSBGA	YZP	8		Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM		J97	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5A3359DCUR	US8	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
TS5A3359YZPR	DSBGA	YZP	8	3000	180.0	8.4	1.02	2.02	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS

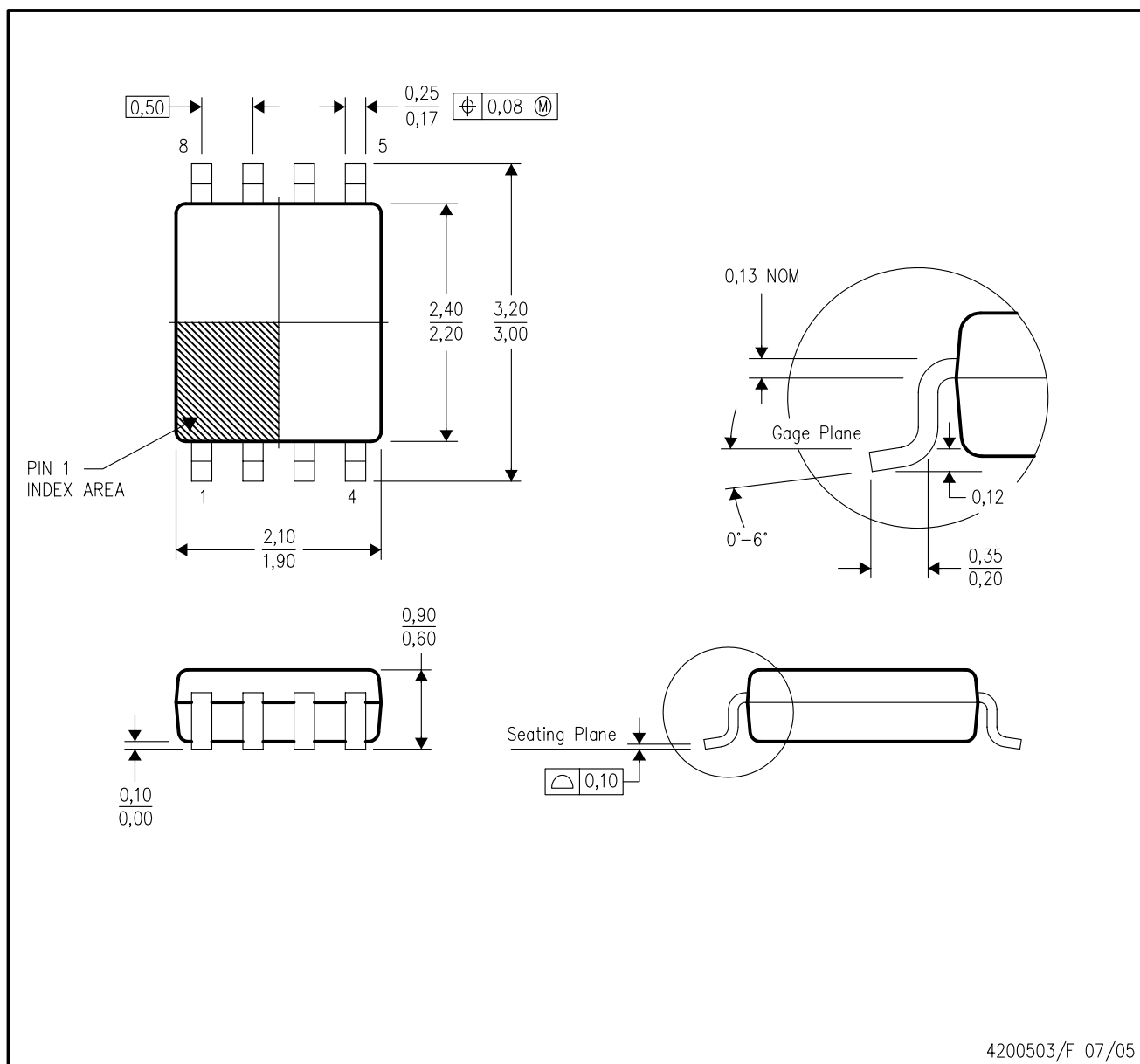


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5A3359DCUR	US8	DCU	8	3000	202.0	201.0	28.0
TS5A3359YZPR	DSBGA	YZP	8	3000	220.0	220.0	34.0

DCU (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE (DIE DOWN)

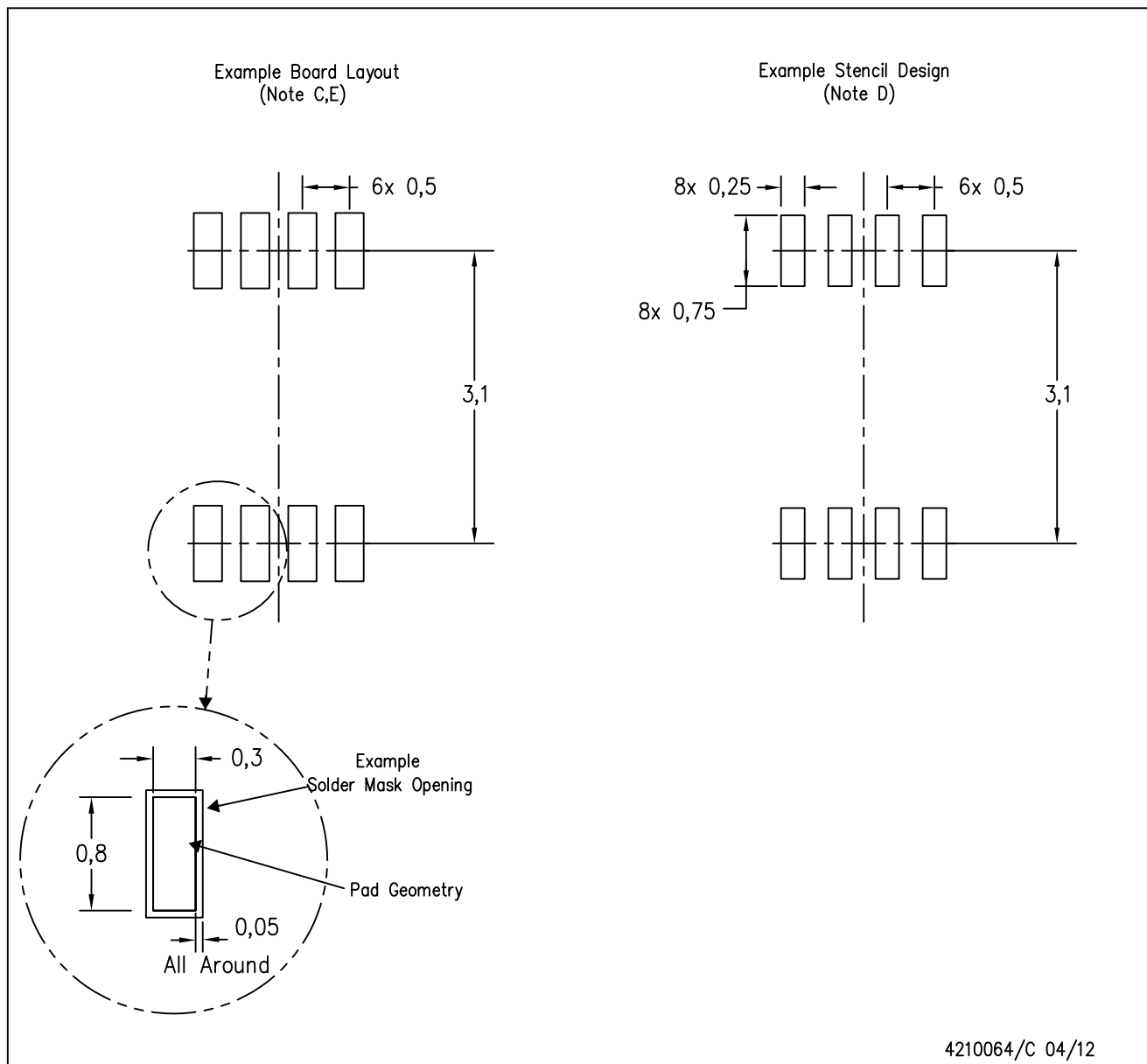


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- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Falls within JEDEC MO-187 variation CA.

DCU (S-PDSO-G8)

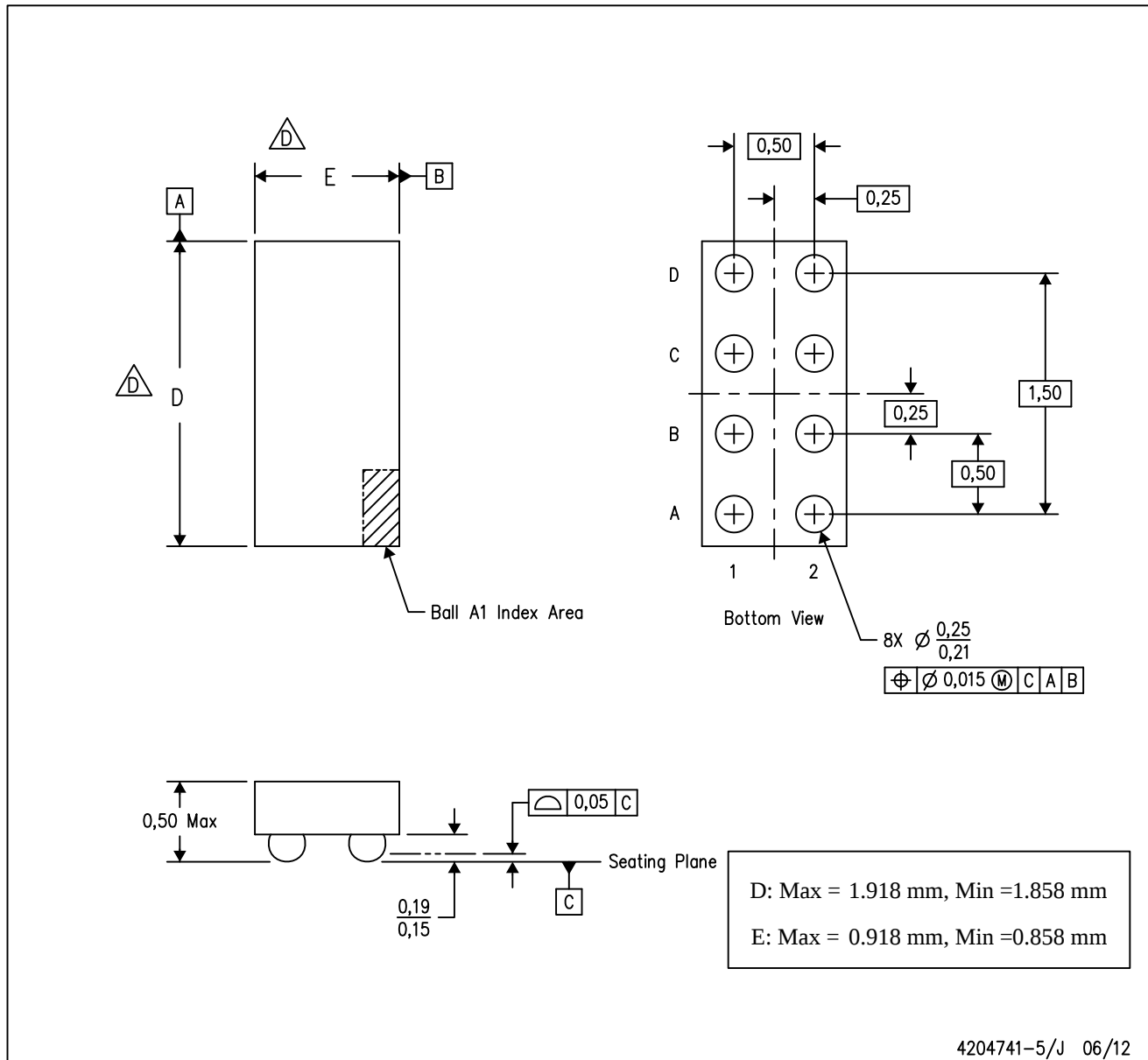
PLASTIC SMALL OUTLINE PACKAGE (DIE DOWN)



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

YZP (R-XBGA-N8)

DIE-SIZE BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. NanoFree™ package configuration.
 - The package size (Dimension D and E) of a particular device is specified in the device Product Data Sheet version of this drawing, in case it cannot be found in the product data sheet please contact a local TI representative.
 - E. This package is a Pb-free solder ball design. Refer to the 8 YEP package (drawing 4204725) for tin-lead (SnPb).

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