



# FG6943010R

Silicon N-channel MOSFET(FET1)  
 Silicon P-channel MOSFET(FET2)

For switching

■ Features

- Low drive voltage: 2.5 V drive
- Halogen-free / RoHS compliant  
 (EU RoHS / UL-94 V-0 / MSL:Level 1 compliant)

■ Marking Symbol V7

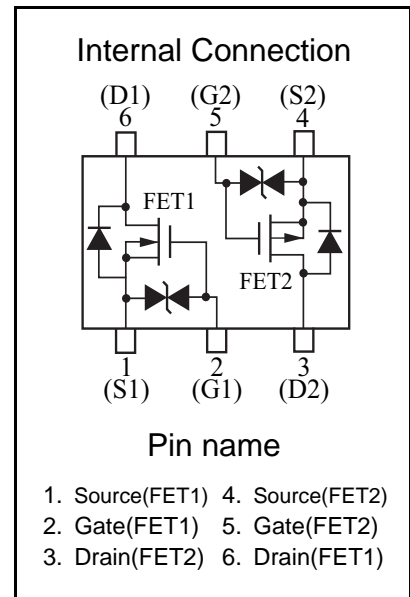
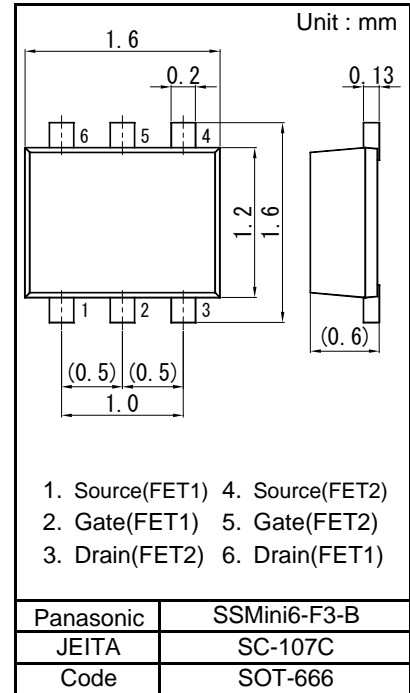
■ Basic Part Number FJ330301 + FK330301 (Individual)

■ Packaging

Embossed type (Thermo-compression sealing) 8 000 pcs / reel (standard)

■ Absolute Maximum Ratings Ta = 25 °C

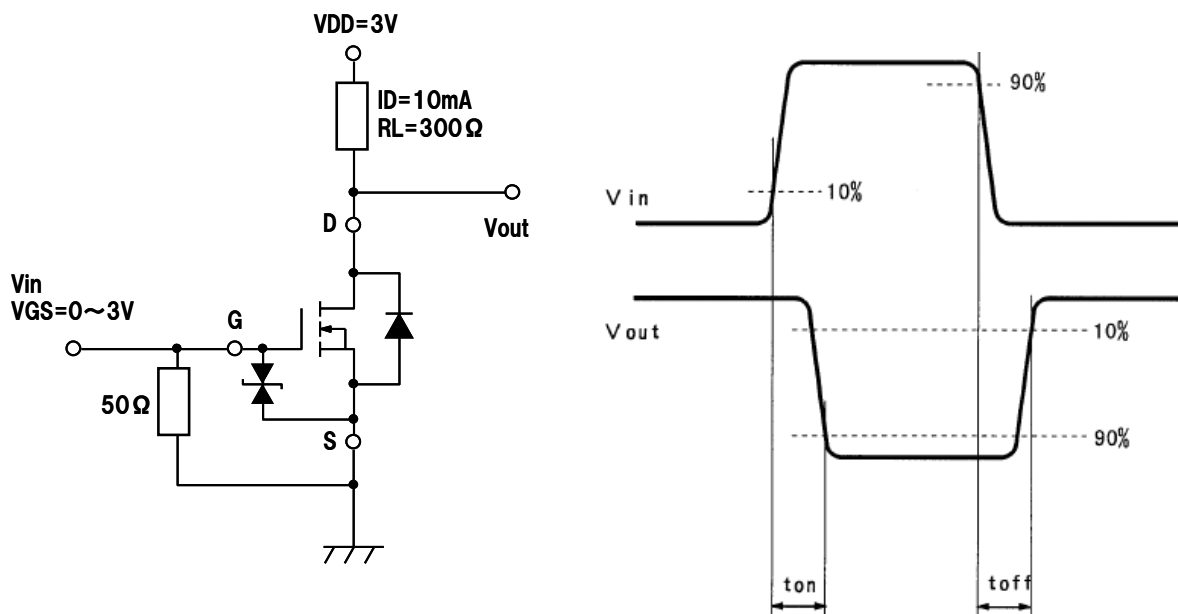
Parameter		Symbol	Rating	Unit
FET1	Drain-source voltage	VDS	30	V
	Gate-source voltage	VGS	±12	V
	Drain current	ID	100	mA
	Pulse drain current	IDp	200	mA
FET2	Drain-source voltage	VDS	-30	V
	Gate-source voltage	VGS	±12	V
	Drain current	ID	-100	mA
	Pulse drain current	IDp	-200	mA
Overall	Total power dissipation	PT	125	mW
	Channel temperature	Tch	150	°C
	Operating ambient temperature	Topr	-40 to + 85	°C
	Storage temperature	Tstg	-55 to +150	°C



■ Electrical Characteristics Ta = 25 °C ± 3 °C  
 FET1

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Drain-source breakdown voltage	VDSS	ID = 1 mA, VGS = 0	30			V
Drain-source cutoff current	IDSS	VDS = 30 V, VGS = 0			1.0	μA
Gate-source cutoff current	IGSS	VGS = ±10 V, VDS = 0			±10	μA
Gate threshold voltage	VTH	ID = 1.0 μA, VDS = 3.0 V	0.5	1.0	1.5	V
Drain-source ON resistance	RDS(on)1	ID = 10 mA, VGS = 2.5 V		3	6	Ω
	RDS(on)2	ID = 10 mA, VGS = 4.0 V		2	3	Ω
Forward transfer admittance	Yfs	ID = 10 mA, VDS = 3.0 V	20	55		mS
Input capacitance	Ciss	VDS = 3 V, VGS = 0, f = 1 MHz		12		pF
Output capacitance	Coss			7		pF
Reverse transfer capacitance	Crss			3		pF
Turn-on time *1	ton	VDD = 3 V, VGS = 0 to 3 V ID = 10 mA		100		ns
Turn-off time *1	toff	VDD = 3 V, VGS = 3 to 0 V ID = 10 mA		100		ns

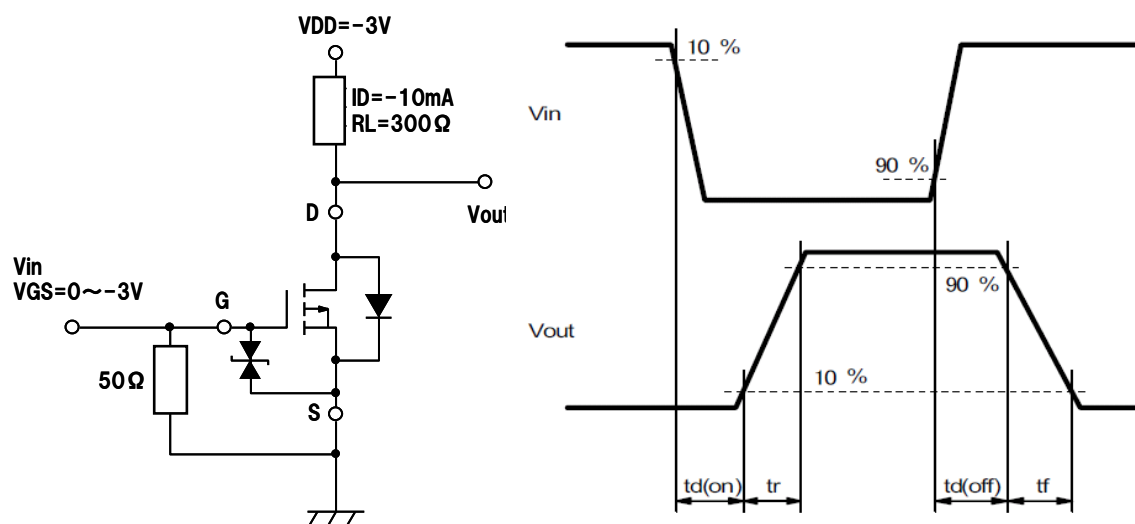
Note) 1. Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.  
 2. \*1 FET1 Turn-on and Turn-off test circuit



■ Electrical Characteristics Ta = 25 °C ± 3 °C  
 FET2

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Drain-source breakdown voltage	VDSS	ID = -1mA, VGS = 0	-30			V
Drain-source cutoff current	IDSS	VDS = -30 V, VGS = 0			-1.0	μA
Gate-source cutoff current	IGSS	VGS = ±10 V, VDS = 0			±10	μA
Gate threshold voltage	VTH	ID = -1.0 μA, VDS = -3.0 V	-0.5	-1.0	-1.5	V
Drain-source ON resistance	RDS(on)1	ID = -10 mA, VGS = -2.5 V		7	17	Ω
	RDS(on)2	ID = -10 mA, VGS = -4.0 V		4	7	Ω
Forward transfer admittance	Yfs	ID = -10 mA, VDS = -3.0 V	20	40		mS
Input capacitance	Ciss	VDS = -3 V, VGS = 0, f = 1 MHz		12		pF
Output capacitance	Coss			7		pF
Reverse transfer capacitance	Crss			3		pF
Turn-on time *1	ton	VDD = -3 V, VGS = 0 to -3 V, ID = -10 mA		100		ns
Turn-off time *1	toff	VDD = -3 V, VGS = -3 to 0 V, ID = -10 mA		100		ns

Note) 1. Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.  
 2. \*1 FET2 Turn-on and Turn-off test circuit



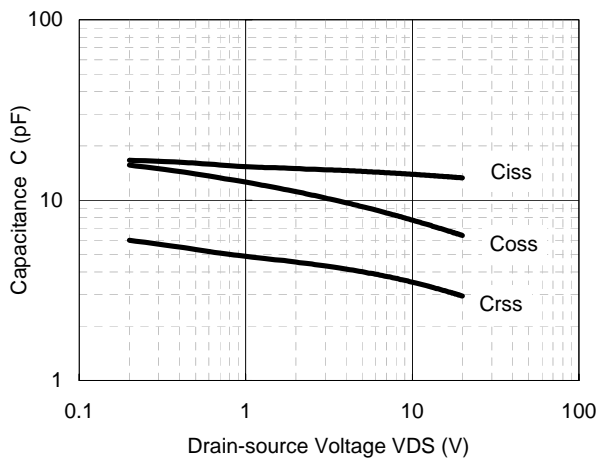
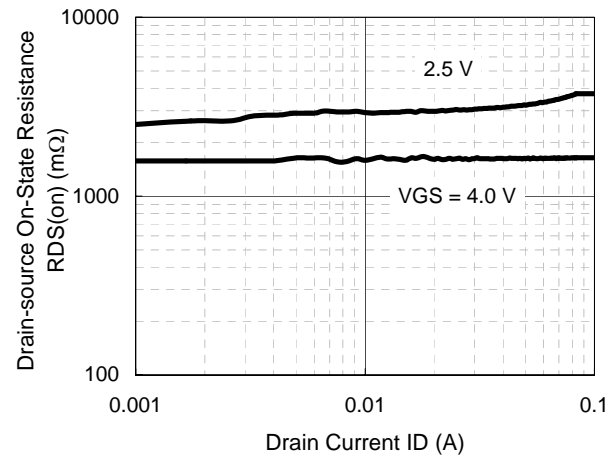
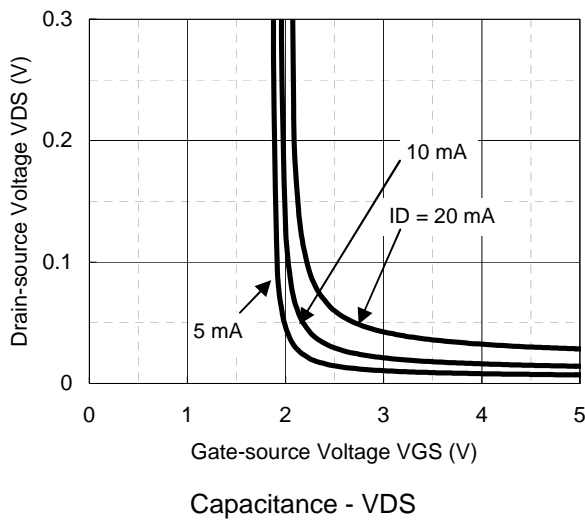
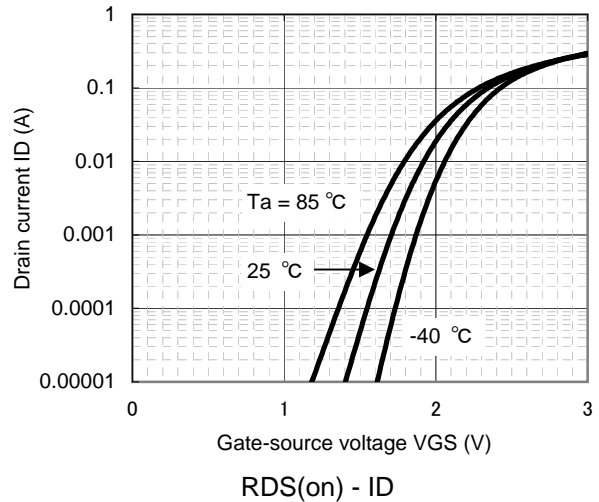
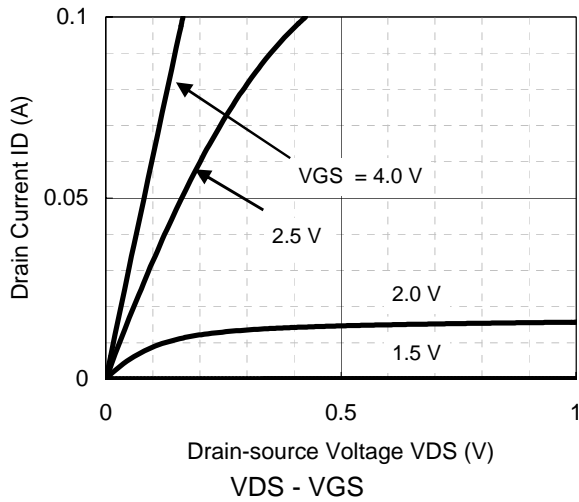


Technical Data ( reference )

FET1(N-ch.)

ID - VDS

ID - VGS

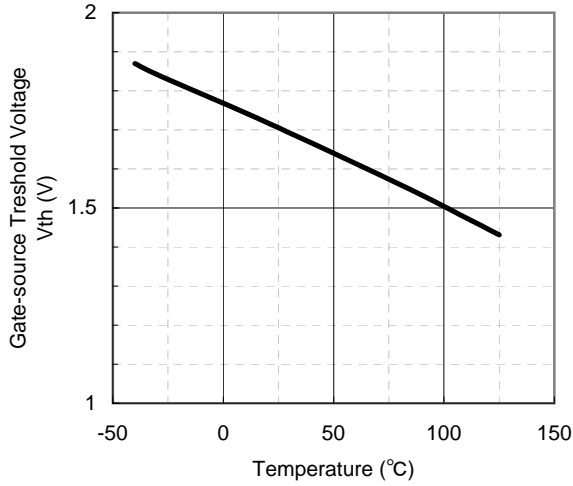




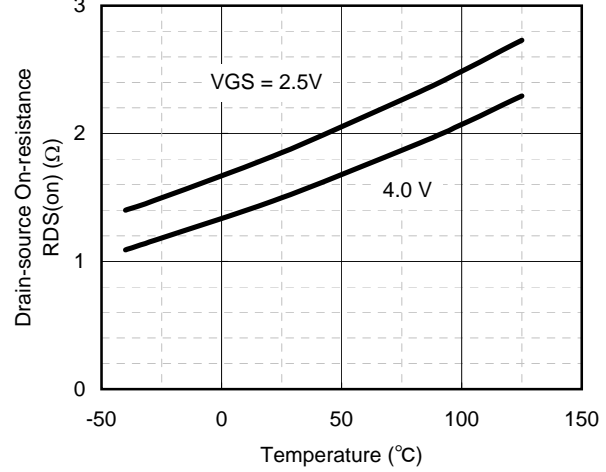
Technical Data ( reference )

FET1(N-ch.)

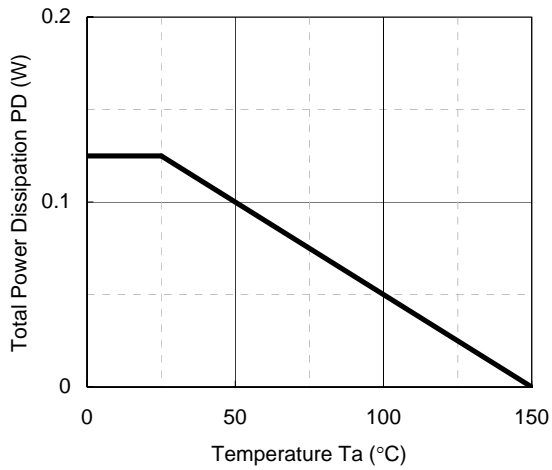
V<sub>th</sub> - T<sub>a</sub>



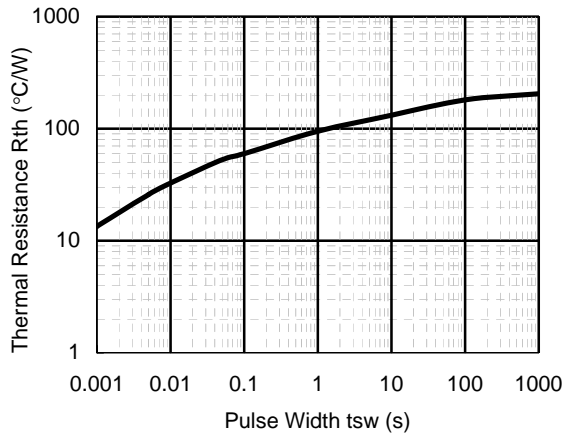
R<sub>DS(on)</sub> - T<sub>a</sub>



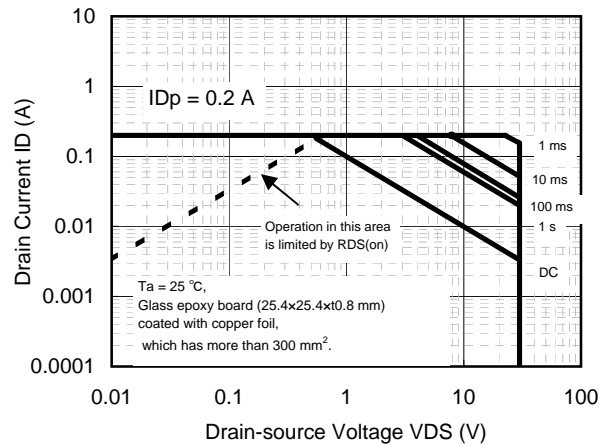
PD - T<sub>a</sub>



R<sub>th</sub> - t<sub>sw</sub>



Safe Operating Area

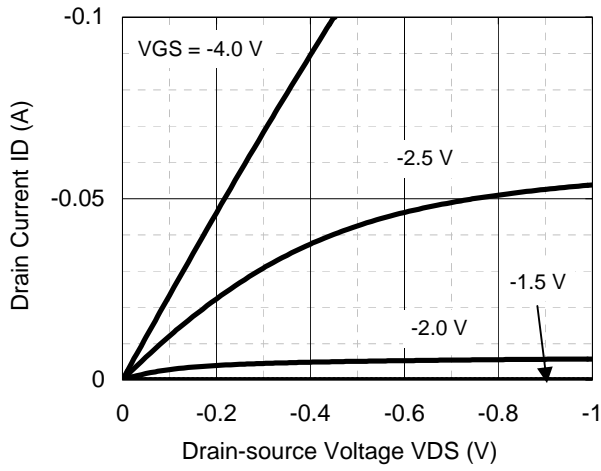




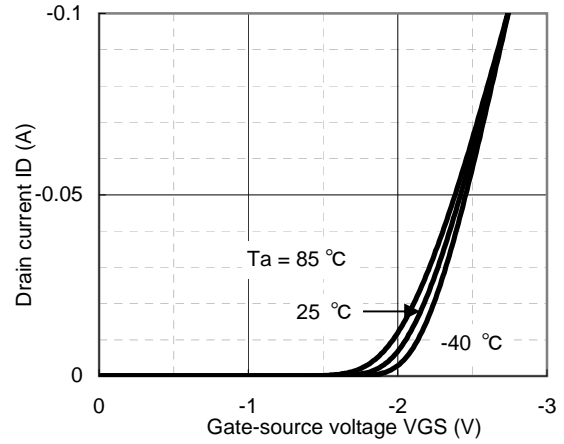
Technical Data ( reference )

FET2(P-ch.)

ID - VDS

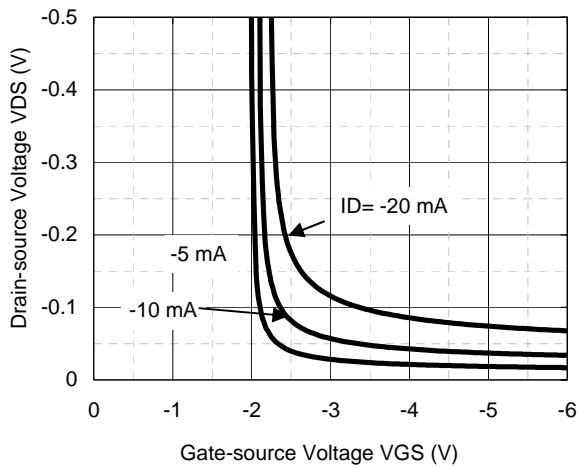


ID - VGS

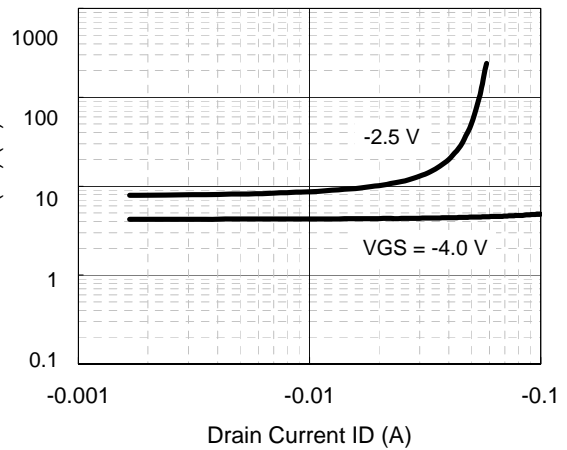


VDS - VGS

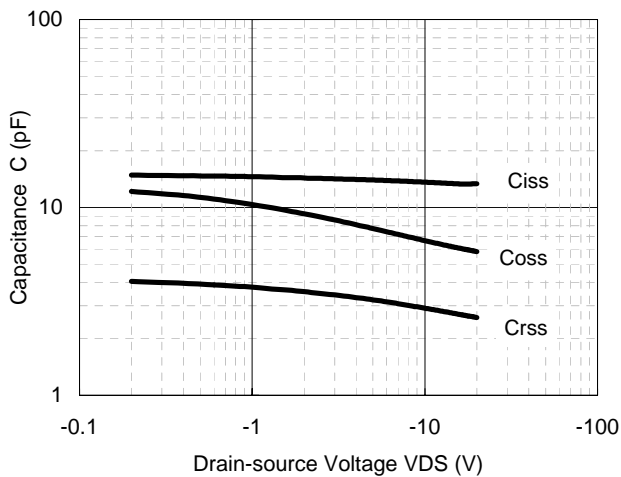
RDS(on) - ID



Drain-source On-state Resistance RDS(on) (Ω)



Capacitance - VDS

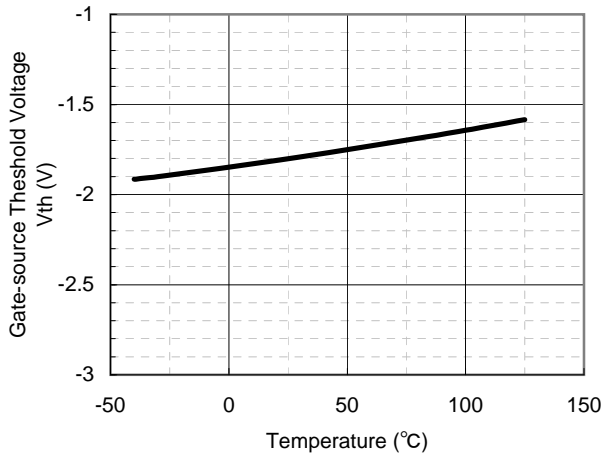




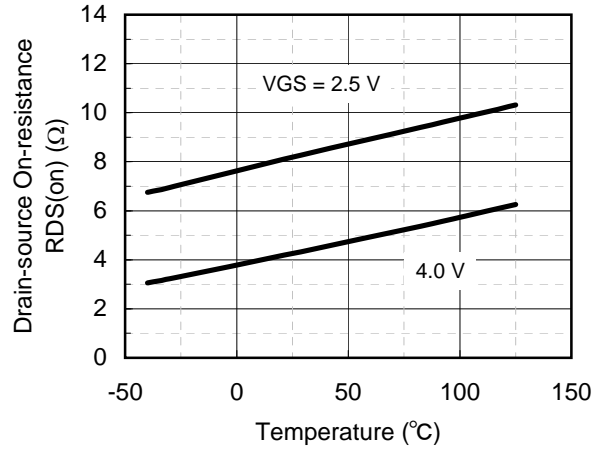
Technical Data ( reference )

FET2(P-ch.)

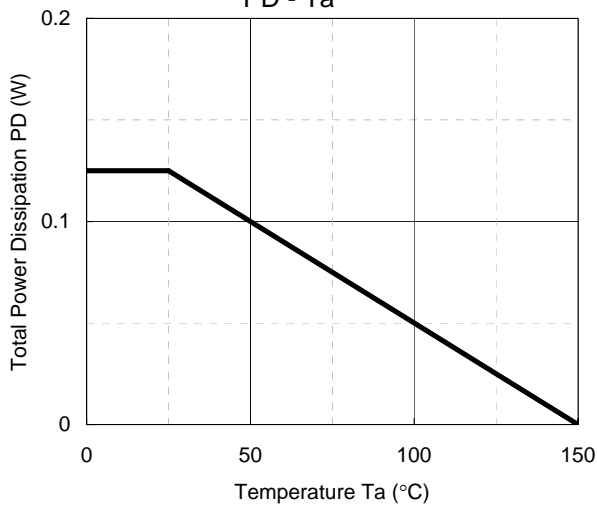
V<sub>th</sub> - T<sub>a</sub>



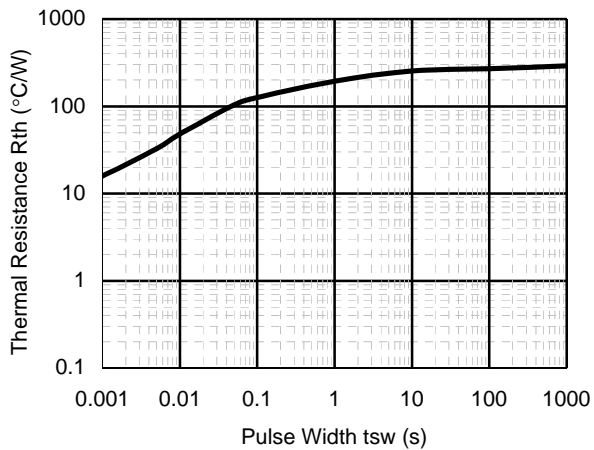
R<sub>DS(on)</sub> - T<sub>a</sub>



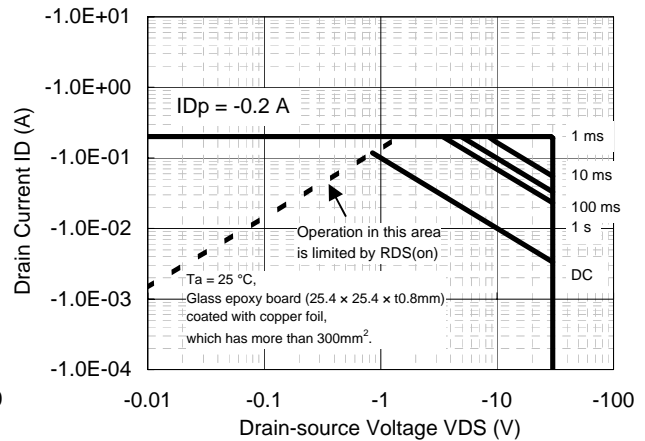
PD - T<sub>a</sub>



R<sub>th</sub> - t<sub>sw</sub>



Safe Operating Area







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