CBT3244A

Octal bus switch with quad output enables Rev. 3 — 8 September 2017

Product data sheet

General description

The CBT3244A provides eight bits of high-speed TTL-compatible bus switching in a standard '244 device pinout. The low ON-state resistance of the switch allows connections to be made with minimal propagation delay.

The CBT3244A device is organized as two 4-bit low-impedance switches with separate output-enable (OE) inputs. When OE is LOW, the switch is on and data can flow from port A to port B, or vice versa. When \overline{OE} is HIGH, the switch is open and high-impedance state exists between the two ports.

The CBT3244A is characterized for operation from -40 °C to +85 °C.

2 Features and benefits

- · Standard '244-type pinout
- 5 Ω switch connection between two ports
- · TTL compatible control input levels
- Latch-up protection exceeds 500 mA per JESD78
- ESD protection:
 - HBM JESD22-A114 exceeds 2000 V
 - MM JESD22-A115 exceeds 200 V
 - CDM JESD22-C101 exceeds 1000 V

Ordering information

Table 1. Ordering information

Type number	Package						
	Temperature range	Name	Description	Version			
CBT3244ABQ	-40 °C to + 85 °C	DHVQFN20	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 × 4.5 × 0.85 mm	SOT764-1			
CBT3244APW	-40 °C to + 85 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1			
CBT3244ADB	-40 °C to + 85 °C	SSOP20	plastic shrink small outline package; 20 leads; body width 5.3 mm	SOT339-1			
CBT3244AD	-40 °C to + 85 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1			



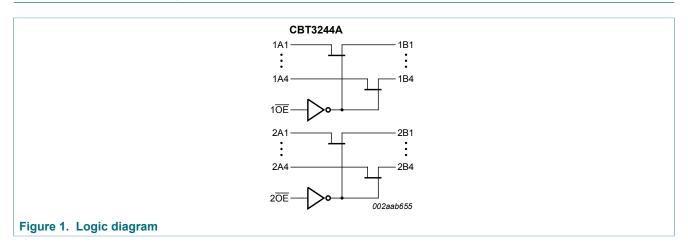
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4 Marking

Table 2. Marking codes

Type number	Marking code
CBT3244ABQ	CT3244A
CBT3244APW	CT3244A
CBT3244ADB	CT3244A
CBT3244AD	CBT3244AD

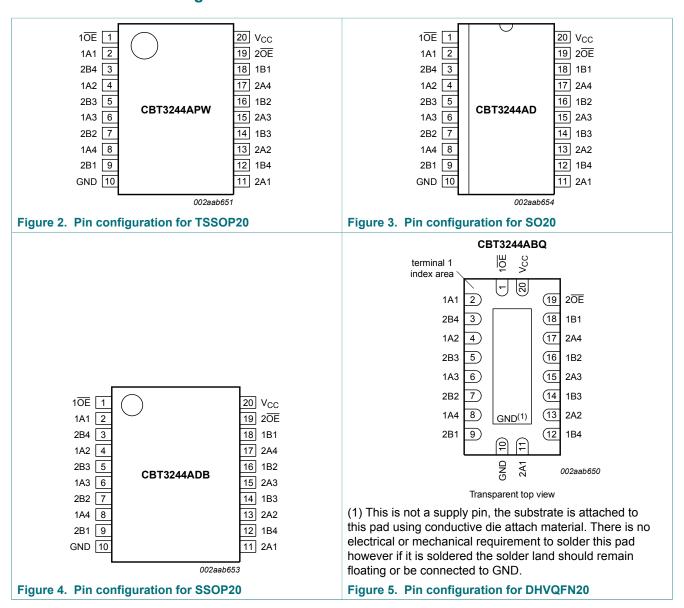
5 Functional diagram



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6 Pinning information

6.1 Pinning



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6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
1OE, 2OE	1, 19	output enable (active LOW)
1A1, 1A2, 1A3, 1A4, 2A1, 2A2, 2A3, 2A4	2, 4, 6, 8, 11, 13, 15, 17	inputs
1B1, 1B2, 1B3, 1B4, 2B1, 2B2, 2B3, 2B4	18, 16, 14, 12, 9, 7, 5, 3	outputs
GND	10	ground (0 V)
Vcc	20	positive supply voltage

7 Functional description

Table 4. Function selection [1]

Inputs		Outputs				
1 OE	2 OE	1An, 1Bn	2An, 2Bn			
L	L	1An = 1Bn	2An = 2Bn			
L	Н	1An = 1Bn	Z			
Н	L	Z	2An = 2Bn			
Н	Н	Z	Z			

^[1] H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF state

8 Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V). [1]

Symbol	Parameter	Conditions		Min	Max	Unit
V _{CC}	supply voltage			-0.5	+7.0	V
VI	input voltage		[2]	-1.2	+7.0	V
Vo	output voltage	output in OFF or HIGH state	[2]	-0.5	+7.0	V
I _{IK}	input clamping current	V _I < 0 V		-	-18	mA
I _{OK}	output clamping current	V _O < 0 V		-	-50	mA
Io	output current	output in LOW state		-	128	mA
T _{stg}	storage temperature			-65	+150	°C

^[1] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.

^[2] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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Recommended operating conditions

Table 6. Operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V_{CC}	supply voltage		4.5	-	5.5	V
T _{amb}	ambient temperature	operating in free-air	-40	-	+85	°C

10 Static characteristics

Table 7. Static characteristics

 T_{amb} = -40 °C to +85 °C. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Typ ^[1]	Max	Unit
V _{IK}	input clamping voltage	V _{CC} = 4.5 V; I _I = -18 mA		-	-	-1.2	V
V _{IH}	HIGH-state input voltage			2.0	-	-	V
V _{IL}	LOW-state input voltage			-	-	0.8	V
I _I	input leakage current	V_{CC} = 5.5 V; V_I = V_{CC} or GND		-	-	±1	μΑ
I _{CC}	supply current	V_{CC} = 5.5 V; I_O = 0 mA; V_I = V_{CC} or GND		-	1	3	μΑ
ΔI _{CC}	additional supply current	per input; V_{CC} = 5.5 V; one input at 3.4 V; other inputs at V_{CC} or GND	[2]	-	-	2.5	mA
C _i	input capacitance	control pins; $V_I = 3 \text{ V or } 0 \text{ V}; n\overline{OE} = V_{CC}$		-	3	-	pF
C _{I/O}	input/output capacitance	$\overline{OE} = V_{CC} = 5.0 \text{ V}$		-	3	-	pF
R _{on}	ON-state resistance	V _{CC} = 4.5 V; V _I = 0 V; I _I = 64 mA	[3]	-	4	7	Ω
		V _{CC} = 4.5 V; V _I = 0 V; I _I = 30 mA		-	4	7	Ω
		V _{CC} = 4.5 V; V _I = 2.4 V; I _I = 15 mA		-	8	15	Ω

All typical values are measured at V_{CC} = 5 V; T_{amb} = 25 °C. This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

Measured by the voltage level between the A and the B terminals at the indicated current through the switch. ON-state resistance is determined by the lowest voltage of the two (A or B) terminals.

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11 Dynamic characteristics

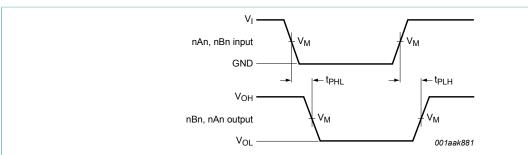
Table 8. Dynamic characteristics

T_{amb} = -40 °C to +85 °C; Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 8.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
t _{pd}	propagation delay	nAn to nBn, or nBn to nAn; [1] [2] $V_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}$; see Figure 6	-	-	0.25	ns
t _{en}	enable time	$n\overline{OE}$ to nAn or nBn; $V_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}$; see Figure 7	1.0	-	5.6	ns
t _{dis}	disable time	$n\overline{OE}$ to nAn or nBn; $V_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}$; see Figure 7	1.0	-	6.0	ns

- This parameter is warranted but not production tested. The propagation delay is based on the RC time constant of the typical ON-state resistance of the [1] switch and a load capacitance of 50 pF, when driven by an ideal voltage source (zero output impedance).
- t_{pd} is the same as t_{PHL} and $t_{\text{PLH}}.$
- t_{en} is the same as t_{PZH} and t_{PZL} .
- [2] [3] [4] t_{dis} is the same as t_{PHZ} and t_{PLZ}

11.1 Waveforms and test circuit

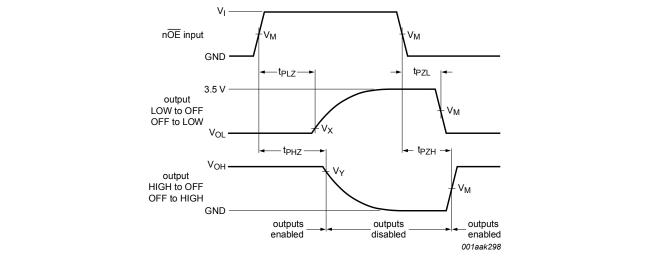


Measurement points are given in Table 9.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 6. The data input (A) to output (nYn) propagation delay times

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Measurement points are given in Table 9.

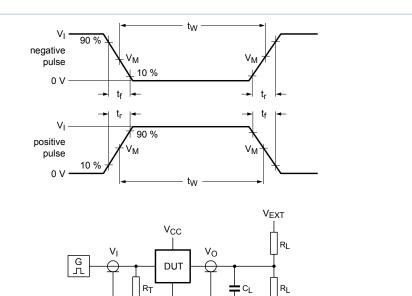
 $\ensuremath{V_{\text{OL}}}$ and $\ensuremath{V_{\text{OH}}}$ are typical output voltage levels that occur with the output load.

Figure 7. Enable and disable times

Table 9. Measurement points

Input		Output				
VI	V _M	V _M	V _X	V _Y		
3.0 V	1.5 V	1.5 V	V _{OL} + 0.3 V	V _{OH} - 0.3 V		

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Test data is given in Table 10

All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz; Z_0 = 50 Ω

The outputs are measured one at a time with one transition per measurement.

 R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

 R_T = Termination resistance should be equal to the output impedance Z_0 of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

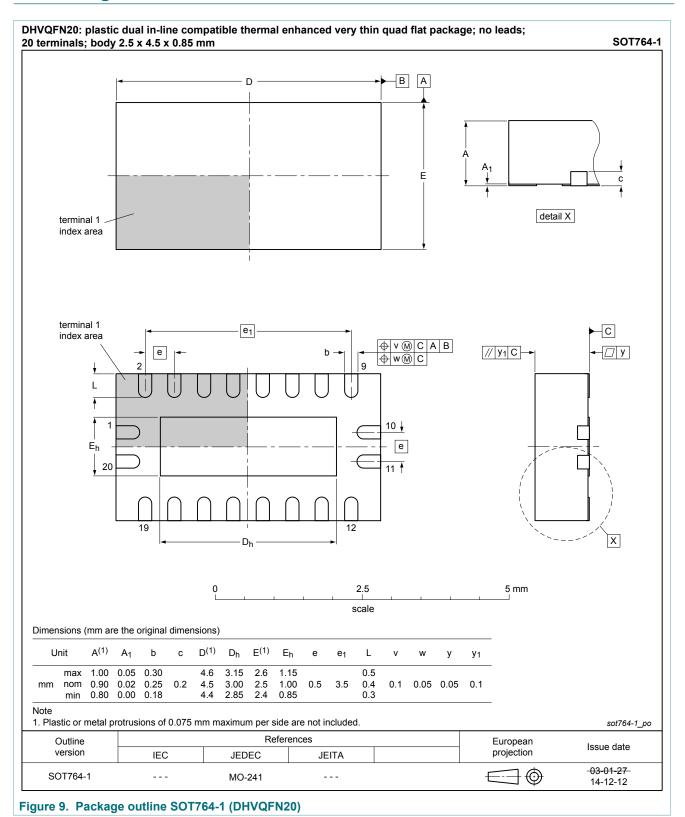
Figure 8. Test circuit for measuring switching times

Table 10. Test data

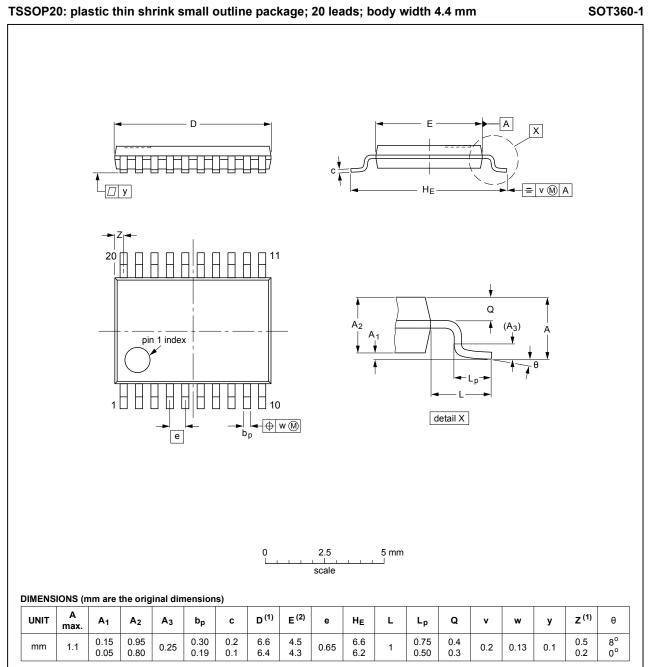
Input		Load		V _{EXT}		
V_{I}	t _r , t _f	C _L	R _L	t _{PLH} , t _{PHL}	t _{PZH} , t _{PHZ}	t _{PZL} , t _{PLZ}
V _{CC}	≤ 2.5 ns	50 pF	500 Ω	open	open	7 V

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12 Package outline



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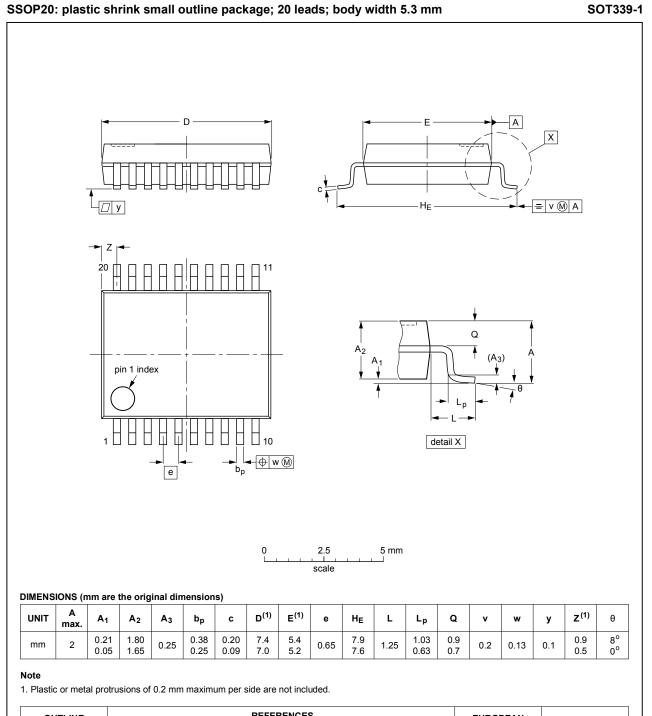


- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE		REFERENCES		REFERENCES		EUROPEAN	ISSUE DATE
VERSION	IEC	JEDEC	JEITA	PROJECTION	ISSUE DATE		
SOT360-1		MO-153			99-12-27 03-02-19		

Figure 10. Package outline SOT360-1 (TSSOP20)

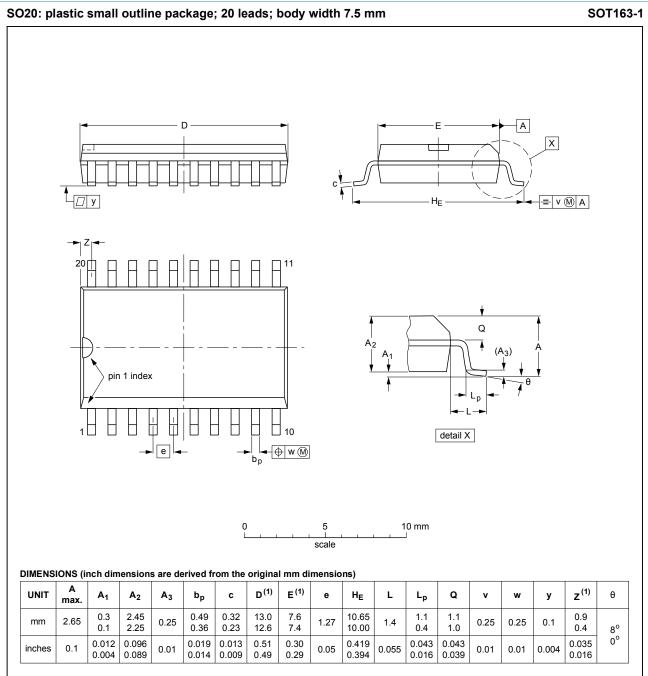
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OUTLINE	REFERENCES				EUROPEAN	ISSUE DATE
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE
SOT339-1		MO-150				99-12-27 03-02-19

Figure 11. Package outline SOT339-1 (SSOP20)

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Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN	ISSUE DATE
	IEC	JEDEC	JEITA		PROJECTION	1330E DATE
SOT163-1	075E04	MS-013				-99-12-27 03-02-19

Figure 12. Package outline SOT163-1 (SO20)

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13 Abbreviations

Table 11. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
НВМ	Human Body Model
MM	Machine Model
PRR	Pulse Rate Repetition
TTL	Transistor-Transistor Logic

14 Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes	
CBT3244A v.3	20170908	Product data sheet	-	CBT3244A v.2	
Modifications:	 The format of this data sheet has been redesigned to comply with the identity guid of Nexperia. Legal texts have been adapted to the new company name where appropriate. Type number CBT3244ADS removed. 				
CBT3244A v.2	20050915	Product data sheet	-	CBT3244A v.1	
Modifications:	 The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors. added DHVQFN20 package option. Section 2, 5th bullet: changed from 'exceeds 1000 V HBM' to 'exceeds 2000 V HBM' added Section 13 Abbreviations 				
CBT3244A v.1	20040526	Product data sheet	-	-	

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Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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