bq2203A

NV Controller With Battery Monitor

Features

- Power monitoring and switching for nonvolatile control of SRAMs
- Write-protect control
- Battery-low and battery-fail indicators
- Reset output for system power-on reset
- Input decoder for control of up to 2 banks of SRAM
- 3-volt primary cell input
- 3-volt rechargeable battery input/output

General Description

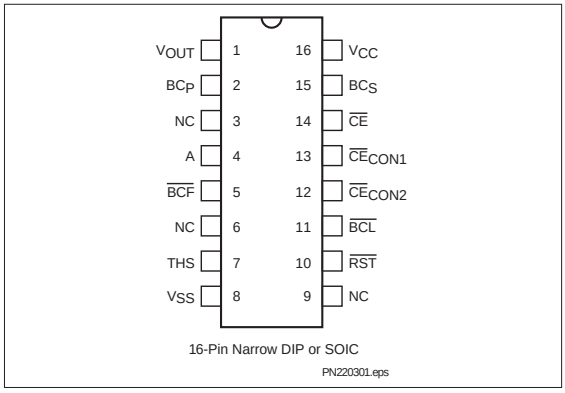
The CMOS bq2203A SRAM Nonvolatile Controller With Battery Monitor provides all the necessary functions for converting one or two banks of standard CMOS SRAM into nonvolatile read/write memory. The bq2203A is compatible with the Personal Computer Memory Card International Association (PCMCIA) recommendations for battery-backed static RAM memory cards.

A precision comparator monitors the 5V V_{CC} input for an out-of-tolerance condition. When out of tolerance is detected, the two conditioned chip-enable outputs are forced inactive to write-protect banks of SRAM.

Power for the external SRAMs is switched from the V_{CC} supply to the battery-backup supply as V_{CC} decays. On a subsequent power-up, the V_{OUT} supply is automatically switched from the backup supply to the V_{CC} supply. The external SRAMs are write-protected until a power-valid condition exists. The reset output provides power-fail and power-on resets for the system. The battery monitor indicates battery-low and battery-fail conditions.

During power-valid operation, the input decoder selects one of two banks of SRAM.

Pin Connections



16-Pin Narrow DIP or SOIC

PN220301.eps

Pin Names

V_{OUT}	Supply output
$\overline{RST}$	Reset output
THS	Threshold select input
$\overline{CE}$	chip-enable active low input
$\overline{CE}_{CON1}$, $\overline{CE}_{CON2}$	Conditioned chip-enable outputs
A	Bank select input
$\overline{BCF}$	Battery fail push-pull output
$\overline{BCL}$	Battery low push-pull output
BC_P	3V backup supply input
BC_S	3V rechargeable backup supply input/output
NC	No connect
V_{CC}	5-volt supply input
V_{SS}	Ground

Functional Description

Two banks of CMOS static RAM can be battery-backed using the V_{OUT} and the conditioned chip-enable output pins from the bq2203A. As the voltage input V_{CC} slews down during a power failure, the two conditioned chip-enable outputs, $\overline{CE}_{CON1}$ and $\overline{CE}_{CON2}$, are forced inactive independent of the chip-enable input $\overline{CE}$.

This activity unconditionally write-protects external SRAM as V_{CC} falls to an out-of-tolerance threshold V_{PFD}. V_{PFD} is selected by the threshold select input pin, THS. If THS is tied to V_{SS}, the power-fail detection occurs at 4.62V typical for 5% supply operation.

If THS is tied to V_{CC}, power-fail detection occurs at 4.37V typical for 10% supply operation. The THS pin must be tied to V_{SS} or V_{CC} for proper operation.

If a memory access is in process to any of the two external banks of SRAM during power-fail detection, that memory cycle continues to completion before the memory is write-protected. If the memory cycle is not terminated within time t_{WPT} (150µs maximum), the two chip-enable outputs are unconditionally driven high, write-protecting the controlled SRAMs.

Nov. 1994 B

As the supply continues to fall past V_{PFD}, an internal switching device forces V_{OUT} to the external backup energy source. $\overline{CE}_{CON1}$ and $\overline{CE}_{CON2}$ are held high by the V_{OUT} energy source.

During power-up, V_{OUT} is switched back to the 5V supply as V_{CC} rises above the backup cell input voltage sourcing V_{OUT}. Outputs $\overline{CE}_{CON1}$ and $\overline{CE}_{CON2}$ are held inactive for time t_{CER} (120ms maximum) after the power supply has reached V_{PFD}, independent of the $\overline{CE}$ input, to allow for processor stabilization.

During power-valid operation, the $\overline{CE}$ input is passed through to one of the two $\overline{CE}_{CON}$ outputs with a propagation delay of less than 10ns. The $\overline{CE}$ input is output on one of the two $\overline{CE}_{CON}$ output pins depending on the level of bank select input A, as shown in the Truth Table.

Bank select input A is usually tied to a high-order address pin so that a large nonvolatile memory can be designed using lower-density memory devices. Nonvolatility and decoding are achieved by hardware hookup as shown in Figure 1.

The reset output ($\overline{RST}$) goes active within t_{PFD} (150µs maximum) after V_{PFD}, and remains active for a minimum of 40ms (120ms maximum) after power returns valid. The $\overline{RST}$ output can be used as the power-on reset for a microprocessor. Access to the external RAM may begin when $\overline{RST}$ returns inactive.

Energy Cell Inputs—BC_P, BC_S

Two backup energy source inputs are provided on the bq2203A—a primary cell BC_P and a secondary cell BC_S. The primary cell input is designed to accept any 3V primary battery (non-rechargeable), typically some type of lithium chemistry. If a primary cell is not to be used, the BC_P pin should be tied to V_{SS}. The secondary cell input BC_S is designed to accept constant-voltage current-limited rechargeable cells.

During normal 5V power valid operation, 3.3V typical is output on the BC_S pin and is current-limited internally. Although this charging method can be used with various 3V secondary cells, it is specifically designed for a Panasonic VL (vanadium-lithium) series of rechargeable cells.

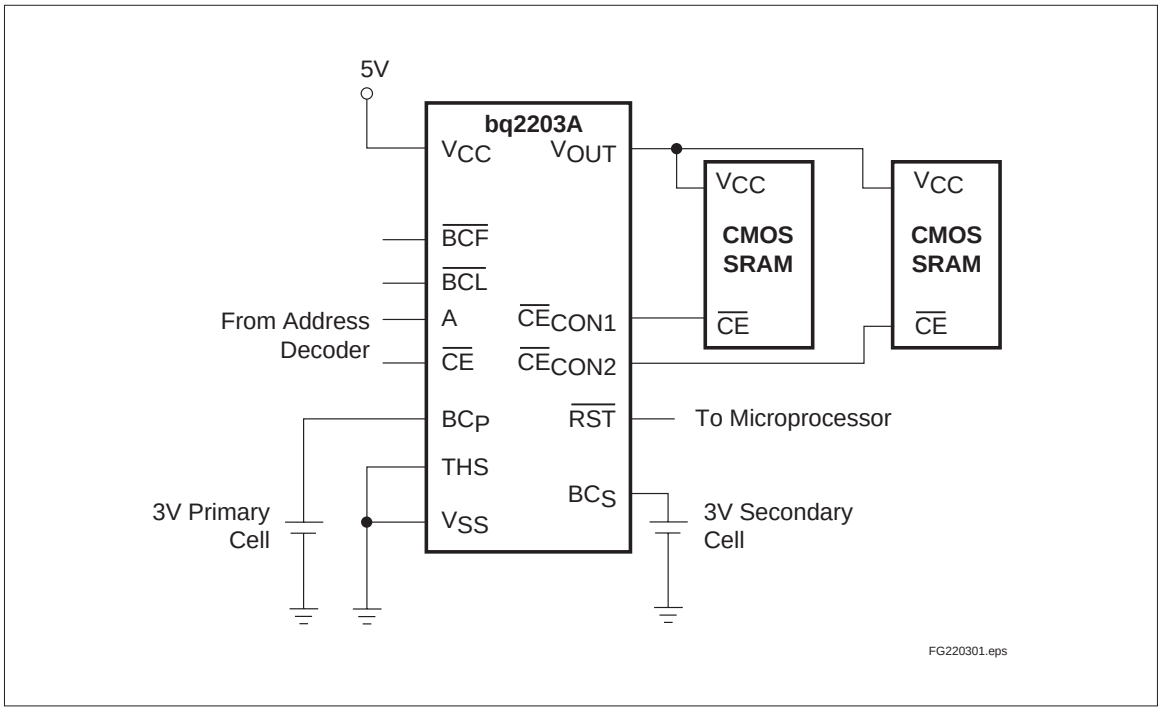


Figure 1. Hardware Hookup (5% Supply Operation)

If a secondary cell is not to be used, the BC_S pin must be tied directly to V_{SS}.

V_{CC} falling below V_{PFD} starts the comparison of BC_S and BC_P. The BC input comparison continues until V_{CC} rises above V_{SO}. Power to V_{OUT} begins with BC_S and switches to BC_P only when BC_S is less than BC_P minus V_{BSO}. The controller alternates to the higher BC voltage when the difference between the BC input voltages is greater than V_{BSO}. Alternating the backup batteries allows one-at-a-time battery replacement and efficient use of both backup batteries.

To prevent battery drain when there is no valid data to retain, V_{OUT}, $\overline{CE}_{CON1}$, and $\overline{CE}_{CON2}$ are internally isolated from BC_P and BC_S by either of two methods:

- Initial connection of a battery to BC_P or BC_S (V_{CC} grounded) or
- Presentation of an isolation signal on $\overline{CE}$.

A valid isolation signal requires $\overline{CE}$ low as V_{CC} crosses both V_{PFD} and V_{SO} during a power-down. See Figure 2. Between these two points in time, $\overline{CE}$ must be brought to V_{CC}*(0.48 to 0.52) and held for at least 700ns. The isolation signal is invalid if $\overline{CE}$ exceeds V_{CC}*0.54 at any point between V_{CC} crossing V_{PFD} and V_{SO}.

The isolation function is terminated and the appropriate battery is connected to V_{OUT}, $\overline{CE}_{CON1}$, and $\overline{CE}_{CON2}$ by powering V_{CC} up through V_{PFD}.

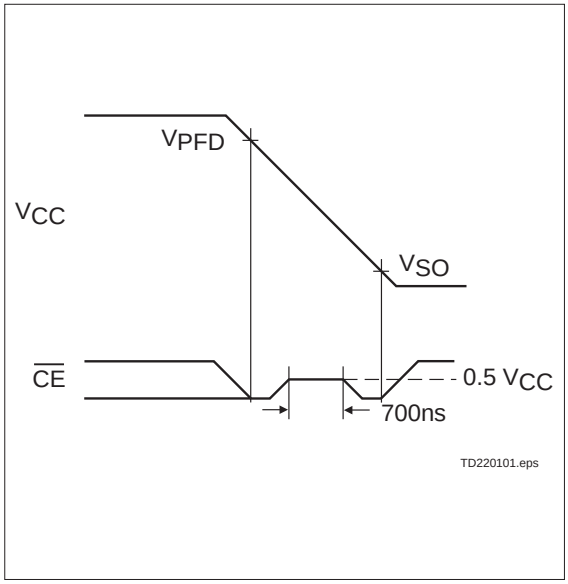


Figure 2. Battery Isolation Signal

Battery Monitor—$\overline{BCL}$, $\overline{BCF}$

As V_{CC} rises past V_{PFD}, the battery voltage on BC_P is compared with a dual-voltage reference. The result of this comparison is latched internally, and output after t_{BC} when V_{CC} rises past V_{PFD}. If the battery voltage on BC_P is below V_{BL}, then $\overline{BCL}$ is asserted low. If the battery is below V_{BF}, then $\overline{BCL}$ and $\overline{BCF}$ are asserted low. The results of this comparison remain latched until V_{CC} falls below V_{PFD}.

Truth Table

Input		Output	
$\overline{CE}$	A	$\overline{CE}_{CON1}$	$\overline{CE}_{CON2}$
H	X	H	H
L	L	L	H
L	H	H	L

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V_{CC}	DC voltage applied on V_{CC} relative to V_{SS}	-0.3 to +7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3 to +7.0	V	$V_T \le V_{CC} + 0.3$
T_{OPR}	Operating temperature	0 to 70	°C	Commercial
		-40 to +85	°C	"N" Industrial
T_{STG}	Storage temperature	-55 to +125	°C	
T_{BIAS}	Temperature under bias	-40 to +85	°C	
T_{SOLDER}	Soldering temperature	260	°C	For 10 seconds
I_{OUT}	V_{OUT} current	200	mA	

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

Recommended DC Operating Conditions ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.75	5.0	5.5	V	THS = V_{SS}
		4.50	5.0	5.5	V	THS = V_{CC}
V_{BCP}	Backup cell input voltage	2.0	-	4.0	V	$V_{CC} < V_{BC}$
V_{BCS}		2.0	-	4.0	V	$V_{CC} < V_{BC}$
V_{SS}	Supply voltage	0	0	0	V	
V_{IL}	Input low voltage	-0.3	-	0.8	V	
V_{IH}	Input high voltage	2.2	-	$V_{CC} + 0.3$	V	
THS	Threshold select	-0.3	-	$V_{CC} + 0.3$	V	

Note: Typical values indicate operation at $T_A = 25°C$, $V_{CC} = 5V$.

bq2203A

DC Electrical Characteristics ($T_A = T_{OPR}$, V_{CC} = 5V ± 10%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
I_{LI}	Input leakage current	-	-	± 1	µA	$V_{IN} = V_{SS}$ to V_{CC}
V_{OH}	Output high voltage	2.4	-	-	V	I_{OH} = -2.0mA
V_{OHB}	V_{OH}, backup supply	V_{BC} - 0.3	-	-	V	$V_{BC} > V_{CC}$, I_{OH} = -10µA
V_{OL}	Output low voltage	-	-	0.4	V	I_{OL} = 4.0mA
I_{CC}	Operating supply current	-	3	6	mA	No load on outputs
V_{PFD}	Power-fail detect voltage	4.55	4.62	4.75	V	THS = V_{SS}
		4.30	4.37	4.50	V	THS = V_{CC}
V_{SO}	Supply switch-over voltage	-	V_{BC}	-	V	
I_{CCDR}	Data-retention mode current	-	-	100	nA	No load on outputs
V_{BC}	Active backup cell voltage	-	V_{BCS}	-	V	$V_{BCS} > V_{BCP} + V_{BSO}$
		-	V_{BCP}	-	V	$V_{BCP} > V_{BCS} + V_{BSO}$
V_{BSO}	Battery switch-over voltage	0.25	0.4	0.6	V	
R_{BCS}	BC_S charge output internal resistance	500	1000	1750	Ω	$V_{BCSO} \geq 3.0V$
V_{BCSO}	BC_S charge output voltage	3.15	3.3	3.5	V	$V_{CC} > V_{PFD}$, $\overline{RST}$ inactive, full charge or no load
I_{OUT1}	V_{OUT} current	-	-	160	mA	$V_{OUT} \geq V_{CC}$ - 0.3V
I_{OUT2}	V_{OUT} current	-	100	-	µA	$V_{OUT} \geq V_{BC}$ - 0.2V
V_{BL}	Voltage battery low	2.3	-	2.5	V	BC_P input only
V_{BF}	Voltage battery fail	2.0	-	2.2	V	BC_P input only

Note: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V or V_{BC}.

Capacitance (T_A = 25°C, F = 1MHz, V_{CC} = 5.0V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
C_{IN}	Input capacitance	-	-	8	pF	Input voltage = 0V
C_{OUT}	Output capacitance	-	-	10	pF	Output voltage = 0V

Note: This parameter is sampled and not 100% tested.

AC Test Conditions

Parameter	Test Conditions
Input pulse levels	0V to 3.0V
Input rise and fall times	5ns
Input and output timing reference levels	1.5V (unless otherwise specified)
Output load (including scope and jig)	See Figure 3

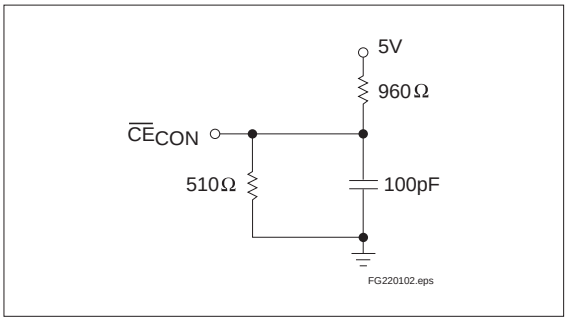


Figure 3. Output Load

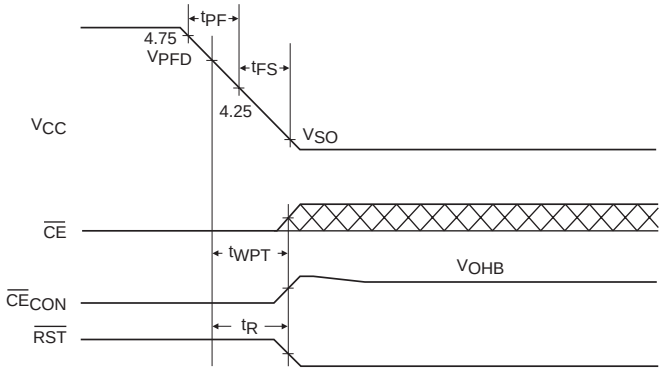
Power-Fail Control ($T_A = T_{OPR}$)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
t_{PF}	V_{CC} slew 4.75 to 4.25 V	300	-	-	µs	
t_{FS}	V_{CC} slew 4.25 V to V_{SO}	10	-	-	µs	
t_{PU}	V_{CC} slew 4.25 to 4.75 V	0	-	-	µs	
t_{CED}	Chip-enable propagation delay		7	10	ns	
t_{CER}	Chip-enable recovery time	40	80	120	ms	Time during which SRAM is write-protected after V_{CC} passes V_{PFD} on power-up
t_{RR}	V_{PFD} to $\overline{RST}$ inactive	t_{CER}	-	t_{CER}	ms	Time, after V_{CC} becomes valid, before $\overline{RST}$ is cleared
t_{AS}	Input A set up to $\overline{CE}$	0	-	-	ns	
t_{WPT}	Write-protect time	40	100	150	µs	Delay after V_{CC} slews down past V_{PFD} before SRAM is write-protected
t_R	V_{PFD} to $\overline{RST}$ active	t_{WPT}	-	t_{WPT}	µs	Delay after V_{CC} slews down past V_{PFD} before $\overline{RST}$ is active
t_{BC}	V_{PFD} to $\overline{BCL}$/$\overline{BCF}$ active	t_{CER}	-	t_{CER}	ms	Delay after V_{CC} slews up past V_{PFD} before $\overline{BCL}$ or $\overline{BCF}$ is active

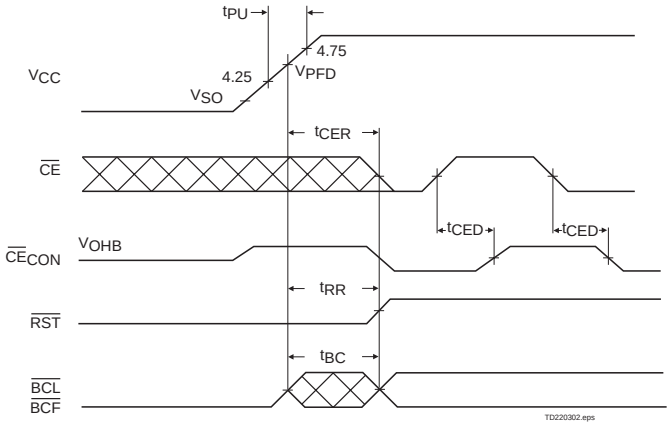
Note: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V.

Caution: Negative undershoots below the absolute maximum rating of -0.3V in battery-backup mode may affect data integrity.

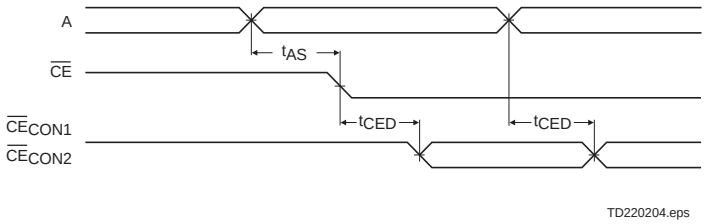
Power-Down Timing



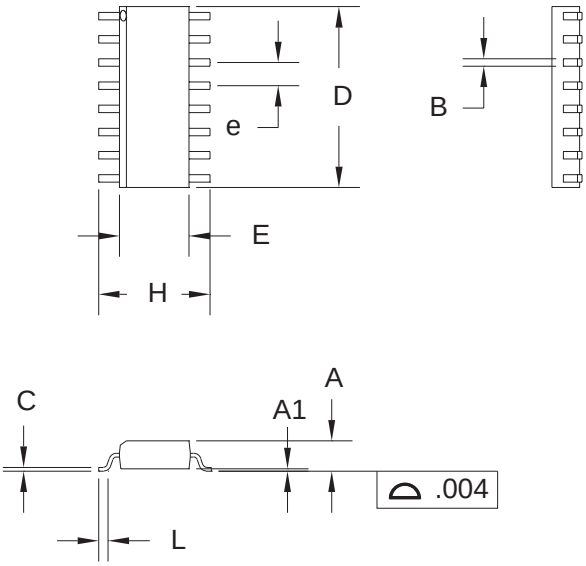
Power-Up Timing



Address-Decode Timing



16-Pin SOIC Narrow

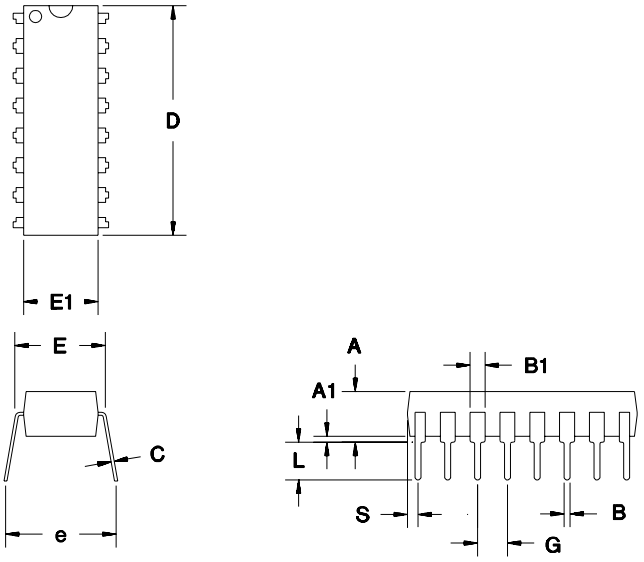


16-Pin SN (SOIC Narrow)

Dimension	Minimum	Maximum
A	0.060	0.070
A1	0.004	0.010
B	0.013	0.020
C	0.007	0.010
D	0.385	0.400
E	0.150	0.160
e	0.045	0.055
H	0.225	0.245
L	0.015	0.035

All dimensions are in inches.

16-Pin DIPNarrow



16-Pin PN (DIP Narrow)

Dimension	Minimum	Maximum
A	0.160	0.180
A1	0.015	0.040
B	0.015	0.022
B1	0.055	0.065
C	0.008	0.013
D	0.740	0.770
E	0.300	0.325
E1	0.230	0.280
e	0.300	0.370
G	0.090	0.110
L	0.115	0.150
S	0.020	0.040

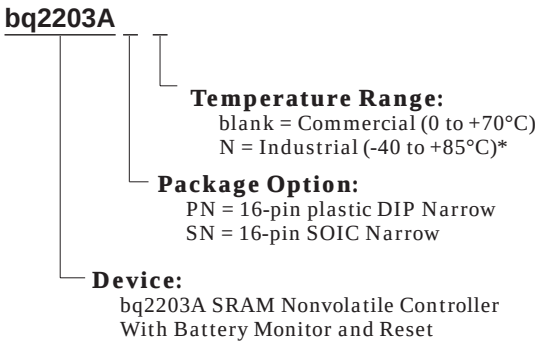
All dimensions are in inches.

Data Sheet Revision History

Change No.	Page No.	Description	Nature of Change
1	-	Changed data sheet from “Preliminary” to “Final”	
1	5	Changed maximum charge output internal resistance (R_{BCS})	Was: 1500Ω Is: 1750Ω

Note: Change 1 = Nov. 1994 B changes from Dec. 1992 A.

Ordering Information



*Contact factory for availability.

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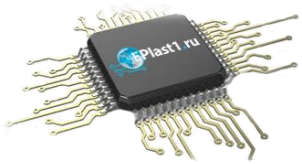
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