SCLS505B - JUNE 2003 - REVISED FEBRUARY 2008

DCK PACKAGE (TOP VIEW)

OF

GND [

Α[

- Qualified for Automotive Applications
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0), 1000-V Charged-Device Model
- Operating Range of 3 V to 5.5 V
- Max t<sub>od</sub> of 6 ns at 5 V
- Low Power Consumption, 10-µA Max I<sub>CC</sub>
- ±8-mA Output Drive at 5 V
- Inputs Are TTL-Voltage Compatible

## description/ordering information

The SN74AHCT1G126 is a single bus buffer gate/line driver with 3-state output. The output is disabled when the output-enable (OE) input is low. When OE is high, true data is passed from the A input to the Y output.

To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

#### ORDERING INFORMATION<sup>†</sup>

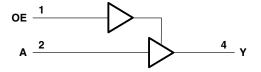
T <sub>A</sub>	PACKAGI	<u></u> ‡	ORDERABLE PART NUMBER	TOP-SIDE MARKING§
-40°C to 125°C	SOT (SC-70) – DCK	Reel of 3000	CAHCT1G126QDCKRQ1	BN_

<sup>&</sup>lt;sup>†</sup> For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at http://www.ti.com.

#### **FUNCTION TABLE**

INPL	JTS	OUTPUT
OE	Α	Υ
Н	Н	Н
Н	L	L
L	Χ	Z

### logic diagram (positive logic)





Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



<sup>&</sup>lt;sup>‡</sup> Package drawings, thermal data, and symbolization are available at http://www.ti.com/packaging.

<sup>§</sup> The actual top-side marking has one additional character that designates the assembly/test site.

### SN74AHCT1G126-Q1 SINGLE BUS BUFFER GATE WITH 3-STATE OUTPUT

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#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	–0.5 V to 7 V
Input voltage range, V <sub>I</sub> (see Note 1)	–0.5 V to 7 V
Output voltage range, V <sub>O</sub> (see Note 1)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, $I_{IK}(V_I < 0)$	–20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	±20 mA
Continuous output current, $I_O(V_O = 0 \text{ to } V_{CC})$	±25 mA
Continuous current through V <sub>CC</sub> or GND	±50 mA
Package thermal impedance, θ <sub>JA</sub> (see Note 2)	252°C/W
Storage temperature range, T <sub>sta</sub>	–65°C to 150°C

<sup>&</sup>lt;sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	3	5.5	V
v	$V_{CC} = 3.0 \text{ V}$	1.4		.,
V <sub>IH</sub>	High-level input voltage $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	2		٧
V	$V_{\rm CC} = 3.0 \text{ V}$		0.53	٧
V <sub>IL</sub>	Low-level input voltage $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$		8.0	٧
VI	Input voltage	0	5.5	٧
V <sub>O</sub>	Output voltage	0	$V_{CC}$	V
I <sub>OH</sub>	High-level output current		-8	mA
I <sub>OL</sub>	Low-level output current		8	mA
Δt/Δν	Input transition rise or fall rate		20	ns/V
T <sub>A</sub>	Operating free-air temperature	-40	125	°C

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

<sup>2.</sup> The package thermal impedance is calculated in accordance with JESD 51-7.

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## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEGT COMPLETIONS		T,	₄ = 25°C	;	14111	11 A V	
PARAMETER	TEST CONDITIONS	v <sub>cc</sub>	MIN	TYP	MAX	MIN	MAX	UNIT
	TO	3 V	2.9	3		2.9		
.,	$I_{OH} = -50 \mu\text{A}$	4.5 V	4.4	4.5		4.4		.,
V <sub>OH</sub>	$I_{OH} = -4 \text{ mA}$	3 V	2.58			2.34		V
	$I_{OH} = -8 \text{ mA}$	4.5 V	3.94			3.66		
	I <sub>OL</sub> = 50 μA				0.1		0.1	
V <sub>OL</sub>	I <sub>OL</sub> = 4 mA	3 V			0.36		0.52	V
	I <sub>OL</sub> = 8 mA	4.5 V			0.36		0.52	
lį	V <sub>I</sub> = 5.5 V or GND	0 V to 5.5 V			±0.1		±1	μΑ
I <sub>OZ</sub>	$V_O = V_{CC}$ or GND	5.5 V			±0.25		±2.5	μΑ
I <sub>CC</sub>	$V_I = V_{CC}$ or GND, $I_O = 0$ , OE high or low	3 V and 5.5 V			1		10	μΑ
$\Delta l_{CC}^{\dagger}$	One input at 3.4 V, Other input at V <sub>CC</sub> or GND	5.5 V			1.35		1.5	mA
C <sub>i</sub>	$V_I = V_{CC}$ or GND	5 V		4	10		10	pF
Co	$V_O = V_{CC}$ or GND	5 V		10				pF

<sup>†</sup> This is the increase in supply current for each input at one of the specified TTL voltage levels, rather than 0 V or V<sub>CC</sub>.

# switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3 V $\pm$ 0.3 V (unless otherwise noted) (see Figure 1)

DADAMETED	FROM	то	LOAD	T <sub>A</sub> = 25°	0	MAIN! MANY		
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN TYP	MAX	MIN MAX	UNIT	
t <sub>PLH</sub>	•	V	0 455	5.6	8	12		
t <sub>PHL</sub>	Α	Υ	C <sub>L</sub> = 15 pF	5.6	8	12	ns	
t <sub>PZH</sub>	<del>~=</del>	V	0 455	5.4	8	11.5		
t <sub>PZL</sub>	ŌĒ	Υ	C <sub>L</sub> = 15 pF	5.4	8	11.5	ns	
t <sub>PHZ</sub>	ŌĒ	Y	C <sub>L</sub> = 15 pF	6.5	9.7	14.5		
t <sub>PLZ</sub>	OE .	ī	CL = 15 pr	6.5	9.7	14.5	ns	
t <sub>PLH</sub>	•		0 50 5	8.1	11.5	16		
t <sub>PHL</sub>	Α	Υ	C <sub>L</sub> = 50 pF	8.1	11.5	16	ns	
t <sub>PZH</sub>	<u> </u>	V	0 50 5	7.9	11.5	15		
t <sub>PZL</sub>	ŌĒ	Υ	C <sub>L</sub> = 50 pF	7.9	11.5	15	ns	
t <sub>PHZ</sub>	ŌĒ	Y	C <sub>L</sub> = 50 pF	8	13.2	18	20	
t <sub>PLZ</sub>	OE .	1	OL = 50 pF	8	13.2	18	ns	



## SN74AHCT1G126-Q1 SINGLE BUS BUFFER GATE WITH 3-STATE OUTPUT

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# switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V $\pm$ 0.5 V (unless otherwise noted) (see Figure 1)

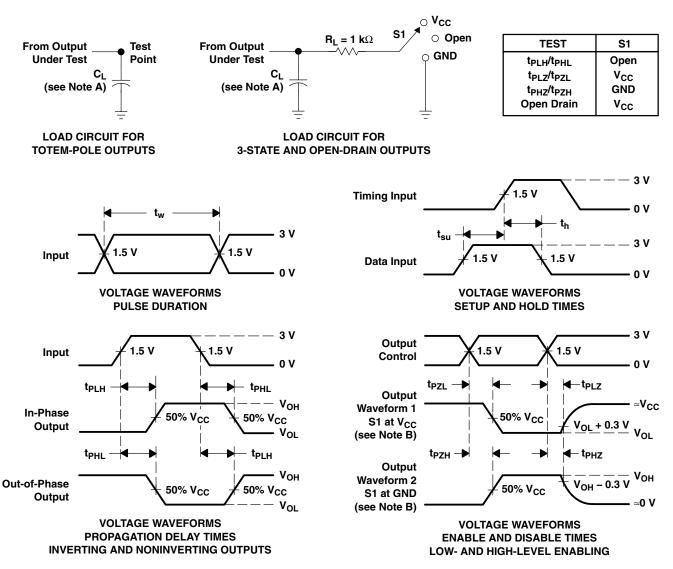
DADAMETED	FROM	то	LOAD	T,	₄ = 25°C	;	BAINI	MAY	LINUT	
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	TYP	MAX	MIN	MAX	UNIT	
t <sub>PLH</sub>	•	V	0 45 = 5		3.8	5.5		8.5		
t <sub>PHL</sub>	А	Y	C <sub>L</sub> = 15 pF		3.8	5.5		8.5	ns	
t <sub>PZH</sub>	OE	V	0 45 -5		3.6	5.1		7.5		
t <sub>PZL</sub>	OE	Υ	C <sub>L</sub> = 15 pF		3.6	5.1		7.5	ns	
t <sub>PHZ</sub>	OE	Y	C <sub>L</sub> = 15 pF		4.8	6.8		10	ns	
t <sub>PLZ</sub>	OE .	ĭ	OL = 15 pr		4.8	6.8		10	115	
t <sub>PLH</sub>			0 50 5		5.3	7.5		10.5		
t <sub>PHL</sub>	Α	Υ	C <sub>L</sub> = 50 pF		5.3	7.5		10.5	ns	
t <sub>PZH</sub>	O.F.	V	0 50 -5		5.1	7.1		9.5		
t <sub>PZL</sub>	OE	Υ	C <sub>L</sub> = 50 pF		5.1	7.1		9.5	ns	
t <sub>PHZ</sub>	0.5	Y	C <sub>L</sub> = 50 pF		7	8.8		12	no	
t <sub>PLZ</sub>	OE	r	C <sub>L</sub> = 50 pr		7	8.8		12	ns	

## operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

	PARAMETER	TEST C	ONDITIONS	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance	No load,	f = 1 MHz	14	pF



#### PARAMETER MEASUREMENT INFORMATION



NOTES: A.  $C_L$  includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_O = 50 \Omega$ ,  $t_f \leq 3$  ns.  $t_f \leq 3$  ns.
- D. The outputs are measured one at a time with one input transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms





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#### PACKAGING INFORMATION

Orderable Device	Status	Package Type	Package	Pins	Package Qty	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Top-Side Markings	Samples
	(1)		Drawing			(2)		(3)		(4)	
CAHCT1G126QDCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	BNU	Samples
CAHCT1G126QDCKRG4Q	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	BNS	Samples
CAHCT1G126QDCKRQ1	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	BNS	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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#### OTHER QUALIFIED VERSIONS OF SN74AHCT1G126-Q1:

<sup>&</sup>lt;sup>(4)</sup> Only one of markings shown within the brackets will appear on the physical device.





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• Catalog: SN74AHCT1G126

NOTE: Qualified Version Definitions:

Catalog - TI's standard catalog product

## PACKAGE MATERIALS INFORMATION

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### TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CAHCT1G126QDCKRG4	SC70	DCK	5	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3

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#### \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CAHCT1G126QDCKRG4	SC70	DCK	5	3000	203.0	203.0	35.0

## DCK (R-PDSO-G5)

## PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO-203 variation AA.



## DCK (R-PDSO-G5)

## PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.



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#### Как с нами связаться

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