LCP1521S

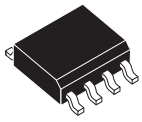
Programmable transient voltage suppressor for SLIC protection

Features

- Programmable transient suppressor
- Wide negative firing voltage range: V_{Gn} = -175 V max.
- Low dynamic switching voltages: V_{FP} and V_{DGL}
- Low gate triggering current: I_{GT} = 5 mA max.
- Peak pulse current: I_{PP} = 30 A (10/1000 µs)
- Holding current: I_H = 150 mA min.

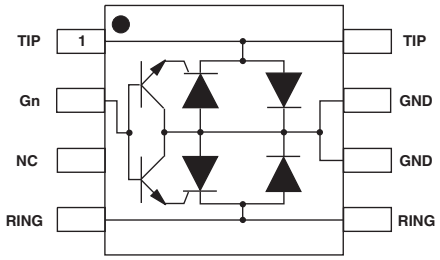
Benefits

- A Trisil™ is not subject to ageing and provides a fail safe mode in short circuit for a better level of protection.
- Trisils are used to ensure equipment meets various standards such as UL60950, IEC 950 / CSA C22.2, UL1459 and FCC part 68.
- Trisils have UL94 V0 approved resin (Trisils are UL497B approved [file: E136224]).



SO-8
LCP1521S

Figure 1. Functional diagram



Description

These devices have been especially designed to protect new high voltage, as well as classical SLICs, against transient overvoltages.

Positive overvoltages are clamped by 2 diodes. Negative surges are suppressed by 2 thyristors, their breakdown voltage being referenced to $-V_{BAT}$ through the gate.

These components present a very low gate triggering current (I_{GT}) in order to reduce the current consumption on printed circuit board during the firing phase.

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1 Characteristics

Table 1. Standards compliance

Standard	Peak surge voltage (V)	Voltage waveform	Required peak current (A)	Current waveform	Minimum serial resistor to meet standard (Ω)
GR-1089 Core First level	2500 1000	2/10 µs 10/1000 µs	500 100	2/10 µs 10/1000 µs	12 24
GR-1089 Core Second level	5000	2/10 µs	500	2/10 µs	24
GR-1089 Core Intra-building	1500	2/10 µs	100	2/10 µs	0
ITU-T-K20/K21	6000 1500	10/700 µs	150 37.5	5/310 µs	110 0
ITU-T-K20 (IEC 61000-4-2)	8000 15000	1/60 ns	ESD contact discharge ESD air discharge		0 0
IEC 61000-4-5	4000 4000	10/700 µs 1.2/50 µs	100 100	5/310 µs 8/20 µs	60 0
TIA-968-A, lightning surge type A	1500 800	10/160 µs 10/560 µs	200 100	10/160 µs 10/560 µs	22.5 15
TIA-968-A, lightning surge type B	1000	9/720 µs	25	5/320 µs	0

Table 2. Thermal resistances

Symbol	Parameter	Value	Unit
$R_{th(j-a)}$	Junction to ambient	120	°C/W

Table 3. Absolute ratings (T_{amb} = 25 °C)

Symbol	Parameter		Value	Unit
I_{PP}	Peak pulse current	10/1000 µs 8/20 µs 10/560 µs 5/310 µs 10/160 µs 1/20 µs 2/10 µs	30 100 35 40 50 100 150	A
I_{TSM}	Non repetitive surge peak on-state current (50 Hz sinusoidal)	t = 20 ms t = 200 ms t = 1 s	18 10 7	A
V_{Gn}	Negative battery voltage range	-40 °C < T_{amb} < +85 °C	-175	V
T_{stg} T_j	Storage temperature range Operating junction temperature range		-55 to +150 -40 to +150	°C
T_L	Maximum lead temperature for soldering during 10 s.		260	°C

Figure 2. Electrical characteristics (definitions)

Symbol		Parameter
I_{GT}	=	Gate triggering current
V_{FP}	=	Peak forward voltage LINE / GND
V_{GT}	=	Gate triggering voltage
V_F	=	Forward drop voltage LINE /GND
I_{RG}	=	Reverse leakage current GATE / LINE
I_H	=	Holding current
V_{RG}	=	Reverse voltage GATE / LINE
V_{DGL}	=	Dynamic switching voltage GATE / LINE
I_{PP}	=	Peak pulse current
I_R	=	Breakdown current
V_F	=	Forward drop voltage LINE / GND
C	=	Capacitance LINE /GND

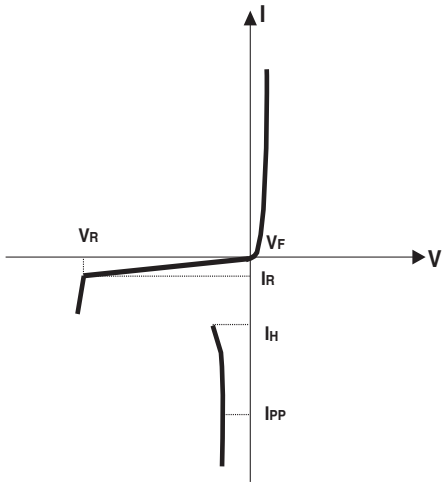


Figure 3. Pulse waveform

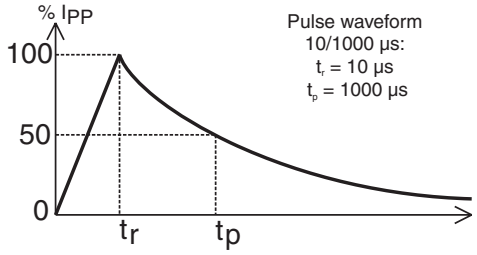


Table 4. Parameters related to the diode LINE / GND (T_{amb} = 25 °C)

Symbol	Test conditions			Max.	Unit
V_F	I_F = 5 A		t = 500 µs	3	V
V_{FP}	10/700 µs	1.5 kV	R_S = 10 Ω	5	V
	1.2/50 µs	1.5 kV	R_S = 10 Ω	9	
	2/10 µs	2.5 kV	R_S = 62 Ω	30	

Table 5. Parameters related to the protection thyristors (T_{amb} = 25 °C)

Symbol	Test conditions				Min.	Max.	Unit
I_{GT}	V_{LINE} = -48 V				0.1	5	mA
I_H	V_{Gn} = -48 V				150		mA
V_{GT}	at I_{GT}					2.5	V
I_{RG}	V_{RG} = -175 V			T_j = 25 °C		5	µA
	V_{RG} = -175 V			T_j = 85 °C		50	
V_{DGL}	V_{Gn} = -48 V(1)						V
	10/700 µs	1.5 kV	R_S = 10 Ω	I_{PP} = 30 A		7	
	1.2/50 µs	1.5 kV	R_S = 10 Ω	I_{PP} = 30 A		10	
	2/10 µs	2.5 kV	R_S = 62 Ω	I_{PP} = 38 A		25	

1. The oscillations with a time duration lower than 50 ns are not taken into account.

Table 6. Parameters related to diode and protection thyristors (T_{amb} = 25 °C)

Symbol	Test conditions			Typ.	Max.	Unit
I_R	$V_{Gn\ /\ LINE}$ = -1 V	V_{LINE} = -175 V	T_j = 25 °C		5	µA
	$V_{Gn\ /\ LINE}$ = -1 V	V_{LINE} = -175 V	T_j = 85 °C		50	
C	V_{LINE} = -50 V, V_{RMS} = 1 V, F = 1 MHz			15		pF
	V_{LINE} = -2 V, V_{RMS} = 1 V, F = 1 MHz			35		

Table 7. Recommended gate capacitance

Symbol	Component	Min.	Typ.	Max.	Unit
C_G	Gate decoupling capacitance	100	220		nF

2 Technical information

Figure 4. LCP concept behavior

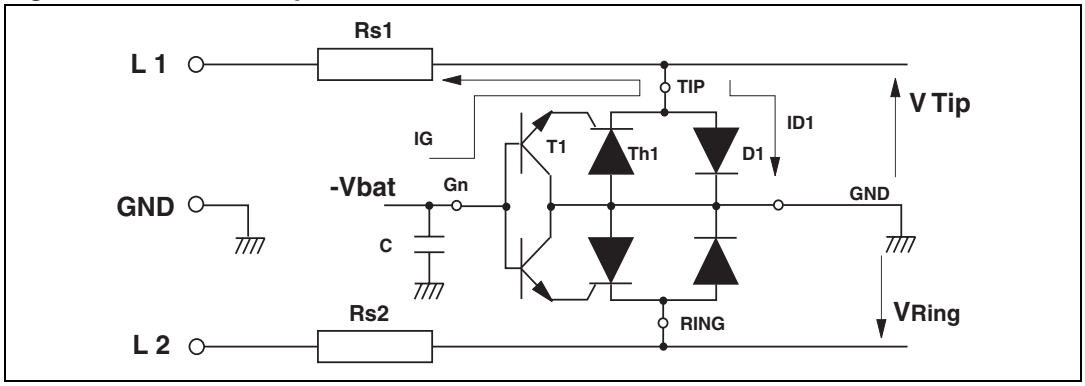


Figure 4 shows the classical protection circuit using the LCP crowbar concept. This topology has been developed to protect the new high voltage SLICs. It allows to program the negative firing threshold while the positive clamping value is fixed at GND.

When a negative surge occurs on one wire (L1 for example) a current IG flows through the base of the transistor T1 and then injects a current in the gate of the thyristor Th1. Th1 fires and all the surge current flows through the ground. After the surge when the current flowing through Th1 becomes less negative than the holding current IH, then Th1 switches off.

When a positive surge occurs on one wire (L1 for example) the diode D1 conducts and the surge current flows through the ground.

Figure 5. Example of PCB layout based on LCP1521S protection

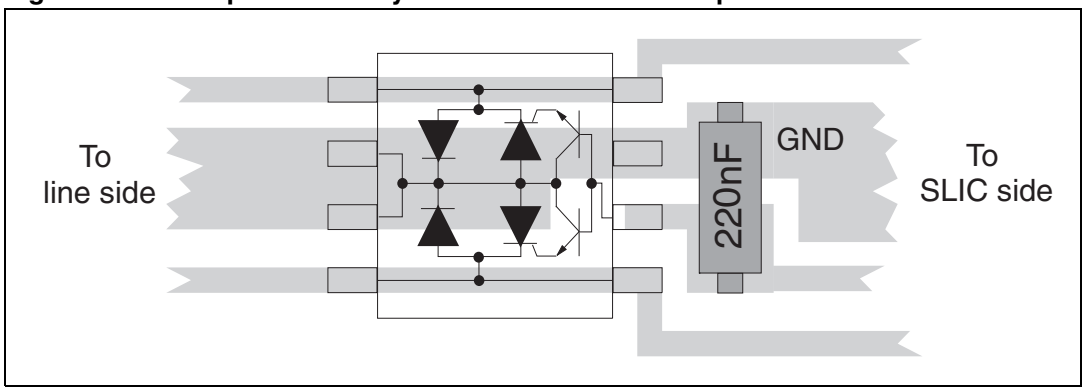


Figure 5 shows the classical PCB layout used to optimize line protection.

The capacitor C is used to speed up the crowbar structure firing during the fast surge edges.

This allows minimization of the dynamic breakover voltage at the SLIC Tip and Ring inputs during fast strikes. Note that this capacitor is generally present around the SLIC - Vbat pin.

So to be efficient it has to be as close as possible from the LCP Gate pin and from the reference ground track (or plan) (see *Figure 5*). The optimized value for C is 220 nF.

The series resistors Rs1 and Rs2 designed in *Figure 4* represent the fuse resistors or the PTC which are mandatory to withstand the power contact or the power induction tests

imposed by the various country standards. Taking into account this fact the actual lightning surge current flowing through the LCP is equal to:

$I_{surge} = V_{surge} / (R_g + R_s)$

With:

V_{surge} = peak surge voltage imposed by the standard.

R_g = series resistor of the surge generator

R_s = series resistor of the line card (e.g. PTC)

e.g. For a line card with 30 Ω of series resistors which has to be qualified under GR1089 Core 1000V 10/1000 µs surge, the actual current through the LCP is equal to:

$I_{surge} = 1000 / (10 + 30) =$ **25 A**

The LCP is particularly optimized for the new telecom applications such as the fiber in the loop, the WLL, the remote central office. In this case, the operating voltages are smaller than in the classical system. This makes the high voltage SLICs particularly suitable.

The schematics of *Figure 6* give the most frequent topology used for these applications.

Figure 6. Protection of high voltage SLIC

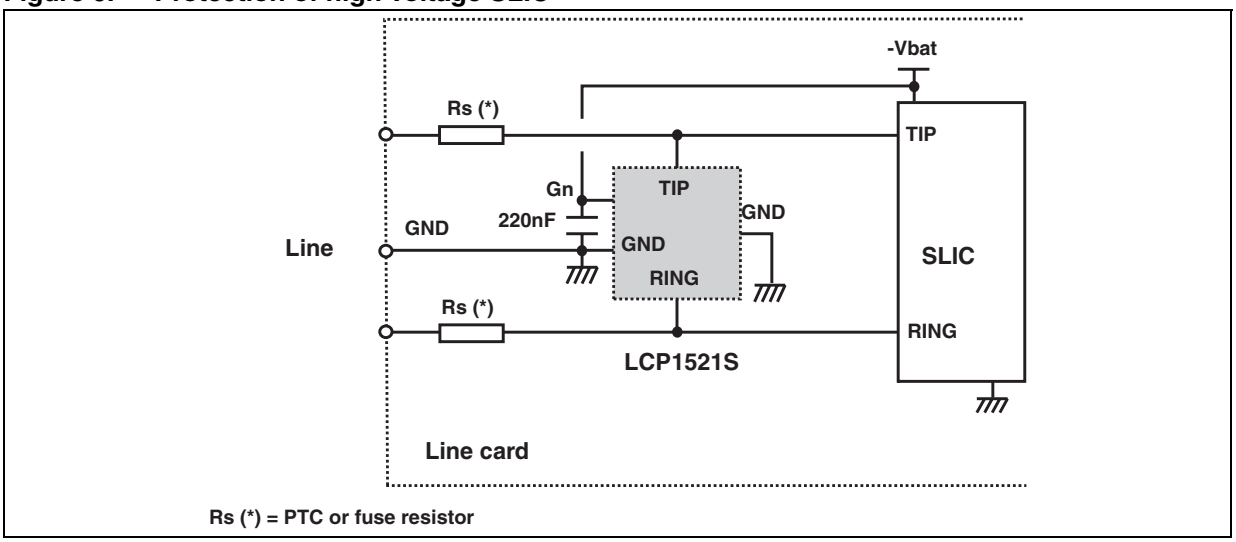


Figure 7. Surge peak current versus overload duration

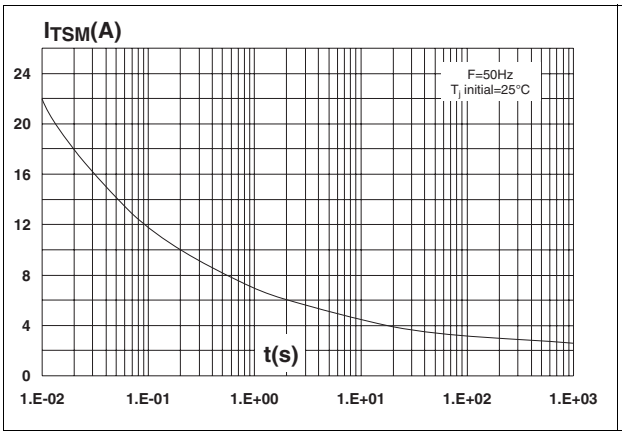
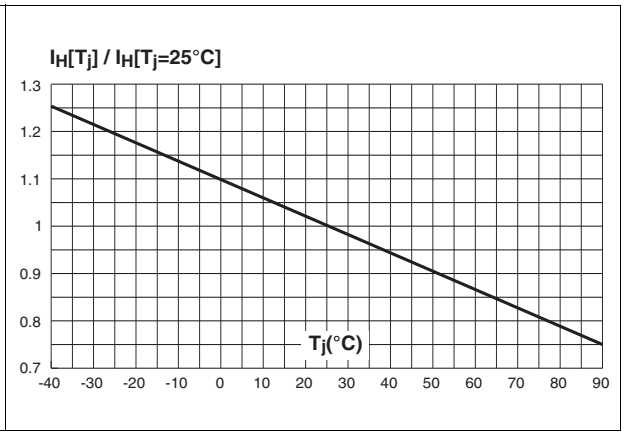


Figure 8. Relative variation of holding current versus junction temperature



3 Package information

- Epoxy meets UL94,V0
- Lead-free package

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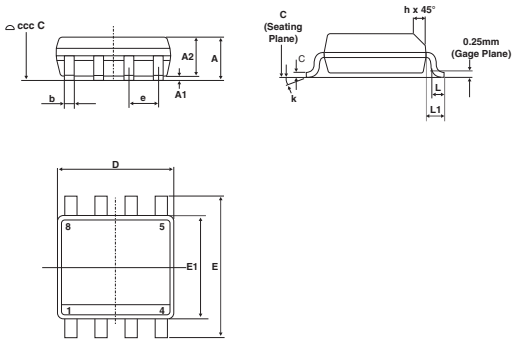
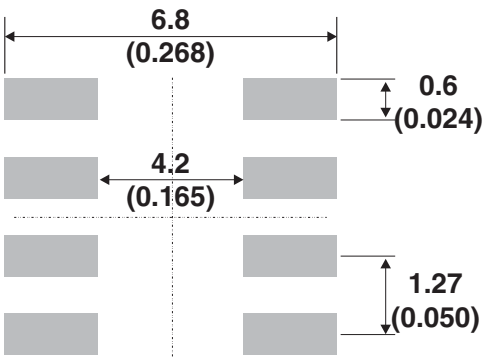
Table 8. SO-8 dimensions



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
A1	0.1		0.25	0.004		0.010
A2	1.25			0.049		
b	0.28		0.48	0.011		0.019
C	0.17		0.23	0.007		0.009
D	4.80	4.90	5.00	0.189	0.193	0.197
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e		1.27			0.050	
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
L1		1.04			0.041	
k°	0		8	0		8
ccc			0.10			0.004

Figure 9. Foot print recommendations



4 Ordering information

Table 9. Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
LCP1521S	CP152S	SO-8	0.078 g	100	Tube
LCP1521SRL[1]	CP152S			2500	Tape and reel

1. Preferred device

5 Revision history

Table 10. Document revision history

Date	Revision	Changes
20-Nov-2009	1	First issue.
23-Feb-2012	2	Standardized nomenclature for Gn.

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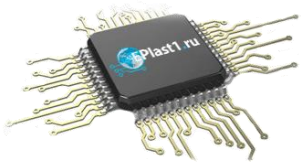

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