

E Series Power MOSFET

PRODUCT SUMMARY	
V_{DS} (V) at T_J max.	550
$R_{DS(on)}$ max. at 25 °C (Ω)	$V_{GS} = 10\text{ V}$ 0.380
Q_g max. (nC)	50
Q_{gs} (nC)	6
Q_{gd} (nC)	10
Configuration	Single

FEATURES

- Low figure-of-merit (FOM) $R_{on} \times Q_g$
- Low input capacitance (C_{iss})
- Reduced switching and conduction losses
- Low gate charge (Q_g)
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

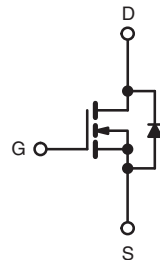
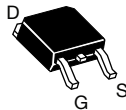


RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Computing
 - PC silver box / ATX power supplies
- Lighting
 - Two stage LED lighting
- Consumer electronics
- Applications using hard switched topologies
 - Power factor correction (PFC)
 - Two switch forward converter
 - Flyback converter
- Switch mode power supplies (SMPS)

DPAK
(TO-252)



N-Channel MOSFET

ORDERING INFORMATION	
Package	DPAK (TO-252)
Lead (Pb)-free and Halogen-free	SiHD12N50E-GE3


ABSOLUTE MAXIMUM RATINGS ($T_C = 25\text{ °C}$, unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	500	V
Gate-Source Voltage	V_{GS}	± 20	
Gate-Source Voltage AC ($f > 1\text{ Hz}$)		30	
Continuous Drain Current ($T_J = 150\text{ °C}$)	V_{GS} at 10 V	$T_C = 25\text{ °C}$	10.5
		$T_C = 100\text{ °C}$	
Pulsed Drain Current ^a	I_{DM}	21	A
Linear Derating Factor		0.91	W/°C
Single Pulse Avalanche Energy ^b	E_{AS}	103	mJ
Maximum Power Dissipation	P_D	114	W
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +150	°C
Drain-Source Voltage Slope	$V_{DS} = 0\text{ V to } 80\% V_{DS}$	70	V/ns
Reverse Diode dV/dt ^d		27	
Soldering Recommendations (Peak Temperature) ^c	for 10 s	300	°C

Notes

- Repetitive rating; pulse width limited by maximum junction temperature.
- $V_{DD} = 50\text{ V}$, starting $T_J = 25\text{ °C}$, $L = 28.2\text{ mH}$, $R_g = 25\text{ }\Omega$, $I_{AS} = 2.7\text{ A}$.
- 1.6 mm from case.
- $I_{SD} \leq I_D$, $dI/dt = 100\text{ A}/\mu\text{s}$, starting $T_J = 25\text{ °C}$.

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	62	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	1.1	



SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	500	-	-	V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = 1 mA	-	0.60	-	V/°C
Gate-Source Threshold Voltage (N)	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	2.0	-	4.0	V
Gate-Source Leakage	I _{GSS}	V _{GS} = ± 20 V	-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 500 V, V _{GS} = 0 V	-	-	1	μA
		V _{DS} = 400 V, V _{GS} = 0 V, T _J = 125 °C	-	-	10	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 6 A	-	0.330	0.380	Ω
Forward Transconductance	g _{fs}	V _{DS} = 30 V, I _D = 6 A	-	3.1	-	S
Dynamic						
Input Capacitance	C _{iSS}	V _{GS} = 0 V, V _{DS} = 100 V, f = 1 MHz	-	886	-	pF
Output Capacitance	C _{oss}		-	52	-	
Reverse Transfer Capacitance	C _{rSS}		-	6	-	
Effective Output Capacitance, Energy Related ^a	C _{o(er)}	V _{DS} = 0 V to 400 V, V _{GS} = 0 V	-	45	-	pF
Effective Output Capacitance, Time Related ^b	C _{o(tr)}		-	131	-	
Total Gate Charge	Q _g	V _{GS} = 10 V, I _D = 6 A, V _{DS} = 400 V	-	25	50	nC
Gate-Source Charge	Q _{gs}		-	6	-	
Gate-Drain Charge	Q _{gd}		-	10	-	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 400 V, I _D = 6 A, V _{GS} = 10 V, R _g = 9.1 Ω	-	13	26	ns
Rise Time	t _r		-	16	32	
Turn-Off Delay Time	t _{d(off)}		-	29	58	
Fall Time	t _f		-	12	24	
Gate Input Resistance	R _g	f = 1 MHz, open drain	-	0.92	-	Ω
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	10.5	A
Pulsed Diode Forward Current	I _{SM}		-	-	21	
Diode Forward Voltage	V _{SD}	T _J = 25 °C, I _S = 7.5 A, V _{GS} = 0 V	-	-	1.2	V
Reverse Recovery Time	t _{rr}	T _J = 25 °C, I _F = I _S = 6 A, di/dt = 100 A/μs, V _R = 25 V	-	244	-	ns
Reverse Recovery Charge	Q _{rr}		-	2.5	-	μC
Reverse Recovery Current	I _{RRM}		-	19	-	A

Notes

- a. C_{oss(er)} is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS}.
- b. C_{oss(tr)} is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS}.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

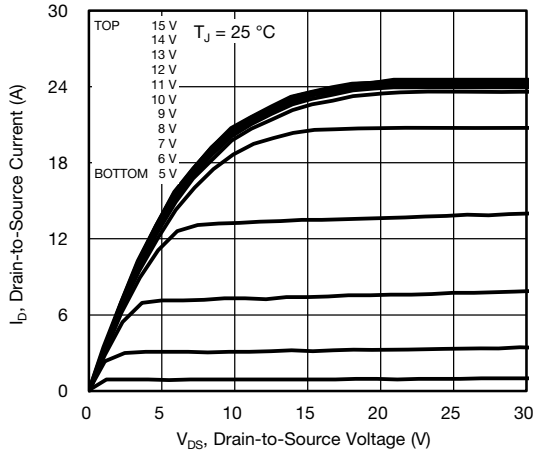


Fig. 1 - Typical Output Characteristics

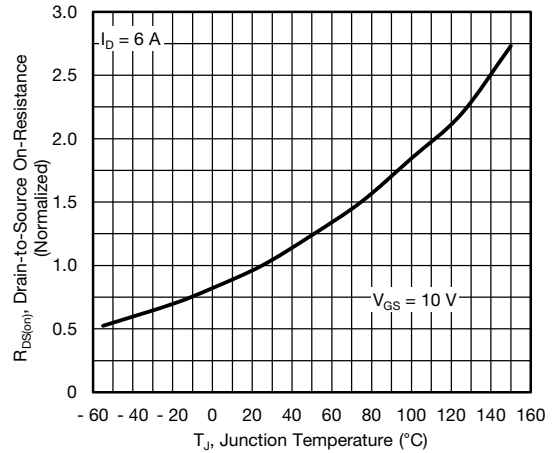


Fig. 4 - Normalized On-Resistance vs. Temperature

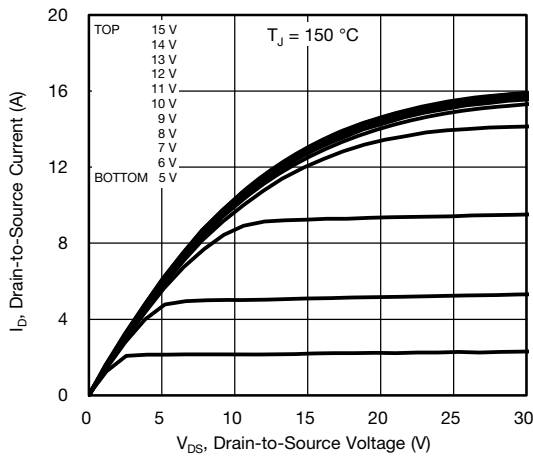


Fig. 2 - Typical Output Characteristics

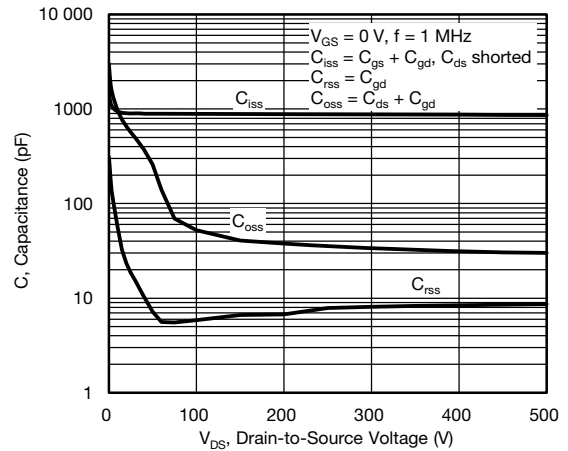


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

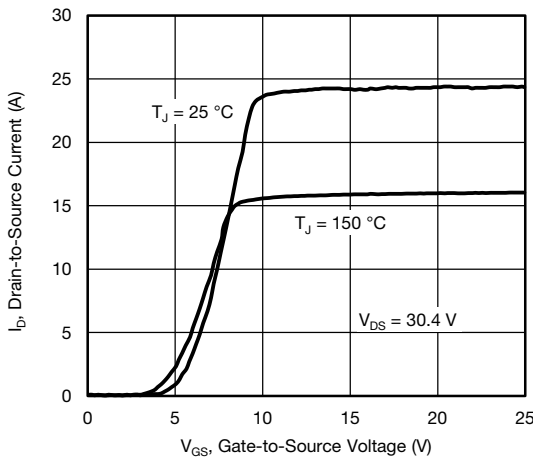


Fig. 3 - Typical Transfer Characteristics

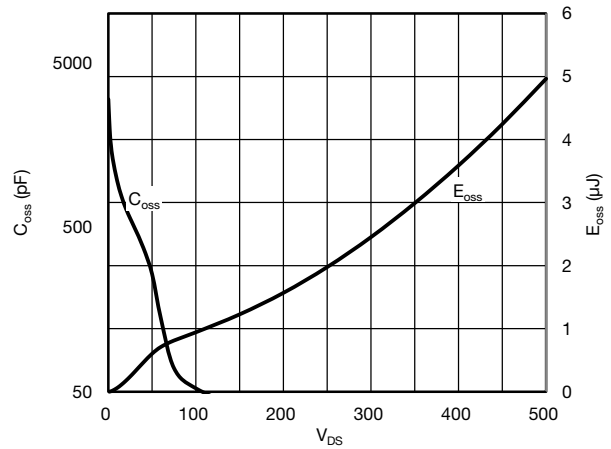


Fig. 6 - C_{oss} and E_{oss} vs. V_{DS}

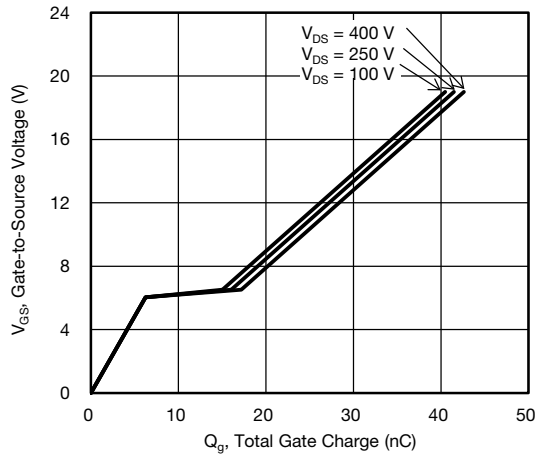


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

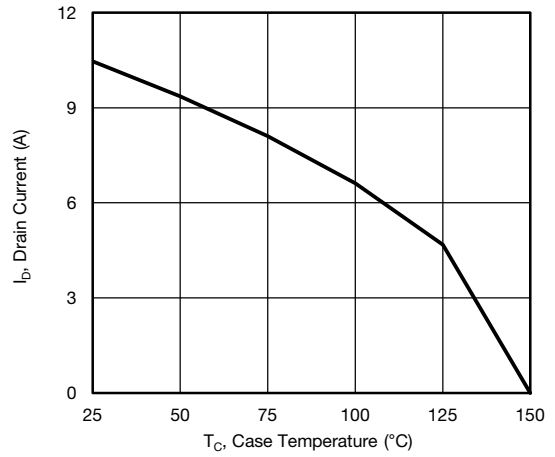


Fig. 10 - Maximum Drain Current vs. Case Temperature

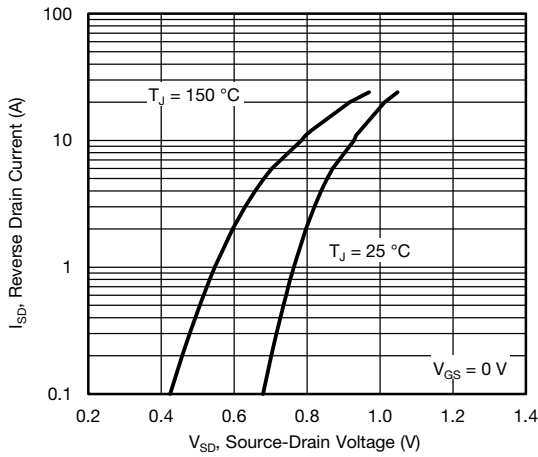


Fig. 8 - Typical Source-Drain Diode Forward Voltage

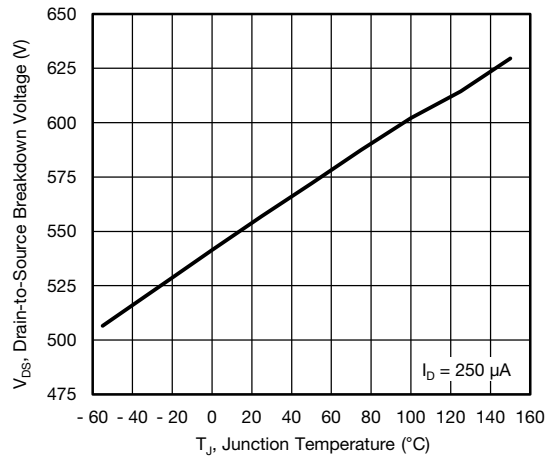


Fig. 11 - Temperature vs. Drain-to-Source Voltage

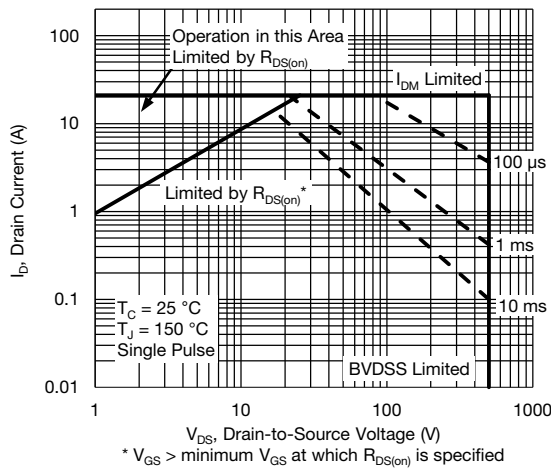


Fig. 9 - Maximum Safe Operating Area

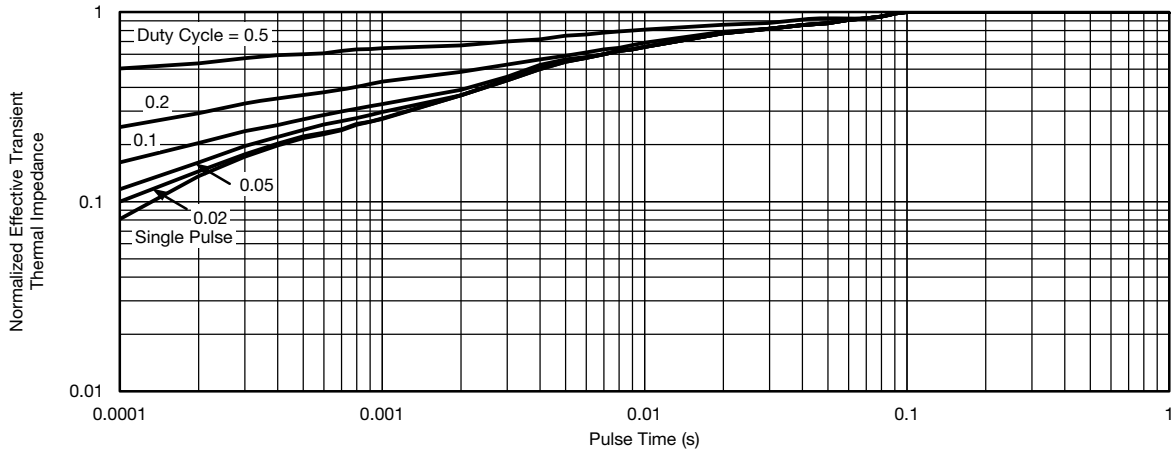


Fig. 12 - Normalized Thermal Transient Impedance, Junction-to-Case



Fig. 13 - Switching Time Test Circuit

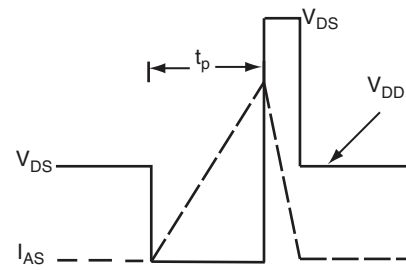


Fig. 16 - Unclamped Inductive Waveforms

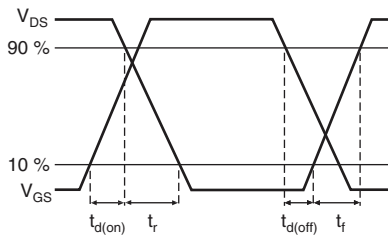


Fig. 14 - Switching Time Waveforms

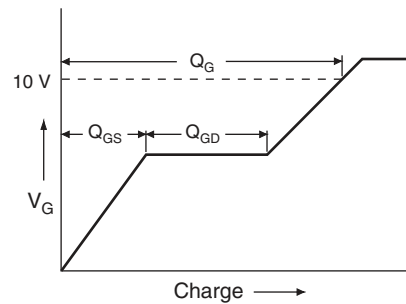


Fig. 17 - Basic Gate Charge Waveform

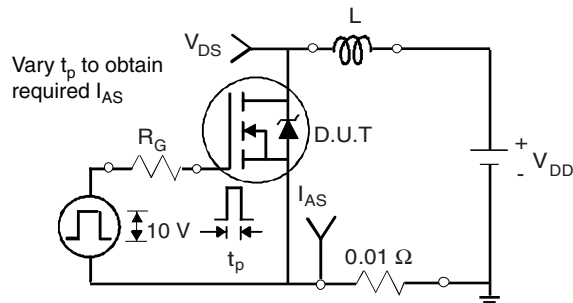


Fig. 15 - Unclamped Inductive Test Circuit

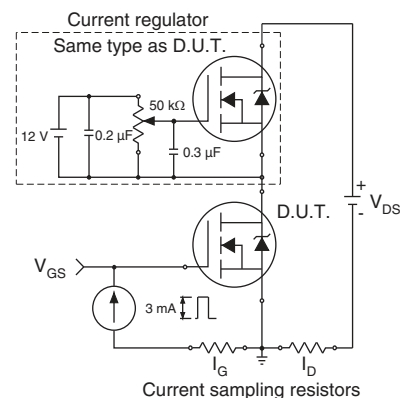


Fig. 18 - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



Note

a. $V_{GS} = 5 V$ for logic level devices

Fig. 19 - For N-Channel

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- Защита от снятия компонента с производства.



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