

**60A, 50V, 0.030 Ohm, ESD Rated,
P-Channel Power MOSFET**

This is a P-Channel power MOSFET manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI circuits, gives optimum utilization of silicon, resulting in outstanding performance. It was designed for use in applications such as switching regulators, switching converters, motor drivers, and relay drivers. This type can be operated directly from integrated circuits.

Formerly developmental type TA09835.

Ordering Information

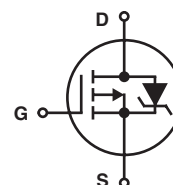
PART NUMBER	PACKAGE	BRAND
RFG60P05E	TO-247	RFG60P05E

NOTE: When ordering, use the entire part number.

Features

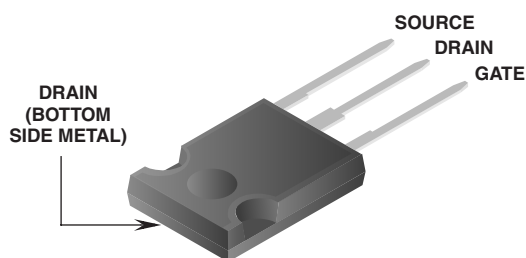
- 60A, 50V
- $r_{DS(ON)} = 0.030\Omega$
- Temperature Compensating PSPICE® Model
- 2kV ESD Rated
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- 175°C Operating Temperature
- Related Literature
 - TB334 "Guidelines for Soldering Surface Mount Components to PC Boards"

Symbol



Packaging

JEDEC STYLE TO-247



RFG60P05E

Absolute Maximum Ratings $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

	RFG60P05E	UNITS
Drain to Source Breakdown Voltage (Note 1)	V_{DS} -50	V
Drain to Gate Voltage ($R_{GS} = 20k\Omega$) (Note 1)	V_{DGR} -50	V
Gate to Source Voltage	V_{GS} ± 20	V
Continuous Drain Current	I_D 60	A
Pulsed Drain Current (Note 3) (Figure 5)	I_{DM} Refer to Peak Current Curve	
Power Dissipation	P_D 215	W
Derate above 25°C	1.43	W/ $^\circ\text{C}$
Single Pulse Avalanche Rating (Figure 6)	E_{AS} Refer to UIS Curve	W/ $^\circ\text{C}$
Electrostatic Discharge Rating.	E_{SD} 2	kV
MIL-STD-883, Category B(2)		
Operating and Storage Temperature	T_J, T_{STG} -55 to 175	$^\circ\text{C}$
Maximum Temperature for Soldering		
Leads at 0.063in (1.6mm) from Case for 10s.	T_L 300	$^\circ\text{C}$
Package Body for 10s, See Techbrief 334	T_{pkg} 260	$^\circ\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^\circ\text{C}$ to 150°C .

Electrical Specifications $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV _{DSS}	I _D = 250μA, V _{GS} = 0V		-50	-	-	V
Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 250μA		-2	-	-4	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -50V, V _{GS} = 0V		-	-	-1	μA
		V _{DS} = 0.8 x Rated BV _{DSS} , T _C = 150°C		-	-	-25	μA
Gate to Source Leakage Current	I _{GSS}	V _{GS} = ±20V		-	-	±100	nA
Drain to Source On Resistance (Note 2)	r _{DS(ON)}	I _D = 60A, V _{GS} = -10V (Figure 9)		-	-	0.030	Ω
Turn-On Time	t _(ON)	V _{DD} = -25V, I _D = 30A, R _L = 0.83Ω, V _{GS} = -10V, R _{GS} = 2.5Ω (Figure 13)		-	-	125	ns
Turn-On Delay Time	t _{d(ON)}			-	20	-	ns
Rise Time	t _r			-	60	-	ns
Turn-Off Delay Time	t _{d(OFF)}			-	65	-	ns
Fall Time	t _F			-	20	-	ns
Turn-Off Time	t _(OFF)			-	-	125	ns
Total Gate Charge	Q _{g(TOT)}	V _{GS} = 0V to -20V	V _{DD} = -40V, I _D = 60A, R _L = 0.67Ω I _{g(REF)} = -4mA	-	-	450	nC
Gate Charge at 10V	Q _{g(-10)}	V _{GS} = 0V to -10V		-	-	225	nC
Threshold Gate Charge	Q _{g(TH)}	V _{GS} = 0V to -2V		-	-	15	nC
Input Capacitance	C _{ISS}	V _{DS} = -25V, V _{GS} = 0V, f = 1MHz (Figure 12)		-	7200	-	pF
Output Capacitance	C _{OSS}			-	1700	-	pF
Reverse Transfer Capacitance	C _{RSS}			-	325	-	pF
Thermal Resistance, Junction to Case	R _{θJC}			-	-	0.70	°C/W
Thermal Resistance, Junction to Ambient	R _{θJA}			-	-	30	°C/W

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage (Note 2)	V_{SD}	$I_{SD} = -60\text{A}$	-	-	-1.75	V
Diode Reverse Recovery Time	t_{RR}	$I_{SD} = -60\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	200	ns

NOTE:

2. Pulse test: pulse width $\leq 300\mu\text{s}$ maximum, duty cycle $\leq 2\%$.
3. Repetitive rating: pulse width limited by maximum junction temperature. See Transient Thermal Impedance curve (Figure 3).

Typical Performance Curves Unless Otherwise Specified

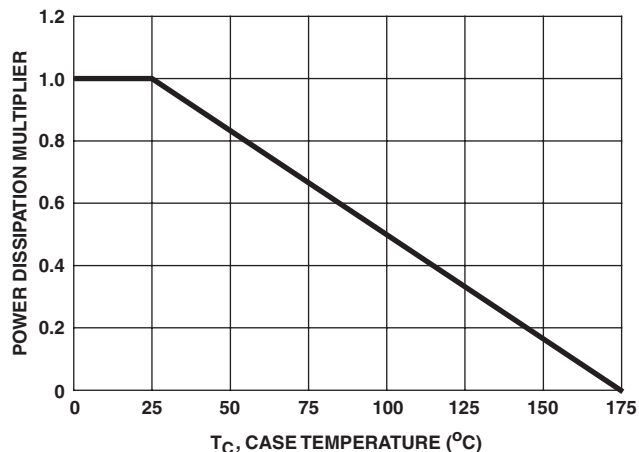


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

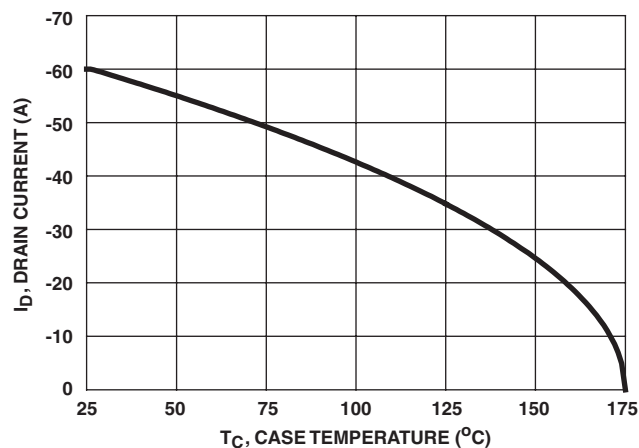


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

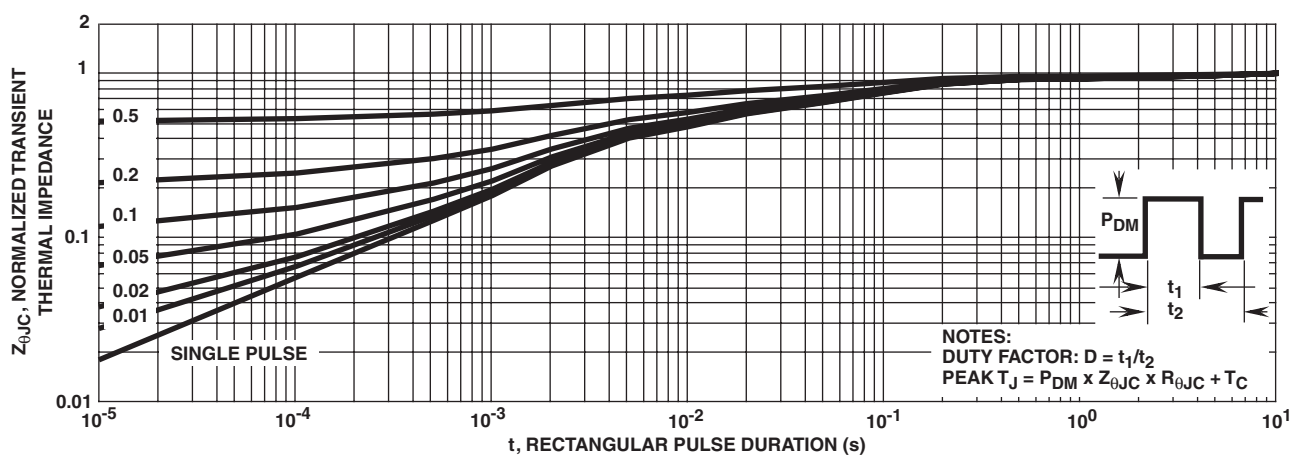


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

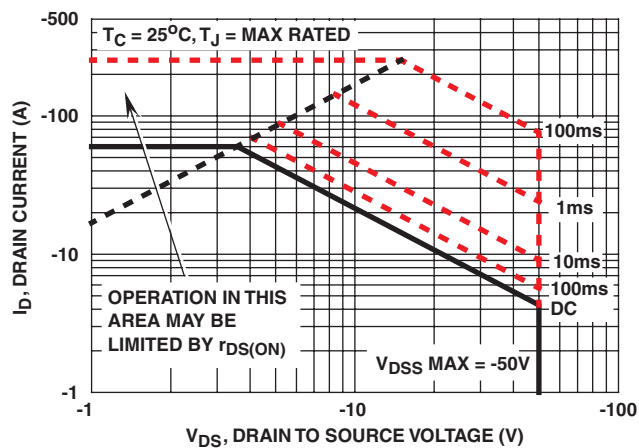


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

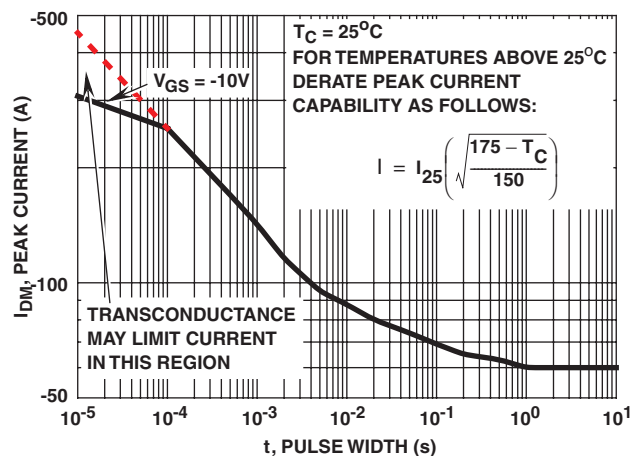
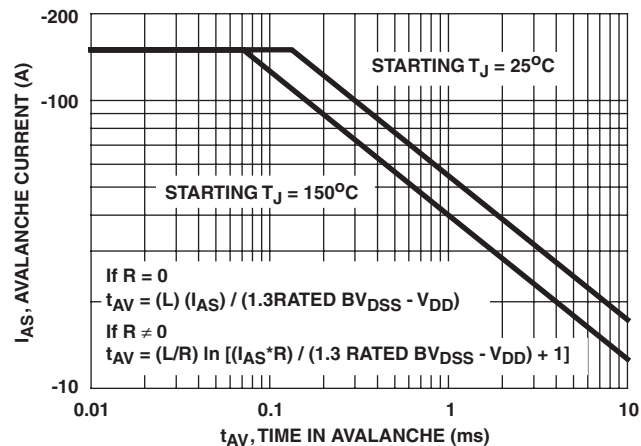


FIGURE 5. PEAK CURRENT CAPABILITY

Typical Performance Curves Unless Otherwise Specified (Continued)



NOTE: Refer to Fairchild Application Notes AN9321 and AN9322.

FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

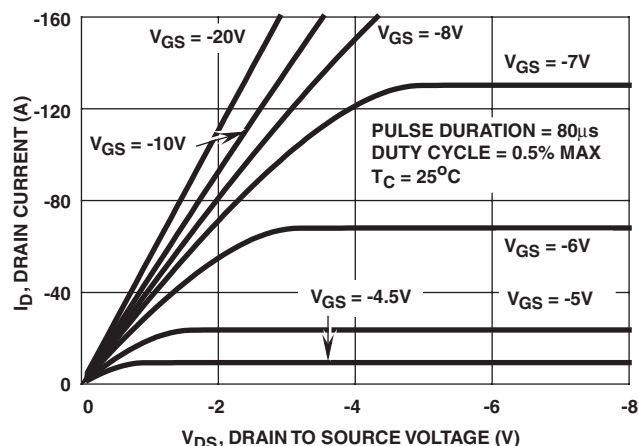


FIGURE 7. SATURATION CHARACTERISTICS

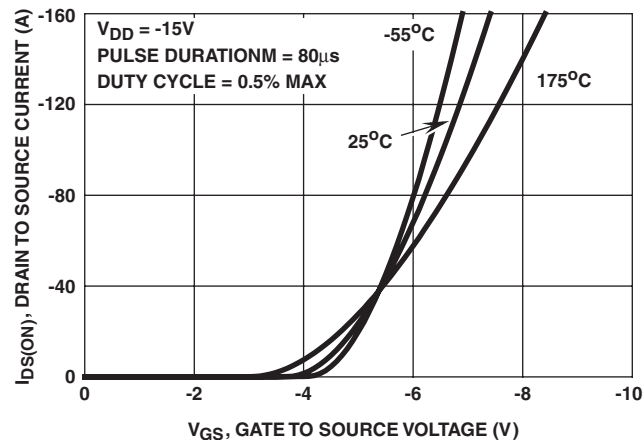


FIGURE 8. TRANSFER CHARACTERISTICS

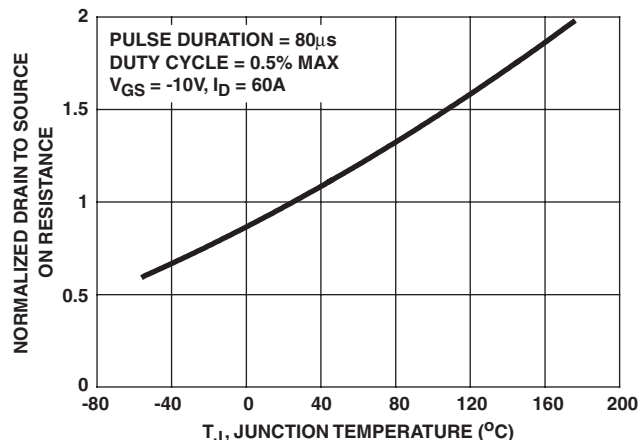


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

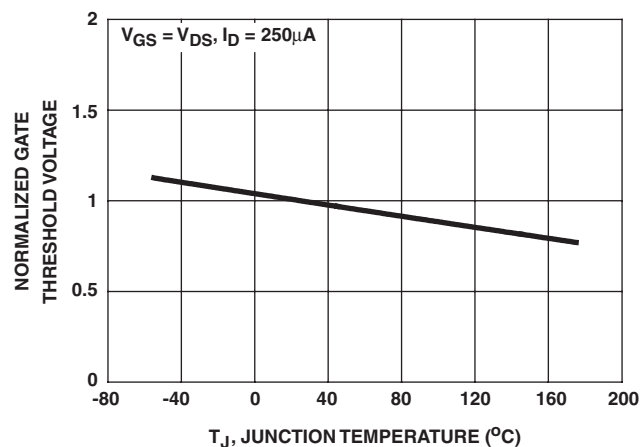


FIGURE 10. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

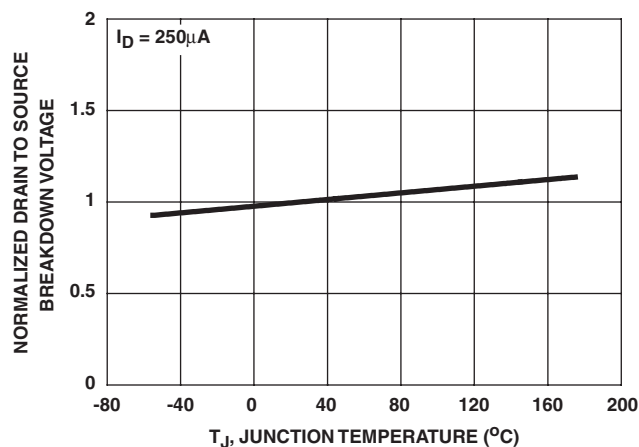


FIGURE 11. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

Typical Performance Curves Unless Otherwise Specified (Continued)

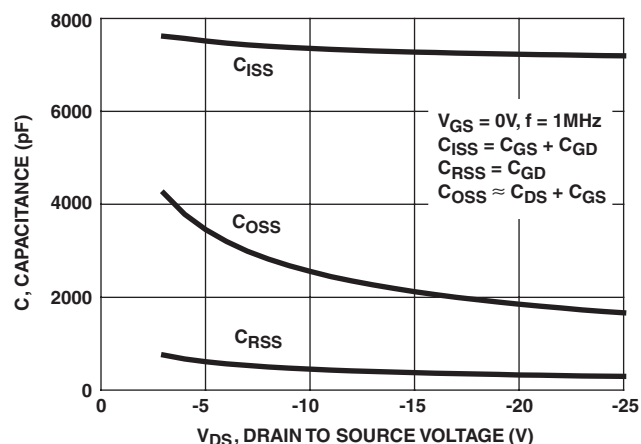
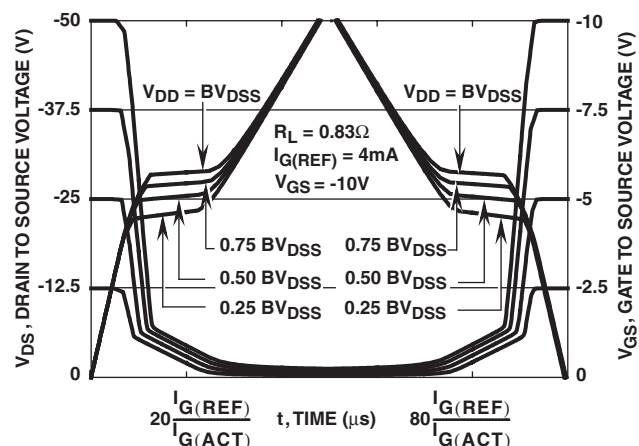


FIGURE 12. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Fairchild Application Notes AN7254 and AN7260.

FIGURE 13. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

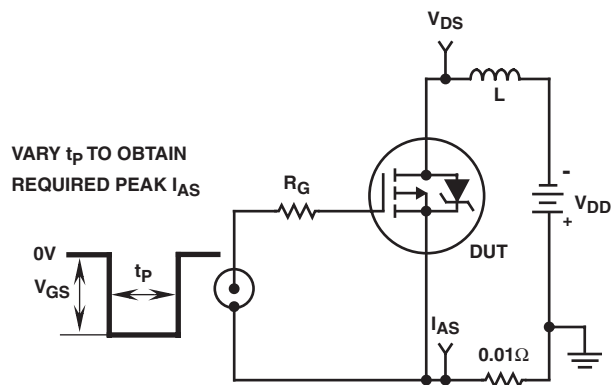


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

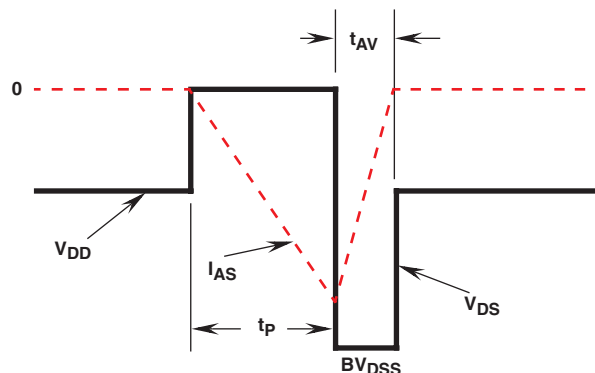


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

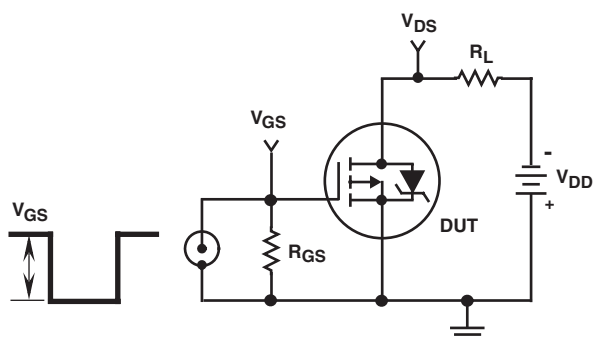


FIGURE 16. SWITCHING TIME TEST CIRCUIT

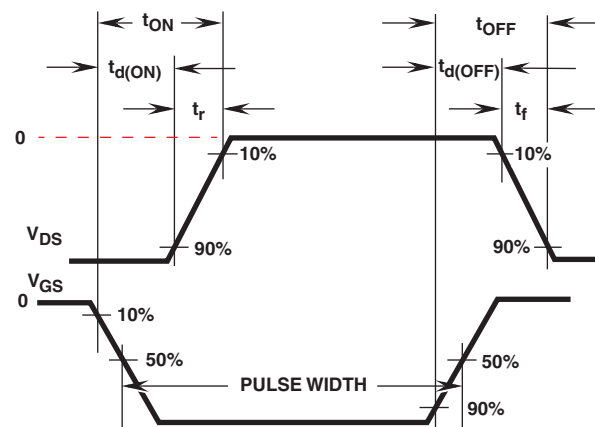


FIGURE 17. RESISTIVE SWITCHING WAVEFORMS

Test Circuits and Waveforms (Continued)

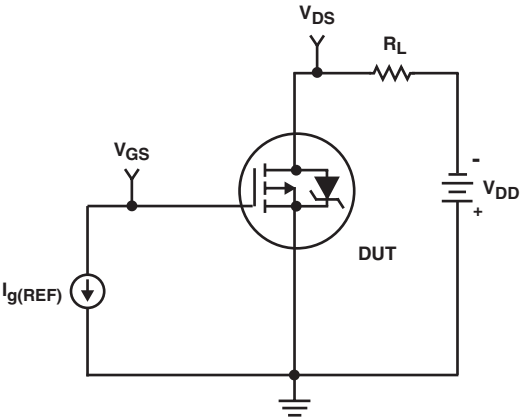


FIGURE 18. GATE CHARGE TEST CIRCUIT

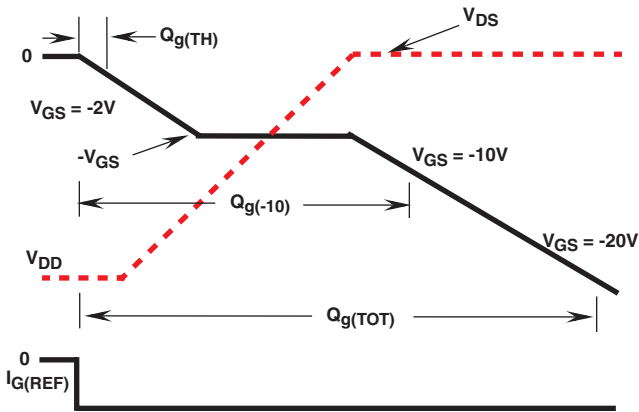


FIGURE 19. GATE CHARGE WAVEFORMS

PSPICE Electrical Model

```
.SUBCKT RFG60P05E 2 1 3;
```

REV 9/20/94

CA 12 8 1.01e-8
CB 15 14 1.05e-8
CIN 6 8 6.9e-9

```
DBODY 5 7 DBDMOD
DBREAK 7 11 DBKMOD
DPLCAP 10 6 DPLCAPMOD
```

EBREAK 5 11 17 18 -76.35
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 5 10 8 6 1
EVTO 20 6 8 18 1

IT 8 17 1

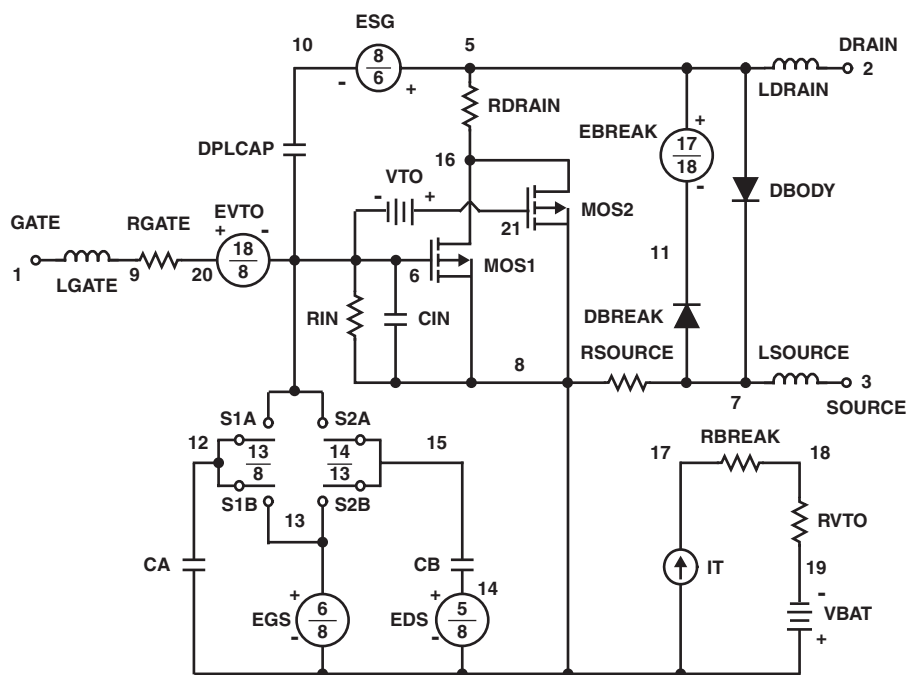
```
LDRAIN 2 5 1e-9
LGATE 1 9 7.9e-9
LSOURCE 3 7 4.18e-9
```

MOS1 16 6 8 8 MOSMOD M = 0.99
MOS2 16 21 8 8 MOSMOD M = 0.01

```
RBREAK 17 18 RBKMOD 1
RDRAIN 5 16 RDSMOD 12.83e-3
RGATE 9 20 1.5
RIN 6 8 1e9
RSOURCE 8 7 RDSMOD 3.25e-3
RVTO 18 19 RVTOMOD 1
```

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

```
VBAT 8 19 DC 1
VTO 21 6 -0.83
```



```
.MODEL DBDMOD D (IS = 1.24e-12 RS = 4.72e-3 TRS1 = 1.43e-3 TRS2 = -4.91e-7 CJO = 6.98e-9 TT = 1.5e-7)
.MODEL DBKMOD D (RS = 1.11e-1 TRS1 = 1.34e-3 TRS2 = 4.46e-12)
.MODEL DPLCAPMOD D (CJO = 15e-10 IS = 1e-30 N = 10)
.MODEL MOSMOD PMOS (VTO = -3.71 KP = 31.5 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
.MODEL RBKMOD RES (TC1 = 9.42e-4 TC2 = 0)
.MODEL RDSMOD RES (TC1 = 5.85e-3 TC2 = 7.69e-6)
.MODEL RVTOMOD RES (TC1 = -3.39e-3 TC2 = 1.07e-6)
.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 4.6 VOFF = 2.6)
.MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 2.6 VOFF = 4.6)
.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 1.16 VOFF = -3.84)
.MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -3.84 VOFF = 1.16)
```

.ENDS

For further discussion of the PSPICE model, consult **A New PSPICE Sub-circuit for the Power MOSFET Featuring Global Temperature Options**; written by William J. Hepp and C. Frank Wheatley.

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