Low-power 2-input NAND gate (open drain)

Rev. 7 — 4 April 2016

Product data sheet

1. General description

The 74AUP1G38 provides the single 2-input NAND gate with open-drain output. The output of the device is an open drain and can be connected to other open-drain outputs to implement active-LOW wired-OR or active-HIGH wired-AND functions.

Schmitt trigger action at all inputs makes the circuit tolerant to slower input rise and fall times across the entire V_{CC} range from 0.8 V to 3.6 V.

This device ensures a very low static and dynamic power consumption across the entire V_{CC} range from 0.8 V to 3.6 V.

This device is fully specified for partial power-down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

2. Features and benefits

- Wide supply voltage range from 0.8 V to 3.6 V
- High noise immunity
- Complies with JEDEC standards:
 - JESD8-12 (0.8 V to 1.3 V)
 - JESD8-11 (0.9 V to 1.65 V)
 - JESD8-7 (1.2 V to 1.95 V)
 - JESD8-5 (1.8 V to 2.7 V)
 - JESD8-B (2.7 V to 3.6 V)
- ESD protection:
 - ◆ HBM JESD22-A114F Class 3A exceeds 5000 V
 - MM JESD22-A115-A exceeds 200 V
 - CDM JESD22-C101E exceeds 1000 V
- Low static power consumption; $I_{CC} = 0.9 \ \mu A$ (maximum)
- Latch-up performance exceeds 100 mA per JESD 78 Class II
- Inputs accept voltages up to 3.6 V
- Low noise overshoot and undershoot < 10 % of V_{CC}
- I_{OFF} circuitry provides partial power-down mode operation
- Multiple package options
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

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3. Ordering information

Type number	Package							
	Temperature range	Name	Description	Version				
74AUP1G38GW	–40 °C to +125 °C	TSSOP5	plastic thin shrink small outline package; 5 leads; body width 1.25 mm	SOT353-1				
74AUP1G38GM	–40 °C to +125 °C	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body 1 \times 1.45 \times 0.5 mm	SOT886				
74AUP1G38GF	–40 °C to +125 °C	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body 1 \times 1 \times 0.5 mm	SOT891				
74AUP1G38GN	–40 °C to +125 °C	XSON6	extremely thin small outline package; no leads; 6 terminals; body $0.9 \times 1.0 \times 0.35$ mm	SOT1115				
74AUP1G38GS	–40 °C to +125 °C	XSON6	extremely thin small outline package; no leads; 6 terminals; body $1.0 \times 1.0 \times 0.35$ mm	SOT1202				
74AUP1G38GX	–40 °C to +125 °C	X2SON5	X2SON5: plastic thermal enhanced extremely thin small outline package; no leads; 5 terminals; body $0.8 \times 0.8 \times 0.35$ mm	SOT1226				

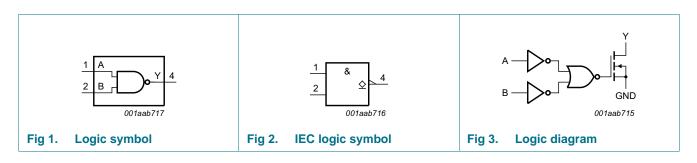
4. Marking

Table 2. Marking

Type number	Marking code ^[1]
74AUP1G38GW	aB
74AUP1G38GM	aB
74AUP1G38GF	aB
74AUP1G38GN	aB
74AUP1G38GS	aB
74AUP1G38GX	aB

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram

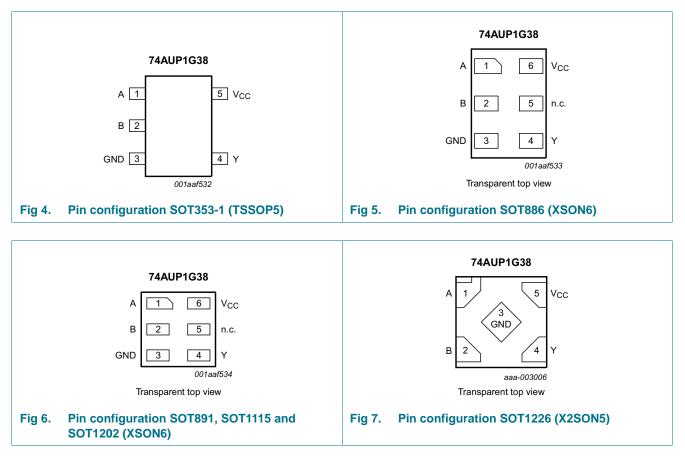


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6. Pinning information

6.1 Pinning



6.2 Pin description

Table 3.Pin description			
Symbol	Pin		Description
	TSSOP5 and X2SON5	XSON6	
A	1	1	data input
В	2	2	data input
GND	3	3	ground (0 V)
Y	4	4	data output
n.c.	-	5	not connected
V _{CC}	5	6	supply voltage

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Functional description 7.

Function table^[1] Table 4.

Input C		Output
Α	В	Y
L	L	Z
L	Н	Z
Н	L	Z
Н	Н	L

[1] H = HIGH voltage level;

L = LOW voltage level;

Z = high-impedance OFF state.

Limiting values 8.

Table 5. **Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{CC}	supply voltage			-0.5	+4.6	V
I _{IK}	input clamping current	V ₁ < 0 V		-50	-	mA
VI	input voltage		<u>[1]</u>	-0.5	+4.6	V
I _{OK}	output clamping current	V _O < 0 V		-50	-	mA
Vo	output voltage	Active mode and Power-down mode	<u>[1]</u>	-0.5	+4.6	V
lo	output current	$V_{O} = 0 V$ to V_{CC}		-	+20	mA
I _{CC}	supply current			-	+50	mA
I _{GND}	ground current			-50	-	mA
T _{stg}	storage temperature			-65	+150	°C
P _{tot}	total power dissipation	$T_{amb} = -40 \text{ °C to } +125 \text{ °C}$	[2]	-	250	mW

[1] The minimum input and output voltage ratings may be exceeded if the input and output current ratings are observed.

For TSSOP5 packages: above 87.5 °C the value of Ptot derates linearly with 4.0 mW/K. [2]

For XSON6 and X2SON5 packages: above 118 °C the value of Ptot derates linearly with 7.8 mW/K.

Recommended operating conditions 9.

	coolinine naca operating condition	2115			
Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		0.8	3.6	V
VI	input voltage		0	3.6	V
Vo	output voltage	Active mode and Power-down mode	0	3.6	V
T _{amb}	ambient temperature		-40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V _{CC} = 0.8 V to 3.6 V	0	200	ns/V

Table 6. **Recommended operating conditions**

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10. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
T _{amb} = 2	5 °C		1			
VIH	HIGH-level input voltage	V _{CC} = 0.8 V	$0.70\times V_{CC}$	-	-	V
		$V_{CC} = 0.9 \text{ V to } 1.95 \text{ V}$	$0.65 \times V_{CC}$	-	-	V
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.6	-	-	V
		V _{CC} = 3.0 V to 3.6 V	2.0	-	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 0.8 V	-	-	$0.30 \times V_{CC}$	V
		$V_{CC} = 0.9 \text{ V} \text{ to } 1.95 \text{ V}$	-	-	$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	-	-	0.7	V
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	-	-	0.9	V
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	-					
		$I_O = 20 \ \mu\text{A}; \ V_{CC} = 0.8 \ V \ to \ 3.6 \ V$	-	-	0.1	V
		I _O = 1.1 mA; V _{CC} = 1.1 V	-	-	$0.3 \times V_{CC}$	V
		I _O = 1.7 mA; V _{CC} = 1.4 V	-	-	0.31	V
		I _O = 1.9 mA; V _{CC} = 1.65 V	-	-	0.31	V
		I_{O} = 2.3 mA; V_{CC} = 2.3 V	-	-	0.31	V
		$I_{O} = 3.1 \text{ mA}; V_{CC} = 2.3 \text{ V}$	-	-	0.44	V
		I_{O} = 2.7 mA; V_{CC} = 3.0 V	-	-	0.31	V
		I_{O} = 4.0 mA; V_{CC} = 3.0 V	-	-	0.44	V
I _I	input leakage current	$V_I = GND$ to 3.6 V; $V_{CC} = 0$ V to 3.6 V	-	-	±0.1	μA
I _{OZ}	OFF-state output current	LOW); $V_0 = 0 V$ to 3.6 V; $V_{CC} = 0 V$ to	-	-	±0.1	μA
I _{OFF}	power-off leakage current	V_{I} or V_{O} = 0 V to 3.6 V; V_{CC} = 0 V	-	-	±0.2	μA
ΔI_{OFF}	•		-	-	±0.2	μA
I _{CC}	supply current		-	-	0.5	μA
ΔI_{CC}	additional supply current	$V_{I} = V_{CC} - 0.6 \text{ V}; I_{O} = 0 \text{ A}; V_{CC} = 3.3 \text{ V}$	-	-	40	μA
CI	input capacitance	$V_{CC} = 0$ V to 3.6 V; $V_I = GND$ or V_{CC}	-	0.8	-	pF
Co	output capacitance	output enabled; $V_0 = GND$; $V_{CC} = 0 V$	-	1.7	-	pF
		output disabled; $V_0 = GND$; $V_{CC} = 0 V$	-	1.1	-	pF
T _{amb} = -	40 °C to +85 °C		1		1	
V _{IH}	HIGH-level input voltage	V _{CC} = 0.8 V	$0.70\times V_{CC}$	-	-	V
		V _{CC} = 0.9 V to 1.95 V	$0.65 \times V_{CC}$	-	-	V
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.6	-	-	V
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	2.0	-	-	V

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Table 7. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{IL}	LOW-level input voltage	V _{CC} = 0.8 V	-	-	$0.30 \times V_{CC}$	V
		$V_{CC} = 0.9 \text{ V}$ to 1.95 V	-	-	$0.35 \times V_{CC}$	V
		V_{CC} = 2.3 V to 2.7 V	-	-	0.7	V
		$V_{CC} = 3.0 \text{ V} \text{ to } 3.6 \text{ V}$	-	-	$0.30 \times V_{CC}$ $0.35 \times V_{CC}$ 0.7 0.9 0.1 $0.3 \times V_{CC}$ $0.33 \times V_{CC}$ $0.35 \times V_{CC}$ $0.35 \times V_{CC}$ $0.35 \times V_{CC}$ 0.37 $0.35 \times V_{CC}$ 0.45 0.45 0.45 0.45 ± 0.5 0.9 50 $ 0.25$	V
V _{OL}	LOW-level output voltage	$V_{I} = V_{IH} \text{ or } V_{IL}$				
		$I_{O} = 20 \ \mu\text{A}; \ V_{CC} = 0.8 \ V \ to \ 3.6 \ V$	-	-	0.1	V
		I _O = 1.1 mA; V _{CC} = 1.1 V	-	-	$0.3\times V_{CC}$	V
		I _O = 1.7 mA; V _{CC} = 1.4 V	-	-	0.37	V
		I _O = 1.9 mA; V _{CC} = 1.65 V	-	-	0.35	V
		I_{O} = 2.3 mA; V_{CC} = 2.3 V	-	-	0.33	V
		I _O = 3.1 mA; V _{CC} = 2.3 V	-	-	0.45	V
		I _O = 2.7 mA; V _{CC} = 3.0 V	-	-	0.33	V
		I _O = 4.0 mA; V _{CC} = 3.0 V	-	-	0.45	V
I _I	input leakage current	$V_{I} = GND$ to 3.6 V; $V_{CC} = 0$ V to 3.6 V	-	-	±0.5	μA
I _{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL} (and at least one input LOW); $V_O = 0$ V to 3.6 V; $V_{CC} = 0$ V to 3.6 V	-	-	±0.5	μA
I _{OFF}	power-off leakage current	V_{I} or V_{O} = 0 V to 3.6 V; V_{CC} = 0 V	-	-	±0.5	μA
ΔI_{OFF}	additional power-off leakage current		-	-	±0.6	μA
I _{CC}	supply current	$\label{eq:VI} \begin{array}{l} V_{I} = GND \text{ or } V_{CC}; I_{O} = 0 \; A; \\ V_{CC} = 0.8 \; V \; to \; 3.6 \; V \end{array}$	-	-	0.9	μA
ΔI_{CC}	additional supply current	$V_{I} = V_{CC} - 0.6 \text{ V}; I_{O} = 0 \text{ A}; V_{CC} = 3.3 \text{ V}$	-	-	50	μA
T _{amb} = -4	40 °C to +125 °C		I.			
VIH	HIGH-level input voltage	V _{CC} = 0.8 V	$0.75 \times V_{CC}$	-	-	V
		V _{CC} = 0.9 V to 1.95 V	$0.70 \times V_{CC}$	-	-	V
		V _{CC} = 2.3 V to 2.7 V	1.6	-	-	V
$V_{OL} \qquad L$ $I_{I} \qquad iI$ $I_{OZ} \qquad C$ $I_{OFF} \qquad F$ $\Delta I_{OFF} \qquad F$ $\Delta I_{OFF} \qquad F$ $I_{CC} \qquad s$ $\Delta I_{CC} \qquad s$ $\Delta I_{CC} \qquad t$ $T_{amb} = -40$ $V_{IH} \qquad H$		V _{CC} = 3.0 V to 3.6 V	2.0	-	-	V
V _{IL}	$ \begin{array}{ c c c c c c } \mbox{LOW-level input voltage} & V_{CC} = 0.8 \ V & V_{CC} = 2.3 \ V to 1.95 \ V & - & - & 0.35 \ \times V_{CC} \ V \\ \hline V_{CC} = 2.3 \ V to 1.95 \ V & - & - & 0.7 \ V \\ \hline V_{CC} = 2.3 \ V to 2.7 \ V & - & - & 0.7 \ V \\ \hline V_{CC} = 3.0 \ V to 3.6 \ V & - & - & 0.9 \ V \\ \hline V_{CC} = 3.0 \ V to 3.6 \ V & - & - & 0.1 \ V \\ \hline V_{CC} = 3.0 \ V to 3.6 \ V & - & - & 0.1 \ V \\ \hline V_{10} = 1.1 \ mA; \ V_{CC} = 1.4 \ V & - & - & 0.3 \ \times V_{CC} \ V \\ \hline I_{0} = 1.1 \ mA; \ V_{CC} = 1.65 \ V & - & - & 0.33 \ V \\ \hline I_{0} = 1.7 \ mA; \ V_{CC} = 2.3 \ V & - & - & 0.33 \ V \\ \hline I_{0} = 1.9 \ mA; \ V_{CC} = 2.3 \ V & - & - & 0.33 \ V \\ \hline I_{0} = 2.7 \ mA; \ V_{CC} = 2.3 \ V & - & - & 0.45 \ V \\ \hline I_{0} = 2.7 \ mA; \ V_{CC} = 0.1 \ V 0 \ - & - & 0.45 \ V \\ \hline I_{0} = 2.7 \ mA; \ V_{CC} = 0.1 \ V 0 \ - & - & 0.45 \ V \\ \hline I_{0} = 2.7 \ mA; \ V_{CC} = 0.1 \ V 0 \ - & - & 0.45 \ V \\ \hline I_{0} = 2.7 \ mA; \ V_{CC} = 0.1 \ V 0 \ - & - & 0.45 \ V \\ \hline I_{0} = 2.7 \ mA; \ V_{CC} = 0 \ V 0 \ 3.6 \ V \ - & - & 0.45 \ V \\ \hline I_{0} = 4.0 \ mA; \ V_{CC} = 0 \ V 0 \ 3.6 \ V \ - & - & 0.45 \ V \\ \hline I_{0} = - 0 \ V 0 \ 3.6 \ V; \ V_{CC} = 0 \ V 0 \ 3.6 \ V \ - & - & 0.45 \ V \\ \hline I_{0} = - 0 \ V 0 \ 3.6 \ V; \ V_{CC} = 0 \ V 0 \ 3.6 \ V \ - & - & - & 0.45 \ V \\ \hline I_{0} = 0 \ V 0 \ 3.6 \ V \ - & - & - & 0.45 \ V \\ \hline I_{0} = - \ V_{0} \ V_{0} = 0 \ V 0 \ 3.6 \ V; \ V_{CC} = 0 \ V \ - & - & - & 0.45 \ V \\ \hline I_{0} = - \ V_{0} \ V_{0} = 0 \ V 0 \ 3.6 \ V \ - & - & - & 0.45 \ V \\ \hline I_{0} = 0 \ V 0 \ 3.6 \ V \ - & - & - & 0.5 \ V \\ \hline I_{0} = 0 \ V 0 \ 3.6 \ V \ - & - & - & 0.7 \ V \\ \hline V_{CC} = 0.8 \ V \ 0.75 \ V_{CC} \ - & - \ V \\ \hline V_{CC} = 0.8 \ V \ 0.75 \ V_{CC} \ - & - \ V \ V_{CC} \ - \ - & V \ V_{CC} \ - \ 0.9 \ V \\ \hline V_{CC} = 0.9 \ V 0 \ 3.6 \ V \ - \ - & 0.75 \ V_{CC} \ - \ - \ V \ V_{CC} \ - \$	V				
		V _{CC} = 0.9 V to 1.95 V	-	-	$0.30\times V_{CC}$	V
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	-	-	0.7	V
		$V_{CC} = 3.0 \text{ V} \text{ to } 3.6 \text{ V}$	-	-	0.9	V
V _{OL}	$ \begin{array}{ c c c c c c } \mbox{LOW-level input voltage} & V_{CC} = 0.8 \ V & - & - & 0.30 \ \times V_{CC} \\ \hline V_{CC} = 0.9 \ V to 1.95 \ V & - & - & 0.7 \\ \hline V_{CC} = 2.3 \ V to 2.7 \ V & - & - & 0.7 \\ \hline V_{CC} = 2.3 \ V to 3.6 \ V & - & - & 0.7 \\ \hline V_{CC} = 2.3 \ V to 3.6 \ V & - & - & 0.7 \\ \hline V_{CC} = 2.3 \ V to 3.6 \ V & - & - & 0.7 \\ \hline V_{CC} = 2.0 \ V to 3.6 \ V & - & - & 0.7 \\ \hline V_{CC} = 0.9 \ V to 3.6 \ V & - & - & 0.7 \\ \hline I_0 = 1.1 \ mA; \ V_{CC} = 1.1 \ V & - & - & 0.3 \ V_{CC} \\ \hline I_0 = 1.7 \ mA; \ V_{CC} = 1.6 \ V & - & - & 0.33 \\ \hline I_0 = 2.3 \ mA; \ V_{CC} = 3.0 \ V & - & - & 0.33 \\ \hline I_0 = 2.3 \ mA; \ V_{CC} = 3.0 \ V & - & - & 0.33 \\ \hline I_0 = 2.7 \ mA; \ V_{CC} = 3.0 \ V & - & - & 0.45 \\ \hline I_0 = 2.7 \ mA; \ V_{CC} = 3.0 \ V & - & - & 0.45 \\ \hline I_0 = 2.7 \ mA; \ V_{CC} = 3.0 \ V & - & - & 0.45 \\ \hline I_0 = 2.7 \ mA; \ V_{CC} = 3.0 \ V & - & - & 0.45 \\ \hline I_0 = -1 \ mA; \ V_{CC} = 0 \ V to 3.6 \ V & - & - & 0.33 \\ \hline I_0 = -4 \ mA; \ V_{CC} = 0 \ V to 3.6 \ V & - & - & 0.45 \\ \hline \ power-off \ leakage \ current \ V_1 = GND \ to 3.6 \ V; \ V_{CC} = 0 \ V to 3.6 \ V & - & - & 0.5 \\ \hline power-off \ leakage \ current \ V_1 \ O \ V_0 = 0 \ V to 3.6 \ V; \ V_{CC} = 0 \ V to 3.6 \ V & - & - & 0.5 \\ \hline \ power-off \ leakage \ current \ V_1 \ O \ V_0 = 0 \ V to 3.6 \ V; \ V_{CC} = 0 \ V to 3.6 \ V & - & - & 0.5 \\ \hline \ power-off \ leakage \ current \ V_1 \ O \ V_0 \ O \ V \ O \ 2 \ V \ O \ 2 \ V \ O \ 2 \ V \ C \ 2 \ V \ O \ 2 \ V \ C \ 2 \ V \$					
		$I_0 = 20 \ \mu\text{A}; \ V_{CC} = 0.8 \ \text{V} \text{ to } 3.6 \ \text{V}$	-	-	0.11	V
		I _O = 1.1 mA; V _{CC} = 1.1 V	-	-	$0.33 \times V_{CC}$	V
		I _O = 1.7 mA; V _{CC} = 1.4 V	-	-	0.41	V
			-	-	0.39	V
				-	0.36	V
			-	-	0.50	V
			-	-		V
					1	1

Low-power 2-input NAND gate (open drain)

At recom	mended operating conditions,	; voltages are referenced to GND (ground = 0	V).			
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
l _l	input leakage current	$V_I = GND$ to 3.6 V; $V_{CC} = 0$ V to 3.6 V	-	-	±0.75	μA
I _{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL} (and at least one input LOW); $V_O = 0$ V to 3.6 V; $V_{CC} = 0$ V to 3.6 V	-	-	±0.75	μA
I _{OFF}	power-off leakage current	V_1 or $V_0 = 0$ V to 3.6 V; $V_{CC} = 0$ V	-	-	±0.75	μA
ΔI_{OFF}	additional power-off leakage current	$V_{I} \text{ or } V_{O} = 0 \text{ V to } 3.6 \text{ V};$ $V_{CC} = 0 \text{ V to } 0.2 \text{ V}$	-	-	±0.75	μA
I _{CC}	supply current	$V_{I} = GND \text{ or } V_{CC}; I_{O} = 0 \text{ A};$ $V_{CC} = 0.8 \text{ V to } 3.6 \text{ V}$	-	-	1.4	μA
ΔI_{CC}	additional supply current	$V_{I} = V_{CC} - 0.6 \text{ V}; \text{ I}_{O} = 0 \text{ A}; V_{CC} = 3.3 \text{ V}$	-	-	75	μA

Table 7. Static characteristics ... continued

11. Dynamic characteristics

Table 8. **Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V; for test circuit see Figure 9

Symbol	Parameter	Conditions	25 °C			-40) °C to +1	25 °C	Unit
			Min	Typ <mark>[1]</mark>	Мах	Min	Max (85 °C)	Max (125 °C)	
C _L = 5 p	F				·				
t _{pd}	propagation delay	A or B to Y; see Figure 8							
		V _{CC} = 0.8 V	-	13.5	-	-	-	-	ns
		V _{CC} = 1.1 V to 1.3 V	1.9	4.6	10.4	1.8	11.4	12.6	ns
		V _{CC} = 1.4 V to 1.6 V	1.5	3.3	6.5	1.4	7.4	8.2	ns
		V _{CC} = 1.65 V to 1.95 V	1.2	2.9	5.1	1.1	5.9	6.5	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.0	2.2	3.8	0.9	4.5	4.9	ns
		V _{CC} = 3.0 V to 3.6 V	0.9	2.3	4.0	0.8	4.5	4.9	ns
C _L = 10	pF								
t _{pd}	propagation delay	A or B to Y; see Figure 8 [2]							
	V _{CC} = 0.8 V	-	16.3	-	-	-	-	ns	
		V _{CC} = 1.1 V to 1.3 V	2.3	5.6	12.3	2.1	13.7	15.1	ns
		V _{CC} = 1.4 V to 1.6 V	1.8	4.1	7.6	1.7	8.8	9.7	ns
		V _{CC} = 1.65 V to 1.95 V	1.6	3.8	6.1	1.4	7.1	7.8	ns
		V_{CC} = 2.3 V to 2.7 V	1.4	2.9	4.6	1.2	5.4	5.9	ns
		V _{CC} = 3.0 V to 3.6 V	1.3	3.2	5.7	1.1	6.4	7.0	ns
C _L = 15	pF								
t _{pd}	propagation delay	A or B to Y; see Figure 8							
		V _{CC} = 0.8 V	-	19.0	-	-	-	-	ns
		V _{CC} = 1.1 V to 1.3 V	2.6	6.6	14.2	2.4	15.8	17.4	ns
		V _{CC} = 1.4 V to 1.6 V	2.1	4.8	8.7	1.9	10.1	11.1	ns
		V _{CC} = 1.65 V to 1.95 V	1.9	4.6	7.6	1.7	8.5	9.3	ns
		V_{CC} = 2.3 V to 2.7 V	1.6	3.6	5.6	1.5	6.3	6.9	ns
		V _{CC} = 3.0 V to 3.6 V	1.6	4.1	7.5	1.4	8.3	9.1	ns

Low-power 2-input NAND gate (open drain)

Symbol	Parameter	Conditions		25 °C		-40) °C to +1	25 °C	Unit
			Min	Typ <mark>[1]</mark>	Мах	Min	Max (85 °C)	Max (125 °C)	
C _L = 30	pF								_
t _{pd}	propagation delay	A or B to Y; see Figure 8 [2]							
		V _{CC} = 0.8 V	-	27.0	-	-	-	-	ns
		V _{CC} = 1.1 V to 1.3 V	3.6	9.5	19.5	3.2	21.8	24.0	ns
		V _{CC} = 1.4 V to 1.6 V	2.9	7.0	11.5	2.6	13.6	15.0	ns
		V _{CC} = 1.65 V to 1.95 V	2.6	7.0	12.1	2.3	13.3	14.6	ns
		V_{CC} = 2.3 V to 2.7 V	2.4	5.4	8.9	2.1	9.9	10.9	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	2.3	6.5	12.7	2.1	13.9	15.3	ns
C _L = 5 pl	F, 10 pF, 15 pF and	30 pF							
C _{PD}	power dissipation capacitance	$ f_i = 1 \text{ MHz}; $ [3] $ V_I = \text{GND to } V_{\text{CC}} $							
		V _{CC} = 0.8 V	-	0.6	-	-	-	-	pF
		V _{CC} = 1.1 V to 1.3 V	-	0.7	-	-	-	-	pF
		V _{CC} = 1.4 V to 1.6 V	-	0.8	-	-	-	-	pF
		V _{CC} = 1.65 V to 1.95 V	-	0.9	-	-	-	-	pF
		V_{CC} = 2.3 V to 2.7 V	-	1.1	-	-	-	-	pF
		V _{CC} = 3.0 V to 3.6 V	-	1.4	-	-	-	-	pF

Table 8. Dynamic characteristics ...continued

Voltages are referenced to GND (ground = 0 V; for test circuit see Figure 9

[1] All typical values are measured at nominal $V_{\mbox{CC}}.$

 $\label{eq:tpd} [2] \quad t_{pd} \text{ is the same as } t_{PZL} \text{ and } t_{PLZ}.$

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μ W).

 P_{D} = $C_{PD} \times V_{CC}{}^{2} \times f_{i} \times N$ where:

 $f_i = input frequency in MHz;$

 V_{CC} = supply voltage in V;

N = number of inputs switching.

Low-power 2-input NAND gate (open drain)

12. Waveforms

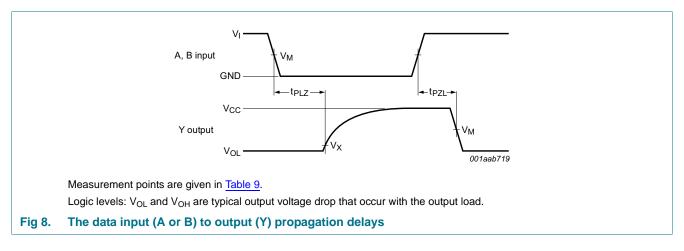


Table 9.Measurement points

Supply voltage	Input	Output	
V _{cc}	V _M	V _M	V _X
0.8 V to 1.6 V	$0.5 imes V_{CC}$	$0.5 imes V_{CC}$	V _{OL} + 0.1 V
1.65 V to 2.7 V	$0.5 imes V_{CC}$	$0.5 imes V_{CC}$	V _{OL} + 0.15 V
3.0 V to 3.6 V	$0.5 imes V_{CC}$	$0.5 imes V_{CC}$	V _{OL} + 0.3 V

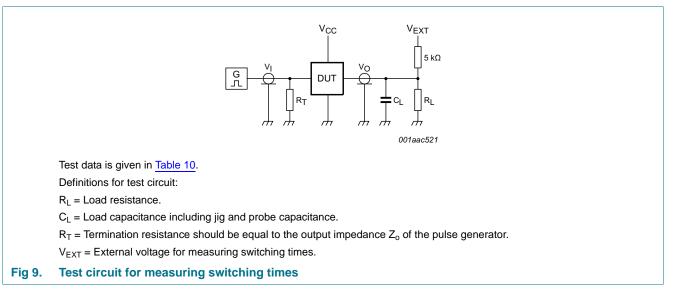


Table 10. Test data

Supply voltage	Load		V _{EXT}		
V _{cc}	CL	R _L [1]	t _{PLH} , t _{PHL}	t _{PZH} , t _{PHZ}	t _{PZL} , t _{PLZ}
0.8 V to 3.6 V	5 pF, 10 pF, 15 pF and 30 pF	5 k Ω or 1 M Ω	open	GND	$2 \times V_{CC}$

[1] For measuring enable and disable times $R_L = 5 k\Omega$, for measuring propagation delays, setup and hold times and pulse width $R_L = 1 M\Omega$.

Low-power 2-input NAND gate (open drain)

13. Package outline

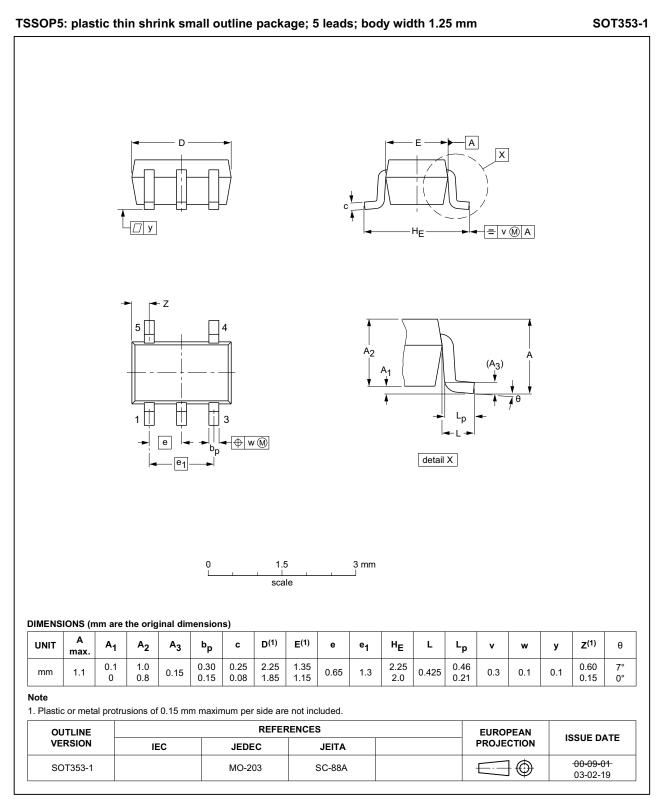


Fig 10. Package outline SOT353-1 (TSSOP5)

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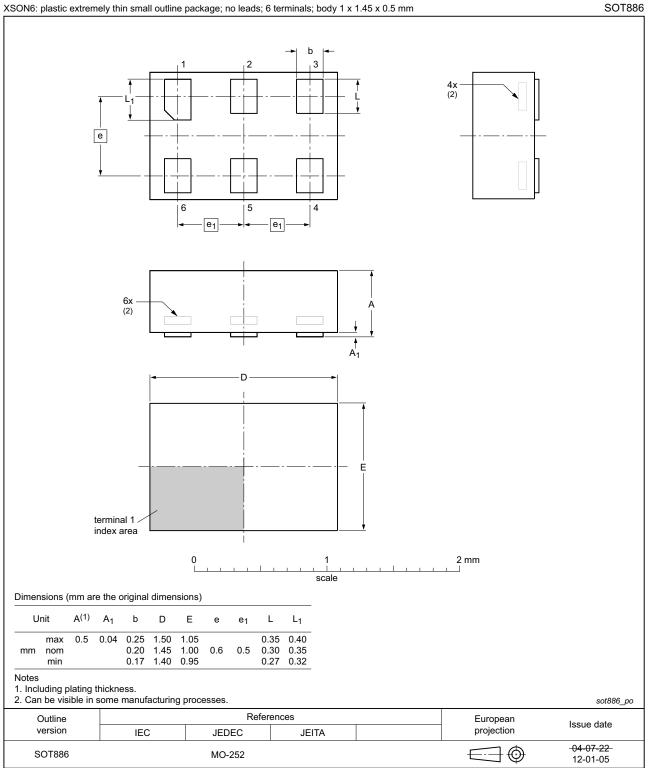


Fig 11. Package outline SOT886 (XSON6)

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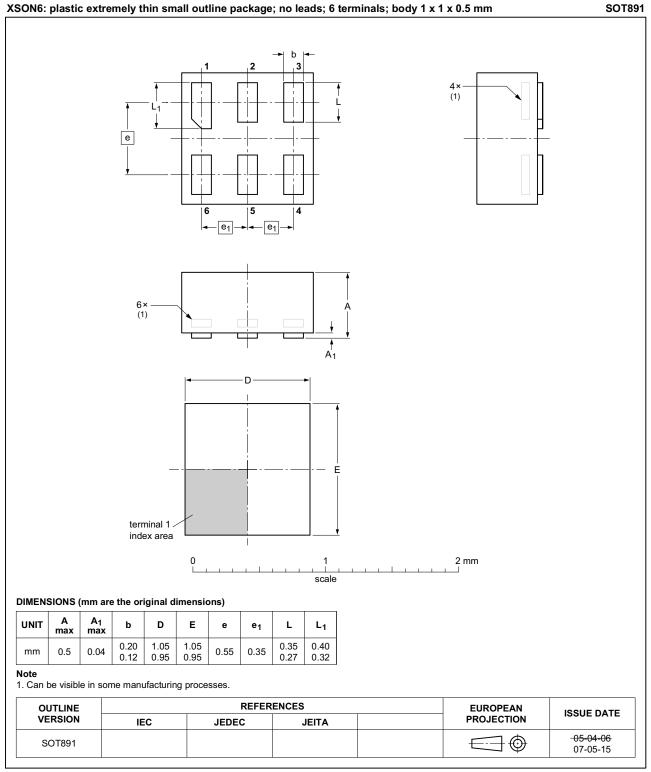
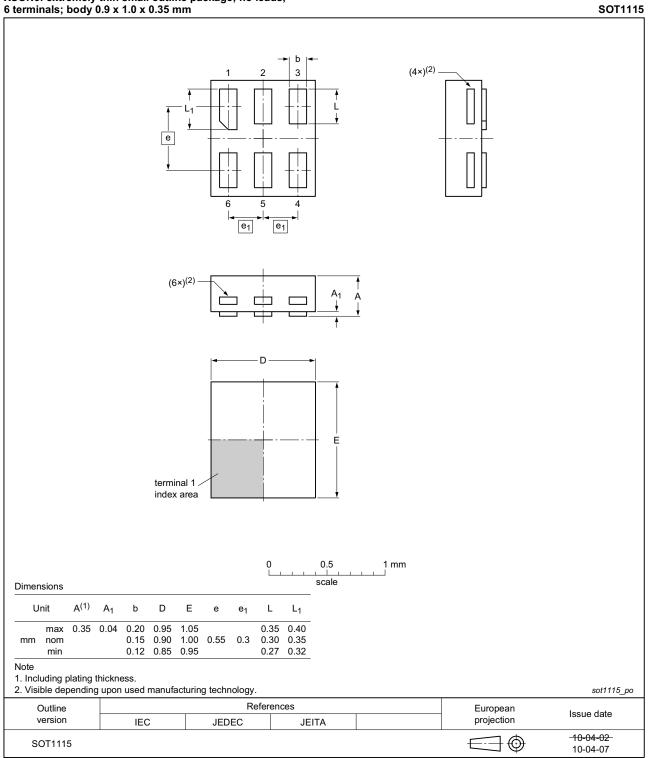


Fig 12. Package outline SOT891 (XSON6)

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Low-power 2-input NAND gate (open drain)

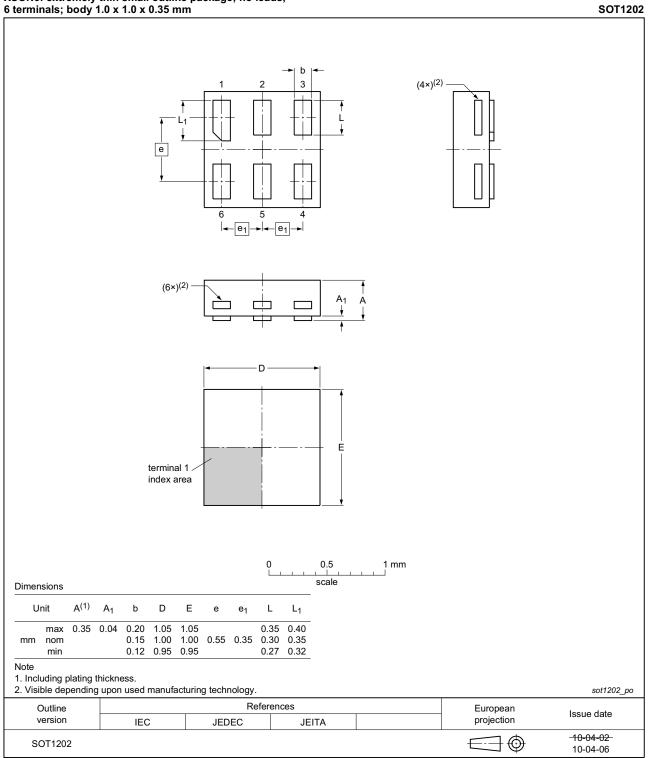


XSON6: extremely thin small outline package; no leads; 6 terminals; body 0.9 x 1.0 x 0.35 mm

Fig 13. Package outline SOT1115 (XSON6)

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Low-power 2-input NAND gate (open drain)

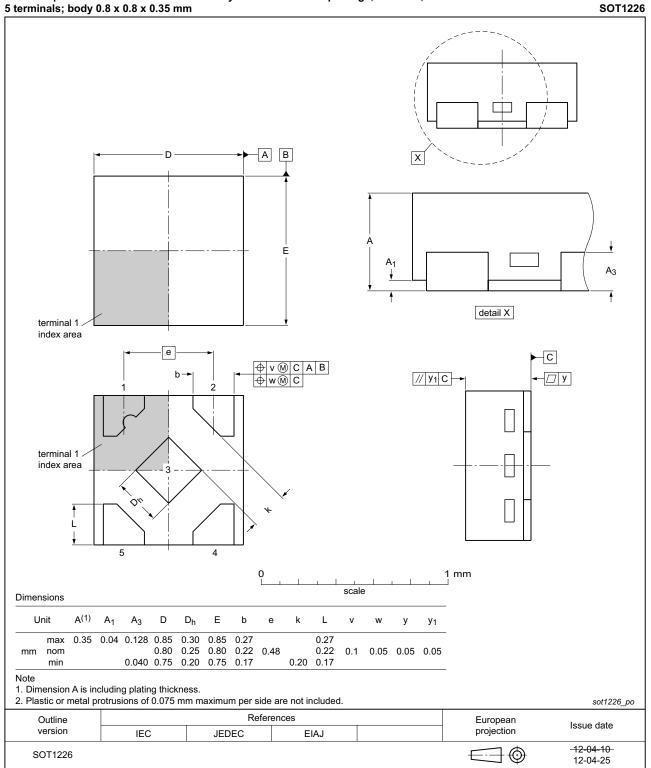


XSON6: extremely thin small outline package; no leads; 6 terminals; body 1.0 x 1.0 x 0.35 mm

Fig 14. Package outline SOT1202 (XSON6)

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X2SON5: plastic thermal enhanced extremely thin small outline package; no leads; 5 terminals: body 0.8 x 0.8 x 0.35 mm

Fig 15. Package outline SOT1226 (X2SON5)

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Low-power 2-input NAND gate (open drain)

14. Abbreviations

Table 11. Abbreviations		
Acronym	Description	
CDM	Charged Device Model	
DUT	Device Under Test	
ESD	ElectroStatic Discharge	
HBM	Human Body Model	
ММ	Machine Model	

15. Revision history

Table 12.Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AUP1G38 v.7	20160404	Product data sheet	-	74AUP1G38 v.6
Modifications:	• Figure 7: Ty	po corrected in pin naming	(pins A and B swapped	(k
74AUP1G38 v.6	20120628	Product data sheet	-	74AUP1G38 v.5
Modifications:	Added type number 74AUP1G38GX (SOT1226)			
	 Package ou 	tline drawing of SOT886 (F	igure 11) modified.	
74AUP1G38 v.5	20111129	Product data sheet	-	74AUP1G38 v.4
Modifications:	 Legal pages 	s updated.		
74AUP1G38 v.4	20101007	Product data sheet	-	74AUP1G38 v.3
74AUP1G38 v.3	20090622	Product data sheet	-	74AUP1G38 v.2
74AUP1G38 v.2	20070614	Product data sheet	-	74AUP1G38 v.1
74AUP1G38 v.1	20061020	Product data sheet	-	-

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16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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[2] The term 'short data sheet' is explained in section "Definitions".

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