

Devices in the S6E2C3 Series are highly integrated 32-bit microcontrollers with high performance and competitive cost. This series is based on the ARM Cortex-M4F processor with on-chip flash memory and SRAM. The series has peripherals such as motor control timers, A/D converters, and communications interfaces (USB, UART, CSIO (SPI), I<sup>2</sup>C, LIN). The products that are described in this data sheet are placed into TYPE3-M4 product categories "FM4 Family Peripheral Manual Main Part (002-04856)."

## Features

### 32-bit ARM Cortex-M4F Core

- Processor version: r0p1
- Up to 200 MHz frequency operation
- FPU built-in
- Support DSP instructions
- Memory protection unit (MPU): improves the reliability of an embedded system
- Integrated nested vectored interrupt controller (NVIC): 1 NMI (non-maskable interrupt) and 128 peripheral interrupts and 16 priority levels
- 24-bit system timer (Sys Tick): system timer for OS task management

### On-chip Memories

#### ■ Flash memory

This series is based on two independent on-chip flash memories.

- Up to 2048 Kbytes
- Built-in flash accelerator system with 16 Kbytes trace buffer memory
- Read access to flash memory that can be achieved without wait-cycle up to an operating frequency of 72 MHz. Even at the operating frequency more than 72 MHz, an equivalent single cycle access to flash memory can be obtained by the flash accelerator system.
- Security function for code protection

#### ■ SRAM

This is composed of three independent SRAMs (SRAM0, SRAM1 and SRAM2). SRAM0 is connected to the I-code bus or D-code bus of Cortex-M4F core. SRAM1 and SRAM2 are connected to system bus of Cortex-M4F core.

- SRAM0: up to 192 Kbytes
- SRAM1: 32 Kbytes
- SRAM2: 32 Kbytes

### External Bus Interface

- Supports SRAM, NOR, NAND flash and SDRAM device
- Up to 9 chip selects CS0 to CS8 (CS8 is only for SDRAM)
- 8-/16-/32-bit data width
- Up to 25-bit address bus
- Maximum Access size: 256M byte
- Supports address/data multiplexing
- Supports external RDY function
- Supports scramble function
- Possible to set the validity/invalidity of the scramble function for the external areas 0x6000\_0000 to 0xDFFF\_FFFF in 4 Mbytes units.
- Possible to set two kinds of the scramble key  
 Note: It is necessary to use the Cypress provided software library to use the scramble function.

### USB Interface (Max two Channels)

The USB interface is composed of a device and a host.

#### ■ USB device

- USB 2.0 Full-speed supported
- Max 6 EndPoint supported
  - EndPoint 0 is control transfer
  - EndPoint 1, 2 can be selected bulk-transfer, interrupt-transfer or isochronous-transfer
  - EndPoint 3 to 5 can select bulk-transfer or interrupt-transfer
  - EndPoint 1 to 5 comprise double buffer
- The size of each endpoint is as follows.
  - Endpoint 0, 2 to 5: 64 byte
  - EndPoint 1: 256 byte

#### ■ USB host

- USB2.0 Full-Speed/Low-Speed supported
- Bulk-transfer, interrupt-transfer, and isochronous-transfer support
- USB Device connected/dis-connected automatically detect
- IN/OUT token handshake packet automatically
- Max 256-byte packet length supported
- Wake-up function supported

### Multi-function Serial Interface (Max 16 channels)

- Separate 64 byte receive and transmit FIFO buffers for channels 0 to 7.
- Operation mode is selectable for each channel from the following:
  - UART
  - CSIO (SPI)
  - LIN
  - I<sup>2</sup>C
- UART
  - Full-duplex double buffer
  - Selection with or without parity supported
  - Built-in dedicated baud rate generator
  - External clock available as a serial clock
  - Various error detect functions available (parity errors, framing errors, and overrun errors)
- CSIO (SPI)
  - Full-duplex double buffer
  - Built-in dedicated baud rate generator
  - Overrun error detect function available
  - Serial chip select function (ch 6 and ch 7 only)
  - Supports high-speed SPI (ch 4 and ch 6 only)
  - Data length 5 to 16-bit
- LIN
  - LIN protocol Rev.2.1 supported
  - Full-duplex double buffer
  - Master/slave mode supported
  - LIN break field generation (can change to 13- to 16-bit length)
  - LIN break delimiter generation (can change to 1- to 4-bit length)
  - Various error detect functions available (parity errors, framing errors, and overrun errors)
- I<sup>2</sup>C
  - Standard mode (Max 100 kbps)/  
Fast mode (Max 400 kbps) supported
  - Fast mode Plus (Fm+) (Max 1000 kbps, only for ch 3 = ch A and ch 7 = ch B) supported

### DMA Controller (Eight channels)

DMA controller has an independent bus, so the CPU and DMA controller can process simultaneously.

- Eight independently configured and operated channels
- Transfer can be started by software or request from the built-in peripherals
- Transfer address area: 32-bit (4 GB)
- Transfer mode: Block transfer/Burst transfer/Demand transfer
- Transfer data type: bytes/half-word/word
- Transfer block count: 1 to 16
- Number of transfers: 1 to 65536

### DSTC (Descriptor System data Transfer Controller; 256 Channels)

The DSTC can transfer data at high-speed without going via the CPU. The DSTC adopts the descriptor system and, following the specified contents of the descriptor that has already been constructed on the memory, can access directly the memory/peripheral device and perform the data-transfer operation.

It supports the software activation, the hardware activation, and the chain activation functions.

### A/D Converter (Max 32 channels)

- 12-bit A/D Converter
  - Successive approximation type
  - Built-in three units
  - Conversion time: 0.5 μs at 5 V
  - Priority conversion available (priority at two levels)
  - Scanning conversion mode
  - Built-in FIFO for conversion data storage (for SCAN conversion: 16 steps, for priority conversion: 4 steps)

### D/A Converter (Max 2 Channels)

- R-2R type
- 12-bit resolution

### Base Timer (Max 16 Channels)

Operation mode is selected from the following for each channel:

- 16-bit PWM timer
- 16-bit PPG timer
- 16-/32-bit reload timer
- 16-/32-bit PWC timer

### General Purpose I/O Port

This series can use its pins as general purpose I/O ports when they are not used for external bus or peripherals; moreover, the port relocate function is built in. It can set the I/O port to which the peripheral function can be allocated.

- Capable of pull-up control per pin
- Capable of reading pin level directly
- Built-in port-relocate function
- Up to 120 high-speed general-purpose I/O ports in 144-pin package
- Some pins 5 V tolerant I/O.  
See 4. Pin Descriptions and 5. I/O Circuit Type for the corresponding pins.

### Multi-function Timer (Max three Units)

The multi-function timer is composed of the following blocks:

Minimum resolution: 5.00 ns

- 16-bit free-run timer × 3 ch/unit
- Input capture × 4 ch/unit
- Output compare × 6 ch/unit
- A/D activation compare × 6 ch/unit
- Waveform generator × 3 ch/unit
- 16-bit PPG timer × 3 ch/unit

The following functions can be used to achieve the motor control:

- PWM signal output function
- DC chopper waveform output function
- Dead time function
- Input capture function
- A/D convertor activate function
- DTIF (motor emergency stop) interrupt function

### Real-Time Clock (RTC)

The real-time clock can count year, month, day, hour, minute, second, or day of the week from 00 to 99.

- Interrupt function with specifying date and time (year/month/day/hour/minute) is available. This function is also available by specifying only year, month, day, hour, or minute.
- Timer interrupt function after set time or each set time.
- Capable of rewriting the time with continuing the time count.
- Leap year automatic count is available.

### Quadrature Position/Revolution Counter (QPRC; Max four Channels)

The Quadrature Position/Revolution Counter (QPRC) is used to measure the position of the position encoder. It is also possible to use up/down counter.

- The detection edge of the three external event input pins AIN, BIN and ZIN is configurable.
- 16-bit position counter
- 16-bit revolution counter
- Two 16-bit compare registers

### Dual Timer (32-/16-bit Down Counter)

The dual timer consists of two programmable 32/16-bit down counters.

Operation mode is selectable from the following for each channel:

- Free-running
- Periodic (= Reload)
- One shot

### Watch Counter

The watch counter is used for wake up from low-power consumption mode. It is possible to select the main clock, sub clock, built-in High-speed CR clock, or built-in low-speed CR clock as the clock source.

- Interval timer: up to 64 s (max) with a sub clock of 32.768 kHz

### External Interrupt Controller Unit

- External interrupt input pin: Max 32 pins
- Include one non-maskable interrupt (NMI)

### Watchdog Timer (2 Channels)

A watchdog timer can generate interrupts or a reset when a time-out value is reached.

This series consists of two different watchdogs: a "hardware" watchdog and a "software" watchdog.

The hardware watchdog timer is clocked by low-speed internal CR oscillator. The hardware watchdog is thus active in any power saving mode except RTC mode and Stop mode.

### Cyclic Redundancy Check (CRC) Accelerator

The CRC accelerator helps to verify data transmission or storage integrity.

CCITT CRC16 and IEEE-802.3 CRC32 are supported.

- CCITT CRC16 generator polynomial: 0x1021
- IEEE-802.3 CRC32 generator polynomial: 0x04C11DB7

### Programmable Cyclic Redundancy Check (PRGCRC) Accelerator

The CRC accelerator helps a verify data transmission or storage integrity.

CCITT CRC16, IEEE-802.3 CRC32 and generating polynomial are supported.

- CCITT CRC16 generator polynomial: 0x1021
- IEEE-802.3 CRC32 generator polynomial: 0x04C11DB7
- Generating polynomial

### SD Card Interface

It is possible to use the SD card that conforms to the following standards.

- Part 1 Physical Layer Specification version 3.01
- Part E1 SDIO Specification version 3.00
- Part A2 SD Host Controller Standard Specification version 3.00
- 1-bit or 4-bit data bus

### I<sup>2</sup>S (Inter-IC Sound Bus) Interface (TX x 1 channel, RX x 1 channel)

- Supports three transfer protocols
  - I<sup>2</sup>S
  - Left justified
  - DSP mode
  - Separate clock generation block for flexible system integration options
- Master/slave mode selectable
- RX Only, TX Only or TX and RX simultaneous operation selectable
- Word length is programmable from 7-bits to 32 bits
- RX/TX FIFO integrated (RX: 66 words x 32-bits, TX: 66 words x 32-bits)
- DMA, interrupts, or polling based data transfer supported

### High-Speed Quad SPI

Up to 66 MHz clock rates for very fast data transfers to and from SPI compatible devices.

Up to 256 Mbytes of memory mapped address space.

- Single data rate (SDR)
- Supports single, dual, and quad data modes
- Built-in direct mode and command sequencer mode
  - Direct mode: Access by use of transmission FIFO/reception FIFO (up to 16 word x 32 bit)
  - Command sequencer mode: Automatic access assigned to external device area.

### Clock and Reset

#### ■ Clocks

Five clock sources (two external oscillators, two internal CR oscillators, and Main PLL) that are dynamically selectable.

- Main clock: 4 MHz to 48 MHz
- Sub clock: 32.768 kHz
- High-speed internal CR clock: 4 MHz
- Low-speed internal CR clock: 100 kHz
- Main PLL Clock

#### ■ Resets

- Reset requests from INITX pin
- Power on reset
- Software reset
- Watchdog timer reset
- Low-voltage detector reset
- Clock supervisor reset

### Clock Supervisor (CSV)

Clocks generated by internal CR oscillators are used to supervise abnormality of the external clocks.

- External OSC clock failure (clock stop) is detected, reset is asserted.
- External OSC frequency anomaly is detected, interrupt or reset is asserted.

### Low-Voltage Detector (LVD)

This Series include two-stage monitoring of voltage on the VCC pins. when the voltage falls below the voltage that has been set, the low-voltage detector function generates an interrupt or reset.

- LVD1: error reporting via interrupt
- LVD2: auto-reset operation

### Low-power Consumption Mode

Six low power consumption modes are supported.

- Sleep
- Timer
- RTC
- Stop
- Deep standby RTC (selectable from with/without RAM retention)
- Deep standby stop (selectable from with/without RAM retention)

### Peripheral Clock Gating

The system can reduce the current consumption of the total system with gating the operation clocks of peripheral functions not used.

### VBAT

The consumption power during the RTC operation can be reduced by supplying the power supply independent from the RTC (calendar circuit)/32 kHz oscillation circuit. The following circuits can also be used.

- RTC
- 32-kHz oscillation circuit
- Power-on circuit
- Back up register: 32 bytes
- Port circuit

### Debug

- Serial wire JTAG debug port (SWJ-DP)
- Embedded trace macrocells (ETM) provide comprehensive debug and trace facilities.
- AHB trace macrocells (HTM)

### Unique ID

Unique value of the device (41-bit) is set.

### Power Supply

- Four power supplies
  - Wide range voltage:
    - VCC = 2.7 V to 5.5 V
  - Power supply for USB ch 0 I/O:
    - USBVCC0 = 3.0 V to 3.6 V (when USB is used)
    - = 2.7 V to 5.5 V (when GPIO is used)
  - Power supply for USB ch 1 I/O:
    - USBVCC1 = 3.0 V to 3.6 V (when USB is used)
    - = 2.7 V to 5.5 V (when GPIO is used)
  - Power supply for VBAT:
    - VBAT = 1.65 V to 5.5 V

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## 1. Product Lineup

### Memory Size

Product Name		S6E2C38H/J/L	S6E2C39H/J/L	S6E2C3AH/J/L
On-chip flash memory		1024 Kbytes	1536 Kbytes	2048 Kbytes
On-chip	SRAM	128 Kbytes	192 Kbytes	256 Kbytes
	SRAM0	64 Kbytes	128 Kbytes	192 Kbytes
	SRAM1	32 Kbytes	32 Kbytes	32 Kbytes
	SRAM2	32 Kbytes	32 Kbytes	32 Kbytes

### Function

Product Name		S6E2C38H0A S6E2C39H0A S6E2C3AH0A	S6E2C38J0A S6E2C39J0A S6E2C3AJ0A	S6E2C38L0A S6E2C39L0A S6E2C3AL0A
Pin count		144	176/192	216
CPU		Cortex-M4F, MPU, NVIC 128 ch		
Freq.		200 MHz		
Power supply voltage range		2.7 V to 5.5 V		
USB2.0 (device/host)		2 ch		
DMAC		8ch		
DSTC		256 ch		
External bus interface		Addr: 25-bit (Max), Data: 8-/16-bit CS: 9 (Max), SRAM, NOR flash NAND flash	Addr: 25-bit (Max), Data: 8-/16-bit CS: 9 (Max), SRAM, NOR flash , NAND flash SDRAM	Addr: 25-bit (Max), Data: 8-/16-/32-bit CS: 9 (Max), SRAM, NOR flash , NAND flash, SDRAM
Multi-function serial interface (UART/CSIO/LIN/I <sup>2</sup> C)		16ch (Max) ch 0 to ch 7 : FIFO, ch 8 to ch 15 : No FIFO		
Base timer (PWC/Reload timer/PWM/PPG)		16 ch (Max)		
MF timer	A/D activation compare	6 ch		
	Input capture	4 ch		
	Free-run timer	3 ch		
	Output compare	6 ch		
	Waveform generator	3 ch		
	PPG	3 ch		
SD card interface		1 unit		
I <sup>2</sup> S		-	1 unit	
High-speed quad SPI		-	1 unit	
QPRC		4 ch (Max)		
Dual timer		1 unit		
Real-time clock		1 unit		
Watch counter		1 unit		
CRC accelerator		Yes (fixed, programmable)		
Watchdog timer		1 ch (SW) + 1 ch (HW)		
External interrupts		32 pins (Max)+ NMI × 1		
I/O ports		120 pins (Max)	152 pins (Max)	190 pins (Max)
12-bit A/D converter		24 ch (3 units)	32 ch (3 units)	
12-bit D/A converter		2 units (Max)		
CSV (clock supervisor)		Yes		
LVD (low-voltage detector)		2 ch		
Built-in CR	High-speed	4 MHz		
	Low-speed	100 kHz		
Debug function		SWJ-DP/ETM/HTM		
Unique ID		Yes		



**Notes:**

- All signals of the peripheral function in each product cannot be allocated by limiting the pins of package. It is necessary to use the port relocate function of the I/O port according to your function use.
- See 12.4.3 Built-In CR Oscillation Characteristics for the accuracy of the built-in CR.

**2. Packages**

Package	Product Name	S6E2C38H0A	S6E2C38J0A	S6E2C38L0A
		S6E2C39H0A	S6E2C39J0A	S6E2C39L0A
		S6E2C3AH0A	S6E2C3AJ0A	S6E2C3AL0A
LQFP: LQS144 (0.5-mm pitch)		○	-	-
LQFP: LQP176 (0.5-mm pitch)		-	○	-
BGA : LBE192 (0.8-mm pitch)		-	○	-
LQFP: LQQ216 (0.4-mm pitch)		-	-	○

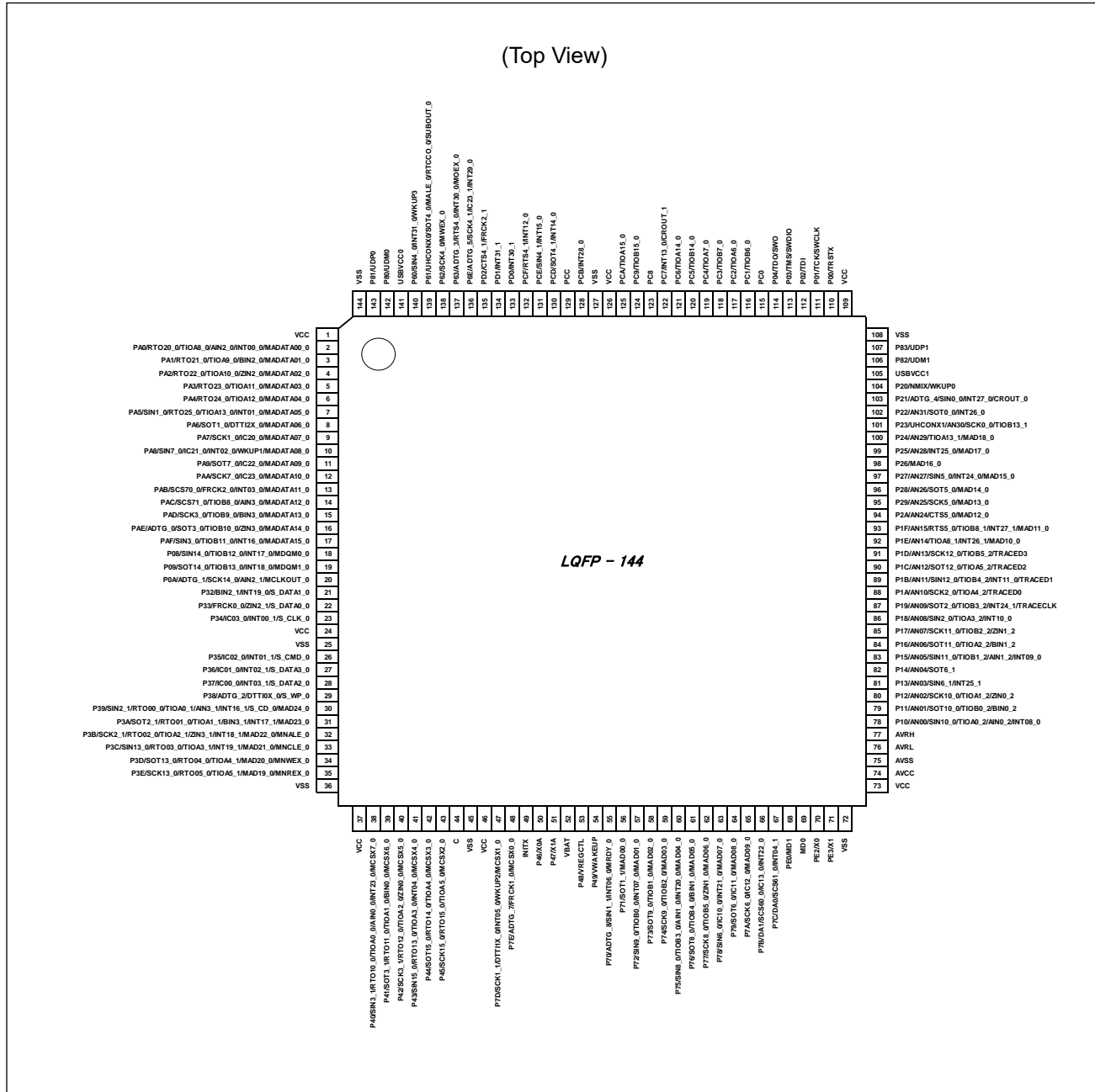
○: Supported

**Note:**

- See 14. Package Diagrams for detailed information on each package.

### 3. Pin Assignments

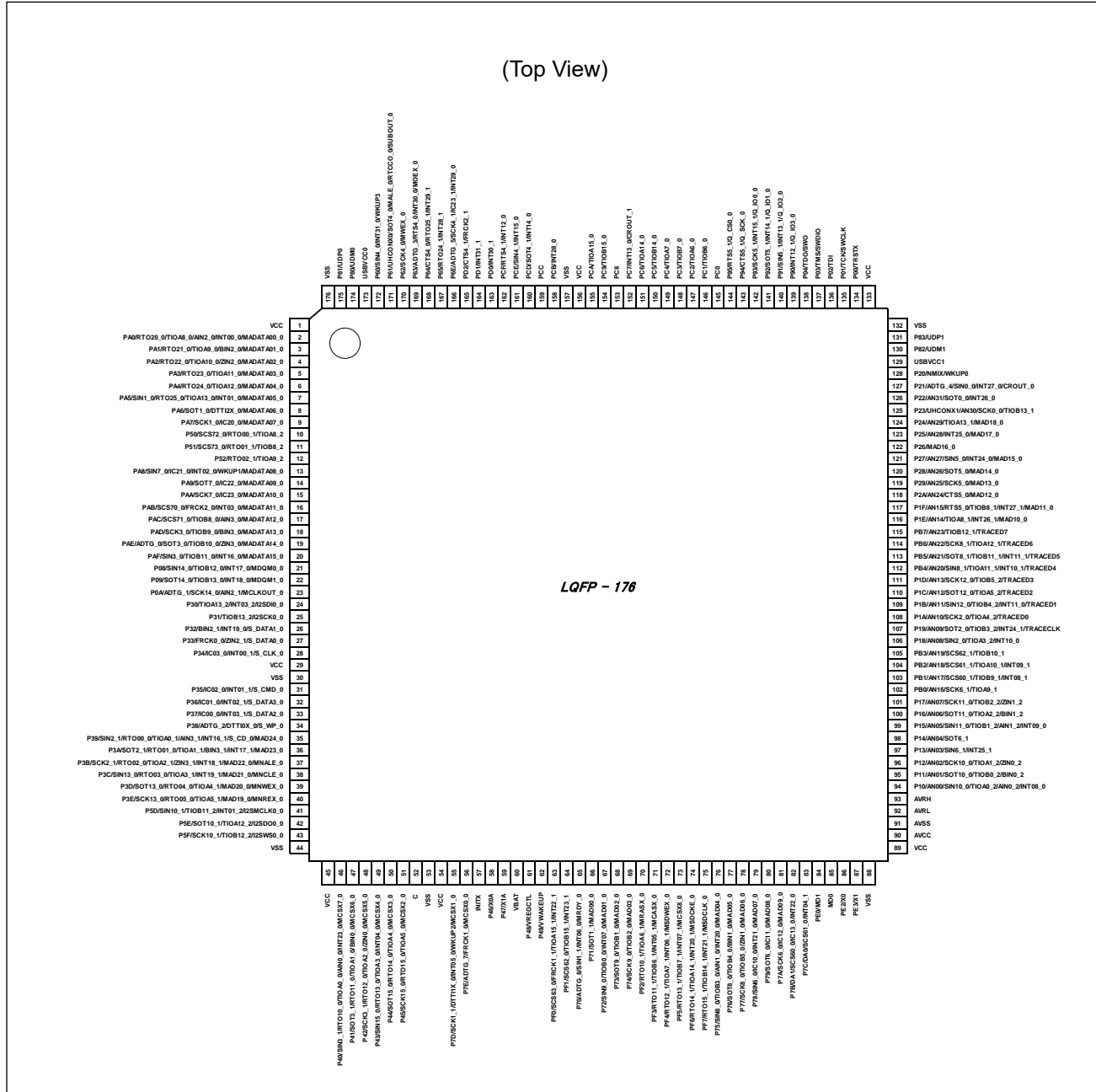
#### LQS144



**Note:**

- The number after the underscore ("\_") in pin names such as XXX\_1 and XXX\_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

LQP176



**Note:**

- The number after the underscore ("\_") in pin names such as XXX\_1 and XXX\_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

LQ216

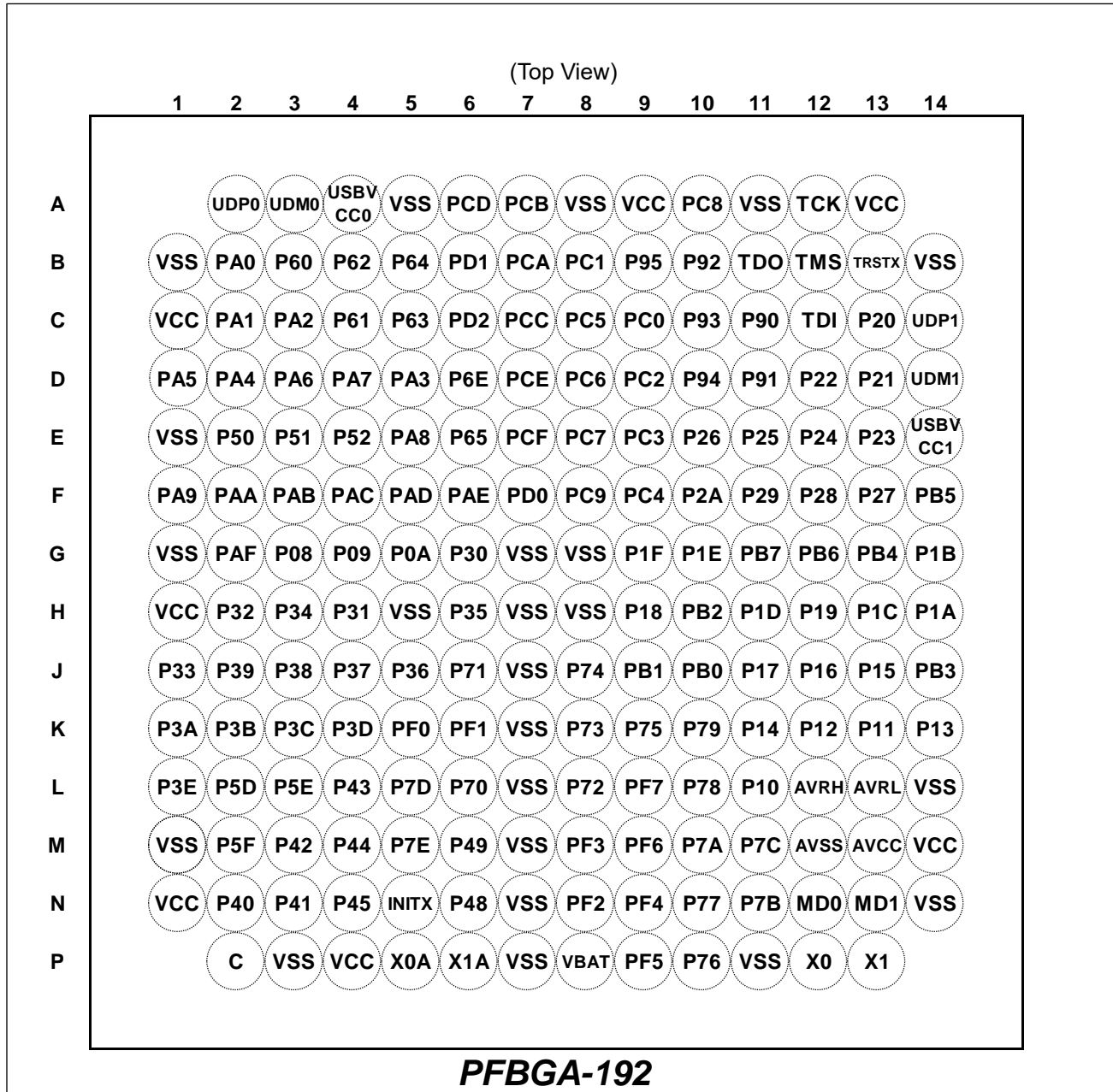
(Top View)

1	VCC	162	VSS
2	PA1RT020_0710A8_0I2N2_0INT08_0IMADAT4A00_0	161	PS3UDP1
3	PA1RT021_0710A8_0I2N2_0IMADAT4A01_0	160	PS3UDM1
4	PA2IRT022_0710A10_0I2N2_0IMADAT4A02_0	159	USBVCC1
5	PA3IRT023_0710A11_0IMADAT4A03_0	158	PS20N0XWKLUP0
6	PA4IRT024_0710A12_0IMADAT4A04_0	157	PS12A070_0I2N2_0INT27_0SCROUT_0
7	PA5ISIN1_0RT025_0710A13_0INT10_0IMADAT4A05_0	156	PS2AN215070_0INT26_0
8	PA6ISOT1_0RT12X_0IMADAT4A06_0	155	PS23UHCONK1AN20SCK0_0710B13_1
9	PA7ISCK1_0IC20_0IMADAT4A07_0	154	PS4AN29710A13_1MAD18_0
10	PS5SCS22_0RT026_1710A8_2MADAT4A16_0	153	PS2AN20B12ES_0MAD17_0
11	PS1VSCF3_0RT001_1710B8_2MADAT4A17_0	152	PS26MAD16_0
12	PS2IRT02_1710A9_2MADAT4A18_0	151	PS1PFB00_1I2N3_2INT11_2TRACED15
13	PS2IRT03_1710B9_2MADAT4A19_0	150	PS2IRT03_1I2N3_2TRACED14
14	PA6ISIN7_0IC21_0INT02_0SWRUP1MADAT4A08_0	149	PSB5SCK6_1I2N3_2INT10_2TRACED13
15	PA6ISOT7_0IC22_0IMADAT4A09_0	148	PSCTRACED12
16	PA6ISCK7_0IC23_0IMADAT4A10_0	147	PS2IAN270BNS_0INT24_0MAD15_0
17	PA6ISCS7_0710B8_0I2N3_0IMADAT4A11_0	146	PS2AN20S07S_0MAD14_0
18	PA6ISCS71_0710B8_0I2N3_0IMADAT4A12_0	145	PS2AN25SCK5_0MAD13_0
19	PS4ISIN15_1I2N04_1710A10_3INT08_2MADAT4A20_0	144	PS2AN24CT8S_0MAD12_0
20	PS5SOT15_1I2N05_1710B10_2MADAT4A21_0	143	PS1FIAN15I2T8S_0710B8_1INT27_1MAD11_0
21	PS5SCK15_1I2N07X_1710B0_1MADAT4A22_0	142	PS1FIAN1710A8_1INT26_1MAD10_0
22	PS7RC00_1710B1_1MADAT4A23_0	141	PS7IAN23710B12_17TRACED7
23	PA6ISCK3_0710B8_0I2N3_0IMADAT4A13_0	140	PS6IAN23SCK4_1710A12_17TRACED6
24	PA6ISOT3_0S071_0710B10_0I2N2_0IMADAT4A14_0	139	PS6IAN21S07S_1710B11_1INT11_17TRACED5
25	PA6ISIN3_0710B11_0INT16_0IMADAT4A15_0	138	PS6IAN20SIN6_1710A11_1SINT10_17TRACED4
26	PS6ISIN11_1M091_1710B8_1INT02_2MADAT4A24_0	137	VCC
27	PS6SOT11_1M02_1710B3_1MADAT4A25_0	136	VSS
28	PS6ISCK11_1M03_1710A4_1MADAT4A26_0	135	PS13AN13SCK12_0710B8_2TRACED3
29	PS6VRC00_1710B8_0I2N3_1MADAT4A27_0	134	PS1CIAN12S0712_0710A5_2TRACED2
30	PS6ISIN14_0710B12_0INT17_0MAD00_0	133	PS1BIAN11SIN12_0710B8_2INT11_0TRACED1
31	PS6SOT14_0710B13_0INT18_0MAD01_0	132	PS1BIAN10SCK1_0710A4_2TRACED0
32	PS6IADT0_15CK14_0I2N2_1M01CLKOUT_0	131	PS1SIAN09S072_0710B3_2INT24_17TRACECLK
33	PSCTIOA11_2MADAT4A28_0RTCCO_1S0B0UT1_0	130	PS18AN08SIN2_0710A3_2INT10_0
34	PS9710A13_2INT03_2MAD0A2_0I2S00_0	129	PS6IAN19SCK62_1710B10_1
35	PS1710B13_2MAD0A2_0I2SCK0_0	128	PS6IAN18SCK1_1710A10_1INT09_1
36	PS32IN2_1SINT19_0I2S_DATA1_0	127	PS6IAN17SCK0_1710B9_1INT08_1
37	PS3VRC00_1I2S_DATA0_0	126	PS6IAN16SCK4_1710A9_1
38	PS4SCK0_0INT06_0I2S_CLK_0	125	PS7IAN07SCK11_0710B2_2SIN1_2
39	VCC	124	PS16AN06S0711_0710A2_2SIN1_2
40	VSS	123	PS15AN05SIN11_0710B1_2AIN1_2INT09_0
41	PS3SCK0_0INT01_1I2S_CMD_0	122	PS6SCK6_1I2N2_2TRACED11
42	PS3SCK1_0INT02_1I2S_DATA1_0	121	PS6S07S_1I2N2_2TRACED10
43	PS37VRC0_0SINT03_1I2S_DATA2_0	120	PS6SIN6_1I2N2_2INT03_2TRACED9
44	PS3IADT0_2I2T0X_0I2S_WP_0	119	PS6IADT0_0SCK3_1INT08_2TRACED8
45	PS38IN2_1I2T00_0710A3_1I2N2_1SINT16_1I2S_CMD_2MAD04_0	118	PS16AN04S07S_1
46	PS4ISOT2_1I2T01_0710A1_0I2N3_1SINT17_1MAD23_0	117	PS13AN03SIN6_1INT25_1
47	PS3VSC2_1I2T02_0710A2_1I2N3_1SINT18_1MAD22_0MNALE_0	116	PS12AN02SCK10_0710A1_2SIN2_2
48	PS3SIN3_0SINT03_0710A3_1SINT19_1MAD21_0MNALE_0	115	PS11AN01S0710_0710B0_2SIN20_2
49	PS3SOT13_0SINT04_0710A4_1MAD20_0MNALE_0	114	PS10AN00SIN6_0710A0_2AIN0_2INT08_0
50	PS3SCK13_0SINT05_0710A5_1MAD19_0MNALE_0	113	AVRH
51	PS3SIN10_1710B11_2INT01_2MADAT4A29_0I2S0MCLK0_0	112	AVRL
52	PS3SOT10_1710A12_2MADAT4A30_0I2S00_0	111	AVB
53	PS3SCK10_1710B12_2MADAT4A31_0I2S0W0_0	110	AVCC
54	VSS	109	VCC

LQFP - 216

**Note:**  
 - The number after the underscore ("\_") in pin names such as XXX\_1 and XXX\_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

LBE192



**Note:**

- The number after the underscore ("\_") in pin names such as XXX\_1 and XXX\_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

## 4. Pin Descriptions

### List of Pin Functions

The number after the underscore ("\_") in pin names such as XXX\_1 and XXX\_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel.

Use the extended port function register (EPFR) to select the pin.

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQQ216	LQP176	LQS144	LBE192			
1	1	1	C1	VCC	-	-
2	2	2	B2	PA0	G	K
				RTO20_0 (PPG20_0)		
				TIOA8_0		
				AIN2_0		
				INT00_0		
MADATA00_0						
3	3	3	C2	PA1	G	I
				RTO21_0 (PPG20_0)		
				TIOA9_0		
				BIN2_0		
MADATA01_0						
4	4	4	C3	PA2	G	I
				RTO22_0 (PPG22_0)		
				TIOA10_0		
				ZIN2_0		
MADATA02_0						
5	5	5	D5	PA3	G	I
				RTO23_0 (PPG22_0)		
				TIOA11_0		
MADATA03_0						
6	6	6	D2	PA4	G	I
				RTO24_0 (PPG24_0)		
				TIOA12_0		
MADATA04_0						
7	7	7	D1	PA5	G	K
				SIN1_0		
				RTO25_0 (PPG24_0)		
				TIOA13_0		
				INT01_0		
MADATA05_0						
8	8	8	D3	PA6	E	I
				SOT1_0 (SDA1_0))		
				DTTI2X_0		
MADATA06_0						
9	9	9	D4	PA7	E	I
				SCK1_0 (SCL1_0)		
				IC20_0		
				MADATA07_0		

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQQ216	LQP176	LQS144	LBE192			
10	10	-	E2	P50	E	I
				SCS72_0		
				RTO00_1 (PPG00_1)		
				TIOA8_2		
				MADATA16_0		
11	11	-	E3	P51	E	I
				SCS73_0		
				RTO01_1 (PPG00_1)		
				TIOB8_2 MADATA17_0		
12	12	-	E4	P52	E	I
				RTO02_1 (PPG02_1)		
				TIOA9_2		
				MADATA18_0		
13	-	-	-	P53	E	I
				RTO03_1 (PPG02_1)		
				TIOB9_2		
				MADATA19_0		
14	13	10	E5	PA8	I	Q
				SIN7_0		
				IC21_0		
				INT02_0		
				WKUP1		
				MADATA08_0		
15	14	11	F1	PA9	N	I
				SOT7_0 (SDA7_0)		
				IC22_0		
				MADATA09_0		
16	15	12	F2	PAA	N	I
				SCK7_0 (SCL7_0)		
				IC23_0		
				MADATA10_0		
17	16	13	F3	PAB	E	K
				SCS70_0		
				FRCK2_0		
				INT03_0 MADATA11_0		
18	17	14	F4	PAC	E	I
				SCS71_0		
				TIOB8_0		
				AIN3_0 MADATA12_0		
19	-	-	-	P54	E	K
				SIN15_1		
				RTO04_1 (PPG04_1)		
				TIOA10_2		
				INT00_2		
				MADATA20_0		

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQQ216	LQP176	LQS144	LBE192			
20	-	-	-	P55	E	I
				SOT15_1 (SDA15_1)		
				RTO05_1 (PPG04_1)		
				TIOB10_2		
				MADATA21_0		
21	-	-	-	P56	E	I
				SCK15_1 (SCL15_1)		
				DTTIOX_1		
				TIOB0_1		
				MADATA22_0		
22	-	-	-	P57	E	I
				IC00_1		
				TIOB1_1		
				MADATA23_0		
23	18	15	F5	PAD	N	I
				SCK3_0 (SCL3_0)		
				TIOB9_0		
				BIN3_0		
				MADATA13_0		
24	19	16	F6	PAE	N	I
				ADTG_0		
				SOT3_0 (SDA3_0)		
				TIOB10_0		
				ZIN3_0		
				MADATA14_0		
25	20	17	G2	PAF	I	K
				SIN3_0		
				TIOB11_0		
				INT16_0		
				MADATA15_0		
26	-	-	-	P58	E	K
				SIN11_1		
				IC01_1		
				TIOB2_1		
				INT02_2		
				MADATA24_0		
27	-	-	-	P59	E	I
				SOT11_1 (SDA11_1)		
				IC02_1		
				TIOB3_1		
				MADATA25_0		
28	-	-	-	P5A	E	I
				SCK11_1 (SCL11_1)		
				IC03_1		
				TIOB4_1		
				MADATA26_0		



Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQQ216	LQP176	LQS144	LBE192			
29	-	-	-	P5B	E	I
				FRCK0_1		
				TIOB5_1		
				MADATA27_0		
30	21	18	G3	P08	E	K
				SIN14_0		
				TIOB12_0		
				INT17_0		
31	22	19	G4	P09	E	K
				SOT14_0 (SDA14_0)		
				TIOB13_0		
				INT18_0		
32	23	20	G5	P0A	L	I
				ADTG_1		
				SCK14_0 (SCL14_0)		
				AIN2_1		
33	-	-	-	MCLKOUT_0	E	I
				P5C		
				TIOA11_2		
				MADATA28_0		
34	24	-	G6	RTCCO_1	E	K
				SUBOUT_1		
				P30		
				TIOA13_2		
35	25	-	H4	INT03_2	E	I
				MDQM2_0		
				I2SDI0_0		
				P31		
36	26	21	H2	TIOB13_2	L	K
				MDQM3_0		
				I2SCK0_0		
				P32		
37	27	22	J1	BIN2_1	L	I
				INT19_0		
				S_DATA1_0		
				P33		
38	28	23	H3	FRCK0_0	L	K
				ZIN2_1		
				S_DATA0_0		
				P34		
39	29	24	H1	IC03_0	-	-
				INT00_1		
				S_CLK_0		
41	31	26	H6	VCC	L	K
				VSS		
				P35		
				IC02_0		
40	30	25	H5	INT01_1	-	-
				S_CMD_0		

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQQ216	LQP176	LQS144	LBE192			
42	32	27	J5	P36	L	K
				IC01_0		
				INT02_1		
				S_DATA3_0		
43	33	28	J4	P37	L	K
				IC00_0		
				INT03_1		
				S_DATA2_0		
44	34	29	J3	P38	E	I
				ADTG_2		
				DTTIOX_0		
				S_WP_0		
45	35	30	J2	P39	G	K
				SIN2_1		
				RTO00_0 (PPG00_0)		
				TIOA0_1		
				AIN3_1		
				INT16_1		
				S_CD_0		
MAD24_0						
46	36	31	K1	P3A	G	K
				SOT2_1 (SDA2_1)		
				RTO01_0 (PPG00_0)		
				TIOA1_1		
				BIN3_1		
				INT17_1		
				MAD23_0		
47	37	32	K2	P3B	G	K
				SCK2_1 (SCL2_1)		
				RTO02_0 (PPG02_0)		
				TIOA2_1		
				ZIN3_1		
				INT18_1		
				MAD22_0		
				MNALE_0		
48	38	33	K3	P3C	G	K
				SIN13_0		
				RTO03_0 (PPG02_0)		
				TIOA3_1		
				INT19_1		
				MAD21_0		
				MNCLE_0		
49	39	34	K4	P3D	G	I
				SOT13_0 (SDA13_0)		
				RTO04_0 (PPG04_0)		
				TIOA4_1		
				MAD20_0		
				MNWEX_0		

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQQ216	LQP176	LQS144	LBE192			
50	40	35	L1	P3E	G	I
				SCK13_0 (SCL13_0)		
				RTO05_0 (PPG04_0)		
				TIOA5_1		
				MAD19_0		
MNREX_0						
51	41	-	L2	P5D	E	K
				SIN10_1		
				TIOB11_2		
				INT01_2		
				MADATA29_0		
I2SMCLK0_0						
52	42	-	L3	P5E	E	I
				SOT10_1 (SDA10_1)		
				TIOA12_2		
				MADATA30_0		
				I2SDO0_0		
53	43	-	M2	P5F	E	I
				SCK10_1 (SCL10_1)		
				TIOB12_2		
				MADATA31_0		
				I2SWS0_0		
54	44	36	M1	VSS	-	-
55	45	37	N1	VCC	-	-
56	46	38	N2	P40	G	K
				SIN3_1		
				RTO10_0 (PPG10_0)		
				TIOA0_0		
				AIN0_0		
				INT23_0		
				MCSX7_0		
57	47	39	N3	P41	G	I
				SOT3_1 (SDA3_1)		
				RTO11_0 (PPG10_0)		
				TIOA1_0		
				BIN0_0		
				MCSX6_0		
58	48	40	M3	P42	G	I
				SCK3_1 (SCL3_1)		
				RTO12_0 (PPG12_0)		
				TIOA2_0		
				ZIN0_0		
				MCSX5_0		

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQQ216	LQP176	LQS144	LBE192			
59	49	41	L4	P43	G	K
				SIN15_0		
				RTO13_0 (PPG12_0)		
				TIOA3_0		
				INT04_0		
MCSX4_0						
60	50	42	M4	P44	G	I
				SOT15_0 (SDA15_0)		
				RTO14_0 (PPG14_0)		
				TIOA4_0		
MCSX3_0						
61	51	43	N4	P45	G	I
				SCK15_0 (SCL15_0)		
				RTO15_0 (PPG14_0)		
				TIOA5_0		
MCSX2_0						
62	52	44	P2	C	-	-
63	53	45	P3	VSS	-	-
64	54	46	P4	VCC	-	-
65	-	-	-	P4A	E	K
				SIN12_1		
				AIN0_1		
INT04_2						
66	-	-	-	P4B	E	I
				SOT12_1 (SDA12_1)		
				BIN0_1		
67	-	-	-	P4C	E	I
				SCK12_1 (SCL12_1)		
				ZIN0_1		
68	-	-	-	P4D	E	K
				SCS72_1		
				INT05_2		
69	-	-	-	P4E	E	I
				SCS73_1		
70	55	47	L5	P7D	L	Q
				SCK1_1 (SCL1_1)		
				DTTI1X_0		
				INT05_0		
				WKUP2		
MCSX1_0						
71	56	48	M5	P7E	L	I
				ADTG_7		
				FRCK1_0		
				MCSX0_0		
72	57	49	N5	INITX	B	C
73	58	50	P5	P46	P	S
				X0A		
74	59	51	P6	P47	Q	T
				X1A		

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQQ216	LQP176	LQS144	LBE192			
75	60	52	P8	VBAT	-	-
76	61	53	N6	P48	O	U
				VREGCTL		
77	62	54	M6	P49	O	U
				VWAKEUP		
78	63	-	K5	PF0	E	K
				SCS63_0		
				FRCK1_1		
				TIOA15_1		
79	64	-	K6	INT22_1	E	K
				PF1		
				SCS62_0		
				TIOB15_1		
80	65	55	L6	INT23_1	I	K
				P70		
				ADTG_8		
				SIN1_1		
81	66	56	J6	INT06_0	E	I
				MRDY_0		
				P71		
				SOT1_1 (SDA1_1)		
82	67	57	L8	MAD00_0	E	K
				P72		
				SIN9_0		
				TIOB0_0		
83	68	58	K8	INT07_0	E	I
				MAD01_0		
				P73		
				SOT9_0 (SDA9_0)		
84	69	59	J8	TIOB1_0	E	I
				MAD02_0		
				P74		
				SCK9_0 (SCL9_0)		
85	70	-	N8	TIOB2_0	L	I
				MAD03_0		
				PF2		
86	71	-	M8	RTO10_1 (PPG10_1)	L	K
				TIOA6_1		
				MRASX_0		
				PF3		
86	71	-	M8	RTO11_1 (PPG10_1)	L	K
				TIOB6_1		
				INT05_1		
				MCASX_0		

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQQ216	LQP176	LQS144	LBE192			
87	72	-	N9	PF4	L	K
				RTO12_1 (PPG12_1)		
				TIOA7_1		
				INT06_1		
				MSDWEX_0		
88	73	-	P9	PF5	L	K
				RTO13_1 (PPG12_1)		
				TIOB7_1		
				INT07_1		
89	74	-	M9	MCSX8_0	L	K
				PF6		
				RTO14_1 (PPG14_1)		
				TIOA14_1		
				INT20_1		
90	75	-	L9	MSDCKE_0	L	K
				PF7		
				RTO15_1 (PPG14_1)		
				TIOB14_1		
				INT21_1		
91	76	60	K9	MSDCLK_0	E	K
				P75		
				SIN8_0		
				TIOB3_0		
				AIN1_0		
92	77	61	P10	INT20_0	E	I
				MAD04_0		
				P76		
				SOT8_0 (SDA8_0)		
				TIOB4_0		
93	78	62	N10	BIN1_0	E	I
				MAD05_0		
				P77		
				SCK8_0 (SCL8_0)		
				TIOB5_0		
94	-	-	-	ZIN1_0	E	I
				MAD06_0		
				PF8		
				SCS70_1		
95	-	-	-	DTT11X_1	E	I
				AIN1_1		
				PF9		
				SCS71_1		
96	79	63	L10	IC10_1	E	K
				BIN1_1		
				P78		
				SIN6_0		
				IC10_0		
				INT21_0		
				MAD07_0		

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQQ216	LQP176	LQS144	LBE192			
97	80	64	K10	P79	L	I
				SOT6_0 (SDA6_0)		
				IC11_0		
				MAD08_0		
98	81	65	M10	P7A	L	I
				SCK6_0 (SCL6_0)		
				IC12_0		
				MAD09_0		
99	82	66	N11	P7B	R	J
				DA1		
				SCS60_0		
				IC13_0		
100	83	67	M11	INT22_0	R	J
				P7C		
				DA0		
				SCS61_0		
101	-	-	-	INT04_1	E	I
				PFA		
				SCK7_1 (SCL7_1)		
				IC11_1		
102	-	-	-	ZIN1_1	E	K
				PFB		
				SOT7_1 (SDA7_1)		
				IC12_1		
103	-	-	-	INT07_2	E	K
				PFC		
				SIN7_1		
				IC13_1		
104	84	68	N13	INT06_2	C	E
				PE0		
105	85	69	N12	MD1	J	D
106	86	70	P12	MD0	A	A
				PE2		
107	87	71	P13	X0	A	B
				PE3		
108	88	72	N14	X1	-	-
109	89	73	M14	VSS	-	-
110	90	74	M13	VCC	-	-
111	91	75	M12	AVCC	-	-
112	92	76	L13	AVSS	-	-
113	93	77	L12	AVRL	-	-
114	94	78	L11	AVRH	F	M
				P10		
				AN00		
				SIN10_0		
				TIOA0_2		
AIN0_2						
				INT08_0		

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQQ216	LQP176	LQS144	LBE192			
115	95	79	K13	P11	F	L
				AN01		
				SOT10_0 (SDA10_0)		
				TIOB0_2		
				BIN0_2		
116	96	80	K12	P12	F	L
				AN02		
				SCK10_0 (SCL10_0)		
				TIOA1_2		
117	97	81	K14	ZIN0_2	F	M
				P13		
				AN03		
				SIN6_1		
118	98	82	K11	INT25_1	F	L
				P14		
				AN04		
				SOT6_1 (SDA6_1)		
119	-	-	-	PB8	E	O
				ADTG_6		
				SCS63_1		
				INT08_2		
				TRACED8		
120	-	-	-	PB9	E	O
				SIN9_1		
				AIN2_2		
				INT09_2		
121	-	-	-	TRACED9	E	N
				PBA		
				SOT9_1 (SDA9_1)		
				BIN2_2		
122	-	-	-	TRACED10	E	N
				PBB		
				SCK9_1 (SCL9_1)		
				ZIN2_2		
123	99	83	J13	TRACED11	F	M
				P15		
				AN05		
				SIN11_0		
				TIOB1_2		
124	100	84	J12	AIN1_2	F	L
				INT09_0		
				P16		
				AN06		
				SOT11_0 (SDA11_0)		
TIOA2_2						
				BIN1_2		



Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQQ216	LQP176	LQS144	LBE192			
125	101	85	J11	P17	F	L
				AN07		
				SCK11_0 (SCL11_0)		
				TIOB2_2		
				ZIN1_2		
126	102	-	J10	PB0	F	L
				AN16		
				SCK6_1 (SCL6_1)		
				TIOA9_1		
127	103	-	J9	PB1	F	M
				AN17		
				SCS60_1		
				TIOB9_1		
				INT08_1		
128	104	-	H10	PB2	F	M
				AN18		
				SCS61_1		
				TIOA10_1		
129	105	-	J14	PB3	F	L
				AN19		
				SCS62_1		
				TIOB10_1		
130	106	86	H9	P18	F	M
				AN08		
				SIN2_0		
				TIOA3_2		
131	107	87	H12	P19	F	O
				AN09		
				SOT2_0 (SDA2_0)		
				TIOB3_2		
				INT24_1		
				TRACECLK		
132	108	88	H14	P1A	F	N
				AN10		
				SCK2_0 (SCL2_0)		
				TIOA4_2		
				TRACED0		
133	109	89	G14	P1B	F	O
				AN11		
				SIN12_0		
				TIOB4_2		
				INT11_0		
134	110	90	H13	P1C	F	N
				AN12		
				SOT12_0 (SDA12_0)		
				TIOA5_2		
				TRACED2		

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQQ216	LQP176	LQS144	LBE192			
135	111	91	H11	P1D	F	N
				AN13		
				SCK12_0 (SCL12_0)		
				TIOB5_2		
				TRACED3		
136	-	-	-	VSS	-	-
137	-	-	-	VCC	-	-
138	112	-	G13	PB4	F	O
				AN20		
				SIN8_1		
				TIOA11_1		
				INT10_1		
				TRACED4		
139	113	-	F14	PB5	F	O
				AN21		
				SOT8_1 (SDA8_1)		
				TIOB11_1		
				INT11_1		
				TRACED5		
140	114	-	G12	PB6	F	N
				AN22		
				SCK8_1 (SCL8_1)		
				TIOA12_1		
				TRACED6		
141	115	-	G11	PB7	F	N
				AN23		
				TIOB12_1		
				TRACED7		
142	116	92	G10	P1E	F	M
				AN14		
				TIOA8_1		
				INT26_1		
				MAD10_0		
143	117	93	G9	P1F	F	M
				AN15		
				RTS5_0		
				TIOB8_1		
				INT27_1		
				MAD11_0		
144	118	94	F10	P2A	F	L
				AN24		
				CTS5_0		
				MAD12_0		
145	119	95	F11	P29	F	L
				AN25		
				SCK5_0 (SCL5_0)		
				MAD13_0		

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQQ216	LQP176	LQS144	LBE192			
146	120	96	F12	P28	F	L
				AN26		
				SOT5_0 (SDA5_0)		
				MAD14_0		
147	121	97	F13	P27	F	M
				AN27		
				SIN5_0		
				INT24_0		
148	-	-	-	PBC	E	N
				TRACED12		
149	-	-	-	PBD	E	O
				SCK0_1 (SCL0_1)		
				AIN3_2		
				INT10_2		
150	-	-	-	TRACED13	E	N
				PBE		
				SOT0_1 (SDA0_1)		
				BIN3_2		
151	-	-	-	TRACED14	E	O
				PBF		
				SIN0_1		
				ZIN3_2		
152	122	98	E10	INT11_2	E	I
				TRACED15		
				P26		
				MAD16_0		
153	123	99	E11	P25	F	M
				AN28		
				INT25_0		
				MAD17_0		
154	124	100	E12	P24	F	L
				AN29		
				TIOA13_1		
				MAD18_0		
155	125	101	E13	P23	F	L
				UHCONX1		
				AN30		
				SCK0_0 (SCL0_0)		
156	126	102	D12	TIOB13_1	F	M
				P22		
				AN31		
				SOT0_0 (SDA0_0)		
157	127	103	D13	INT26_0	I	K
				P21		
				ADTG_4		
				SIN0_0		
				INT27_0		
				CROUT_0		

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQQ216	LQP176	LQS144	LBE192			
158	128	104	C13	P20	I	F
				NMIX		
				WKUP0		
159	129	105	E14	USBVCC1	-	-
160	130	106	D14	P82	H	R
				UDM1		
161	131	107	C14	P83	H	R
				UDP1		
162	132	108	B14	VSS	-	-
163	133	109	A13	VCC	-	-
164	134	110	B13	P00	E	G
				TRSTX		
165	135	111	A12	P01	E	G
				TCK		
				SWCLK		
166	136	112	C12	P02	E	G
				TDI		
167	137	113	B12	P03	E	G
				TMS		
				SWDIO		
168	138	114	B11	P04	E	G
				TDO		
				SWO		
169	139	-	C11	P90	S	K
				INT12_1		
				Q_IO3_0		
170	140	-	D11	P91	S	K
				SIN5_1		
				INT13_1		
				Q_IO2_0		
171	141	-	B10	P92	S	K
				SOT5_1 (SDA5_1)		
				INT14_1		
				Q_IO1_0		
172	142	-	C10	P93	S	K
				SCK5_1 (SCL5_1)		
				INT15_1		
				Q_IO0_0		
173	143	-	D10	P94	S	I
				CTS5_1		
				Q_SCK_0		
174	144	-	B9	P95	S	I
				RTS5_1		
				Q_CS0_0		
175	-	-	-	P96	S	K
				INT12_2		
				Q_CS1_0		
176	-	-	-	P97	S	K
				INT13_2		
				Q_CS2_0		
177	145	115	C9	PC0	K	V

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQQ216	LQP176	LQS144	LBE192			
178	146	116	B8	PC1	K	V
				TIOB6_0		
179	147	117	D9	PC2	K	V
				TIOA6_0		
180	148	118	E9	PC3	K	V
				TIOB7_0		
181	149	119	F9	PC4	K	V
				TIOA7_0		
182	150	120	C8	PC5	K	V
				TIOB14_0		
183	151	121	D8	PC6	K	V
				TIOA14_0		
184	152	122	E8	PC7	E	W
				INT13_0		
				CROUT_1		
185	153	123	A10	PC8	K	V
186	154	124	F8	PC9	K	V
				TIOB15_0		
187	155	125	B7	PCA	K	V
				TIOA15_0		
188	156	126	A9	VCC	-	-
189	157	127	A8	VSS	-	-
190	158	128	A7	PCB	L	W
				INT28_0		
191	159	129	C7	PCC	K	V
192	160	130	A6	PCD	L	W
				SOT4_1 (SDA4_1)		
				INT14_0		
193	161	131	D7	PCE	L	W
				SIN4_1		
				INT15_0		
194	162	132	E7	PCF	L	W
				RTS4_1		
				INT12_0		
195	163	133	F7	PD0	L	W
				INT30_1		
196	164	134	B6	PD1	L	W
				INT31_1		
197	165	135	C6	PD2	L	V
				CTS4_1		
				FRCK2_1		
198	166	136	D6	P6E	E	W
				ADTG_5		
				SCK4_1 (SCL4_1)		
				IC23_1		
				INT29_0		

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQQ216	LQP176	LQS144	LBE192			
199	-	-	-	P6D	E	I
				SCK14_1 (SCL14_1)		
				IC22_1		
				TIOB6_2		
200	-	-	-	P6C	E	I
				SOT14_1 (SDA14_1)		
				IC21_1		
				TIOA6_2		
201	-	-	-	P6B	E	K
				SIN14_1		
				IC20_1		
				TIOB7_2		
202	-	-	-	P6A	E	I
				DTTI2X_1		
				TIOA7_2		
203	-	-	-	P69	E	I
				RTO20_1 (PPG20_1)		
				TIOB14_2		
204	-	-	-	P68	E	I
				SCK13_1 (SCL13_0)		
				RTO21_1 (PPG20_1)		
				TIOA14_2		
205	-	-	-	P67	E	I
				SOT13_1 (SDA13_1)		
				RTO22_1 (PPG22_1)		
				TIOB15_2		
206	-	-	-	P66	E	K
				SIN13_1		
				RTO23_1 (PPG22_1)		
				TIOA15_2		
207	167	-	E6	P65	E	K
				RTO24_1 (PPG24_1)		
				INT28_1		
208	168	-	B5	P64	I	K
				CTS4_0		
				RTO25_1 (PPG24_1)		
209	169	137	C5	P63	L	K
				ADTG_3		
				RTS4_0		
				INT30_0		
				MOEX_0		

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQQ216	LQP176	LQS144	LBE192			
210	170	138	B4	P62	L	I
				SCK4_0 (SCL4_0)		
				MWEX_0		
211	171	139	C4	P61	L	I
				UHCONX0		
				SOT4_0 (SDA4_0)		
				MALE_0		
				RTCCO_0 SUBOUT_0		
212	172	140	B3	P60	I	Q
				SIN4_0		
				INT31_0		
				WKUP3		
213	173	141	A4	USBVCC0	-	-
214	174	142	A3	P80	H	R
				UDM0		
215	175	143	A2	P81	H	R
				UDP0		
216	176	144	B1	VSS	-	-
-	-	-	E1		-	-
-	-	-	G1		-	-
-	-	-	P7		-	-
-	-	-	P11		-	-
-	-	-	L14		-	-
-	-	-	A11		-	-
-	-	-	A5		-	-
-	-	-	N7		-	-
-	-	-	M7		-	-
-	-	-	L7		-	-
-	-	-	K7		-	-
-	-	-	J7		-	-
--	-	-	G7		-	-
-	-	-	H7		-	-
-	-	-	H8		-	-
-	-	-	G8		-	-

**Signal Descriptions**

The number after the underscore ("\_") in pin names such as XXX\_1 and XXX\_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel.

Use the extended port function register (EPFR) to select the pin.

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
A/D converter	ADTG_0	A/D converter external trigger input pin	24	19	16	F6
	ADTG_1		32	23	20	G5
	ADTG_2		44	34	29	J3
	ADTG_3		209	169	137	C5
	ADTG_4		157	127	103	D13
	ADTG_5		198	166	136	D6
	ADTG_6		119	-	-	-
	ADTG_7		71	56	48	M5
	ADTG_8		80	65	55	L6
	AN00	A/D converter analog input pin. ANxx describes A/D converter ch xx.	114	94	78	L11
	AN01		115	95	79	K13
	AN02		116	96	80	K12
	AN03		117	97	81	K14
	AN04		118	98	82	K11
	AN05		123	99	83	J13
	AN06		124	100	84	J12
	AN07		125	101	85	J11
	AN08		130	106	86	H9
	AN09		131	107	87	H12
	AN10		132	108	88	H14
	AN11		133	109	89	G14
	AN12		134	110	90	H13
	AN13		135	111	91	H11
	AN14		142	116	92	G10
	AN15		143	117	93	G9
	AN16		126	102	-	J10
	AN17		127	103	-	J9
	AN18		128	104	-	H10
	AN19		129	105	-	J14
	AN20		138	112	-	G13
	AN21		139	113	-	F14
AN22	140		114	-	G12	
AN23	141		115	-	G11	
AN24	144		118	94	F10	
AN25	145		119	95	F11	
AN26	146		120	96	F12	
AN27	147		121	97	F13	
AN28	153		123	99	E11	
AN29	154		124	100	E12	
AN30	155		125	101	E13	
AN31	156	126	102	D12		



Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
Base Timer 0	TIOA0_0	Base Timer ch 0 TIOA pin	56	46	38	N2
	TIOA0_1		45	35	30	J2
	TIOA0_2		114	94	78	L11
	TIOB0_0	Base Timer ch 0 TIOB pin	82	67	57	L8
	TIOB0_1		21	-	-	-
	TIOB0_2		115	95	79	K13
Base Timer 1	TIOA1_0	Base Timer ch 1 TIOA pin	57	47	39	N3
	TIOA1_1		46	36	31	K1
	TIOA1_2		116	96	80	K12
	TIOB1_0	Base Timer ch 1 TIOB pin	83	68	58	K8
	TIOB1_1		22	-	-	-
	TIOB1_2		123	99	83	J13
Base Timer 2	TIOA2_0	Base Timer ch 2 TIOA pin	58	48	40	M3
	TIOA2_1		47	37	32	K2
	TIOA2_2		124	100	84	J12
	TIOB2_0	Base Timer ch 2 TIOB pin	84	69	59	J8
	TIOB2_1		26	-	-	-
	TIOB2_2		125	101	85	J11
Base Timer 3	TIOA3_0	Base Timer ch 3 TIOA pin	59	49	41	L4
	TIOA3_1		48	38	33	K3
	TIOA3_2		130	106	86	H9
	TIOB3_0	Base Timer ch 3 TIOB pin	91	76	60	K9
	TIOB3_1		27	-	-	-
	TIOB3_2		131	107	87	H12
Base Timer 4	TIOA4_0	Base Timer ch 4 TIOA pin	60	50	42	M4
	TIOA4_1		49	39	34	K4
	TIOA4_2		132	108	88	H14
	TIOB4_0	Base Timer ch 4 TIOB pin	92	77	61	P10
	TIOB4_1		28	-	-	-
	TIOB4_2		133	109	89	G14
Base Timer 5	TIOA5_0	Base Timer ch 5 TIOA pin	61	51	43	N4
	TIOA5_1		50	40	35	L1
	TIOA5_2		134	110	90	H13
	TIOB5_0	Base Timer ch 5 TIOB pin	93	78	62	N10
	TIOB5_1		29	-	-	-
	TIOB5_2		135	111	91	H11
Base Timer 6	TIOA6_0	Base Timer ch 6 TIOA pin	179	147	117	D9
	TIOA6_1		85	70	-	N8
	TIOA6_2		200	-	-	-
	TIOB6_0	Base Timer ch 6 TIOB pin	178	146	116	B8
	TIOB6_1		86	71	-	M8
	TIOB6_2		199	-	-	-

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
Base Timer 7	TIOA7_0	Base Timer ch 7 TIOA pin	181	149	119	F9
	TIOA7_1		87	72	-	N9
	TIOA7_2		202	-	-	-
	TIOB7_0	Base Timer ch 7 TIOB pin	180	148	118	E9
	TIOB7_1		88	73	-	P9
	TIOB7_2		201	-	-	-
Base Timer 8	TIOA8_0	Base Timer ch 8 TIOA pin	2	2	2	B2
	TIOA8_1		142	116	92	G10
	TIOA8_2		10	10	-	E2
	TIOB8_0	Base Timer ch 8 TIOB pin	18	17	14	F4
	TIOB8_1		143	117	93	G9
	TIOB8_2		11	11	-	E3
Base Timer 9	TIOA9_0	Base Timer ch 9 TIOA pin	3	3	3	C2
	TIOA9_1		126	102	-	J10
	TIOA9_2		12	12	-	E4
	TIOB9_0	Base Timer ch 9 TIOB pin	23	18	15	F5
	TIOB9_1		127	103	-	J9
	TIOB9_2		13	-	-	-
Base Timer 10	TIOA10_0	Base Timer ch 10 TIOA pin	4	4	4	C3
	TIOA10_1		128	104	-	H10
	TIOA10_2		19	-	-	-
	TIOB10_0	Base Timer ch 10 TIOB pin	24	19	16	F6
	TIOB10_1		129	105	-	J14
	TIOB10_2		20	-	-	-
Base Timer 11	TIOA11_0	Base Timer ch 11 $\emptyset$ TIOA pin	5	5	5	D5
	TIOA11_1		138	112	-	G13
	TIOA11_2		33	-	-	-
	TIOB11_0	Base Timer ch 11 TIOB pin	25	20	17	G2
	TIOB11_1		139	113	-	F14
	TIOB11_2		51	41	-	L2
Base Timer 12	TIOA12_0	Base Timer ch 12 TIOA pin	6	6	6	D2
	TIOA12_1		140	114	-	G12
	TIOA12_2		52	42	-	L3
	TIOB12_0	Base Timer ch 12 TIOB pin	30	21	18	G3
	TIOB12_1		141	115	-	G11
	TIOB12_2		53	43	-	M2

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
Base Timer 13	TIOA13_0	Base Timer ch 13 TIOA pin	7	7	7	D1
	TIOA13_1		154	124	100	E12
	TIOA13_2		34	24	-	G6
	TIOB13_0	Base Timer ch 13 TIOB pin	31	22	19	G4
	TIOB13_1		155	125	101	E13
	TIOB13_2		35	25	-	H4
Base Timer 14	TIOA14_0	Base Timer ch 14 TIOA pin	183	151	121	D8
	TIOA14_1		89	74	-	M9
	TIOA14_2		204	-	-	-
	TIOB14_0	Base Timer ch 14 TIOB pin	182	150	120	C8
	TIOB14_1		90	75	-	L9
	TIOB14_2		203	-	-	-
Base Timer 15	TIOA15_0	Base Timer ch 15 TIOA pin	187	155	125	B7
	TIOA15_1		78	63	-	K5
	TIOA15_2		206	-	-	-
	TIOB15_0	Base timer ch 15 TIOB pin	186	154	124	F8
	TIOB15_1		79	64	-	K6
	TIOB15_2		205	-	-	-
Debugger	SWCLK	Serial wire debug interface clock input pin	165	135	111	A12
	SWDIO	Serial wire debug interface data input/output pin	167	137	113	B12
	SWO	Serial wire viewer output pin	168	138	114	B11
	TCK	JTAG test clock input pin	165	135	111	A12
	TDI	JTAG test data input pin	166	136	112	C12
	TDO	JTAG debug data output pin	168	138	114	B11
	TMS	JTAG test mode state input/output pin	167	137	113	B12
	TRACECLK	Trace CLK output pin of ETM/HTM	131	107	87	H12
	TRACED0	Trace data output pin of ETM/ Trace data output pin of HTM	132	108	88	H14
	TRACED1		133	109	89	G14
	TRACED2		134	110	90	H13
	TRACED3		135	111	91	H11
	TRACED4	Trace data output pin of HTM	138	112	-	G13
	TRACED5		139	113	-	F14
	TRACED6		140	114	-	G12
	TRACED7		141	115	-	G11
	TRACED8		119	-	-	-
	TRACED9		120	-	-	-
TRACED10	121		-	-	-	
TRACED11	122		-	-	-	

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
Debugger	TRACED12	Trace data output pin of HTM	148	-	-	-
	TRACED13		149	-	-	-
	TRACED14		150	-	-	-
	TRACED15		151	-	-	-
	TRSTX	JTAG test reset Input pin	164	134	110	B13
External bus	MAD00_0	External bus interface address bus	81	66	56	J6
	MAD01_0		82	67	57	L8
	MAD02_0		83	68	58	K8
	MAD03_0		84	69	59	J8
	MAD04_0		91	76	60	K9
	MAD05_0		92	77	61	P10
	MAD06_0		93	78	62	N10
	MAD07_0		96	79	63	L10
	MAD08_0		97	80	64	K10
	MAD09_0		98	81	65	M10
	MAD10_0		142	116	92	G10
	MAD11_0		143	117	93	G9
	MAD12_0		144	118	94	F10
	MAD13_0		145	119	95	F11
	MAD14_0		146	120	96	F12
	MAD15_0		147	121	97	F13
	MAD16_0		152	122	98	E10
	MAD17_0		153	123	99	E11
	MAD18_0		154	124	100	E12
	MAD19_0		50	40	35	L1
	MAD20_0		49	39	34	K4
	MAD21_0		48	38	33	K3
	MAD22_0		47	37	32	K2
	MAD23_0		46	36	31	K1
	MAD24_0	45	35	30	J2	
	MCSX0_0	External bus interface chip select output pin	71	56	48	M5
	MCSX1_0		70	55	47	L5
	MCSX2_0		61	51	43	N4
	MCSX3_0		60	50	42	M4
	MCSX4_0		59	49	41	L4
	MCSX5_0		58	48	40	M3
	MCSX6_0		57	47	39	N3
MCSX7_0	56		46	38	N2	
MCSX8_0	88		73	-	P9	

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
External bus	MADATA00_0	External bus interface data bus (address/data multiplex bus)	2	2	2	B2
	MADATA01_0		3	3	3	C2
	MADATA02_0		4	4	4	C3
	MADATA03_0		5	5	5	D5
	MADATA04_0		6	6	6	D2
	MADATA05_0		7	7	7	D1
	MADATA06_0		8	8	8	D3
	MADATA07_0		9	9	9	D4
	MADATA08_0		14	13	10	E5
	MADATA09_0		15	14	11	F1
	MADATA10_0		16	15	12	F2
	MADATA11_0		17	16	13	F3
	MADATA12_0		18	17	14	F4
	MADATA13_0		23	18	15	F5
	MADATA14_0		24	19	16	F6
	MADATA15_0		25	20	17	G2
	MADATA16_0		10	-	-	-
	MADATA17_0		11	-	-	-
	MADATA18_0		12	-	-	-
	MADATA19_0		13	-	-	-
	MADATA20_0		19	-	-	-
	MADATA21_0		20	-	-	-
	MADATA22_0		21	-	-	-
	MADATA23_0		22	-	-	-
	MADATA24_0		26	-	-	-
	MADATA25_0	27	-	-	-	
	MADATA26_0	28	-	-	-	
	MADATA27_0	29	-	-	-	
	MADATA28_0	33	-	-	-	
	MADATA29_0	51	-	-	-	
	MADATA30_0	52	-	-	-	
	MADATA31_0	53	-	-	-	
	MDQM0_0	External bus interface byte mask signal output pin	30	21	18	G3
MDQM1_0	31		22	19	G4	
MDQM2_0	34		-	-	-	
MDQM3_0	35		-	-	-	
MALE_0	External bus interface address latch enable output signal for multiplex	211	171	139	C4	
MRDY_0	External bus interface external RDY input signal	80	65	55	L6	

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
External bus	MCLKOUT_0	External bus interface external clock output pin	32	23	20	G5
	MNALE_0	External bus interface ALE signal to control NAND flash output pin	47	37	32	K2
	MNCLE_0	External bus interface CLE signal to control NAND flash output pin	48	38	33	K3
	MNREX_0	External bus interface read enable signal to control NAND flash	50	40	35	L1
	MNWEX_0	External bus interface write enable signal to control NAND flash	49	39	34	K4
	MOEX_0	External bus interface read enable signal for SRAM	209	169	137	C5
	MWEX_0	External bus interface write enable signal for SRAM	210	170	138	B4
	MSDCLK_0	SDRAM interface SDRAM clock output pin	90	75	-	L9
	MSDCKE_0	SDRAM interface SDRAM clock enable pin	89	74	-	M9
	MRASX_0	SDRAM interface SDRAM column active strobe pin	85	70	-	N8
	MCASX_0	SDRAM interface SDRAM row active strobe pin	86	71	-	M8
	MSDWEX_0	SDRAM interface SDRAM write enable pin	87	72	-	N9
External interrupt	INT00_0	External interrupt request 00 input pin	2	2	2	B2
	INT00_1		38	28	23	H3
	INT00_2		19	-	-	-
	INT01_0	External interrupt request 01 input pin	7	7	7	D1
	INT01_1		41	31	26	H6
	INT01_2		51	41	-	L2
	INT02_0	External interrupt request 02 input pin	14	13	10	E5
	INT02_1		42	32	27	J5
	INT02_2		26	-	-	-
	INT03_0	External interrupt request 03 input pin	17	16	13	F3
	INT03_1		43	33	28	J4
	INT03_2		34	24	-	G6
	INT04_0	External interrupt request 04 input pin	59	49	41	L4
	INT04_1		100	83	67	M11
	INT04_2		65	-	-	-
	INT05_0	External interrupt request 05 input pin	70	55	47	L5
	INT05_1		86	71	-	M8
	INT05_2		68	-	-	-

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
External interrupt	INT06_0	External interrupt request 06 input pin	80	65	55	L6
	INT06_1		87	72	-	N9
	INT06_2		103	-	-	-
	INT07_0	External interrupt request 07 input pin	82	67	57	L8
	INT07_1		88	73	-	P9
	INT07_2		102	-	-	-
	INT08_0	External interrupt request 08 input pin	114	94	78	L11
	INT08_1		127	103	-	J9
	INT08_2		119	-	-	-
	INT09_0	External interrupt request 09 input pin	123	99	83	J13
	INT09_1		128	104	-	H10
	INT09_2		120	-	-	-
	INT10_0	External interrupt request 10 input pin	130	106	86	H9
	INT10_1		138	112	-	G13
	INT10_2		149	-	-	-
	INT11_0	External interrupt request 11 input pin	133	109	89	G14
	INT11_1		139	113	-	F14
	INT11_2		151	-	-	-
	INT12_0	External interrupt request 12 input pin	194	162	132	E7
	INT12_1		169	139	-	C11
	INT12_2		175	-	-	-
	INT13_0	External interrupt request 13 input pin	184	152	122	E8
	INT13_1		170	140	-	D11
	INT13_2		176	-	-	-
	INT14_0	External interrupt request 14 input pin	192	160	130	A6
	INT14_1		171	141	-	B10
	INT14_2		201	-	-	-
	INT15_0	External interrupt request 15 input pin	193	161	131	D7
	INT15_1		172	142	-	C10
	INT15_2		206	-	-	-
	INT16_0	External interrupt request 16 input pin	25	20	17	G2
	INT16_1		45	35	30	J2
	INT17_0	External interrupt request 17 input pin	30	21	18	G3
INT17_1	46		36	31	K1	
INT18_0	External interrupt request 18 input pin	31	22	19	G4	
INT18_1		47	37	32	K2	
INT19_0	External interrupt request 19 input pin	36	26	21	H2	
INT19_1		48	38	33	K3	

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
External interrupt	INT20_0	External interrupt request 20 input pin	91	76	60	K9
	INT20_1		89	74	-	M9
	INT21_0	External interrupt request 21 input pin	96	79	63	L10
	INT21_1		90	75	-	L9
	INT22_0	External interrupt request 22 input pin	99	82	66	N11
	INT22_1		78	63	-	K5
	INT23_0	External interrupt request 23 input pin	56	46	38	N2
	INT23_1		79	64	-	K6
	INT24_0	External interrupt request 24 input pin	147	121	97	F13
	INT24_1		131	107	87	H12
	INT25_0	External interrupt request 25 input pin	153	123	99	E11
	INT25_1		117	97	81	K14
	INT26_0	External interrupt request 26 input pin	156	126	102	D12
	INT26_1		142	116	92	G10
	INT27_0	External interrupt request 27 input pin	157	127	103	D13
	INT27_1		143	117	93	G9
	INT28_0	External interrupt request 28 input pin	190	158	128	A7
	INT28_1		207	167	-	E6
	INT29_0	External interrupt request 29 input pin	198	166	136	D6
	INT29_1		208	168	-	B5
	INT30_0	External interrupt request 30 input pin	209	169	137	C5
INT30_1	195		163	133	F7	
INT31_0	External interrupt request 31 input pin	212	172	140	B3	
INT31_1		196	164	134	B6	
NMIX	Non-maskable interrupt input pin	158	128	104	C13	



Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
GPIO	P00	General-purpose I/O port 0	164	134	110	B13
	P01		165	135	111	A12
	P02		166	136	112	C12
	P03		167	137	113	B12
	P04		168	138	114	B11
	P08		30	21	18	G3
	P09		31	22	19	G4
	P0A		32	23	20	G5
	P10		General-purpose I/O port 1	114	94	78
	P11	115		95	79	K13
	P12	116		96	80	K12
	P13	117		97	81	K14
	P14	118		98	82	K11
	P15	123		99	83	J13
	P16	124		100	84	J12
	P17	125		101	85	J11
	P18	130		106	86	H9
	P19	131		107	87	H12
	P1A	132		108	88	H14
	P1B	133		109	89	G14
	P1C	134		110	90	H13
	P1D	135		111	91	H11
	P1E	142		116	92	G10
	P1F	143	117	93	G9	
	P20	General-purpose I/O port 2	158	128	104	C13
	P21		157	127	103	D13
	P22		156	126	102	D12
	P23		155	125	101	E13
	P24		154	124	100	E12
	P25		153	123	99	E11
P26	152		122	98	E10	
P27	147		121	97	F13	
P28	146		120	96	F12	
P29	145		119	95	F11	
P2A	144		118	94	F10	

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
GPIO	P30	General-purpose I/O port 3	34	24	-	G6
	P31		35	25	-	H4
	P32		36	26	21	H2
	P33		37	27	22	J1
	P34		38	28	23	H3
	P35		41	31	26	H6
	P36		42	32	27	J5
	P37		43	33	28	J4
	P38		44	34	29	J3
	P39		45	35	30	J2
	P3A		46	36	31	K1
	P3B		47	37	32	K2
	P3C		48	38	33	K3
	P3D		49	39	34	K4
	P3E		50	40	35	L1
	P40	General-purpose I/O port 4	56	46	38	N2
	P41		57	47	39	N3
	P42		58	48	40	M3
	P43		59	49	41	L4
	P44		60	50	42	M4
	P45		61	51	43	N4
	P46		73	58	50	P5
	P47		74	59	51	P6
	P48		76	61	53	N6
	P49		77	62	54	M6
	P4A		65	-	-	-
	P4B		66	-	-	-
	P4C		67	-	-	-
	P4D		68	-	-	-
	P4E		69	-	-	-

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
GPIO	P50	General-purpose I/O port 5	10	10	-	E2
	P51		11	11	-	E3
	P52		12	12	-	E4
	P53		13	-	-	-
	P54		19	-	-	-
	P55		20	-	-	-
	P56		21	-	-	-
	P57		22	-	-	-
	P58		26	-	-	-
	P59		27	-	-	-
	P5A		28	-	-	-
	P5B		29	-	-	-
	P5C		33	-	-	-
	P5D		51	41	-	L2
	P5E		52	42	-	L3
	P5F		53	43	-	M2
	P60		General-purpose I/O port 6	212	172	140
	P61	211		171	139	C4
	P62	210		170	138	B4
	P63	209		169	137	C5
	P64	208		168	-	B5
	P65	207		167	-	E6
	P66	206		-	-	-
	P67	205		-	-	-
	P68	204		-	-	-
	P69	203		-	-	-
	P6A	202		-	-	-
	P6B	201		-	-	-
	P6C	200		-	-	-
	P6D	199	-	-	-	
P6E	198	166	136	D6		

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
GPIO	P70	General-purpose I/O port 7	80	65	55	L6
	P71		81	66	56	J6
	P72		82	67	57	L8
	P73		83	68	58	K8
	P74		84	69	59	J8
	P75		91	76	60	K9
	P76		92	77	61	P10
	P77		93	78	62	N10
	P78		96	79	63	L10
	P79		97	80	64	K10
	P7A		98	81	65	M10
	P7B		99	82	66	N11
	P7C		100	83	67	M11
	P7D		70	55	47	L5
	P7E	71	56	48	M5	
	P80	General-purpose I/O port 8	214	174	142	A3
	P81		215	175	143	A2
	P82		160	130	106	D14
	P83		161	131	107	C14
	P90	General-purpose I/O port 9	169	139	-	C11
	P91		170	140	-	D11
	P92		171	141	-	B10
	P93		172	142	-	C10
	P94		173	143	-	D10
	P95		174	144	-	B9
	P96		175	-	-	-
	P97		176	-	-	-

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
GPIO	PA0	General-purpose I/O port A	2	2	2	B2
	PA1		3	3	3	C2
	PA2		4	4	4	C3
	PA3		5	5	5	D5
	PA4		6	6	6	D2
	PA5		7	7	7	D1
	PA6		8	8	8	D3
	PA7		9	9	9	D4
	PA8		14	13	10	E5
	PA9		15	14	11	F1
	PAA		16	15	12	F2
	PAB		17	16	13	F3
	PAC		18	17	14	F4
	PAD		23	18	15	F5
	PAE		24	19	16	F6
	PAF		25	20	17	G2
	PB0		General-purpose I/O port B	126	102	-
	PB1	127		103	-	J9
	PB2	128		104	-	H10
	PB3	129		105	-	J14
	PB4	138		112	-	G13
	PB5	139		113	-	F14
	PB6	140		114	-	G12
	PB7	141		115	-	G11
	PB8	119		-	-	-
	PB9	120		-	-	-
	PBA	121		-	-	-
	PBB	122		-	-	-
	PBC	148		-	-	-
	PBD	149	-	-	-	
PBE	150	-	-	-		
PBF	151	-	-	-		

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
GPIO	PC0	General-purpose I/O port C	177	145	115	C9
	PC1		178	146	116	B8
	PC2		179	147	117	D9
	PC3		180	148	118	E9
	PC4		181	149	119	F9
	PC5		182	150	120	C8
	PC6		183	151	121	D8
	PC7		184	152	122	E8
	PC8		185	153	123	A10
	PC9		186	154	124	F8
	PCA		187	155	125	B7
	PCB		190	158	128	A7
	PCC		191	159	129	C7
	PCD		192	160	130	A6
	PCE		193	161	131	D7
	PCF		194	162	132	E7
	PD0	General-purpose I/O port D	195	163	133	F7
	PD1		196	164	134	B6
	PD2		197	165	135	C6
	PE0	General-purpose I/O port E	104	84	68	N13
	PE2		106	86	70	P12
	PE3		107	87	71	P13
	PF0	General-purpose I/O port F	78	63	-	K5
	PF1		79	64	-	K6
	PF2		85	70	-	N8
	PF3		86	71	-	M8
	PF4		87	72	-	N9
	PF5		88	73	-	P9
	PF6		89	74	-	M9
	PF7		90	75	-	L9
PF8	94		-	-	-	
PF9	95		-	-	-	
PFA	101		-	-	-	
PFB	102		-	-	-	
PFC	103		-	-	-	

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
Multi-Function Serial 0	SIN0_0	Multi-function serial interface ch 0 input pin	157	127	103	D13
	SIN0_1		151	-	-	-
	SOT0_0 (SDA0_0)	Multi-function serial interface ch 0 output pin	156	126	102	D12
	SOT0_1 (SDA0_1)	This pin operates as SOT0 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA0 when it is used in an I <sup>2</sup> C (operation mode 4).	150	-	-	-
	SCK0_0 (SCL0_0)	Multi-function serial interface ch 0 clock I/O pin. This pin operates as SCK0 when it is used in a CSIO (operation mode 2) and as SCL0 when it is used in an I <sup>2</sup> C (operation mode 4)	155	125	101	E13
	SCK0_1 (SCL0_1)		149	-	-	-
Multi-Function Serial 1	SIN1_0	Multi-function serial interface ch 1 input pin	7	7	7	D1
	SIN1_1		80	65	55	L6
	SOT1_0 (SDA1_0)	Multi-function serial interface ch 1 output pin.	8	8	8	D3
	SOT1_1 (SDA1_1)	This pin operates as SOT1 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA1 when it is used in an I <sup>2</sup> C (operation mode 4).	81	66	56	J6
	SCK1_0 (SCL1_0)	Multi-function serial interface ch 1 clock I/O pin.	9	9	9	D4
	SCK1_1 (SCL1_1)	This pin operates as SCK1 when it is used in a CSIO (operation mode 2) and as SCL1 when it is used in an I <sup>2</sup> C (operation mode 4).	70	55	47	L5
Multi-Function Serial 2	SIN2_0	Multi-function serial interface ch 2 input pin	130	106	86	H9
	SIN2_1		45	35	30	J2
	SOT2_0 (SDA2_0)	Multi-function serial interface ch 2 output pin.	131	107	87	H12
	SOT2_1 (SDA2_1)	This pin operates as SOT2 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA2 when it is used in an I <sup>2</sup> C (operation mode 4).	46	36	31	K1
	SCK2_0 (SCL2_0)	Multi-function serial interface ch 2 clock I/O pin.	132	108	88	H14
	SCK2_1 (SCL2_1)	This pin operates as SCK2 when it is used in a CSIO (operation mode 2) and as SCL2 when it is used in an I <sup>2</sup> C (operation mode 4).	47	37	32	K2

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
Multi-Function Serial 3	SIN3_0	Multi-function serial interface ch 3 input pin	25	20	17	G2
	SIN3_1		56	46	38	N2
	SOT3_0 (SDA3_0)	Multi-function serial interface ch 3 output pin.	24	19	16	F6
	SOT3_1 (SDA3_1)	This pin operates as SOT3 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA3 when it is used in an I <sup>2</sup> C (operation mode 4).	57	47	39	N3
	SCK3_0 (SCL3_0)	Multi-function serial interface ch 3 clock I/O pin.	23	18	15	F5
	SCK3_1 (SCL3_1)	This pin operates as SCK3 when it is used in a CSIO (operation modes 2) and as SCL3 when it is used in an I <sup>2</sup> C (operation mode 4).	58	48	40	M3
Multi-Function Serial 4	SIN4_0	Multi-function serial interface ch 4 input pin	212	172	140	B3
	SIN4_1		193	161	131	D7
	SOT4_0 (SDA4_0)	Multi-function serial interface ch 4 output pin.	211	171	139	C4
	SOT4_1 (SDA4_1)	This pin operates as SOT4 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA4 when it is used in an I <sup>2</sup> C (operation mode 4).	192	160	130	A6
	SCK4_0 (SCL4_0)	Multi-function serial interface ch 4 clock I/O pin.	210	170	138	B4
	SCK4_1 (SCL4_1)	This pin operates as SCK4 when it is used in a CSIO (operation mode 2) and as SCL4 when it is used in an I <sup>2</sup> C (operation mode 4).	198	166	136	D6
	CTS4_0	Multi-function serial interface ch 4 CTS input pin	208	168	-	B5
	CTS4_1		197	165	135	C6
	RTS4_0	Multi-function serial interface ch 4 RTS output pin	209	169	137	C5
	RTS4_1		194	162	132	E7



Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
Multi-Function Serial 5	SIN5_0	Multi-function serial interface ch 5 input pin	147	121	97	F13
	SIN5_1		170	140	-	D11
	SOT5_0 (SDA5_0)	Multi-function serial interface ch 5 output pin.	146	120	96	F12
	SOT5_1 (SDA5_1)	This pin operates as SOT5 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA5 when it is used in an I <sup>2</sup> C (operation mode 4).	171	141	-	B10
	SCK5_0 (SCL5_0)	Multi-function serial interface ch 5 clock I/O pin.	145	119	95	F11
	SCK5_1 (SCL5_1)	This pin operates as SCK5 when it is used in a CSIO (operation mode 2) and as SCL5 when it is used in an I <sup>2</sup> C (operation mode 4).	172	142	-	C10
	CTS5_0	Multi-function serial interface ch 5 CTS input pin	144	118	94	F10
	CTS5_1		173	143	-	D10
	RTS5_0	Multi-function serial interface ch 5 RTS output pin	143	117	93	G9
	RTS5_1		174	144	-	B9
Multi-Function Serial 6	SIN6_0	Multi-function serial interface ch 6 input pin	96	79	63	L10
	SIN6_1		117	97	81	K14
	SOT6_0 (SDA6_0)	Multi-function serial interface ch 6 output pin.	97	80	64	K10
	SOT6_1 (SDA6_1)	This pin operates as SOT6 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA6 when it is used in an I <sup>2</sup> C (operation mode 4).	118	98	82	K11
	SCK6_0 (SCL6_0)	Multi-function serial interface ch 6 clock I/O pin.	98	81	65	M10
	SCK6_1 (SCL6_1)	This pin operates as SCK6 when it is used in a CSIO (operation mode 2) and as SCL6 when it is used in an I <sup>2</sup> C (operation mode 4).	126	102	-	J10
	SCS60_0	Multi-function serial interface ch 6 chip select 0 input/output pin	99	82	66	N11
	SCS60_1		127	103	-	J9
	SCS61_0	Multi-function serial interface ch 6 chip select1 input/output pin	100	83	67	M11
	SCS61_1		128	104	-	H10
	SCS62_0	Multi-function serial interface ch 6 chip select2 input/output pin	79	64	-	K6
	SCS62_1		129	105	-	J14
	SCS63_0	Multi-function serial interface ch 6 chip select3 input/output pin	78	63	-	K5
	SCS63_1		119	-	-	-

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
Multi-Function Serial 7	SIN7_0	Multi-function serial interface ch 7 input pin	14	13	10	E5
	SIN7_1		103	-	-	-
	SOT7_0 (SDA7_0)	Multi-function serial interface ch 7 output pin.	15	14	11	F1
	SOT7_1 (SDA7_1)	This pin operates as SOT7 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA7 when it is used in an I <sup>2</sup> C (operation mode 4).	102	-	-	-
	SCK7_0 (SCL7_0)	Multi-function serial interface ch 7 clock I/O pin.	16	15	12	F2
	SCK7_1 (SCL7_1)	This pin operates as SCK7 when it is used in a CSIO (operation mode 2) and as SCL7 when it is used in an I <sup>2</sup> C (operation mode 4).	101	-	-	-
	SCS70_0	Multi-function serial interface ch 7 chip select 0 input/output pin	17	16	13	F3
	SCS70_1		94	-	-	-
	SCS71_0	Multi-function serial interface ch 7 chip select 1 input/output pin	18	17	14	F4
	SCS71_1		95	-	-	-
	SCS72_0	Multi-function serial interface ch 7 chip select 2 input/output pin	10	10	-	E2
	SCS72_1		68	-	-	-
	SCS73_0	Multi-function serial interface ch 7 chip select 3 input/output pin	11	11	-	E3
	SCS73_1		69	-	-	-
Multi-Function Serial 8	SIN8_0	Multi-function serial interface ch 8 input pin	91	76	60	K9
	SIN8_1		138	112	-	G13
	SOT8_0 (SDA8_0)	Multi-function serial interface ch 8 output pin.	92	77	61	P10
	SOT8_1 (SDA8_1)	This pin operates as SOT8 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA8 when it is used in an I <sup>2</sup> C (operation mode 4).	139	113	-	F14
	SCK8_0 (SCL8_0)	Multi-function serial interface ch 8 clock I/O pin.	93	78	62	N10
	SCK8_1 (SCL8_1)	This pin operates as SCK8 when it is used in a CSIO (operation mode 2) and as SCL8 when it is used in an I <sup>2</sup> C (operation mode 4).	140	114	-	G12

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
Multi-Function Serial 9	SIN9_0	Multi-function serial interface ch 9 input pin	82	67	57	L8
	SIN9_1		120	-	-	-
	SOT9_0 (SDA9_0)	Multi-function serial interface ch 9 output pin.	83	68	58	K8
	SOT9_1 (SDA9_1)	This pin operates as SOT9 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA9 when it is used in an I <sup>2</sup> C (operation mode 4).	121	-	-	-
	SCK9_0 (SCL9_0)	Multi-function serial interface ch 9 clock I/O pin.	84	69	59	J8
	SCK9_1 (SCL9_1)	This pin operates as SCK9 when it is used in a CSIO (operation mode 2) and as SCL9 when it is used in an I <sup>2</sup> C (operation mode 4).	122	-	-	-
Multi-Function Serial 10	SIN10_0	Multi-function serial interface ch 10 input pin	114	94	78	L11
	SIN10_1		51	41	-	L2
	SOT10_0 (SDA10_0)	Multi-function serial interface ch 10 output pin.	115	95	79	K13
	SOT10_1 (SDA10_1)	This pin operates as SOT10 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA10 when it is used in an I <sup>2</sup> C (operation mode 4).	52	42	-	L3
	SCK10_0 (SCL10_0)	Multi-function serial interface ch 10 clock I/O pin.	116	96	80	K12
	SCK10_1 (SCL10_1)	This pin operates as SCK10 when it is used in a CSIO (operation mode 2) and as SCL10 when it is used in an I <sup>2</sup> C (operation mode 4).	53	43	-	M2
Multi-Function Serial 11	SIN11_0	Multi-function serial interface ch 11 input pin	123	99	83	J13
	SIN11_1		26	-	-	-
	SOT11_0 (SDA11_0)	Multi-function serial interface ch 11 output pin.	124	100	84	J12
	SOT11_1 (SDA11_1)	This pin operates as SOT11 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA11 when it is used in an I <sup>2</sup> C (operation mode 4).	27	-	-	-
	SCK11_0 (SCL11_0)	Multi-function serial interface ch 11 clock I/O pin.	125	101	85	J11
	SCK11_1 (SCL11_1)	This pin operates as SCK11 when it is used in a CSIO (operation mode 2) and as SCL11 when it is used in an I <sup>2</sup> C (operation mode 4).	28	-	-	-

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
Multi-Function Serial 12	SIN12_0	Multi-function serial interface ch 12 input pin	133	109	89	G14
	SIN12_1		65	-	-	-
	SOT12_0 (SDA12_0)	Multi-function serial interface ch 12 output pin.	134	110	90	H13
	SOT12_1 (SDA12_1)	This pin operates as SOT12 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA12 when it is used in an I <sup>2</sup> C (operation mode 4).	66	-	-	-
	SCK12_0 (SCL12_0)	Multi-function serial interface ch 12 clock I/O pin.	135	111	91	H11
	SCK12_1 (SCL12_1)	This pin operates as SCK12 when it is used in a CSIO (operation mode 2) and as SCL12 when it is used in an I <sup>2</sup> C (operation mode 4).	67	-	-	-
Multi-Function Serial 13	SIN13_0	Multi-function serial interface ch 13 input pin	48	38	33	K3
	SIN13_1		206	-	-	-
	SOT13_0 (SDA13_0)	Multi-function serial interface ch 13 output pin.	49	39	34	K4
	SOT13_1 (SDA13_1)	This pin operates as SOT13 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA13 when it is used in an I <sup>2</sup> C (operation mode 4).	205	-	-	-
	SCK13_0 (SCL13_0)	Multi-function serial interface ch 13 clock I/O pin.	50	40	35	L1
	SCK13_1 (SCL13_1)	This pin operates as SCK13 when it is used in a CSIO (operation mode 2) and as SCL13 when it is used in an I <sup>2</sup> C (operation mode 4).	204	-	-	-
Multi-Function Serial 14	SIN14_0	Multi-function serial interface ch 14 input pin	30	21	18	G3
	SIN14_1		201	-	-	-
	SOT14_0 (SDA14_0)	Multi-function serial interface ch 14 output pin.	31	22	19	G4
	SOT14_1 (SDA14_1)	This pin operates as SOT14 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA14 when it is used in an I <sup>2</sup> C (operation mode 4).	200	-	-	-
	SCK14_0 (SCL14_0)	Multi-function serial interface ch 14 clock I/O pin.	32	23	20	G5
	SCK14_1 (SCL14_1)	This pin operates as SCK14 when it is used in a CSIO (operation mode 2) and as SCL14 when it is used in an I <sup>2</sup> C (operation mode 4).	199	-	-	-

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
Multi-Function Serial 15	SIN15_0	Multi-function serial interface ch 15 input pin	59	49	41	L4
	SIN15_1		19	-	-	-
	SOT15_0 (SDA15_0)	Multi-function serial interface ch 15 output pin.	60	50	42	M4
	SOT15_1 (SDA15_1)	This pin operates as SOT15 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA15 when it is used in an I <sup>2</sup> C (operation mode 4).	20	-	-	-
	SCK15_0 (SCL15_0)	Multi-function serial interface ch 15 clock I/O pin.	61	51	43	N4
	SCK15_1 (SCL15_1)	This pin operates as SCK15 when it is used in a CSIO (operation mode 2) and as SCL15 when it is used in an I <sup>2</sup> C (operation mode 4).	21	-	-	-

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
Multi-Function Timer 0	DTTIOX_0	Input signal controlling waveform generator outputs RTO00 to RTO05 of Multi-Function Timer 0.	44	34	29	J3
	DTTIOX_1		21	-	-	-
	FRCK0_0	16-bit free-run timer ch 0 external clock input pin	37	27	22	J1
	FRCK0_1		29	-	-	-
	IC00_0	16-bit input capture input pin of Multi-Function Timer 0. ICxx describes channel number.	43	33	28	J4
	IC00_1		22	-	-	-
	IC01_0		42	32	27	J5
	IC01_1		26	-	-	-
	IC02_0		41	31	26	H6
	IC02_1		27	-	-	-
	IC03_0		38	28	23	H3
	IC03_1		28	-	-	-
	RTO00_0 (PPG00_0)	Waveform generator output pin of Multi-Function Timer 0. This pin operates as PPG00 when it is used in PPG0 output modes.	45	35	30	J2
	RTO00_1 (PPG00_1)		10	10	-	E2
	RTO01_0 (PPG00_0)	Waveform generator output pin of Multi-Function Timer 0. This pin operates as PPG00 when it is used in PPG0 output modes.	46	36	31	K1
	RTO01_1 (PPG00_1)		11	11	-	E3
	RTO02_0 (PPG02_0)	Waveform generator output pin of Multi-Function Timer 0. This pin operates as PPG02 when it is used in PPG0 output modes.	47	37	32	K2
	RTO02_1 (PPG02_1)		12	12	-	E4
	RTO03_0 (PPG02_0)	Waveform generator output pin of Multi-Function Timer 0. This pin operates as PPG02 when it is used in PPG0 output modes.	48	38	33	K3
	RTO03_1 (PPG02_1)		13	-	-	-
RTO04_0 (PPG04_0)	Waveform generator output pin of Multi-Function Timer 0. This pin operates as PPG04 when it is used in PPG0 output modes.	49	39	34	K4	
RTO04_1 (PPG04_1)		19	-	-	-	
RTO05_0 (PPG04_0)	Waveform generator output pin of Multi-Function Timer 0. This pin operates as PPG04 when it is used in PPG0 output modes.	50	40	35	L1	
RTO05_1 (PPG04_1)		20	-	-	-	

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
Multi-Function Timer 1	DTTI1X_0	Input signal controlling waveform generator outputs RTO10 to RTO15 of Multi-Function Timer 1.	70	55	47	L5
	DTTI1X_1		94	-	-	-
	FRCK1_0	16-bit free-run timer ch 1 external clock input pin	71	56	48	M5
	FRCK1_1		78	63	-	K5
	IC10_0	16-bit input capture input pin of Multi-Function Timer 1. ICxx describes channel number.	96	79	63	L10
	IC10_1		95	-	-	-
	IC11_0		97	80	64	K10
	IC11_1		101	-	-	-
	IC12_0		98	81	65	M10
	IC12_1		102	-	-	-
	IC13_0		99	82	66	N11
	IC13_1		103	-	-	-
	RTO10_0 (PPG10_0)	Waveform generator output pin of Multi-Function Timer 1. This pin operates as PPG10 when it is used in PPG1 output modes.	56	46	38	N2
	RTO10_1 (PPG10_1)		85	70	-	N8
	RTO11_0 (PPG10_0)	Waveform generator output pin of Multi-Function Timer 1. This pin operates as PPG10 when it is used in PPG1 output modes.	57	47	39	N3
	RTO11_1 (PPG10_1)		86	71	-	M8
	RTO12_0 (PPG12_0)	Waveform generator output pin of Multi-Function Timer 1. This pin operates as PPG12 when it is used in PPG1 output modes.	58	48	40	M3
	RTO12_1 (PPG12_1)		87	72	-	N9
	RTO13_0 (PPG12_0)	Waveform generator output pin of Multi-Function Timer 1. This pin operates as PPG12 when it is used in PPG1 output modes.	59	49	41	L4
	RTO13_1 (PPG12_1)		88	73	-	P9
RTO14_0 (PPG14_0)	Waveform generator output pin of Multi-Function Timer 1. This pin operates as PPG14 when it is used in PPG1 output modes.	60	50	42	M4	
RTO14_1 (PPG14_1)		89	74	-	M9	
RTO15_0 (PPG14_0)	Waveform generator output pin of Multi-Function Timer 1. This pin operates as PPG14 when it is used in PPG1 output modes.	61	51	43	N4	
RTO15_1 (PPG14_1)		90	75	-	L9	

Module	Pin Name	Function	Pin Number				
			LQQ 216	LQP 176	LQS 144	LBE 192	
Multi-Function Timer 2	DTTI2X_0	Input signal controlling waveform generator outputs RTO20 to RTO25 of Multi-Function Timer 1.	8	8	8	D3	
	DTTI2X_1		202	-	-	-	
	FRCK2_0	16-bit free-run timer ch 2 external clock input pin	17	16	13	F3	
	FRCK2_1		197	165	135	C6	
	IC20_0	16-bit input capture input pin of Multi-Function Timer 2. ICxx describes channel number.	9	9	9	D4	
	IC20_1		201	-	-	-	
	IC21_0		14	13	10	E5	
	IC21_1		200	-	-	-	
	IC22_0		15	14	11	F1	
	IC22_1		199	-	-	-	
	IC23_0		16	15	12	F2	
	IC23_1		198	166	136	D6	
	RTO20_0 (PPG20_0)		Waveform generator output pin of Multi-Function Timer 2. This pin operates as PPG20 when it is used in PPG2 output modes.	2	2	2	B2
	RTO20_1 (PPG20_1)			203	-	-	-
	RTO21_0 (PPG20_0)	Waveform generator output pin of Multi-Function Timer 2. This pin operates as PPG20 when it is used in PPG2 output modes.	3	3	3	C2	
	RTO21_1 (PPG20_1)		204	-	-	-	
	RTO22_0 (PPG22_0)	Waveform generator output pin of Multi-Function Timer 2. This pin operates as PPG22 when it is used in PPG2 output modes.	4	4	4	C3	
	RTO22_1 (PPG22_1)		205	-	-	-	
	RTO23_0 (PPG22_0)	Waveform generator output pin of Multi-Function Timer 2. This pin operates as PPG22 when it is used in PPG2 output modes.	5	5	5	D5	
	RTO23_1 (PPG22_1)		206	-	-	-	
RTO24_0 (PPG24_0)	Waveform generator output pin of Multi-Function Timer 2. This pin operates as PPG24 when it is used in PPG2 output modes.	6	6	6	D2		
RTO24_1 (PPG24_1)		207	167	-	E6		
RTO25_0 (PPG24_0)	Waveform generator output pin of Multi-Function Timer 2. This pin operates as PPG24 when it is used in PPG2 output modes.	7	7	7	D1		
RTO25_1 (PPG24_1)		208	168	-	B5		



Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
Quadrature Position/ Revolution Counter 0	AIN0_0	QPRC ch 0 AIN input pin	56	46	38	N2
	AIN0_1		65	-	-	-
	AIN0_2		114	94	78	L11
	BIN0_0	QPRC ch 0 BIN input pin	57	47	39	N3
	BIN0_1		66	-	-	-
	BIN0_2		115	95	79	K13
	ZIN0_0	QPRC ch 0 ZIN input pin	58	48	40	M3
	ZIN0_1		67	-	-	-
	ZIN0_2		116	96	80	K12
Quadrature Position/ Revolution Counter 1	AIN1_0	QPRC ch 1 AIN input pin	91	76	60	K9
	AIN1_1		94	-	-	-
	AIN1_2		123	99	83	J13
	BIN1_0	QPRC ch 1 BIN input pin	92	77	61	P10
	BIN1_1		45	-	-	-
	BIN1_2		124	100	84	J12
	ZIN1_0	QPRC ch 1 ZIN input pin	93	78	62	N10
	ZIN1_1		101	-	-	-
ZIN1_2	125		101	85	J11	
Quadrature Position/ Revolution Counter 2	AIN2_0	QPRC ch 2 AIN input pin	2	2	2	B2
	AIN2_1		32	23	20	G5
	AIN2_2		120	-	-	-
	BIN2_0	QPRC ch 2 BIN input pin	3	3	3	C2
	BIN2_1		36	26	21	H2
	BIN2_2		121	-	-	-
	ZIN2_0	QPRC ch 2 ZIN input pin	4	4	4	C3
	ZIN2_1		37	27	22	J1
	ZIN2_2		122	-	-	-
Quadrature Position/ Revolution Counter 3	AIN3_0	QPRC ch 3 AIN input pin	18	17	14	F4
	AIN3_1		45	35	30	J2
	AIN3_2		149	-	-	-
	BIN3_0	QPRC ch 3 BIN input pin	23	18	15	F5
	BIN3_1		46	36	31	K1
	BIN3_2		150	-	-	-
	ZIN3_0	QPRC ch 3 ZIN input pin	24	19	16	F6
	ZIN3_1		47	37	32	K2
	ZIN3_2		151	-	-	-

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
Real-time clock	RTCCO_0	0.5 seconds pulse output pin of real-time clock	211	171	139	C4
	RTCCO_1		33	-	-	-
	SUBOUT_0	Sub-clock output pin	211	171	139	C4
	SUBOUT_1		33	-	-	-
USB0	UDM0	USB ch 0 device/host D – pin	214	174	142	A3
	UDP0	USB ch 0 device/host D + pin	215	175	143	A2
	UHCONX0	USB ch 0 external pull-up control pin	211	171	139	C4
USB1	UDM1	USB ch 1 device/host D – pin	160	130	106	D14
	UDP1	USB ch 1 device/host D + pin	161	131	107	C14
	UHCONX1	USB ch 1 external pull-up control pin	155	125	101	E13
Low power consumption mode	WKUP0	Deep standby mode return signal input pin 0	158	128	104	C13
	WKUP1	Deep standby mode return signal input pin 1	14	13	10	E5
	WKUP2	Deep standby mode return signal input pin 2	70	55	47	L5
	WKUP3	Deep standby mode return signal input pin 3	212	172	140	B3
D/A converter	DA0	D/A converter ch 0 analog output pin	100	83	67	M11
	DA1	D/A converter ch 1 analog output pin	99	82	66	N11
VBAT	VREGCTL	On-board regulator control pin	76	61	53	N6
	VWAKEUP	The return signal input pin from a hibernation state	77	62	54	M6
SD I/F	S_CLK_0	SD memory card interface SD memory card clock output pin	38	28	23	H3
	S_CMD_0	SD memory card interface SD memory card command output	41	31	26	H6
	S_DATA1_0	SD memory card interface SD memory card data bus	36	26	21	H2
	S_DATA0_0		37	27	22	J1
	S_DATA3_0		42	32	27	J5
	S_DATA2_0		43	33	28	J4
	S_CD_0	SD memory card interface SD memory card detection pin	45	35	30	J2
S_WP_0	SD memory card interface SD memory card write protection	44	34	29	J3	

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
I <sup>2</sup> S	I2SMCLK0_0	I <sup>2</sup> S external clock pin	51	41	-	L2
	I2SDO0_0	I <sup>2</sup> S serial transition data output pin	52	42	-	L3
	I2SWS0_0	I <sup>2</sup> S frame synchronization signal pin	53	43	-	M2
	I2SDI0_0	I <sup>2</sup> S serial received data input pin	34	24	-	G6
	I2SCK0_0	I <sup>2</sup> S bit clock pin	35	25	-	H4
High-speed quad SPI	Q_SCK_0	SPI clock output pin	173	143	-	D10
	Q_IO0_0	SPI data input/output pin	172	142	-	C10
	Q_IO1_0		171	141	-	B10
	Q_IO2_0		170	140	-	D11
	Q_IO3_0		169	139	-	C11
	Q_CS0_0	SPI chip select output pin	174	144	-	B9
	Q_CS1_0		175	-	-	-
	Q_CS2_0		176	-	-	-

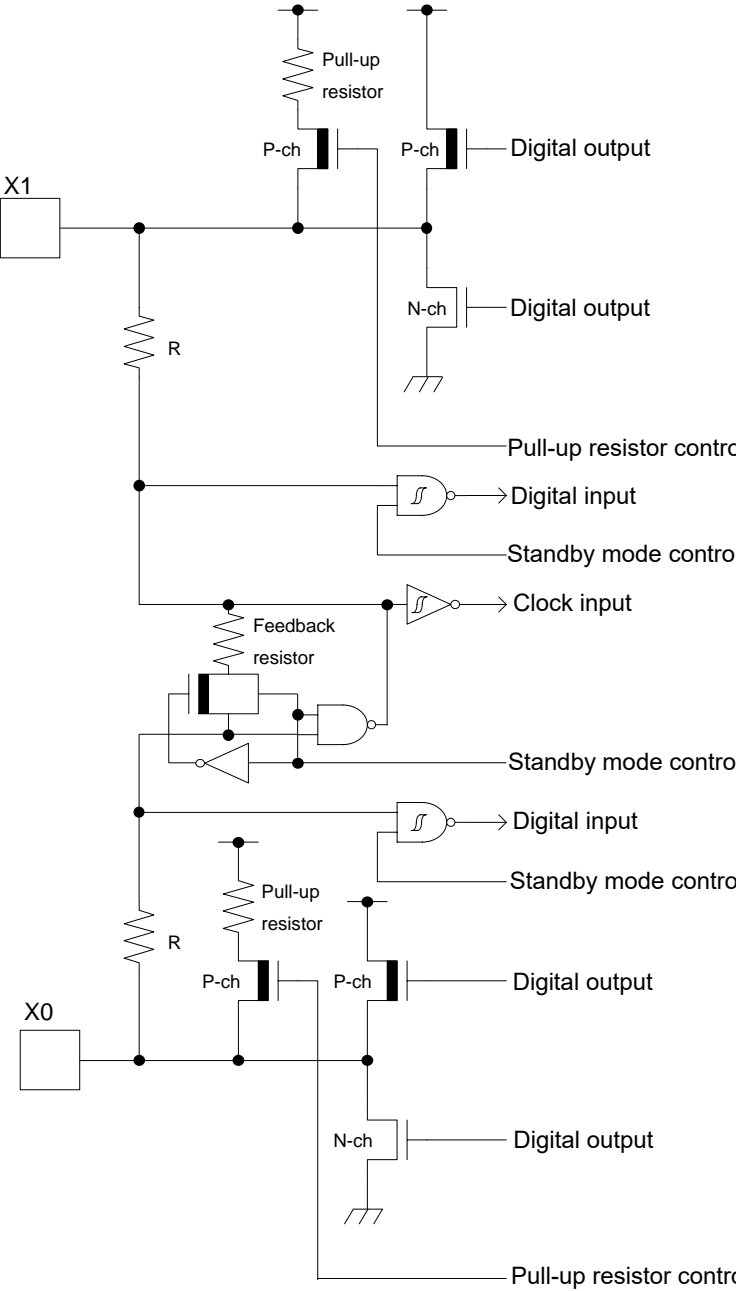
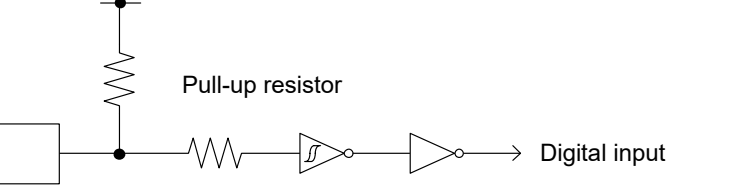
Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
Reset	INITX	External reset Input pin A reset is valid when INITX = L.	72	57	49	N5
Mode	MD1	Mode 1 pin During serial programming to flash memory, MD1 = L must be input.	104	84	68	N13
	MD0	Mode 0 pin During normal operation, MD0 = L must be input. During serial programming to flash memory, MD0 = H must be input.	105	85	69	N12
Power	VCC	Power supply pin	1	1	1	C1
			39	29	24	H1
			55	45	37	N1
			64	54	46	P4
			109	89	73	M14
			137	-	-	-
			163	133	109	A13
			188	156	126	A9
	USBVCC0	3.3 V power supply port for USB I/O	213	173	141	A4
USBVCC1	159		129	105	E14	
GND	VSS	GND pin	40	30	25	H5
			54	44	36	M1
			63	53	45	P3
			108	88	72	N14
			136	-	-	-
			162	132	108	B14
			189	157	127	A8
			216	176	144	B1
			-	-	-	E1
			-	-	-	G1
			-	-	-	P7
			-	-	-	P11
			-	-	-	L14
			-	-	-	A11
			-	-	-	A5
			-	-	-	N7
			-	-	-	M7
			-	-	-	K7
			-	-	-	J7
			-	-	-	G7
-	-	-	H7			
-	-	-	H8			
-	-	-	G8			

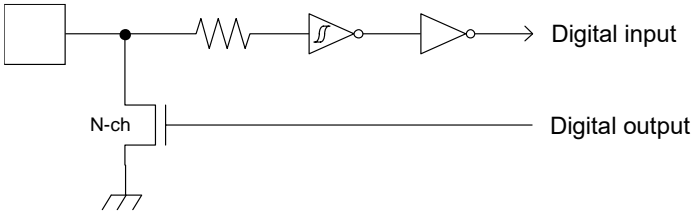
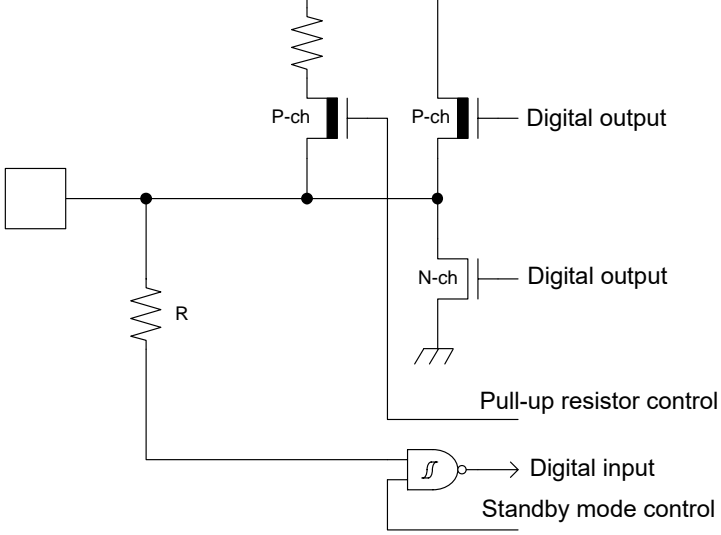
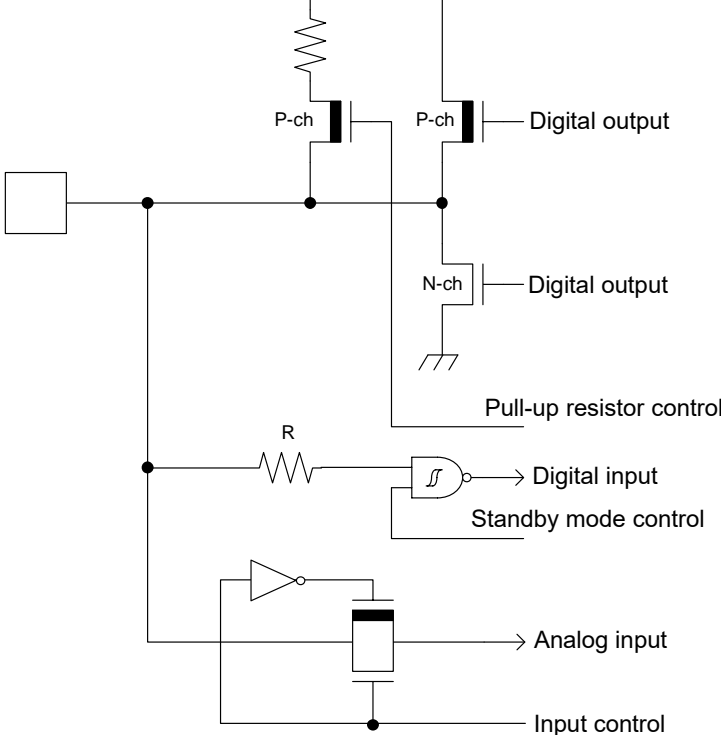
Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
Clock	X0	Main clock (oscillation) input pin	106	86	70	P12
	X1	Main clock (oscillation) I/O pin	107	87	71	P13
	X0A	Sub clock (oscillation) input pin	73	58	50	P5
	X1A	Sub clock (oscillation) I/O pin	74	59	51	P6
	CROUT_0	Built-in High-speed CR-oscillation clock output port	157	127	103	D13
	CROUT_1		184	152	122	E8
Analog Power	AVCC	A/D converter and D/A converter analog power-supply pin	110	90	74	M13
	AVRL	A/D converter analog reference voltage input pin	112	92	76	L13
	AVRH	A/D converter analog reference voltage input pin	113	93	77	L12
VBAT Power	VBAT	VBAT power supply pin Backup power supply (battery etc.) and system power supply	75	60	52	P8
Analog GND	AVSS	A/D converter and D/A converter GND pin	111	91	75	M12
C pin	C	Power supply stabilization capacity pin	62	52	44	P2

**Note:**

- While this device contains a Test Access Port (TAP) based on the IEEE 1149.1-2001 JTAG standard, it is not fully compliant to all requirements of that standard. This device may contain a 32-bit device ID that is the same as the 32-bit device ID in other devices with different functionality. The TAP pins may also be configurable for purposes other than access to the TAP controller.

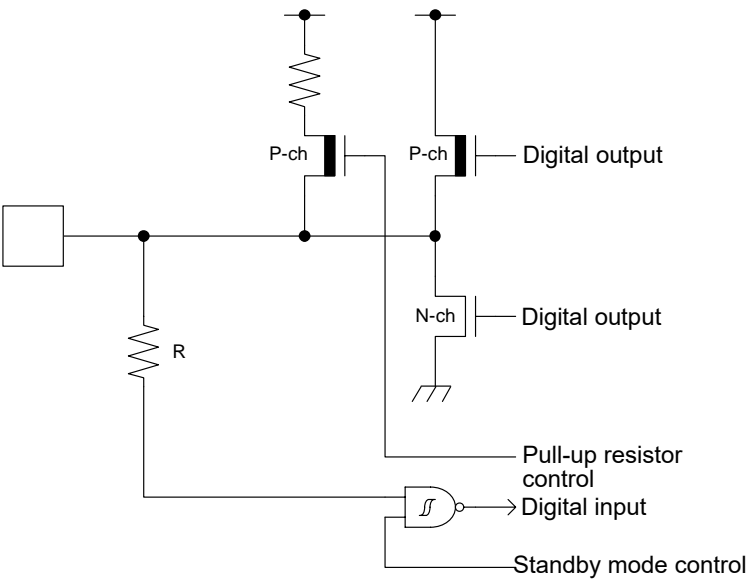
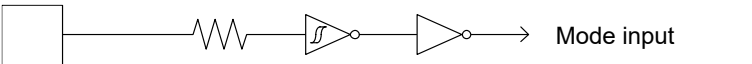
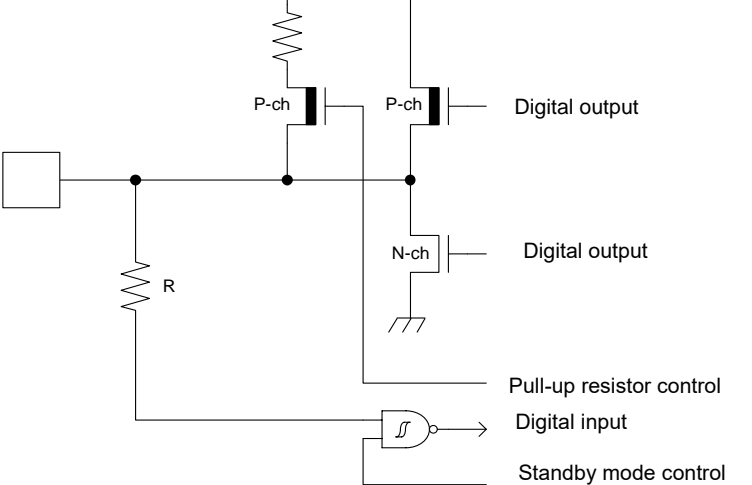
### 5. I/O Circuit Type

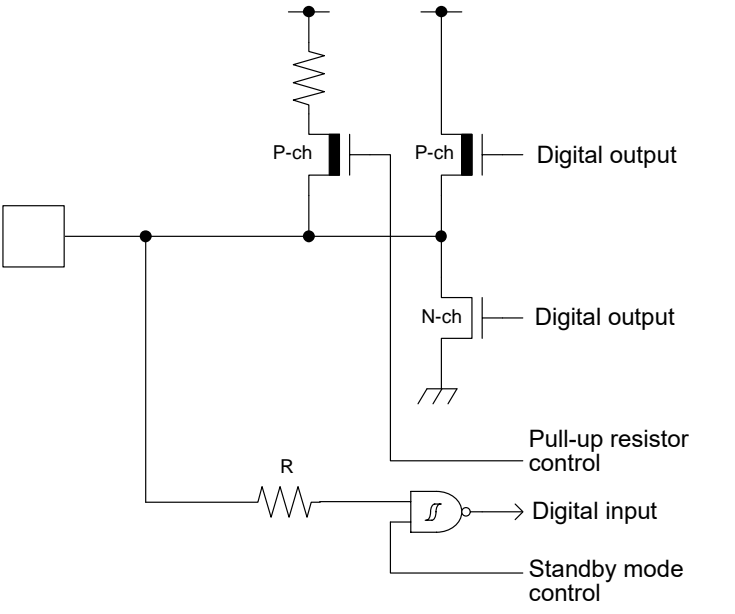
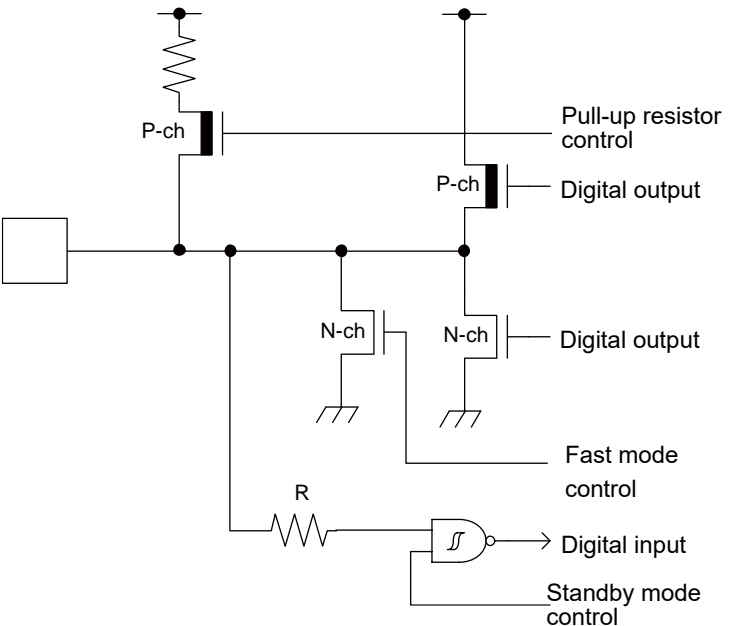
Type	Circuit	Remarks
A		<p>It is possible to select the main oscillation/GPIO function.</p> <p>When the main oscillation is selected:</p> <ul style="list-style-type: none"> <li>• Oscillation feedback resistor: approximately 1 MΩ</li> <li>• Standby mode control</li> </ul> <p>When the GPIO is selected:</p> <ul style="list-style-type: none"> <li>• CMOS level output.</li> <li>• CMOS level hysteresis input</li> <li>• Pull-up resistor control</li> <li>• Standby mode control</li> <li>• Pull-up resistor: approximately 50 kΩ</li> <li>• <math>I_{OH} = -4 \text{ mA}</math>, <math>I_{OL} = 4 \text{ mA}</math></li> </ul>
B		<ul style="list-style-type: none"> <li>• CMOS level hysteresis input</li> <li>• Pull-up resistor: approximately 50 kΩ</li> </ul>

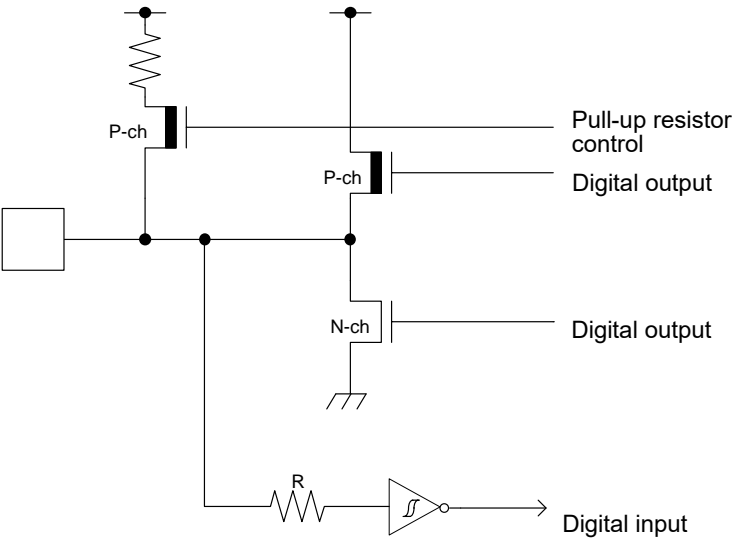
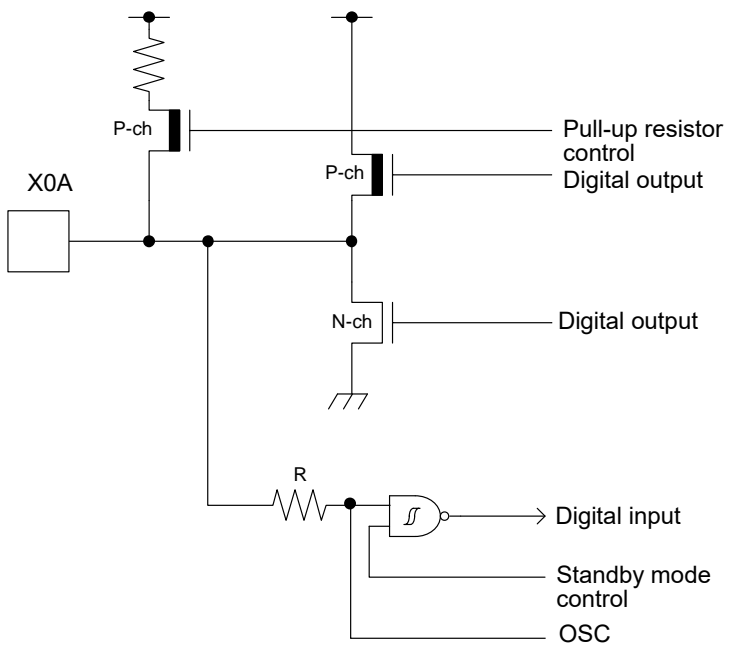
Type	Circuit	Remarks
C		<ul style="list-style-type: none"> <li>• Open drain output</li> <li>• CMOS level hysteresis input</li> </ul>
E		<ul style="list-style-type: none"> <li>• CMOS level output</li> <li>• CMOS level hysteresis input</li> <li>• Pull-up resistor control</li> <li>• Standby mode control</li> <li>• Pull-up resistor: approximately 50 kΩ</li> <li>• <math>I_{OH} = -4</math> mA, <math>I_{OL} = 4</math> mA</li> <li>• When this pin is used as an I<sup>2</sup>C pin, the digital output P-ch transistor is always off.</li> </ul>
F		<ul style="list-style-type: none"> <li>• CMOS level output</li> <li>• CMOS level hysteresis input</li> <li>• Input control</li> <li>• Analog input</li> <li>• Pull-up resistor control</li> <li>• Standby mode control</li> <li>• Pull-up resistor: approximately 50 kΩ</li> <li>• <math>I_{OH} = -4</math> mA, <math>I_{OL} = 4</math> mA</li> <li>• When this pin is used as an I<sup>2</sup>C pin, the digital output P-ch transistor is always off.</li> </ul>

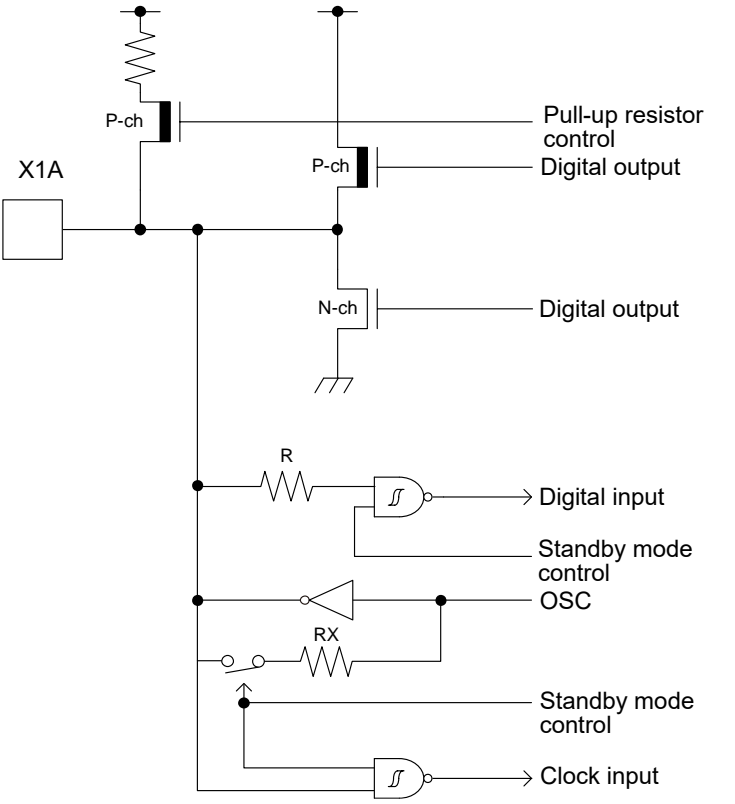
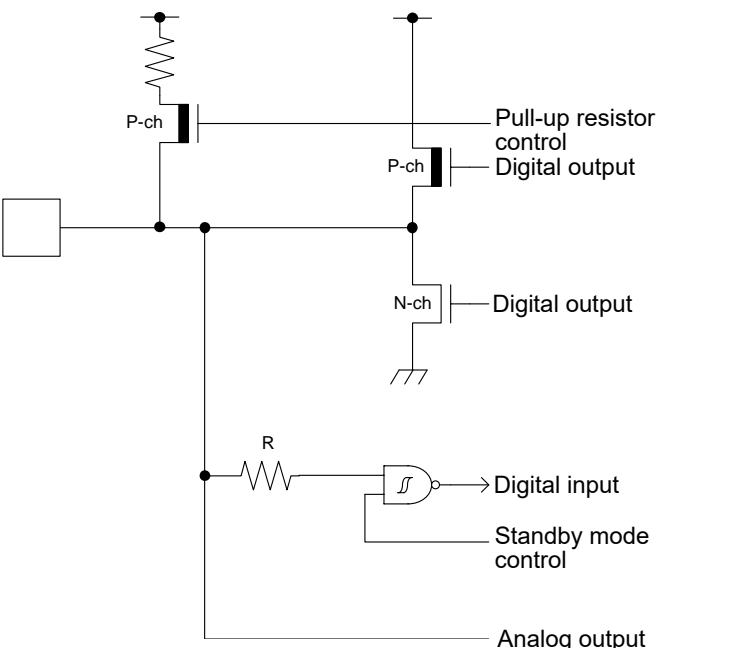
Type	Circuit	Remarks
G	<p>The diagram shows a pull-up resistor R connected to a node that branches into a P-ch transistor (Digital output) and an N-ch transistor (Digital output). A Digital input signal is connected to the node through an AND gate controlled by a Standby mode control signal. The N-ch transistor is controlled by a Pull-up resistor control signal.</p>	<ul style="list-style-type: none"> <li>• CMOS level output</li> <li>• CMOS level hysteresis input</li> <li>• Pull-up resistor control</li> <li>• Standby mode control</li> <li>• Pull-up resistor: approximately 50 kΩ</li> <li>• <math>I_{OH} = -12 \text{ mA}</math>, <math>I_{OL} = 12 \text{ mA}</math></li> <li>• When this pin is used as an I<sup>2</sup>C pin, the digital output P-ch transistor is always off.</li> </ul>
H	<p>The diagram shows a complex digital circuit with multiple inputs and outputs. It includes logic gates (AND, OR, NOT) and buffers. Labels include: GPIO Digital output, GPIO Digital input/output direction, GPIO Digital input, GPIO Digital input circuit control, UDP output, USB Full-speed/Low-speed control, UDP input, Differential input, USB/GPIO select, UDM input, UDM output, USB Digital input/output direction, GPIO Digital output, GPIO Digital input/output direction, GPIO Digital input, and GPIO Digital input circuit control. There are also two UDP/Pxx and two UDM/Pxx input blocks.</p>	<p>It is possible to select either USB I/O or GPIO function.</p> <p>When the USB I/O is selected:</p> <ul style="list-style-type: none"> <li>• Full-speed, low-speed control</li> </ul> <p>When the GPIO is selected:</p> <ul style="list-style-type: none"> <li>• CMOS level output</li> <li>• CMOS level hysteresis input</li> <li>• Standby mode control</li> <li>• <math>I_{OH} = -20.5 \text{ mA}</math>, <math>I_{OL} = 18.5 \text{ mA}</math></li> </ul>

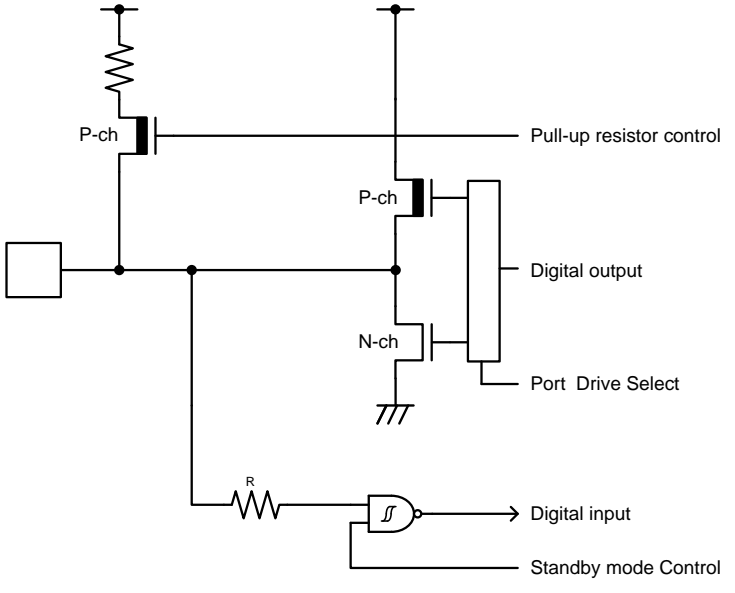


Type	Circuit	Remarks
I		<ul style="list-style-type: none"> <li>• CMOS level output</li> <li>• CMOS level hysteresis input</li> <li>• 5V tolerant</li> <li>• Pull-up resistor control</li> <li>• Standby mode control</li> <li>• Pull-up resistor: approximately 50 kΩ</li> <li>• <math>I_{OH} = -4 \text{ mA}</math>, <math>I_{OL} = 4 \text{ mA}</math></li> <li>• Available to control of PZR registers (pseudo-open drain control)</li> <li>• For PZR registers, refer to GPIO in the “FM4 Family Peripheral Manual Main Part (002-04856)”.</li> </ul>
J		<p>CMOS level hysteresis input</p>
K		<ul style="list-style-type: none"> <li>• CMOS level output</li> <li>• TTL level hysteresis input</li> <li>• Pull-up resistor control</li> <li>• Standby mode control</li> <li>• Pull-up resistor: approximately 50 kΩ</li> <li>• <math>I_{OH} = -4 \text{ mA}</math>, <math>I_{OL} = 4 \text{ mA}</math></li> </ul>

Type	Circuit	Remarks
L		<ul style="list-style-type: none"> <li>• CMOS level output</li> <li>• CMOS level hysteresis input</li> <li>• Pull-up resistor control</li> <li>• Standby mode control</li> <li>• Pull-up resistor: approximately 50 kΩ</li> <li>• <math>I_{OH} = -8 \text{ mA}</math>, <math>I_{OL} = 8 \text{ mA}</math></li> <li>• When this pin is used as an I<sup>2</sup>C pin, the digital output P-ch transistor is always off.</li> </ul>
N		<ul style="list-style-type: none"> <li>• CMOS level output</li> <li>• CMOS level hysteresis input</li> <li>• 5V tolerant</li> <li>• Pull-up resistor control</li> <li>• Standby mode control</li> <li>• Pull-up resistor: approximately 50 kΩ</li> <li>• <math>I_{OH} = -4 \text{ mA}</math>, <math>I_{OL} = 4 \text{ mA}</math> (GPIO)</li> <li>• <math>I_{OL} = 20 \text{ mA}</math> (Fast mode Plus)</li> <li>• Available to control of PZR register (pseudo-open drain control)</li> <li>• For PZR registers, refer to GPIO in the "FM4 Family Peripheral Manual Main Part (002-04856)".</li> <li>• When this pin is used as an I<sup>2</sup>C pin, the digital output P-ch transistor is always off.</li> </ul>

Type	Circuit	Remarks
O		<ul style="list-style-type: none"> <li>• CMOS level output</li> <li>• CMOS level hysteresis input</li> <li>• 5V tolerant</li> <li>• Pull-up resistor control</li> <li>• Pull-up resistor: approximately 50 kΩ</li> <li>• <math>I_{OH} = -4 \text{ mA}</math>, <math>I_{OL} = 4 \text{ mA}</math></li> <li>• Available to control of PZR register (pseudo-open drain control)</li> <li>• For PZR registers, refer to GPIO in the "FM4 Family Peripheral Manual Main Part (002-04856)".</li> <li>• For I/O setting, refer to VBAT Domain in the "FM4 Family Peripheral Manual Main Part (002-04856)."</li> </ul>
P		<ul style="list-style-type: none"> <li>• CMOS level output</li> <li>• CMOS level hysteresis input</li> <li>• Pull-up resistor control</li> <li>• Pull-up resistor: approximately 50 kΩ</li> <li>• <math>I_{OH} = -4 \text{ mA}</math>, <math>I_{OL} = 4 \text{ mA}</math></li> <li>• For I/O setting, refer to VBAT Domain in the "FM4 Family Peripheral Manual Main Part (002-04856)."</li> </ul>

Type	Circuit	Remarks
Q		<p>It is possible to select the sub oscillation/GPIO function.</p> <p>When the sub oscillation is selected:</p> <ul style="list-style-type: none"> <li>Oscillation feedback resistor: approximately 10 MΩ</li> </ul> <p>When the GPIO is selected:</p> <ul style="list-style-type: none"> <li>CMOS level output.</li> <li>CMOS level hysteresis input</li> <li>Pull-up resistor control</li> <li>Pull-up resistor: approximately 50 kΩ</li> <li><math>I_{OH} = -4 \text{ mA}</math>, <math>I_{OL} = 4 \text{ mA}</math></li> <li>For I/O setting, refer to VBAT Domain in the "FM4 Family Peripheral Manual Main Part (002-04856)."</li> </ul>
R		<ul style="list-style-type: none"> <li>CMOS level output</li> <li>CMOS level hysteresis input</li> <li>Analog output</li> <li>Pull-up resistor control</li> <li>Standby mode control</li> <li>Pull-up resistor: approximately 50 kΩ</li> <li><math>I_{OH} = -4 \text{ mA}</math>, <math>I_{OL} = 4 \text{ mA}</math> (4.5 V to 5.5 V)</li> <li><math>I_{OH} = -2 \text{ mA}</math>, <math>I_{OL} = 2 \text{ mA}</math> (2.7 V to 4.5 V)</li> </ul>

Type	Circuit	Remarks
S	 <p>The diagram shows a circuit for a digital pin. A pull-up resistor is connected to the supply rail and the output node. A P-channel MOSFET (P-ch) is connected between the supply rail and the output node, controlled by a 'Pull-up resistor control' signal. An N-channel MOSFET (N-ch) is connected between the output node and ground, controlled by a 'Port Drive Select' signal. The output node is labeled 'Digital output'. A 'Digital input' is connected to the output node through a resistor 'R'. A 'Standby mode Control' signal is connected to the input of an AND gate, which also has one input connected to the output node. The output of the AND gate is connected to the 'Standby mode Control' signal.</p>	<ul style="list-style-type: none"> <li>• CMOS level output</li> <li>• (It is possible to select by port drive capability. Select register [PDSR])</li> <li>• CMOS level hysteresis input</li> <li>• Pull-up resistor control</li> <li>• Standby mode control</li> <li>• Pull-up resistor: approximately 50 kΩ</li> <li>• <math>I_{OH} = -10 \text{ mA}</math>, <math>I_{OL} = 10 \text{ mA}</math> (PDSR = 1)</li> <li>• <math>I_{OH} = -4 \text{ mA}</math>, <math>I_{OL} = 4 \text{ mA}</math> (PDSR = 0)</li> <li>• When this pin is used as an I<sup>2</sup>C pin, the digital output P-ch transistor is always off.</li> </ul>

## 6. Handling Precautions

Every semiconductor device has a characteristic, inherent rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Cypress semiconductor devices.

### 6.1 Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

#### Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

#### Recommended Operating Conditions

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

#### Processing and Protection of Pins

These precautions must be followed when handling the pins that connect semiconductor devices to power supply and I/O functions.

1. Preventing Over-Voltage and Over-Current Conditions

Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.

2. Protection of Output Pins

Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions, if present for extended periods of time, can damage the device; therefore, avoid this type of connection.

3. Handling of Unused Input Pins

Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power-supply pin or ground pin.

### **Latch-Up**

Semiconductor devices are constructed by the formation of p-type and n-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic pnpn junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred milliamps to flow continuously at the power supply pin. This condition is called latch-up.

CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

1. Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.
2. Be sure that abnormal current flows do not occur during the power-on sequence.

### **Observance of Safety Regulations and Standards**

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

### **Fail-Safe Design**

As previously mentioned, all semiconductor devices have inherent rates of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

### **Precautions Related to Usage of Devices**

Cypress semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

## **6.2 Precautions for Package Mounting**

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Cypress's recommended conditions. For detailed information about mount conditions, contact your sales representative.

### **Lead Insertion Type**

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Cypress recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

### **Surface Mount Type**

Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. Cypress recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Cypress ranking of recommended conditions.

### **Lead-Free Packaging**

CAUTION: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

### **Storage of Semiconductor Devices**

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent this, do the following:

1. Avoid exposure to rapid temperature changes, which can cause moisture to condense inside the product. Store products in locations where temperature changes are slight.
2. Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5°C and 30°C.
3. When Dry Packages are opened, it is recommended to have humidity between 40% and 70%.
4. When necessary, Cypress packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in these aluminum laminate bags for storage.
5. Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

### **Baking**

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Cypress recommended conditions for baking.

Condition: 125 °C/24 h

### **Static Electricity**

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

1. Maintain relative humidity in the working environment between 40% and 70%. Use of an apparatus for ion generation may be needed to remove electricity.
2. Electrically ground all conveyors, solder vessels, soldering irons, and peripheral equipment.
3. Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ). Wearing of conductive clothing and shoes, and the use of conductive floor mats and other measures to minimize shock loads is recommended.
4. Ground all fixtures and instruments, or protect with anti-static measures.
5. Avoid the use of Styrofoam or other highly static-prone materials for storage of completed board assemblies.



### 6.3 Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

1. Humidity

Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.

2. Discharge of static electricity

When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.

3. Corrosive gases, dust, or oil

Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.

4. Radiation, including cosmic radiation

Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.

5. Smoke, flame

**CAUTION:** Plastic molded devices are flammable and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of Cypress products in other special environmental conditions should consult with sales representatives.

## 7. Handling Devices

### Power-Supply Pins

In products with multiple VCC and VSS pins, respective pins at the same potential are interconnected within the device in order to prevent malfunctions such as latch-up. All of these pins should be connected externally to the power supply or ground lines, however, in order to reduce electromagnetic emission levels, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating.

Be sure to connect the current-supply source with the power pins and GND pins of this device at low impedance. It is also advisable that a ceramic capacitor of approximately 0.1  $\mu\text{F}$  be connected as a bypass capacitor between VCC and VSS near this device.

A malfunction may occur when the power-supply voltage fluctuates rapidly even though the fluctuation is within the guaranteed operating range of the VCC power supply voltage. As a rule of voltage stabilization, suppress voltage fluctuation so that the fluctuation in VCC ripple (peak-to-peak value) at the commercial frequency (50 Hz/60 Hz) does not exceed 10% of the standard VCC value, and the transient fluctuation rate does not exceed 0.1 V/ $\mu\text{s}$  at a momentary fluctuation such as switching the power supply.

### Crystal Oscillator Circuit

Noise near the X0/X1 and X0A/X1A pins may cause the device to malfunction. Design the printed circuit board so that X0/X1, X0A/X1A pins, the crystal oscillator (or ceramic oscillator), and the bypass capacitor to ground are located as close to the device as possible.

It is strongly recommended that the PC board artwork be designed such that the X0/X1 and X0A/X1A pins are surrounded by ground plane, as this is expected to produce stable operation.

Evaluate the oscillation introduced by the use of the crystal oscillator by your mount board.

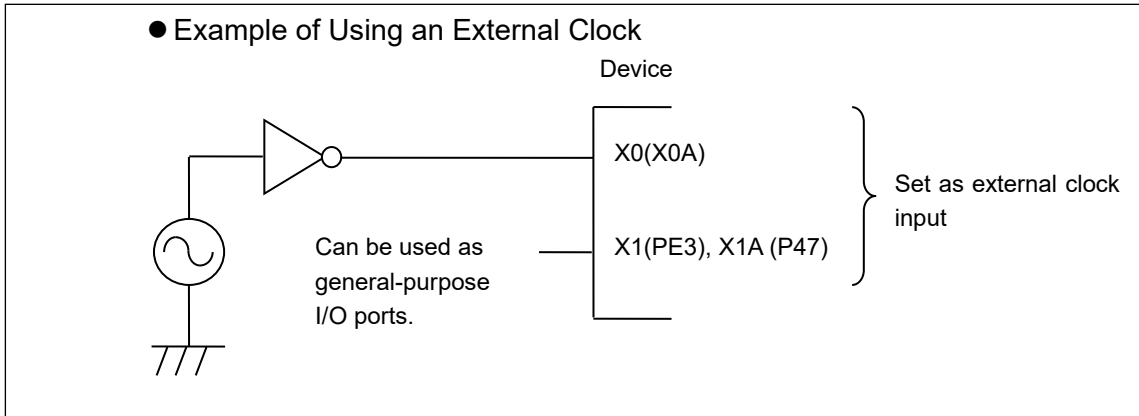
### Sub Crystal Oscillator

The sub-oscillator circuit for devices in this family is low gain to keep current consumption low. To stabilize the oscillation, Cypress recommends a crystal oscillator that meets the following conditions:

- Surface mount type
  - Size: More than 3.2 mm  $\times$  1.5 mm
  - Load capacitance: approximately 6 pF to 7 pF
- Lead type
  - Load capacitance: approximately 6 pF to 7 pF

### Using an External Clock

When using an external clock as an input of the main clock, set X0/X1 to the external clock input, and input the clock to X0. X1(PE3) can be used as a general-purpose I/O port. Similarly, when using an external clock as an input of the sub clock, set X0A/X1A to the external clock input and input the clock to X0A. X1A (P47) can be used as a general-purpose I/O port.

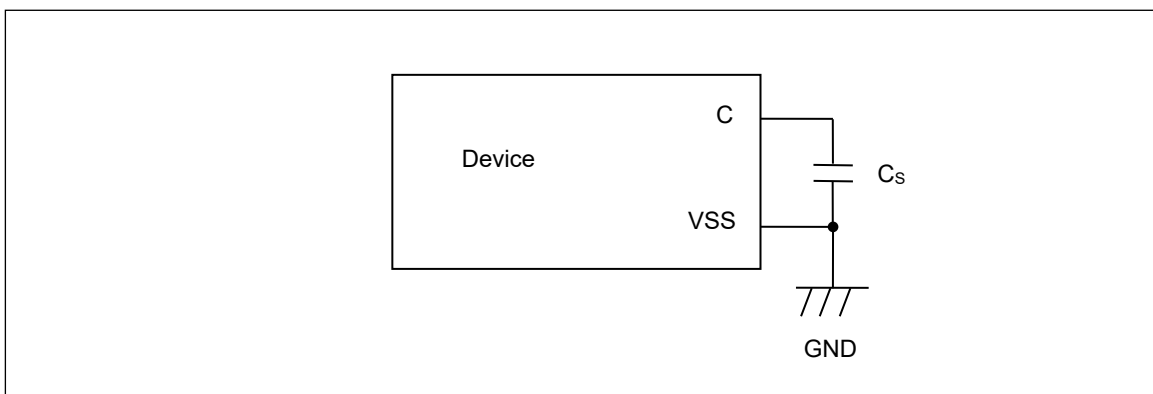


### Handling When Using Multi-Function Serial Pin as I<sup>2</sup>C Pin

If the application uses the multi-function serial pin as an I<sup>2</sup>C pin, the P-channel transistor of the digital output must be disabled. I<sup>2</sup>C pins need to conform to electrical limitations like other pins, however, and avoid connecting to live external systems with the MCU power off.

### C Pin

Devices in this series contain a regulator. Be sure to connect a smoothing capacitor ( $C_s$ ) for the regulator between the C pin and the GND pin. Please use a ceramic capacitor or a capacitor of equivalent frequency characteristics as a smoothing capacitor. Some laminated ceramic capacitors have a large capacitance variation due to thermal fluctuation. Please select a capacitor that meets the specifications in the operating conditions to use by evaluating the temperature characteristics of the device. A smoothing capacitor of about 4.7  $\mu\text{F}$  would be recommended for this series.



### Mode Pins (MD0)

Connect the MD pin (MD0) directly to VCC or VSS pins. Design the printed circuit board such that the pull-up/down resistance stays low, the distance between the mode pins and VCC pins or VSS pins is as short as possible, and the connection impedance is low when the pins are pulled up/down such as for switching the pin level and rewriting the flash memory data. This is important to prevent the device from erroneously switching to test mode as a result of noise.

### Notes on Power-on

Turn power on/off in the following order or at the same time. The device operates normally after all power on.

VBAT only Power-on is possible when VBAT and VCC turns Power-on and Hibernation control is setting and then VCC turns Power-off. About Hibernation control, see Chapter 7-2: VBAT Domain(B) in FM4 Family Peripheral Manual Main Part(002-04856).

Turning on: VBAT → VCC → USBVCC0  
VBAT → VCC → USBVCC1  
VCC → AVCC → AVRH  
Turning off: AVRH → AVCC → VCC  
USBVCC1 → VCC → VBAT  
USBVCC0 → VCC → VBAT

### Serial Communication

There is a possibility of receiving incorrect data as a result of noise or other issues introduced by the serial communication. Take care to design the printed circuit board to minimize noise.

Consider the case of introducing error as a result of noise, perform error detection such as by applying a checksum of data at the end. If an error is detected, retransmit the data.

### Differences in Characteristics within the Product Line

The electric characteristics including power consumption, ESD, latch-up, noise, and oscillation differ among members of the product line because chip layout and memory structures are not the same; for example, different sizes, flash versus ROM, etc. If you are switching to a different product of the same series, please make sure to evaluate the electric characteristics.

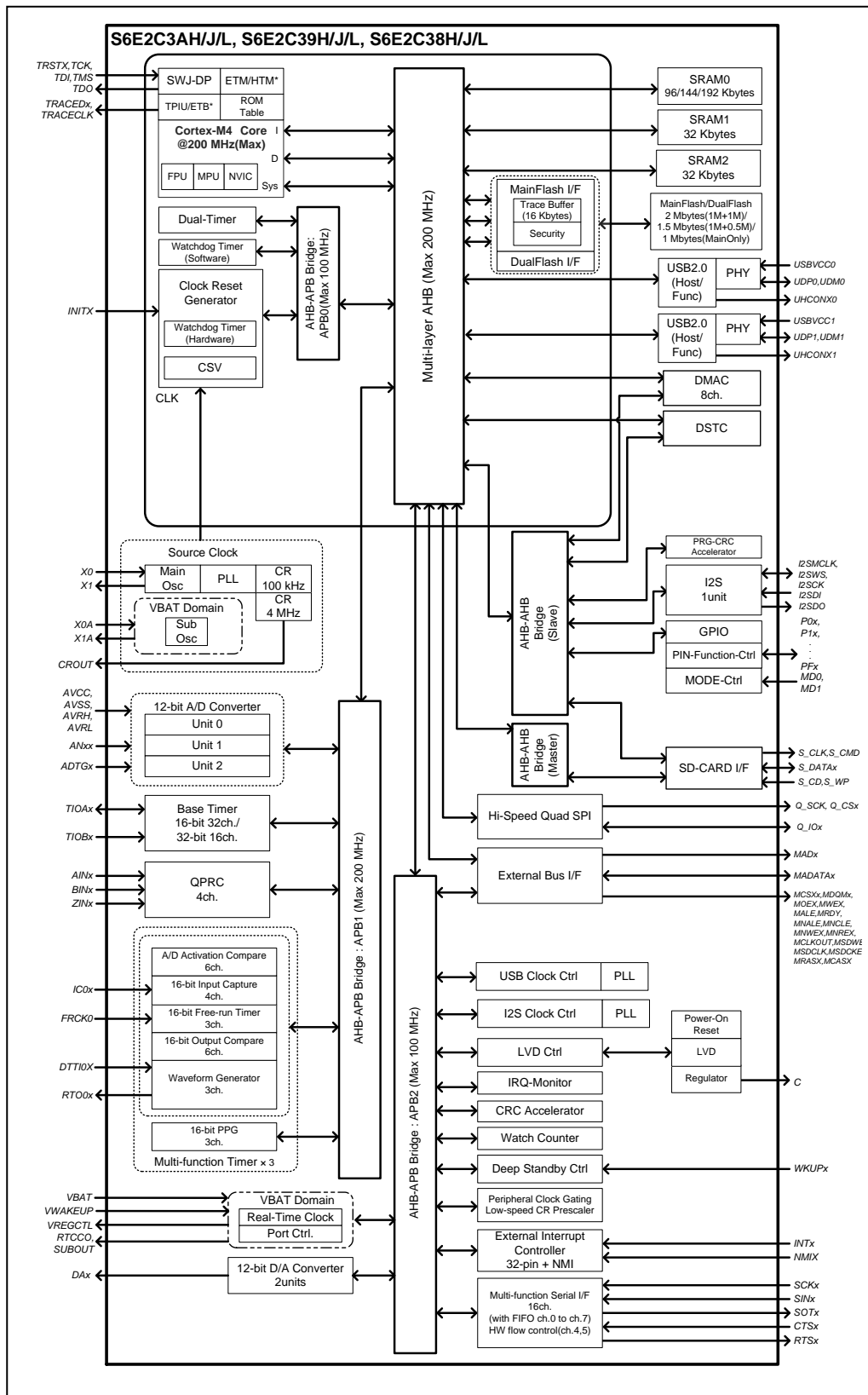
### Pull-Up Function of 5 V Tolerant I/O

Please do not input the signal more than VCC voltage at the time of Pull-Up function use of 5 V tolerant I/O.

### Pin Doubled as Debug Function

The pin doubled as TDO/TMS/TDI/TCK/TRSTX, SWO/SWDIO/SWCLK should be used as output only. Do not use as input.

### 8. Block Diagram

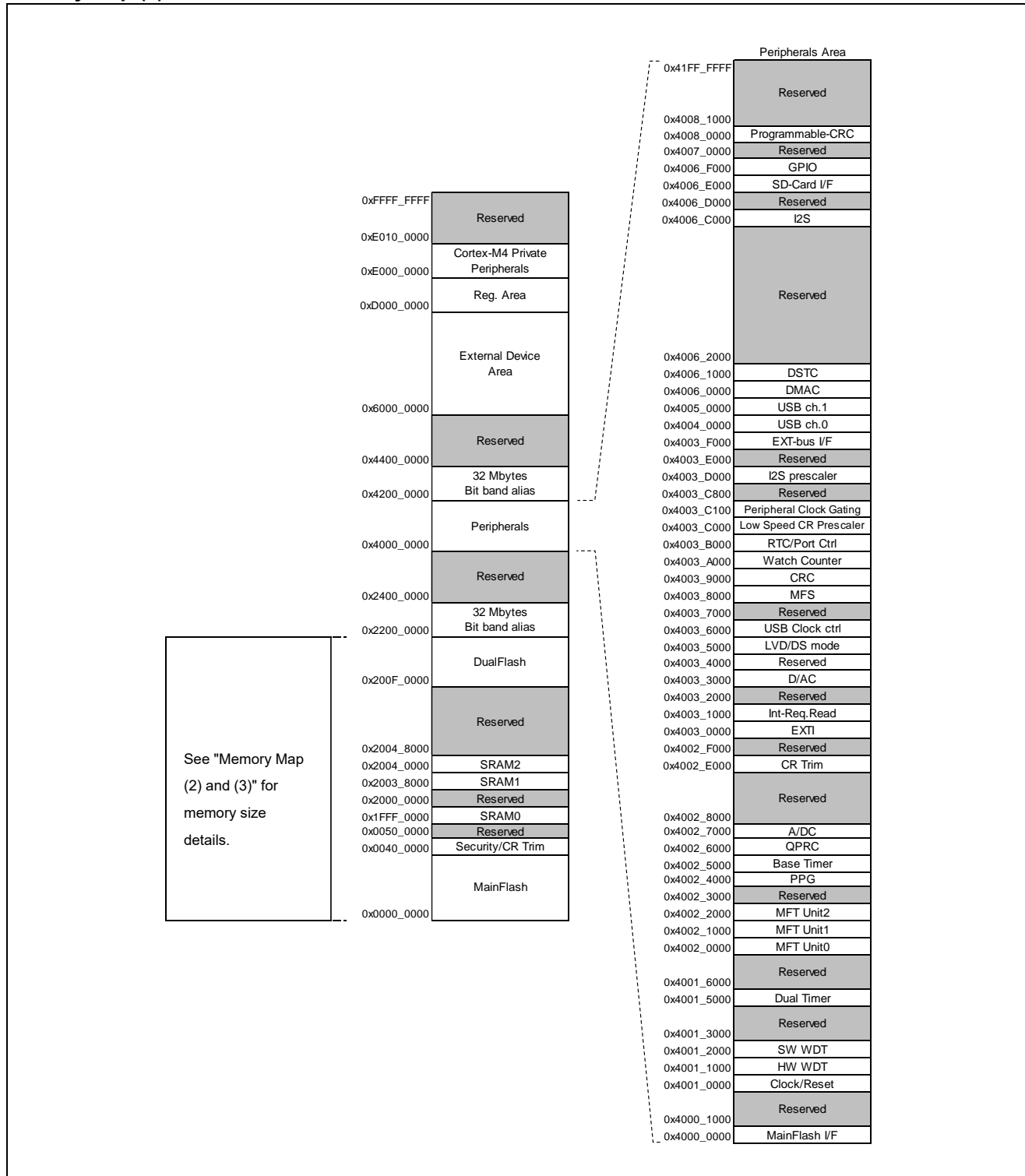


## 9. Memory Size

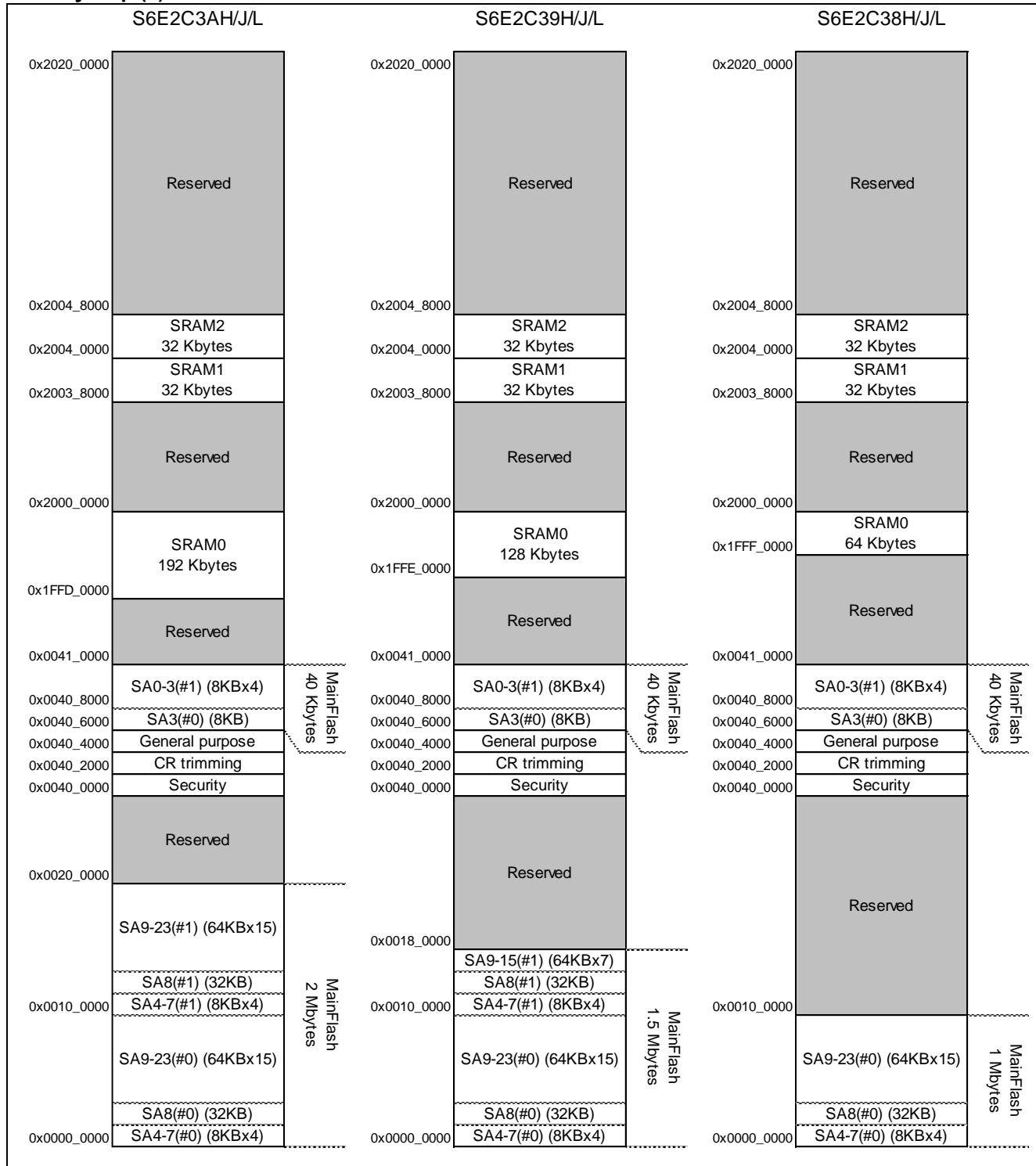
See Memory size in 1. Product Lineup to confirm the memory size.

## 10. Memory Map

### Memory Map (1)

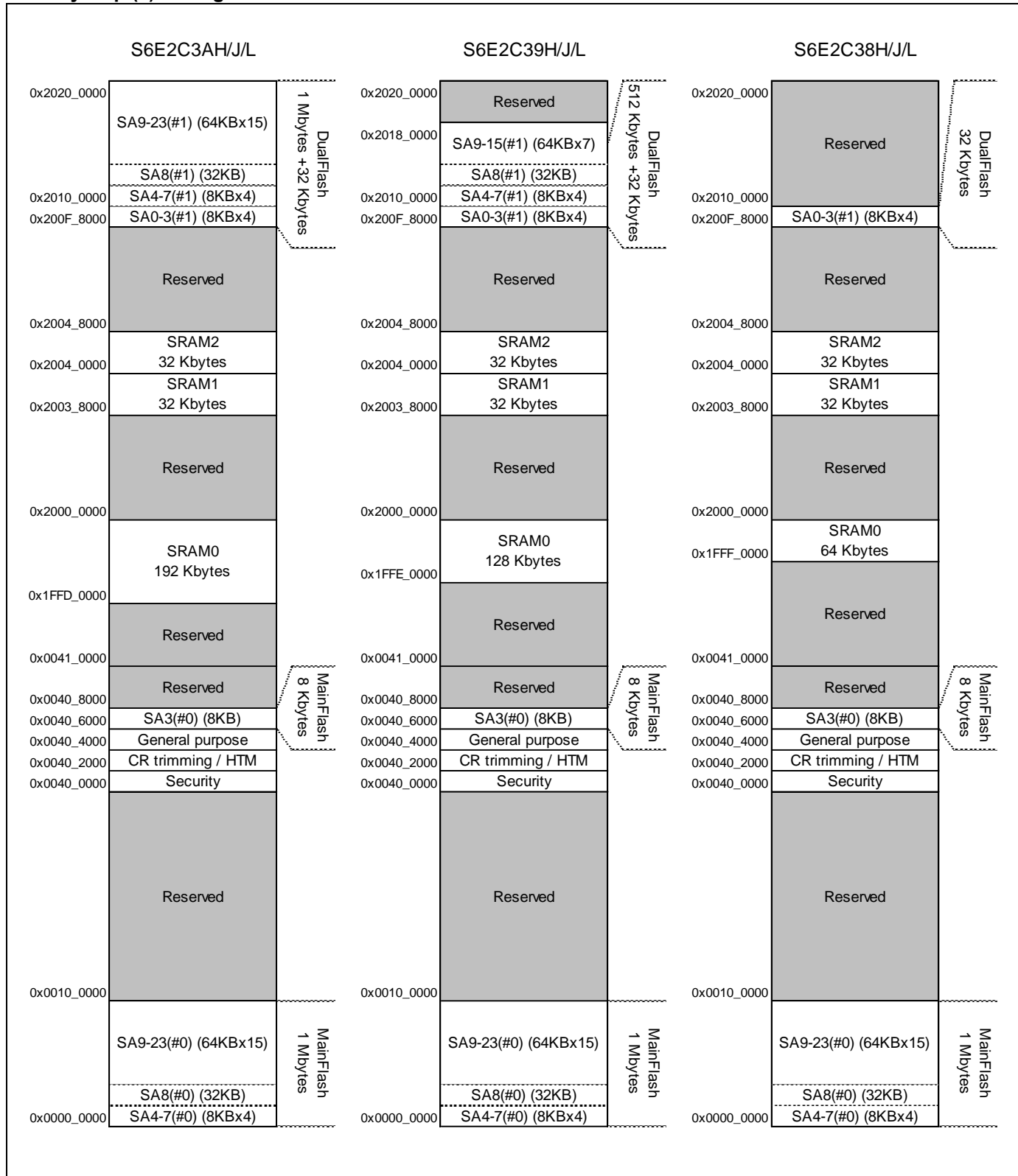


Memory Map (2)

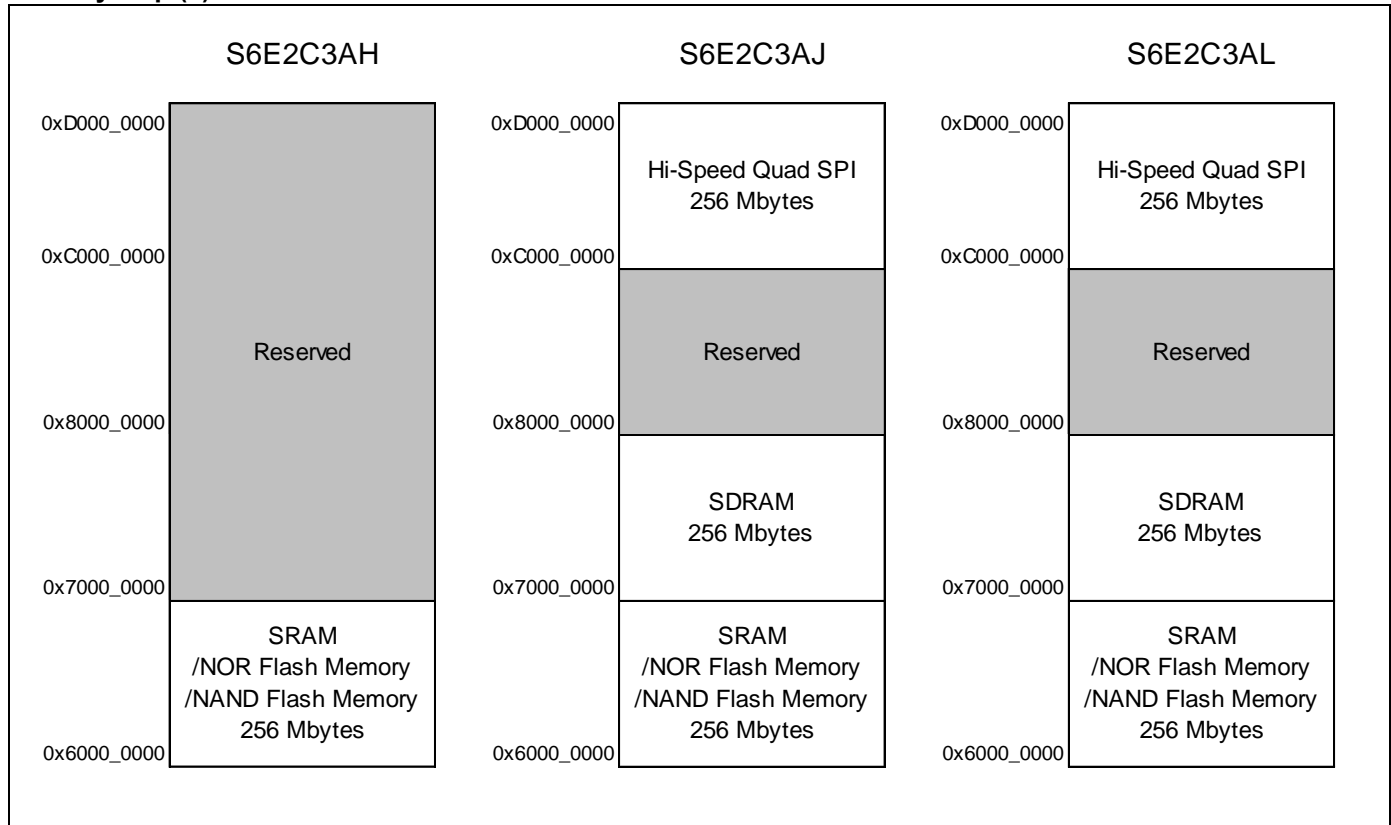


\*: See S6E2CC/S6E2C5/S6E2C4/S6E2C3/S6E2C2/S6E2C1 Series Flash Programming Manual to confirm the detail of flash Memory.

Memory Map (2) During Dual Flash Mode





**Memory Map (3)**


**Peripheral Address Map**

Start Address	End Address	Bus	Peripherals	
0x4000_0000	0x4000_0FFF	AHB	MainFlash I/F register	
0x4000_1000	0x4000_FFFF		Reserved	
0x4001_0000	0x4001_0FFF	APB0	Clock/reset control	
0x4001_1000	0x4001_1FFF		Hardware watchdog timer	
0x4001_2000	0x4001_2FFF		Software watchdog timer	
0x4001_3000	0x4001_4FFF		Reserved	
0x4001_5000	0x4001_5FFF		Dual-timer	
0x4001_6000	0x4001_FFFF		Reserved	
0x4002_0000	0x4002_0FFF		APB1	Multi-Function Timer unit 0
0x4002_1000	0x4002_1FFF	Multi-Function Timer unit 1		
0x4002_2000	0x4002_2FFF	Multi-Function Timer unit 2		
0x4002_3000	0x4002_3FFF	Reserved		
0x4002_4000	0x4002_4FFF	PPG		
0x4002_5000	0x4002_5FFF	Base timer		
0x4002_6000	0x4002_6FFF	Quadrature position/revolution counter		
0x4002_7000	0x4002_7FFF	A/D converter		
0x4002_8000	0x4002_DFFF	Reserved		
0x4002_E000	0x4002_EFFF	Internal CR trimming		
0x4002_F000	0x4002_FFFF	Reserved		
0x4003_0000	0x4003_0FFF	APB2		External interrupt controller
0x4003_1000	0x4003_1FFF			Interrupt request batch-read function
0x4003_2000	0x4003_2FFF			Reserved
0x4003_3000	0x4003_3FFF			D/A converter
0x4003_4000	0x4003_4FFF		Reserved	
0x4003_5000	0x4003_57FF		Low voltage detector	
0x4003_5800	0x4003_5FFF		Deep standby mode Controller	
0x4003_6000	0x4003_6FFF		USB clock generator	
0x4003_7000	0x4003_7FFF		Reserved	
0x4003_8000	0x4003_8FFF		Multi-function serial interface	
0x4003_9000	0x4003_9FFF		CRC	
0x4003_A000	0x4003_AFFF		Watch counter	
0x4003_B000	0x4003_BFFF		RTC/port control	
0x4003_C000	0x4003_C0FF		Low-speed CR prescaler	
0x4003_C100	0x4003_C7FF		Peripheral clock gating	
0x4003_C800	0x4003_CFFF		Reserved	
0x4003_D000	0x4003_DFFF		I <sup>2</sup> S prescaler	
0x4003_E000	0x4003_EFFF		Reserved	
0x4003_F000	0x4003_FFFF		External memory interface	
0x4004_0000	0x4004_FFFF		AHB	USB ch 0
0x4005_0000	0x4005_FFFF			USB ch 1
0x4006_0000	0x4006_0FFF			DMAC register
0x4006_1000	0x4006_1FFF			DSTC register
0x4006_2000	0x4006_BFFF	Reserved		
0x4006_C000	0x4006_CFFF	I <sup>2</sup> S		
0x4006_D000	0x4006_DFFF	Reserved		
0x4006_E000	0x4006_EFFF	SD card I/F		
0x4006_F000	0x4006_FFFF	GPIO		
0x4007_0000	0x4007_FFFF	Reserved		
0x4008_0000	0x4008_0FFF	Programmable-CRC		
0x4008_1000	0x41FF_FFFF	Reserved		
0x200E_0000	0x200E_FFFF	Workflash I/F register		
0xD000_0000	0xDFFF_FFFF	High-speed quad SPI control register		

## 11. Pin Status in Each CPU State

The terms used for pin status have the following meanings:

■ **INITX = 0**

This is the period when the INITX pin is at the L level.

■ **INITX = 1**

This is the period when the INITX pin is at the H level.

■ **SPL = 0**

This is the status that the standby pin level setting bit (SPL) in the standby mode control register (STB\_CTL) is set to 0.

■ **SPL = 1**

This is the status that the standby pin level setting bit (SPL) in the standby mode control register (STB\_CTL) is set to 1.

■ **Input enabled**

Indicates that the input function can be used.

■ **Internal input fixed at 0**

This is the status that the input function cannot be used. Internal input is fixed at L.

■ **Hi-Z**

Indicates that the pin drive transistor is disabled and the pin is put in the Hi-Z state.

■ **Setting disabled**

Indicates that the setting is disabled.

■ **Maintain previous state**

Maintains the state that was immediately prior to entering the current mode.  
If a built-in peripheral function is operating, the output follows the peripheral function.  
If the pin is being used as a port, that output is maintained.

■ **Analog input is enabled**

Indicates that the analog input is enabled.

■ **Trace output**

Indicates that the trace function can be used.

■ **GPIO selected**

In Deep standby mode, pins switch to the general-purpose I/O port.

■ **Setting prohibition**

Prohibition of a setting by specification limitation

List of Pin Behavior by Mode State

Pin Status Type	Function Group	Power-On Reset or Low-Voltage Detection State	INITX Input State	Device Internal Reset State	Run mode or Sleep mode State	Timer mode, RTC mode, or Stop mode State		Deep Standby RTC Mode or Deep Standby Stop mode State		Return from Deep Standby Mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1		INITX = 1		INITX = 1
		-	-	-	-	SPL = 0	SPL = 1	SPL = 0	SPL = 1	-
A	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/internal input fixed at 0	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	Main crystal oscillator input pin/ external main clock input selected	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input Enabled
B	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/internal input fixed at 0	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	External main clock input selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/internal input fixed at 0	Maintain previous state	Hi-Z/internal input fixed at 0	Maintain previous State
	Main crystal oscillator output pin	Hi-Z/ internal input fixed at 0/ or input enable	Hi-Z/ internal input fixed at 0	Hi-Z/ internal input fixed at 0	Maintain previous state while oscillator active/ When oscillation stops*1, it will be Hi-Z/ Internal input fixed at 0					
C	INITX input pin	Pull-up/ input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled
D	Mode input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
E	Mode input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/ input enabled	GPIO selected	Hi-Z/ input enabled	GPIO selected

Pin Status Type	Function Group	Power-On Reset or Low-Voltage Detection State	INITX Input State	Device Internal Reset State	Run mode or Sleep mode State	Timer mode, RTC mode, or Stop mode State		Deep Standby RTC Mode or Deep Standby Stop mode State		Return from Deep Standby Mode State		
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable		
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1		INITX = 1		INITX = 1		
		-	-	-	-	SPL = 0	SPL = 1	SPL = 0	SPL = 1	-		
F	NMIX selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	WKUP input enabled	Hi-Z/ WKUP input enabled	Maintain previous state		
	Resource other than above selected	Hi-Z	Hi-Z/ input enabled	Hi-Z/ input enabled			Hi-Z/ internal input fixed at 0			GPIO selected		
	GPIO selected											
G	JTAG selected	Hi-Z	Pull-up/ input enabled	Pull-up/ input enabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state		
	GPIO selected	Setting disabled	Setting disabled	Setting disabled			Hi-Z/ internal input fixed at 0			GPIO selected, internal input fixed at 0	Hi-Z/ internal input fixed at 0	GPIO selected
H	JTAG selected	Hi-Z	Pull-up/ input enabled	Pull-up/ input enabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state		
	Resource other than above selected	Setting disabled	Setting disabled	Setting disabled			Hi-Z/Internal input fixed at 0			GPIO selected, internal input fixed at 0	Hi-Z/Internal input fixed at 0	GPIO selected
	GPIO selected											
I	Resource selected	Hi-Z	Hi-Z/ input enabled	Hi-Z/ input enabled	Maintain previous state	Maintain previous state	Hi-Z/Internal input fixed at 0	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected		
	GPIO selected											

Pin Status Type	Function Group	Power-On Reset or Low-Voltage Detection State	INITX Input State	Device Internal Reset State	Run mode or Sleep mode State	Timer mode, RTC mode, or Stop mode State		Deep Standby RTC Mode or Deep Standby Stop mode State		Return from Deep Standby Mode State	
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable	
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1		INITX = 1		INITX = 1	
		-	-	-	-	SPL = 0	SPL = 1	SPL = 0	SPL = 1	-	
J	Analog output selected	Hi-Z	Hi-Z/ input enabled	Hi-Z/ input enabled	Maintain previous state	*2	*3	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected	
	External interrupt enable selected					Maintain previous state	Maintain previous state				
	Resource other than above selected						Hi-Z/internal input fixed at 0				
	GPIO selected										
K	External interrupt enable selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected	
	Resource other than above selected	Hi-Z	Hi-Z/ input enabled	Hi-Z/ input enabled			Hi-Z/internal input fixed at 0				
	GPIO selected										
L	Analog input selected	Hi-Z	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	
	Resource other than above selected		Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/internal input fixed at 0	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	GPIO selected										

Pin Status Type	Function Group	Power-On Reset or Low-Voltage Detection State	INITX Input State	Device Internal Reset State	Run mode or Sleep mode State	Timer mode, RTC mode, or Stop mode State		Deep Standby RTC Mode or Deep Standby Stop mode State		Return from Deep Standby Mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1		INITX = 1		INITX = 1
		-	-	-	-	SPL = 0	SPL = 1	SPL = 0	SPL = 1	-
M	Analog input selected	Hi-Z	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled
	External interrupt enable selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	Resource other than above selected						Hi-Z/internal input fixed at 0			
	GPIO selected									
N	Analog input selected	Hi-Z	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled
	Trace selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Trace output	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	Resource other than above selected						Hi-Z/internal input fixed at 0			
	GPIO selected									

Pin Status Type	Function Group	Power-On Reset or Low-Voltage Detection State	INITX Input State	Device Internal Reset State	Run mode or Sleep mode State	Timer mode, RTC mode, or Stop mode State		Deep Standby RTC Mode or Deep Standby Stop mode State		Return from Deep Standby Mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1		INITX = 1		INITX = 1
		-	-	-	-	SPL = 0	SPL = 1	SPL = 0	SPL = 1	-
O	Analog input selected	Hi-Z	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled
	Trace selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Trace output	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	External interrupt enable selected						Maintain previous state			
	Resource other than above selected						Hi-Z/internal input fixed at 0			
	GPIO selected									
P	Analog input selected	Hi-Z	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled
	WKUP enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	WKUP input enabled	Hi-Z/ WKUP input enabled	GPIO selected
	Resource other than above selected						Hi-Z/internal input fixed at 0	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	
	GPIO selected									



Pin Status Type	Function Group	Power-On Reset or Low-Voltage Detection State	INITX Input State	Device Internal Reset State	Run mode or Sleep mode State	Timer mode, RTC mode, or Stop mode State		Deep Standby RTC Mode or Deep Standby Stop mode State		Return from Deep Standby Mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1		INITX = 1		INITX = 1
		-	-	-	-	SPL = 0	SPL = 1	SPL = 0	SPL = 1	-
Q	WKUP enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	WKUP input enabled	Hi-Z/ WKUP input enabled	WKUP input enabled
	External interrupt enable selected							GPIO selected, internal input fixed at 0	Hi-Z/ internal input fixed at 0	GPIO selected
	Resource other than above selected	Hi-Z	Hi-Z/ input enabled	Hi-Z/ input enabled						
	GPIO selected									
R	GPIO selected	Hi-Z	Hi-Z/ input enabled	Hi-Z/ input enabled	Maintain previous state	Maintain previous state	Hi-Z/ internal input fixed at 0	GPIO selected, internal input fixed at 0	Hi-Z/ internal input fixed at 0	GPIO selected
	USB I/O pin	Setting disabled	Setting disabled	Setting disabled	Hi-Z at transmission/ input enabled/ internal input fixed at 0 at reception	Hi-Z at transmission/ input enabled/ internal input fixed at 0 at reception	Hi-Z at transmission/ input enabled/ internal input fixed at 0 at reception	Hi-Z/ input enabled	Hi-Z/ input enabled	Hi-Z/ input enabled

\*1: Oscillation is stopped at sub Timer mode, sub CR Timer mode, RTC mode, Stop mode, Deep Standby RTC mode, and Deep Standby Stop mode.

\*2: Maintain previous state at Timer mode. GPIO selected internal input fixed at 0 at RTC mode, Stop mode.

\*3: Maintain previous state at Timer mode. Hi-Z/internal input fixed at 0 at RTC mode, Stop mode.

\*4: It shows the case selected by EPFR14.E\_SPLC register.

**List of VBAT Domain Pin Status**

VBAT Pin Status Type	Function Group	Power-on reset*1	INITX Input State	Device Internal Reset State	Run mode or Sleep mode State	Timer mode, RTC mode, or Stop mode State		Deep Standby RTC mode or Deep Standby Stop mode State		Return From Deep Standby Mode State	VBAT RTC Mode State	Return From VBAT RTC Mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable	Power Supply Stable	Power Supply Stable
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1		INITX = 1		INITX = 1	-	-
		-	-	-	-	SPL = 0	SPL = 1	SPL = 0	SPL = 1	-	-	-
S	GPIO selected	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Setting prohibition	-
	Sub crystal oscillator input pin/ external sub clock input selected	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Maintain previous state	Maintain previous state
T	GPIO selected	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Setting prohibition	-
	External sub clock input selected	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state
	Sub crystal oscillator output pin	Hi-Z/ internal input fixed at 0/ or input enable	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state/ When oscillation stops, Hi-Z*2	Maintain previous state/ When oscillation stops, Hi-Z*2	Maintain previous state/ When oscillation stops, Hi-Z*2	Maintain previous state/ When oscillation stops, Hi-Z*2	Maintain previous state	Maintain previous state	Maintain previous state
U	Resource selected	Hi-Z	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state
	GPIO selected		Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state

\*1: When VBAT and VCC power on.

\*2: When the SOSCNTL bit in the WTOSCCNT register is 0, the sub crystal oscillator output pin is maintained in the previous state. When the SOSCNTL bit in the WTOSCCNT register is 1, oscillation is stopped at Stop mode and Deep Standby Stop mode

## 12. Electrical Characteristics

### 12.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage <sup>*1,*2</sup>	V <sub>CC</sub>	V <sub>SS</sub> - 0.5	V <sub>SS</sub> + 6.5	V	
Power supply voltage (for USB) <sup>*1,*3</sup>	USBV <sub>CC0</sub>	V <sub>SS</sub> - 0.5	V <sub>SS</sub> + 6.5	V	
Power supply voltage (for USB) <sup>*1,*3</sup>	USBV <sub>CC1</sub>	V <sub>SS</sub> - 0.5	V <sub>SS</sub> + 6.5	V	
Power supply voltage (VBAT) <sup>*1,*4</sup>	V <sub>BAT</sub>	V <sub>SS</sub> - 0.5	V <sub>SS</sub> + 6.5	V	
Analog power supply voltage <sup>*1,*5</sup>	AV <sub>CC</sub>	V <sub>SS</sub> - 0.5	V <sub>SS</sub> + 6.5	V	
Analog reference voltage <sup>*1,*5</sup>	AV <sub>RH</sub>	V <sub>SS</sub> - 0.5	V <sub>SS</sub> + 6.5	V	
Input voltage <sup>*1</sup>	V <sub>I</sub>	V <sub>SS</sub> - 0.5	V <sub>CC</sub> + 0.5 (≤ 6.5 V)	V	Except for USB pin
		V <sub>SS</sub> - 0.5	USBV <sub>CC0</sub> + 0.5 (≤ 6.5 V)	V	USB ch 0 pin
		V <sub>SS</sub> - 0.5	USBV <sub>CC1</sub> + 0.5 (≤ 6.5 V)	V	USB ch 1 pin
		V <sub>SS</sub> - 0.5	V <sub>SS</sub> + 6.5	V	5V tolerant
Analog pin input voltage <sup>*1</sup>	V <sub>IA</sub>	V <sub>SS</sub> - 0.5	AV <sub>CC</sub> + 0.5 (≤ 6.5 V)	V	
Output voltage <sup>*1</sup>	V <sub>O</sub>	V <sub>SS</sub> - 0.5	V <sub>CC</sub> + 0.5 (≤ 6.5 V)	V	
L level maximum output current <sup>*6</sup>	I <sub>OL</sub>	-	10	mA	4 mA type
			20	mA	8 mA type
			10	mA	10 mA type
			20	mA	12 mA type
			22.4	mA	I <sup>2</sup> C Fm+
L level average output current <sup>*7</sup>	I <sub>OLAV</sub>	-	4	mA	4 mA type
			8	mA	8 mA type
			10	mA	10 mA type
			12	mA	12 mA type
			20	mA	I <sup>2</sup> C Fm+
L level total maximum output current	∑I <sub>OL</sub>	-	100	mA	
L level total maximum output current <sup>*8</sup>	∑I <sub>OLAV</sub>	-	50	mA	
H level maximum output current <sup>*6</sup>	I <sub>OH</sub>	-	-10	mA	4 mA type
			-20	mA	8 mA type
			-20	mA	10 mA type
			-20	mA	12 mA type
H level average output current <sup>*7</sup>	I <sub>OHAV</sub>	-	-4	mA	4 mA type
			-8	mA	8 mA type
			-10	mA	10 mA type
			-12	mA	12 mA type
H level total maximum output current	∑I <sub>OH</sub>	-	-100	mA	
H level total average output current <sup>*8</sup>	∑I <sub>OHAV</sub>	-	-50	mA	
Power consumption	P <sub>D</sub>	-	200	mW	
Storage temperature	T <sub>STG</sub>	-55	+ 150	°C	

\*1: These parameters are based on the condition that V<sub>SS</sub> = AV<sub>SS</sub> = 0.0 V.

\*2: V<sub>CC</sub> must not drop below V<sub>SS</sub> - 0.5 V.

\*3: USBV<sub>CC0</sub>, USBV<sub>CC1</sub> must not drop below V<sub>SS</sub> - 0.5 V.

\*4: V<sub>BAT</sub> must not drop below V<sub>SS</sub> - 0.5 V.

\*5: Ensure that the voltage does not exceed V<sub>CC</sub> + 0.5 V, for example, when the power is turned on.

\*6: The maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

- \*7: The average output current is defined as the average current value flowing through any one of the corresponding pins for a 100-ms period.
- \*8: The total average output current is defined as the average current value flowing through all of corresponding pins for a 100-ms period.

**WARNING:**

- *Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings. Do not exceed any of these ratings.*

**12.2 Recommended Operating Conditions**

Parameter	Symbol	Conditions	Value		Unit	Remarks
			Min	Max		
Power supply voltage	V <sub>CC</sub>	-	2.7 <sup>*7</sup>	5.5	V	
Power supply voltage (for USB ch 0)	USBV <sub>CC0</sub>	-	3.0	3.6 (≤V <sub>CC</sub> )	V	*1
			2.7	5.5 (≤V <sub>CC</sub> )		*2
Power supply voltage (for USB ch 1)	USBV <sub>CC1</sub>	-	3.0	3.6 (≤V <sub>CC</sub> )	V	*3
			2.7	5.5 (≤V <sub>CC</sub> )		*4
Power supply voltage (VBAT)	V <sub>BAT</sub>	-	1.65	5.5	V	
Analog power supply voltage	AV <sub>CC</sub>	-	2.7	5.5	V	AV <sub>CC</sub> = V <sub>CC</sub>
Analog reference voltage	AVRH	-	*6	AV <sub>CC</sub>	V	
	AVRL	-	AV <sub>SS</sub>	AV <sub>SS</sub>	V	
Operating temperature	Junction temperature	T <sub>J</sub>	-	-40	+ 125	°C
	Ambient temperature	T <sub>A</sub>	-	-40	*5	°C

\*1: When P81/UDP0 and P80/UDM0 pins are used as USB (UDP0, UDM0)

\*2: When P81/UDP0 and P80/UDM0 pins are used as GPIO (P81, P80)

\*3: When P83/UDP1 and P82/UDM1 pins are used as USB (UDP1, UDM1)

\*4: When P83/UDP1 and P82/UDM1 pins are used as GPIO (P83, P82)

\*5: The maximum temperature of the ambient temperature (T<sub>A</sub>) can guarantee a range that does not exceed the junction temperature (T<sub>J</sub>).

The calculation formula of the ambient temperature (T<sub>A</sub>) is:

$$T_A (\text{Max}) = T_J(\text{Max}) - P_d(\text{Max}) \times \theta_{JA}$$

P<sub>d</sub>: Power dissipation (W)

θ<sub>JA</sub>: Package thermal resistance (°C/W)

$$P_d (\text{Max}) = V_{CC} \times I_{CC} (\text{Max}) + \sum (I_{OL} \times V_{OL}) + \sum ((V_{CC} - V_{OH}) \times (-I_{OH}))$$

I<sub>OL</sub>: L level output current

I<sub>OH</sub>: H level output current

V<sub>OL</sub>: L level output voltage

V<sub>OH</sub>: H level output voltage

\*6: The minimum value of analog reference voltage depends on the value of compare clock cycle (t<sub>CCK</sub>). See 12.5. 12-bit A/D Converter for the details.

\*7: For the voltage range between V<sub>CC(min)</sub> and the low voltage detection reset (VDH), the MCU must be clocked from either the High-speed CR or the low-speed CR."

Package thermal resistance and maximum permissible power for each package are shown below. The operation is guaranteed maximum permissible power or less for semiconductor devices.

**Table for Package Thermal Resistance and Maximum Permissible Power**

Package	Printed Circuit Board	Thermal Resistance $\theta_{JA}$ ( $^{\circ}\text{C}/\text{W}$ )	Maximum Permissible Power (mW)	
			$T_A = +85\text{ }^{\circ}\text{C}$	$T_A = +105\text{ }^{\circ}\text{C}$
LQS144 (0.5-mm pitch)	Single-layered both sides	48	833	417
	4 layers	33	1212	606
LQP176 (0.5-mm pitch)	Single-layered both sides	45	889	444
	4 layers	31	1290	645
LQQ216 (0.4-mm pitch)	Single-layered both sides	46	870	435
	4 layers	32	1250	625
LBE192 (0.8-mm pitch)	Single-layered both sides	-	-	-
	4 layers	35	1143	571

**WARNING:**

1. The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.
2. Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.
3. No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet.
4. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

### Calculation Method of Power Dissipation (Pd)

The power dissipation is shown in the following formula.

$$P_d = V_{CC} \times I_{CC} + \sum (I_{OL} \times V_{OL}) + \sum ((V_{CC} - V_{OH}) \times (-I_{OH}))$$

$I_{OL}$ : L level output current

$I_{OH}$ : H level output current

$V_{OL}$ : L level output voltage

$V_{OH}$ : H level output voltage

$I_{CC}$  is the current drawn by the device.

It can be analyzed as follows.

$$I_{CC} = I_{CC}(\text{INT}) + \sum I_{CC}(\text{IO})$$

$I_{CC}(\text{INT})$ : Current drawn by internal logic and memory, etc. through the regulator

$\sum I_{CC}(\text{IO})$ : Sum of current (I/O switching current) drawn by the output pin

For  $I_{CC}(\text{INT})$ , it can be anticipated by (1) Current Rating in 12.3. DC Characteristics (This rating value does not include  $I_{CC}(\text{IO})$  for a value at pin fixed).

For  $I_{CC}(\text{IO})$ , it depends on system used by customers.

The calculation formula is shown below.

$$I_{CC}(\text{IO}) = (C_{\text{INT}} + C_{\text{EXT}}) \times V_{CC} \times f_{\text{SW}}$$

$C_{\text{INT}}$ : Pin internal load capacitance  
 $C_{\text{EXT}}$ : External load capacitance of output pin  
 $f_{\text{SW}}$ : Pin switching frequency

Parameter	Symbol	Conditions	Capacitance Value
Pin internal load capacitance	$C_{\text{INT}}$	4 mA type	1.93 pF
		8 mA type	3.45 pF
		12 mA type	3.42 pF

Calculate  $I_{CC}(\text{Max})$  as follows when the power dissipation can be evaluated by yourself:

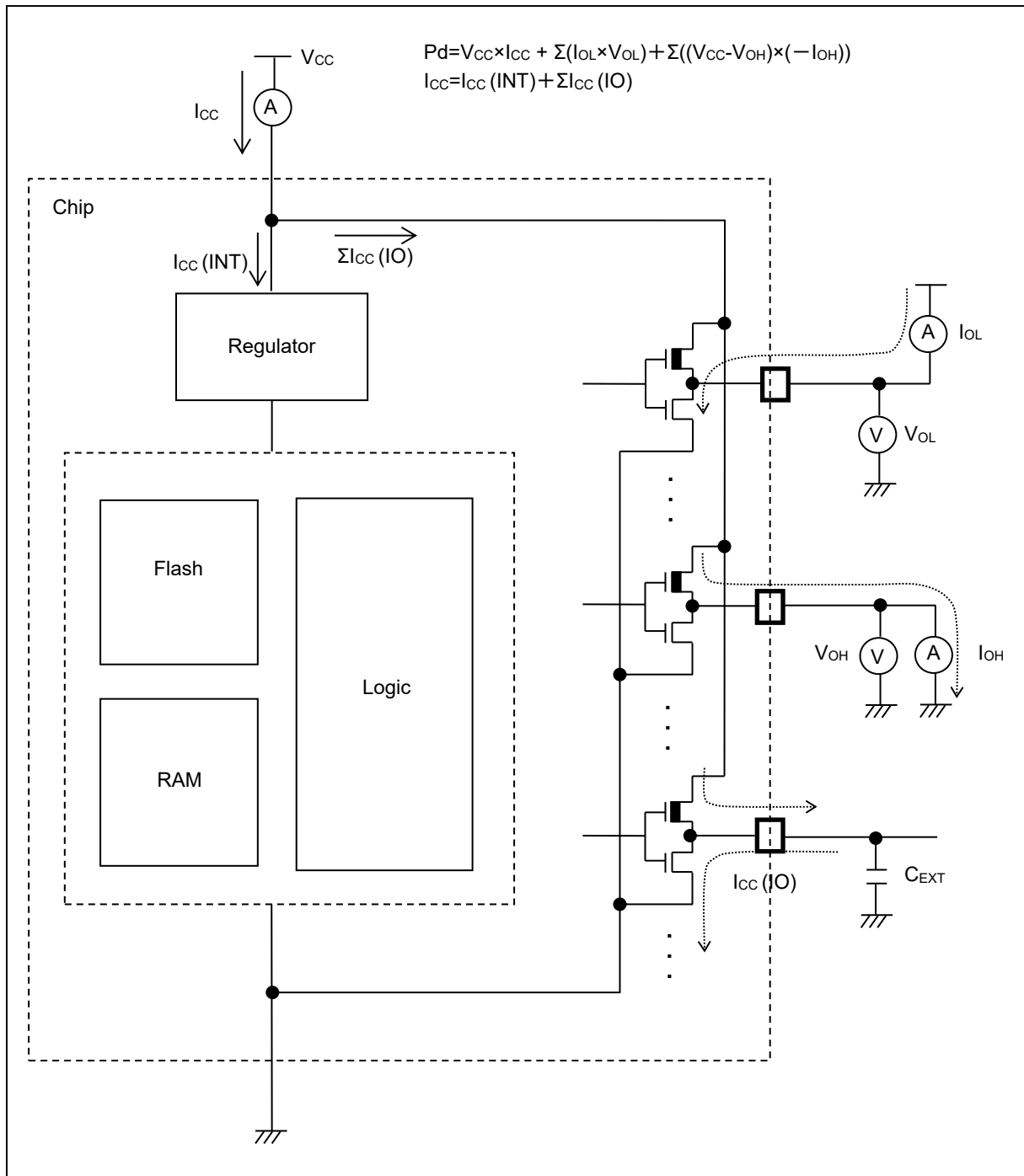
Measure current value  $I_{CC}(\text{Typ})$  at normal temperature (+25 °C).

Add maximum leakage current value  $I_{CC}(\text{leak\_max})$  at operating on a value in (1).

$$I_{CC}(\text{Max}) = I_{CC}(\text{Typ}) + I_{CC}(\text{leak\_max})$$

Parameter	Symbol	Conditions	Current Value
Maximum leakage current at operating	$I_{CC}(\text{leak\_max})$	$T_J = +125\text{ °C}$	79.2 mA
		$T_J = +105\text{ °C}$	39.4 mA
		$T_J = +85\text{ °C}$	26.5 mA

Current Explanation Diagram





12.3 DC Characteristics

12.3.1 Current Rating

Table 12-1 Typical and Maximum Current Consumption in Normal Operation (PLL), Code Running from Flash Memory (Flash Accelerator Mode and Trace Buffer Function Enabled)

Parameter	Symbol	Pin Name	Conditions	Frequency*4	Value		Unit	Remarks		
					Typ*1	Max*2				
Power supply current	I <sub>CC</sub>	V <sub>CC</sub>	Normal operation *7,*8 (PLL)	*5	200 MHz	117	224	mA	*3 When all peripheral clocks are on	
					192 MHz	113	219	mA		
					180 MHz	106	211	mA		
				*6	160 MHz	95	197	mA		
					144 MHz	86	186	mA		
					120 MHz	73	169	mA		
					100 MHz	61	155	mA		
					80 MHz	50	140	mA		
					60 MHz	39	126	mA		
					40 MHz	27	112	mA		
				*6	20 MHz	16	97	mA		
					8 MHz	8.7	88.9	mA		
					4 MHz	6.4	86.1	mA		
					*5	200 MHz	71	168	mA	*3 When all peripheral clocks are off
						192 MHz	68	165	mA	
						180 MHz	64	159	mA	
					*6	160 MHz	58	151	mA	
				144 MHz		52	144	mA		
				120 MHz		44	134	mA		
				100 MHz		38	126	mA		
80 MHz	31	117	mA							
60 MHz	24	109	mA							
40 MHz	17	100	mA							
*6	20 MHz	10	91	mA						
	8 MHz	6.3	86.1	mA						
	4 MHz	5.0	84.5	mA						

\*1: T<sub>A</sub> = +25 °C, V<sub>CC</sub> = 3.3 V

\*2: T<sub>J</sub> = +125 °C, V<sub>CC</sub> = 5.5 V

\*3: When all ports are fixed

\*4: Frequency is a value of HCLK when PCLK0 = PCLK1 = PCLK2 = HCLK

\*5: When stopping flash accelerator mode and trace buffer function (FRWTR.RWT = 11, FBFCR.BE = 1)

\*6: When stopping flash accelerator mode and trace buffer function (FRWTR.RWT = 10, FBFCR.BE = 1)

\*7: Firmware being executed during data collection for this table is not being accessed from the MainFlash memory.”

\*8: When using the crystal oscillator of 4 MHz (including the current consumption of the oscillation circuit)

**Table 12-2 Typical and Maximum Current Consumption in Normal Operation (PLL), Code with Data Accessing Running from Flash Memory (Flash Accelerator Mode and Trace Buffer Function Disabled)**

Parameter	Symbol	Pin Name	Conditions	Frequency*4	Value		Unit	Remarks		
					Typ*1	Max*2				
Power supply current	I <sub>CC</sub>	V <sub>CC</sub>	Normal operation *7,*8 (PLL)	*5	200 MHz	128	236	mA	*3 When all peripheral clocks are on	
					192 MHz	123	230	mA		
					180 MHz	116	221	mA		
				*6	160 MHz	102	205	mA		
					144 MHz	93	193	mA		
					120 MHz	79	175	mA		
					100 MHz	67	161	mA		
					80 MHz	54	145	mA		
					60 MHz	42	130	mA		
					40 MHz	30	115	mA		
				20 MHz	17	99	mA			
				8 MHz	9.2	90.0	mA			
				4 MHz	6.7	86.9	mA			
				*5	200 MHz	74	170	mA	*3 When all peripheral clocks are off	
					192 MHz	71	167	mA		
					180 MHz	67	162	mA		
					*6	160 MHz	59	152		mA
						144 MHz	53	145		mA
						120 MHz	45	135		mA
						100 MHz	39	127		mA
80 MHz	32	118	mA							
60 MHz	25	110	mA							
40 MHz	18	101	mA							
20 MHz	11	92	mA							
8 MHz	6.5	86.8	mA							
4 MHz	5.1	85.0	mA							

\*1: T<sub>A</sub> = +25 °C, V<sub>CC</sub> = 3.3 V

\*2: T<sub>J</sub> = +125 °C, V<sub>CC</sub> = 5.5 V

\*3: When all ports are fixed

\*4: Frequency is a value of HCLK when PCLK0 = PCLK1 = PCLK2 = HCLK

\*5: When stopping flash accelerator mode and trace buffer function (FRWTR.RWT = 11, FBFCR.BE = 0)

\*6: When stopping flash accelerator mode and trace buffer function (FRWTR.RWT = 10, FBFCR.BE = 0)

\*7: With data access to a MainFlash memory.

\*8: When using the crystal oscillator of 4 MHz (including the current consumption of the oscillation circuit)

**Table 12-3 Typical and Maximum Current Consumption in Normal Operation (PLL), Code with Data Accessing Running from Flash Memory (Flash 0 Wait-cycle Mode and Read Access 0 Wait)**

Parameter	Symbol	Pin Name	Conditions	Frequency*4	Value		Unit	Remarks	
					Typ*1	Max*2			
Power supply current	I <sub>CC</sub>	VCC	Normal operation *6,*7 (PLL)	*5	72 MHz	71	161	mA	*3 When all peripheral clocks are on
					60 MHz	62	150	mA	
					48 MHz	51	138	mA	
					36 MHz	40	125	mA	
					24 MHz	29	112	mA	
					12 MHz	17	98	mA	
					8 MHz	13	93	mA	
				4 MHz	8.4	88.5	mA		
				*5	72 MHz	46	132	mA	*3 When all peripheral clocks are off
					60 MHz	41	125	mA	
					48 MHz	34	118	mA	
					36 MHz	27	110	mA	
					24 MHz	20	102	mA	
					12 MHz	12	93	mA	
8 MHz	9.4	89.7	mA						
4 MHz	6.5	86.4	mA						

\*1: T<sub>A</sub> = +25 °C, V<sub>CC</sub> = 3.3 V

\*2: T<sub>J</sub> = +125 °C, V<sub>CC</sub> = 5.5 V

\*3: When all ports are fixed

\*4: Frequency is a value of HCLK when PCLK0 = PCLK1 = PCLK2 = HCLK

\*5: When operating flash 0 wait-cycle mode and read access 0 wait (FRWTR.RWT = 00, FBFCR.SD = 000)

\*6: With data access to a MainFlash memory.

\*7: When using the crystal oscillator of 4 MHz (including the current consumption of the oscillation circuit)

**Table 12-4 Typical and Maximum Current Consumption in Normal Operation (Other Than PLL), Code with Data Accessing Running from Flash Memory (Flash 0 Wait-cycle Mode and Read Access 0 Wait)**

Parameter	Symbol	Pin Name	Conditions		Frequency* <sup>4</sup>	Value		Unit	Remarks
						Typ* <sup>1</sup>	Max* <sup>2</sup>		
Power supply current	I <sub>CC</sub>	V <sub>CC</sub>	Normal operation *6, *7 (main oscillation)	*5	4 MHz	4.7	84.9	mA	*3 When all peripheral clocks are on
						3.9	83.8	mA	*3 When all peripheral clocks are off
			Normal operation *6 (built-in High-speed CR)	*5	4 MHz	3.0	83.2	mA	*3 When all peripheral clocks are on
						2.1	82.0	mA	*3 When all peripheral clocks are off
			Normal operation *6, *8 (sub oscillation)	*5	32 kHz	0.78	80.37	mA	*3 When all peripheral clocks are on
						0.77	80.36	mA	*3 When all peripheral clocks are off
			Normal operation *6 (built-in low-speed CR)	*5	100 kHz	0.81	80.39	mA	*3 When all peripheral clocks are on
						0.78	80.38	mA	*3 When all peripheral clocks are off

\*1: T<sub>A</sub> = +25 °C, V<sub>CC</sub> = 3.3 V

\*2: T<sub>J</sub> = +125 °C, V<sub>CC</sub> = 5.5 V

\*3: When all ports are fixed

\*4: Frequency is a value of HCLK when PCLK0 = PCLK1 = PCLK2 = HCLK/2

\*5: When operating flash 0 wait-cycle mode and read access 0 wait (FRWTR.RWT = 00, FBFCR.SD = 000)

\*6: With data access to a MainFlash memory.

\*7: When using the crystal oscillator of 4 kHz (including the current consumption of the oscillation circuit)

\*8: When using the crystal oscillator of 32 kHz (including the current consumption of the oscillation circuit)

**Table 12-5 Typical and Maximum Current Consumption in Sleep Operation (PLL), when PCLK0 = PCLK1 = PCLK2 = HCLK/2**

Parameter	Symbol	Pin Name	Conditions	Frequency* <sup>4</sup>	Value		Unit	Remarks
					Typ* <sup>1</sup>	Max* <sup>2</sup>		
Power supply current	I <sub>CCS</sub>	V <sub>CC</sub>	Sleep operation* <sup>5</sup> (PLL)	200 MHz	88	188	mA	* <sub>3</sub> When all peripheral clocks are on
				192 MHz	85	184	mA	
				180 MHz	80	178	mA	
				160 MHz	72	164	mA	
				144 MHz	65	156	mA	
				120 MHz	55	144	mA	
				100 MHz	47	134	mA	
				80 MHz	38	124	mA	
				60 MHz	30	114	mA	
				40 MHz	21	104	mA	
				20 MHz	12	93	mA	
				8 MHz	7.4	87.2	mA	
				4 MHz	5.8	85.2	mA	
				200 MHz	44	134	mA	* <sub>3</sub> When all peripheral clocks are off
				192 MHz	42	132	mA	
				180 MHz	40	129	mA	
				160 MHz	36	123	mA	
				144 MHz	33	119	mA	
				120 MHz	28	113	mA	
				100 MHz	24	108	mA	
				80 MHz	20	103	mA	
				60 MHz	16	98	mA	
				40 MHz	12	93	mA	
				20 MHz	7.6	87.6	mA	
8 MHz	5.2	84.7	mA					
4 MHz	4.4	83.7	mA					

\*1: T<sub>A</sub> = +25 °C, V<sub>CC</sub> = 3.3 V

\*2: T<sub>J</sub> = +125 °C, V<sub>CC</sub> = 5.5 V

\*3: When all ports are fixed

\*4: Frequency is a value of HCLK when PCLK0 = PCLK1 = PCLK2 = HCLK/2

\*5: When using the crystal oscillator of 4 MHz (including the current consumption of the oscillation circuit)

**Table 12-6 Typical and Maximum Current Consumption in Sleep Operation (PLL), when PCLK0 = PCLK1 = PCLK2 = HCLK**

Parameter	Symbol	Pin Name	Conditions	Frequency* <sup>4</sup>	Value		Unit	Remarks
					Typ* <sup>1</sup>	Max* <sup>2</sup>		
Power supply current	I <sub>CCS</sub>	VCC	Sleep operation* <sup>5</sup> (PLL)	72 MHz	45	130	mA	* <sup>3</sup> When all peripheral clocks are on
				60 MHz	38	122	mA	
				48 MHz	31	114	mA	
				36 MHz	24	106	mA	
				24 MHz	18	99	mA	
				12 MHz	11	91	mA	
				8 MHz	8.6	88.3	mA	
				4 MHz	6.3	85.7	mA	
				72 MHz	20	103	mA	* <sup>3</sup> When all peripheral clocks are off
				60 MHz	18	99	mA	
				48 MHz	15	96	mA	
				36 MHz	12	93	mA	
				24 MHz	9.1	89.3	mA	
				12 MHz	6.5	86.1	mA	
				8 MHz	5.5	84.9	mA	
				4 MHz	4.6	83.8	mA	

\*1: T<sub>A</sub> = +25 °C, V<sub>CC</sub> = 3.3 V

\*2: T<sub>J</sub> = +125 °C, V<sub>CC</sub> = 5.5 V

\*3: When all ports are fixed

\*4: Frequency is a value of HCLK when PCLK0 = PCLK1 = PCLK2 = HCLK

\*5: When using the crystal oscillator of 4 MHz (including the current consumption of the oscillation circuit)

**Table 12-7 Typical and Maximum Current Consumption in Sleep Operation (Other Than PLL), when PCLK0 = PCLK1 = PCLK2 = HCLK/2**

Parameter	Symbol	Pin Name	Conditions	Frequency*4	Value		Unit	Remarks
					Typ*1	Max*2		
Power supply current	I <sub>CCS</sub>	V <sub>CC</sub>	Sleep operation*5 (main oscillation)	4 MHz	3.4	82.6	mA	*3 When all peripheral clocks are on
					2.5	81.7	mA	*3 When all peripheral clocks are off
			Sleep operation (built-in High-speed CR)	4 MHz	2.5	81.7	mA	*3 When all peripheral clocks are on
					1.7	80.9	mA	*3 When all peripheral clocks are off
			Sleep operation*6 (sub oscillation)	32 kHz	0.75	79.97	mA	*3 When all peripheral clocks are on
					0.74	79.96	mA	*3 When all peripheral clocks are off
			Sleep operation (built-in low-speed CR)	100 kHz	0.79	80.01	mA	*3 When all peripheral clocks are on
					0.76	79.98	mA	*3 When all peripheral clocks are off

\*1: T<sub>A</sub> = +25 °C, V<sub>CC</sub> = 3.3 V

\*2: T<sub>J</sub> = +125 °C, V<sub>CC</sub> = 5.5 V

\*3: When all ports are fixed.

\*4: Frequency is a value of HCLK when PCLK0 = PCLK1 = PCLK2 = HCLK/2

\*5: When using the crystal oscillator of 4 MHz (including the current consumption of the oscillation circuit)

\*6: When using the crystal oscillator of 32 kHz (including the current consumption of the oscillation circuit)

**Table 12-8 Typical and Maximum Current Consumption in Stop Mode, Timer Mode and RTC Mode**

Parameter	Symbol	Pin Name	Conditions	Frequency	Value		Unit	Remarks
					Typ*1	Max*2		
Power supply current	I <sub>CCH</sub>	V <sub>CC</sub>	Stop mode	-	0.56	3.01	mA	*3, *4 T <sub>A</sub> = +25 °C
					-	27.03	mA	*3, *4 T <sub>A</sub> = +85 °C
					-	39.92	mA	*3, *4 T <sub>A</sub> = +105 °C
	I <sub>CCT</sub>		Timer mode* <sup>5</sup> (main oscillation)	4 MHz	1.40	3.85	mA	*3, *4 T <sub>A</sub> = +25 °C
					-	27.87	mA	*3, *4 T <sub>A</sub> = +85 °C
					-	40.76	mA	*3, *4 T <sub>A</sub> = +105 °C
			Timer mode (built-in High-speed CR)	4 MHz	0.95	3.40	mA	*3, *4 T <sub>A</sub> = +25 °C
					-	27.42	mA	*3, *4 T <sub>A</sub> = +85 °C
					-	40.31	mA	*3, *4 T <sub>A</sub> = +105 °C
			Timer mode* <sup>6</sup> (sub oscillation)	32 kHz	0.57	3.02	mA	*3, *4 T <sub>A</sub> = +25 °C
					-	27.04	mA	*3, *4 T <sub>A</sub> = +85 °C
					-	39.93	mA	*3, *4 T <sub>A</sub> = +105 °C
	Timer mode (built-in Low-speed CR)		100 kHz	0.58	3.03	mA	*3, *4 T <sub>A</sub> = +25 °C	
				-	27.05	mA	*3, *4 T <sub>A</sub> = +85 °C	
				-	39.94	mA	*3, *4 T <sub>A</sub> = +105 °C	
	I <sub>CCR</sub>		RTC mode* <sup>6</sup> (sub oscillation)	32 kHz	0.57	3.02	mA	*3, *4 T <sub>A</sub> = +25 °C
					-	27.04	mA	*3, *4 T <sub>A</sub> = +85 °C
					-	39.93	mA	*3, *4 T <sub>A</sub> = +105 °C

\*1: V<sub>CC</sub> = 3.3 V

\*2: V<sub>CC</sub> = 5.5 V

\*3: When all ports are fixed

\*4: When LVD is off

\*5: When using the crystal oscillator of 4 MHz (including the current consumption of the oscillation circuit)

\*6: When using the crystal oscillator of 32 kHz (including the current consumption of the oscillation circuit)



**Table 12-9 Typical and Maximum Current Consumption in Deep Standby Stop Mode, Deep Standby RTC Mode and VBAT**

Parameter	Symbol	Pin Name	Conditions	Frequency	Value		Unit	Remarks
					Typ*1	Max*2		
Power supply current	I <sub>CCHD</sub>	V <sub>CC</sub>	Deep Standby Stop mode (When RAM is off)	-	96	248	μA	*3, *4 T <sub>A</sub> = +25 °C
					-	3009	μA	*3, *4 T <sub>A</sub> = +85 °C
					-	3889	μA	*3, *4 T <sub>A</sub> = +105 °C
			Deep Standby Stop mode (When RAM is on)		106	259	μA	*3, *4 T <sub>A</sub> = +25 °C
					-	3020	μA	*3, *4 T <sub>A</sub> = +85 °C
					-	3900	μA	*3, *4 T <sub>A</sub> = +105 °C
	I <sub>CCRD</sub>		32 kHz	Deep Standby RTC mode (When RAM is off)	96	248	μA	*3, *4 T <sub>A</sub> = +25 °C
					-	3009	μA	*3, *4 T <sub>A</sub> = +85 °C
					-	3889	μA	*3, *4 T <sub>A</sub> = +105 °C
				Deep Standby RTC mode (When RAM is on)	106	259	μA	*3, *4 T <sub>A</sub> = +25 °C
					-	3020	μA	*3, *4 T <sub>A</sub> = +85 °C
					-	3900	μA	*3, *4 T <sub>A</sub> = +105 °C
	I <sub>CCVBAT</sub>	-	RTC stop*6	0.058	0.1	μA	*3, *4, *5 T <sub>A</sub> = +25 °C	
				-	1.4	μA	*3, *4, *5 T <sub>A</sub> = +85 °C	
-				3.3	μA	*3, *4, *5 T <sub>A</sub> = +105 °C		
RTC operation*6			1.0	1.8	μA	*3, *4 T <sub>A</sub> = +25 °C		
			-	3.2	μA	*3, *4 T <sub>A</sub> = +85 °C		
			-	5.1	μA	*3, *4 T <sub>A</sub> = +105 °C		

\*1: V<sub>CC</sub> = 3.3 V

\*2: V<sub>CC</sub> = 5.5 V

\*3: When all ports are fixed

\*4: When LVD is off

\*5: When sub oscillation is off

\*6: In the case of setting RTC after V<sub>CC</sub> power on

**Table 12-10 Typical and Maximum Current Consumption in Low-voltage Detection Circuit, Main Flash Memory Write/erase**

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Low-voltage detection circuit (LVD) power supply current	I <sub>CC</sub> LVD	VCC	At operation	-	4	7	μA	For occurrence of interrupt
MainFlash memory write/erase current	I <sub>CC</sub> FLASH		At write/erase	-	13.4	15.9	mA	*1

\*1: When programming or erase in flash memory, Flash Memory Write/Erase current (I<sub>CC</sub>FLASH) is added to the Power supply current (I<sub>CC</sub>).

**Peripheral Current Dissipation**

Clock system	Peripheral	Unit	Frequency (MHz)			Unit	Remarks
			50	100	200		
HCLK	GPIO	All ports	0.39	0.81	1.56	mA	
	DMAC	-	0.99	1.97	3.82		
	DSTC	-	0.73	1.49	2.86		
	External bus I/F	-	0.25	0.48	0.97		
	SD card I/F	-	0.74	1.47	2.90		
	USB	1 ch	0.48	0.95	1.89		
	I <sup>2</sup> S	-	0.51	1.02	1.99		
	High-Speed Quad SPI	-	0.48	0.97	1.49		
	Programmable CRC	-	0.05	0.10	0.22		
PCLK1	Base timer	4 ch	0.21	0.42	0.83	mA	
	Multi-functional timer/PPG	1 unit/4 ch	0.83	1.65	3.25		
	Quadrature position/revolution counter	1 unit	0.07	0.13	0.27		
	A/D converter	1 unit	0.31	0.60	1.17		
PCLK2	Multi-function serial	1 ch	0.41	0.81	-	mA	

**12.3.2 Pin Characteristics**
 $(V_{CC} = USBV_{CC0} = USBV_{CC1} = AV_{CC} = 2.7\text{ V to }5.5\text{ V}, V_{SS} = AV_{SS} = 0\text{ V})$ 

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
H level input voltage (hysteresis input)	$V_{IHS}$	CMOS hysteresis input pin, MD0, MD1	-	$V_{CC} \times 0.8$	-	$V_{CC} + 0.3$	V	
		MADATAxx	$V_{CC} > 3.0\text{ V}, V_{CC} \leq 3.6\text{ V},$	2.4	-	$V_{CC} + 0.3$	V	At External Bus
		5 V tolerant input pin	-	$V_{CC} \times 0.8$	-	$V_{SS} + 5.5$	V	
		Input pin doubled as I <sup>2</sup> C Fm+	-	$V_{CC} \times 0.7$	-	$V_{SS} + 5.5$	V	
		TTL Schmitt input pin	-	2.0	-	$V_{CC} + 0.3$	V	
L level input voltage (hysteresis input)	$V_{ILS}$	CMOS hysteresis input pin, MD0, MD1	-	$V_{SS} - 0.3$	-	$V_{CC} \times 0.2$	V	
		5 V tolerant input pin	-	$V_{SS} - 0.3$	-	$V_{CC} \times 0.2$	V	
		Input pin doubled as I <sup>2</sup> C Fm+	-	$V_{SS}$	-	$V_{CC} \times 0.3$	V	
		TTL Schmitt input pin	-	$V_{SS} - 0.3$	-	0.8	V	
H level output voltage	$V_{OH}$	4 mA type	$V_{CC} \geq 4.5\text{ V}, I_{OH} = -4\text{ mA}$	$V_{CC} - 0.5$	-	$V_{CC}$	V	
			$V_{CC} < 4.5\text{ V}, I_{OH} = -2\text{ mA}$					
		8 mA type	$V_{CC} \geq 4.5\text{ V}, I_{OH} = -8\text{ mA}$	$V_{CC} - 0.5$	-	$V_{CC}$	V	
			$V_{CC} < 4.5\text{ V}, I_{OH} = -4\text{ mA}$					
		10 mA type	$V_{CC} \geq 4.5\text{ V}, I_{OH} = -10\text{ mA}$	$V_{CC} - 0.5$	-	$V_{CC}$	V	
			$V_{CC} < 4.5\text{ V}, I_{OH} = -8\text{ mA}$					
		12 mA type	$V_{CC} \geq 4.5\text{ V}, I_{OH} = -12\text{ mA}$	$V_{CC} - 0.5$	-	$V_{CC}$	V	
			$V_{CC} < 4.5\text{ V}, I_{OH} = -8\text{ mA}$					
		The pin doubled as USB I/O	$USBV_{CC} \geq 4.5\text{ V}, I_{OH} = -20.5\text{ mA}$	$USBV_{CC} - 0.4$	-	$USBV_{CC}$	V	*1
			$USBV_{CC} < 4.5\text{ V}, I_{OH} = -13.0\text{ mA}$					
		The pin doubled as I <sup>2</sup> C Fm+	$V_{CC} \geq 4.5\text{ V}, I_{OH} = -4\text{ mA}$	$V_{CC} - 0.5$	-	$V_{CC}$	V	At GPIO
			$V_{CC} < 4.5\text{ V}, I_{OH} = -3\text{ mA}$					

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
L level output voltage	V <sub>OL</sub>	4 mA type	V <sub>CC</sub> ≥ 4.5 V, I <sub>OL</sub> = 4 mA	V <sub>SS</sub>	-	0.4	V	
			V <sub>CC</sub> < 4.5 V, I <sub>OL</sub> = 2 mA					
		8 mA type	V <sub>CC</sub> ≥ 4.5 V, I <sub>OL</sub> = 8 mA	V <sub>SS</sub>	-	0.4	V	
			V <sub>CC</sub> < 4.5 V, I <sub>OL</sub> = 4 mA					
		10 mA type	V <sub>CC</sub> ≥ 4.5 V, I <sub>OL</sub> = 10 mA	V <sub>SS</sub>	-	0.4	V	
			V <sub>CC</sub> < 4.5 V, I <sub>OL</sub> = 8 mA					
		12 mA type	V <sub>CC</sub> ≥ 4.5 V, I <sub>OL</sub> = 12 mA	V <sub>SS</sub>	-	0.4	V	
			V <sub>CC</sub> < 4.5 V, I <sub>OL</sub> = 8 mA					
		The pin doubled as USB I/O	USBV <sub>CC</sub> ≥ 4.5 V, I <sub>OL</sub> = 18.5 mA	V <sub>SS</sub>	-	0.4	V	*1
			USBV <sub>CC</sub> < 4.5 V, I <sub>OL</sub> = 10.5 mA					
		The pin doubled as I <sup>2</sup> C Fm+	V <sub>CC</sub> ≥ 4.5 V, I <sub>OL</sub> = 4 mA	V <sub>SS</sub>	-	0.4	V	At GPIO
			V <sub>CC</sub> < 4.5 V, I <sub>OL</sub> = 3 mA					At I <sup>2</sup> C Fm+
V <sub>CC</sub> ≤ 4.5 V, I <sub>OL</sub> = 20 mA								
Input leak current	I <sub>IL</sub>	-	-	- 5	-	+ 5	μA	
Pull-up resistor value	R <sub>PU</sub>	Pull-up pin	V <sub>CC</sub> ≥ 4.5 V	25	50	100	kΩ	
			V <sub>CC</sub> < 4.5 V	30	80	200		
Input capacitance	C <sub>IN</sub>	Other than V <sub>CC</sub> , USBV <sub>CC0</sub> , USBV <sub>CC1</sub> , V <sub>BAT</sub> , V <sub>SS</sub> , AV <sub>CC</sub> , AV <sub>SS</sub> , AV <sub>RH</sub>	-	-	5	15	pF	

\*1: USBV<sub>cc0</sub> and USBV<sub>cc1</sub> are described as USBV<sub>cc</sub>.

## 12.4 AC Characteristics

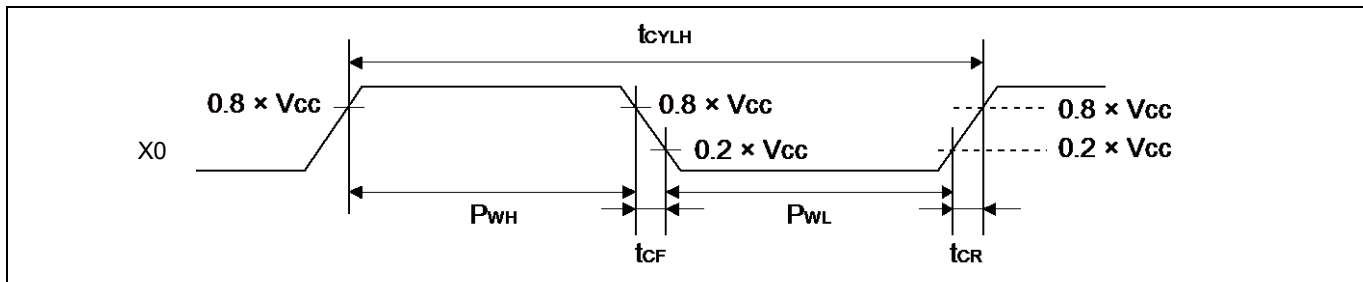
### 12.4.1 Main Clock Input Characteristics

( $V_{CC} = AV_{CC} = 2.7\text{ V to }5.5\text{ V}$ ,  $V_{SS} = AV_{SS} = 0\text{ V}$ ,  $T_a = -40\text{ }^\circ\text{C to }+105\text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input frequency	$f_{CH}$	X0, X1	$V_{CC} \geq 4.5\text{ V}$	4	48	MHz	When crystal oscillator is connected
			$V_{CC} < 4.5\text{ V}$	4	20		
			$V_{CC} \geq 4.5\text{ V}$	4	48	MHz	When using external clock
			$V_{CC} < 4.5\text{ V}$	4	20		
Input clock cycle	$t_{CYLH}$		$V_{CC} \geq 4.5\text{ V}$	20.83	250	ns	When using external clock
			$V_{CC} < 4.5\text{ V}$	50	250		
Input clock pulse width	-		$P_{WH}/t_{CYLH}$ , $P_{WL}/t_{CYLH}$	45	55	%	When using external clock
Input clock rise time and fall time	$t_{CF}$ , $t_{CR}$		-	-	5	ns	When using external clock
Internal operating clock *1 frequency	$f_{CC}$	-	-	-	200	MHz	Base clock (HCLK/FCLK)
	$f_{CP0}$	-	-	-	100	MHz	APB0bus clock *2
	$f_{CP1}$	-	-	-	200	MHz	APB1bus clock *2
	$f_{CP2}$	-	-	-	100	MHz	APB2bus clock *2
Internal operating clock *1 cycle time	$t_{CYCC}$	-	-	5	-	ns	Base clock (HCLK/FCLK)
	$t_{CYCP0}$	-	-	10	-	ns	APB0bus clock *2
	$t_{CYCP1}$	-	-	5	-	ns	APB1bus clock *2
	$t_{CYCP2}$	-	-	10	-	ns	APB2bus clock *2

\*1: For more information about each internal operating clock, see "CHAPTER 2-1: Clock" in FM4 Family Peripheral Manual Main Part (002-04856).

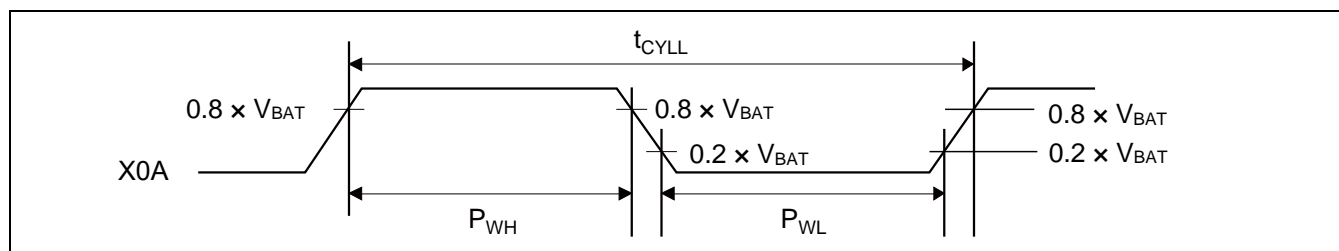
\*2: For more about each APB bus to which each peripheral is connected, see 8. Block Diagram in this data sheet.



**12.4.2 Sub Clock Input Characteristics**
 $(V_{BAT} = 1.65\text{ V to } 5.5\text{ V}, V_{SS} = 0\text{ V})$ 

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input frequency	$1/t_{CYLL}$	X0A, X1A	-	-	32.768	-	kHz	When crystal oscillator is connected *
			-	32	-	100		kHz
Input clock cycle	$t_{CYLL}$		-	10	-	31.25	$\mu\text{s}$	When using external clock
Input clock pulse width	-		$P_{WH}/t_{CYLL}, P_{WL}/t_{CYLL}$	45	-	55	%	When using external clock

\*: For more information about crystal oscillator, see Sub crystal oscillator in 7. Handling Devices.


**12.4.3 Built-In CR Oscillation Characteristics**
**Built-In High-speed CR**
 $(V_{CC} = 2.7\text{ V to } 5.5\text{ V}, V_{SS} = 0\text{ V})$ 

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	$f_{CRH}$	$T_J = -20^\circ\text{C to } +105^\circ\text{C}$	3.92	4	4.08	MHz	When trimming *1
		$T_J = -40^\circ\text{C to } +125^\circ\text{C}$	3.88	4	4.12		When not trimming
		$T_J = -40^\circ\text{C to } +125^\circ\text{C}$	3	4	5		
Frequency stabilization time	$t_{CRWT}$	-	-	-	30	$\mu\text{s}$	*2

\*1: In the case of using the values in CR trimming area of flash memory at shipment for frequency/temperature trimming

\*2: This is the time to stabilize the frequency of the High-speed CR clock after setting trimming value. During this period, it is able to use the High-speed CR clock as a source clock.

**Built-In Low-speed CR**
 $(V_{CC} = 2.7\text{ V to } 5.5\text{ V}, V_{SS} = 0\text{ V})$ 

Parameter	Symbol	Condition	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	$f_{CRL}$	-	50	100	150	kHz	

**12.4.4 Operating Conditions of Main PLL (in the Case of Using Main Clock for Input Clock of PLL)**

 (V<sub>CC</sub> = 2.7 V to 5.5 V, V<sub>SS</sub> = 0 V)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time* <sup>1</sup> (lock up time)	t <sub>LOCK</sub>	100	-	-	μs	
PLL input clock frequency	f <sub>PLLI</sub>	4	-	16	MHz	
PLL multiplication rate	-	13	-	100	multiplier	
PLL macro oscillation clock frequency	f <sub>PLLO</sub>	200	-	400	MHz	
Main PLL clock frequency* <sup>2</sup>	f <sub>CLKPLL</sub>	-	-	200	MHz	

\*1: Time from when the PLL starts operating until the oscillation stabilizes

\*2: For more information about Main PLL clock (CLKPLL), see Chapter 2-1: Clock in FM4 Family Peripheral Manual Main Part (002-04856).

**12.4.5 Operating Conditions of USB PLL · I<sup>2</sup>S PLL (in the Case of Using Main Clock for Input Clock of PLL)**

 (V<sub>CC</sub> = 2.7 V to 5.5 V, V<sub>SS</sub> = 0 V)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time* <sup>1</sup> (lock up time)	t <sub>LOCK</sub>	100	-	-	μs	
PLL input clock frequency	f <sub>PLLI</sub>	4	-	16	MHz	
PLL multiplication rate	-	13	-	100	multiplier	
PLL macro oscillation clock frequency	f <sub>PLLO</sub>	200	-	400	MHz	USB
				384	MHz	I <sup>2</sup> S
USB clock frequency * <sup>2</sup>	f <sub>CLKPLL</sub>	-	-	50	MHz	After the M frequency division
I <sup>2</sup> S clock frequency * <sup>3</sup>	f <sub>CLKPLL</sub>	-	-	12.288	MHz	After the M frequency division

\*1: Time from when the PLL starts operating until the oscillation stabilizes

\*2: For more information about USB/Ethernet clock, see Chapter 2-2: USB/Ethernet Clock Generation in FM4 Family Peripheral Manual Communication Macro Part (002-04862).

\*3: For more information about I<sup>2</sup>S clock, see Chapter 7-1: I<sup>2</sup>S Clock Generation in FM4 Family Peripheral Manual Communication Macro Part (002-04862).

**12.4.6 Operating Conditions of Main PLL (in the Case of Using Built-in High-speed CR Clock for Input Clock of Main PLL)**  
 (V<sub>CC</sub> = 2.7 V to 5.5 V, V<sub>SS</sub> = 0 V)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time <sup>*1</sup> (lock up time)	t <sub>LOCK</sub>	100	-	-	μs	
PLL input clock frequency	f <sub>PLLI</sub>	3.8	4	4.2	MHz	
PLL multiplication rate	-	50	-	95	multiplier	
PLL macro oscillation clock frequency	f <sub>PLO</sub>	190	-	400	MHz	
Main PLL clock frequency <sup>*2</sup>	f <sub>CLKPLL</sub>	-	-	200	MHz	

\*1: Time from when the PLL starts operating until the oscillation stabilizes

\*2: For more information about Main PLL clock (CLKPLL), see Chapter 2-1: Clock in FM4 Family Peripheral Manual Main Part (002-04856).

**Note:**

- The High-speed CR clock (CLKHC) should be set with frequency/temperature trimming to act as the source clock of the Main PLL.

**12.4.7 Reset Input Characteristics**

 (V<sub>CC</sub> = 2.7 V to 5.5 V, V<sub>SS</sub> = 0 V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Typ		
Reset input time	t <sub>INITX</sub>	INITX	-	500	-	ns	



**12.4.8 Power-On Reset Timing**

 (V<sub>SS</sub> = 0 V)

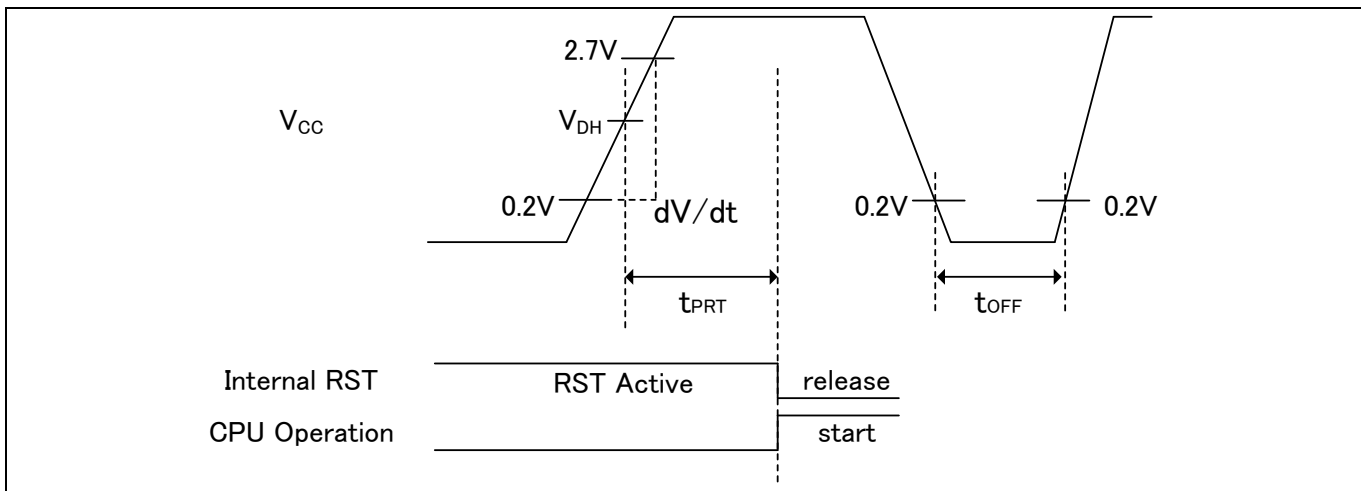
Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply shut down time	t <sub>OFF</sub>	VCC	-	1	-	-	ms	*1
Power ramp rate	dV/dt		V <sub>CC</sub> : 0.2 V to 2.70 V	0.6	-	1000	mV/μs	*2
Time until releasing Power-on reset	t <sub>PRT</sub>		-	0.33	-	0.60	ms	

\*1: V<sub>CC</sub> must be held below 0.2 V for a minimum period of t<sub>OFF</sub>. Improper initialization may occur if this condition is not met.

\*2: This dV/dt characteristic is applied at the power-on of cold start (t<sub>OFF</sub>>1ms).

**Note:**

- If t<sub>OFF</sub> cannot be satisfied designs must assert external reset(INITX) at power-up and at any brownout event per 12. 4. 7.


**Glossary**

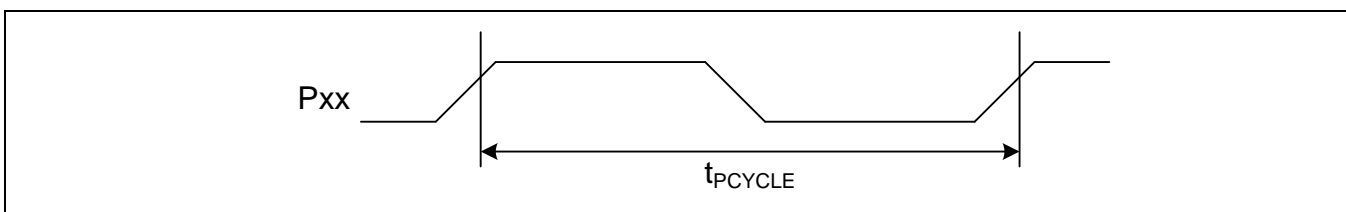
- V<sub>DH</sub>: detection voltage of Low Voltage detection reset. See “12.8. Low-Voltage Detection Characteristics”.

**12.4.9 GPIO Output Characteristics**

 (V<sub>CC</sub> = 2.7 V to 5.5 V, V<sub>SS</sub> = 0 V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Typ		
Output frequency	t <sub>PCYCLE</sub>	Pxx*	V <sub>CC</sub> ≥ 4.5 V	-	50	MHz	
			V <sub>CC</sub> < 4.5 V	-	32	MHz	

\*: GPIO is a target.



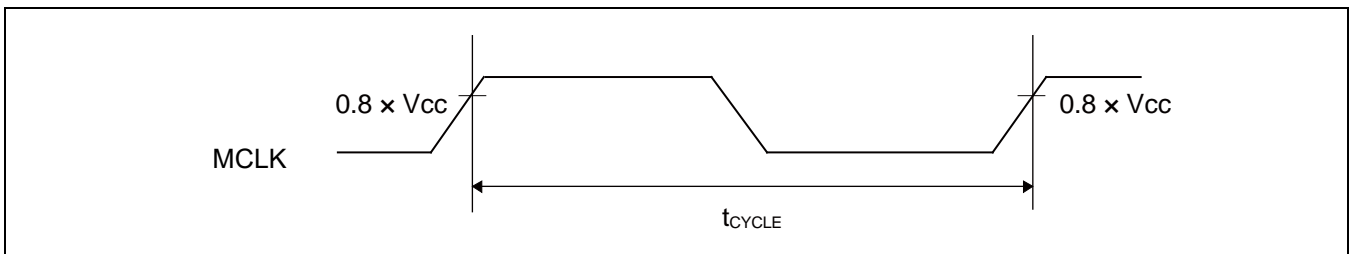
12.4.10 External Bus Timing

External Bus Clock Output Characteristics

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Typ		
Output frequency	t <sub>CYCLE</sub>	MCLKOUT *1		-	50 *2	MHz	

\*1: The external bus clock (MCLKOUT) is a divided clock of HCLK.  
 For more information about setting of clock divider, see Chapter 14: External Bus Interface in FM4 Family Peripheral Manual Main Part (002-04856).

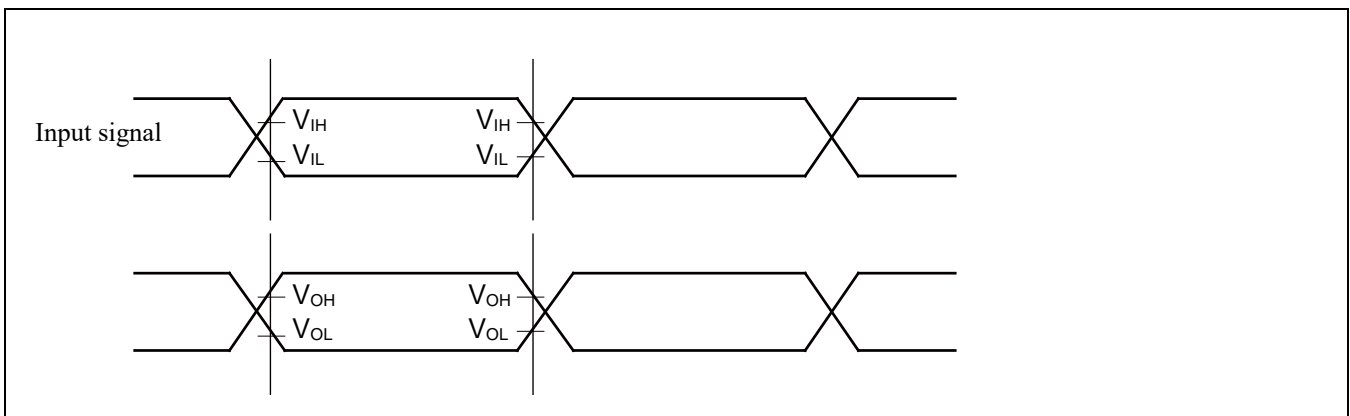
\*2: Generate MCLKOUT at setting more than four divisions when the AHB bus clock exceeds 100 MHz.



External Bus Signal I/O Characteristics

(V<sub>CC</sub> = 2.7 V to 5.5 V, V<sub>SS</sub> = 0 V)

Parameter	Symbol	Conditions	Value	Unit	Remarks
Signal input characteristics	V <sub>IH</sub>	-	0.8 x V <sub>CC</sub>	V	
	V <sub>IL</sub>		0.2 x V <sub>CC</sub>	V	
Signal output characteristics	V <sub>OH</sub>		0.8 x V <sub>CC</sub>	V	
	V <sub>OL</sub>		0.2 x V <sub>CC</sub>	V	

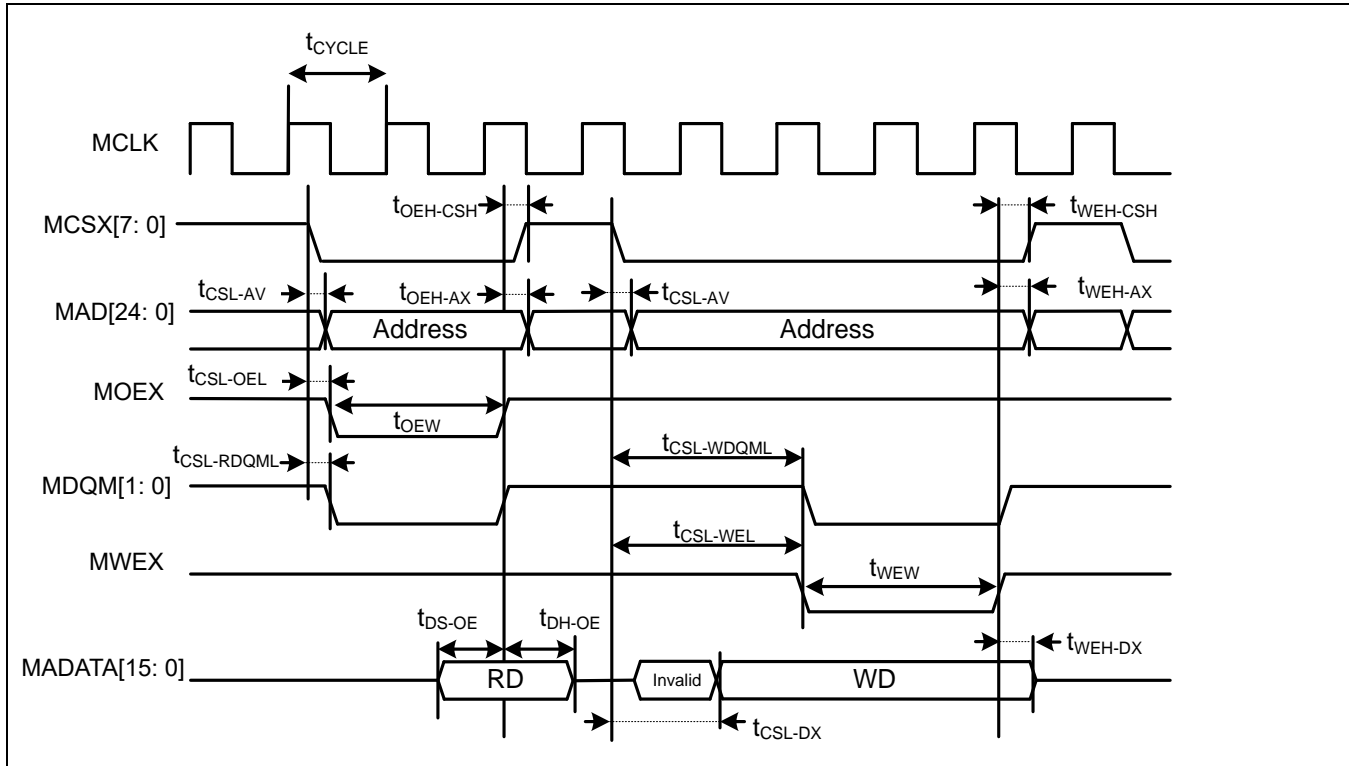


**Separate Bus Access Asynchronous SRAM Mode**
*(V<sub>CC</sub> = 2.7 V to 5.5 V, V<sub>SS</sub> = 0 V)*

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
MOEX Minimum pulse width	t <sub>OE</sub>	MOEX	-	MCLK×n-3	-	ns	
MCSX ↓ → Address output delay time	t <sub>CSL - AV</sub>	MCSX[7: 0], MAD[24: 0]	-	-9	+9	ns	
MOEX ↑ → Address hold time	t <sub>OEH - AX</sub>	MOEX, MAD[24: 0]	-	0	MCLK×m+9	ns	
MCSX ↓ → MOEX ↓ delay time	t <sub>CSL - OEL</sub>	MOEX, MCSX[7: 0]	-	MCLK×m-9	MCLK×m+9	ns	
MOEX ↑ → MCSX ↑ time	t <sub>OEH - CSH</sub>		-	0	MCLK×m+9	ns	
MCSX ↓ → MDQM ↓ delay time	t <sub>CSL - RDQML</sub>	MCSX, MDQM[3: 0]	-	MCLK×m-9	MCLK×m+9	ns	
Data set up → MOEX ↑ time	t <sub>DS - OE</sub>	MOEX, MADATA[31: 0]	-	20	-	ns	
MOEX ↑ → Data hold time	t <sub>DH - OE</sub>	MOEX, MADATA[31: 0]	-	0	-	ns	
MWEX Minimum pulse width	t <sub>WE</sub>	MWEX	-	MCLK×n-3	-	ns	
MWEX ↑ → Address output delay time	t <sub>WEH - AX</sub>	MWEX, MAD[24: 0]	-	0	MCLK×m+9	ns	
MCSX ↓ → MWEX ↓ delay time	t <sub>CSL - WEL</sub>	MWEX, MCSX[7: 0]	-	MCLK×n-9	MCLK×n+9	ns	
MWEX ↑ → MCSX ↑ delay time	t <sub>WEH - CSH</sub>		-	0	MCLK×m+9	ns	
MCSX ↓ → MDQM ↓ delay time	t <sub>CSL - WDQML</sub>	MCSX, MDQM[3: 0]	-	MCLK×n-9	MCLK×n+9	ns	
MCSX ↓ → Data output time	t <sub>CSL - DX</sub>	MCSX, MADATA[31: 0]	-	MCLK-9	MCLK+9	ns	
MWEX ↑ → Data hold time	t <sub>WEH - DX</sub>	MWEX, MADATA[31: 0]	-	0	MCLK×m+9	ns	

**Note:**

- When the external load capacitance C<sub>L</sub> = 30 pF (m = 0 to 15, n = 1 to 16)

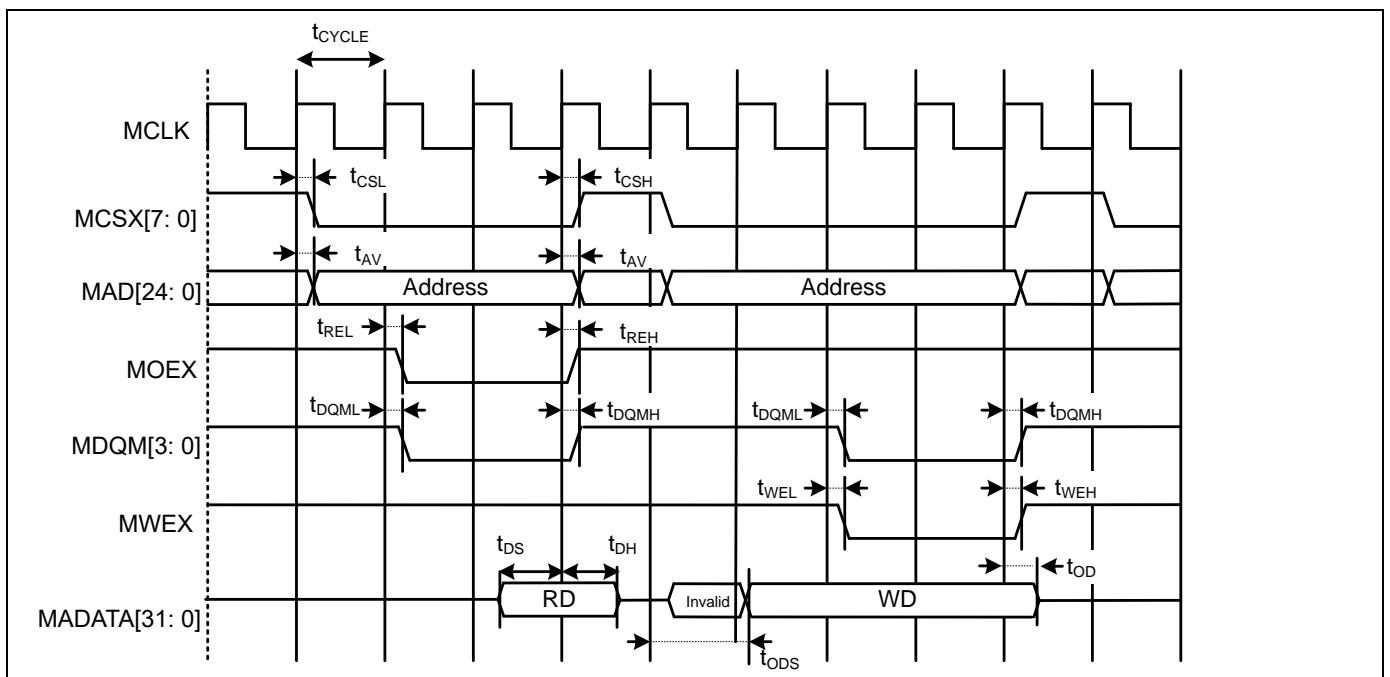


**Separate Bus Access Synchronous SRAM Mode**
 $(V_{CC} = 2.7\text{ V to } 5.5\text{ V}, V_{SS} = 0\text{ V})$ 

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Address delay time	$t_{AV}$	MCLK, MAD[24: 0]	-	1	9	ns	
MCSX delay time	$t_{CSL}$	MCLK, MCSX[7: 0]	-	1	9	ns	
	$t_{CSH}$		-	1	9	ns	
MOEX delay time	$t_{REL}$	MCLK, MOEX	-	1	9	ns	
	$t_{REH}$		-	1	9	ns	
Data set up →MCLK ↑ time	$t_{DS}$	MCLK, MADATA[31: 0]	-	19	-	ns	
MCLK ↑ → Data hold time	$t_{DH}$	MCLK, MADATA[31: 0]	-	0	-	ns	
MWEX delay time	$t_{WEL}$	MCLK, MWEX	-	1	9	ns	
	$t_{WEH}$		-	1	9	ns	
MDQM[1: 0] delay time	$t_{DQML}$	MCLK, MDQM[3: 0]	-	1	9	ns	
	$t_{DQMH}$		-	1	9	ns	
MCLK ↑ → Data output time	$t_{ODS}$	MCLK, MADATA[31: 0]	-	MCLK + 1	MCLK + 18	ns	
MCLK ↑ → Data hold time	$t_{OD}$	MCLK, MADATA[31: 0]	-	1	18	ns	

**Note:**

- When the external load capacitance  $C_L = 30\text{ pF}$



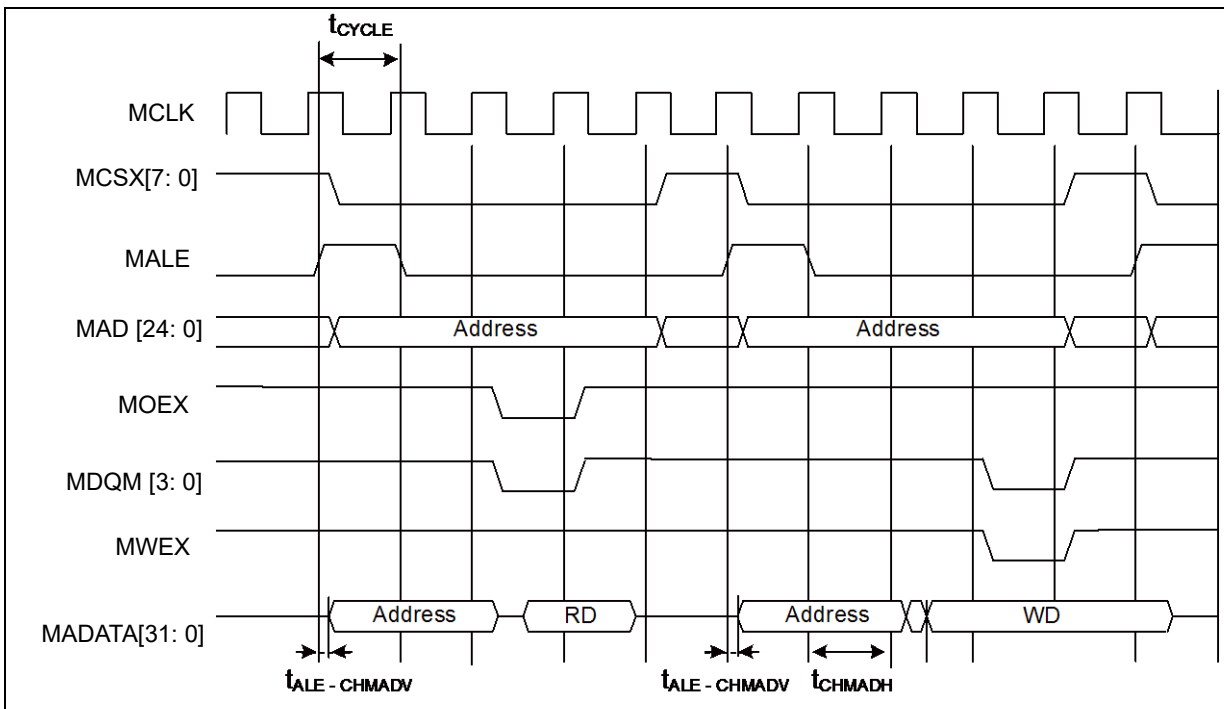
**Multiplexed Bus Access Asynchronous SRAM Mode**

 (V<sub>CC</sub> = 2.7 V to 5.5 V, V<sub>SS</sub> = 0 V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Multiplexed address delay time	t <sub>ALE-CHMADV</sub>	MALE, MAD[24: 0]	-	0	10	ns	
Multiplexed address hold time	t <sub>CHMADH</sub>		-	MCLK × n + 0	MCLK × n + 10	ns	

**Note:**

- When the external load capacitance C<sub>L</sub> = 30 pF (m = 0 to 15, n = 1 to 16)



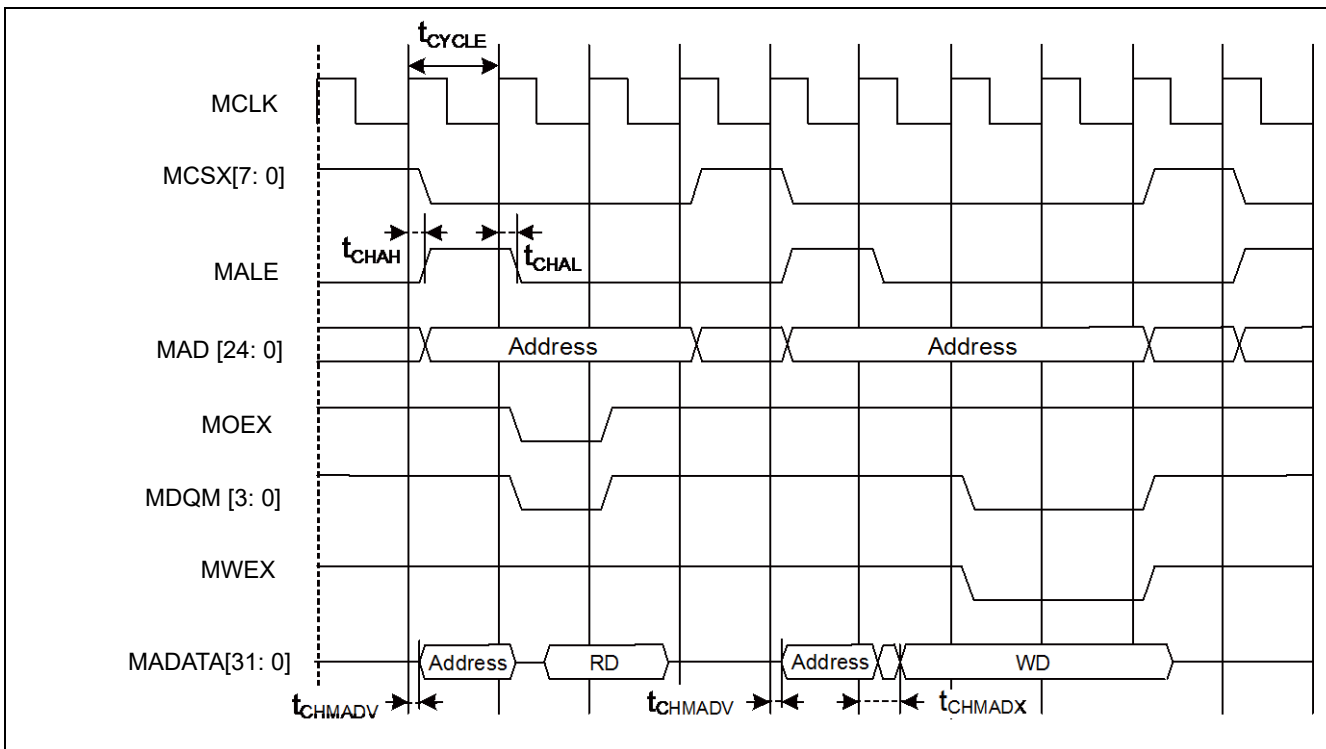
**Multiplexed Bus Access Synchronous SRAM Mode**

 ( $V_{CC} = 2.7\text{ V to }5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
MALE delay time	$t_{CHAL}$	MCLK, MALE	-	1	9		
	$t_{CHAH}$		-	1	9		
MCLK $\uparrow$ $\rightarrow$ Multiplexed address delay time	$t_{CHMADV}$	MCLK, MADATA[31: 0]	-	1	$t_{OD}$	ns	
MCLK $\uparrow$ $\rightarrow$ Multiplexed data output time	$t_{CHMADX}$		-	1	$t_{OD}$	ns	

**Note:**

- When the external load capacitance  $C_L = 30\text{ pF}$



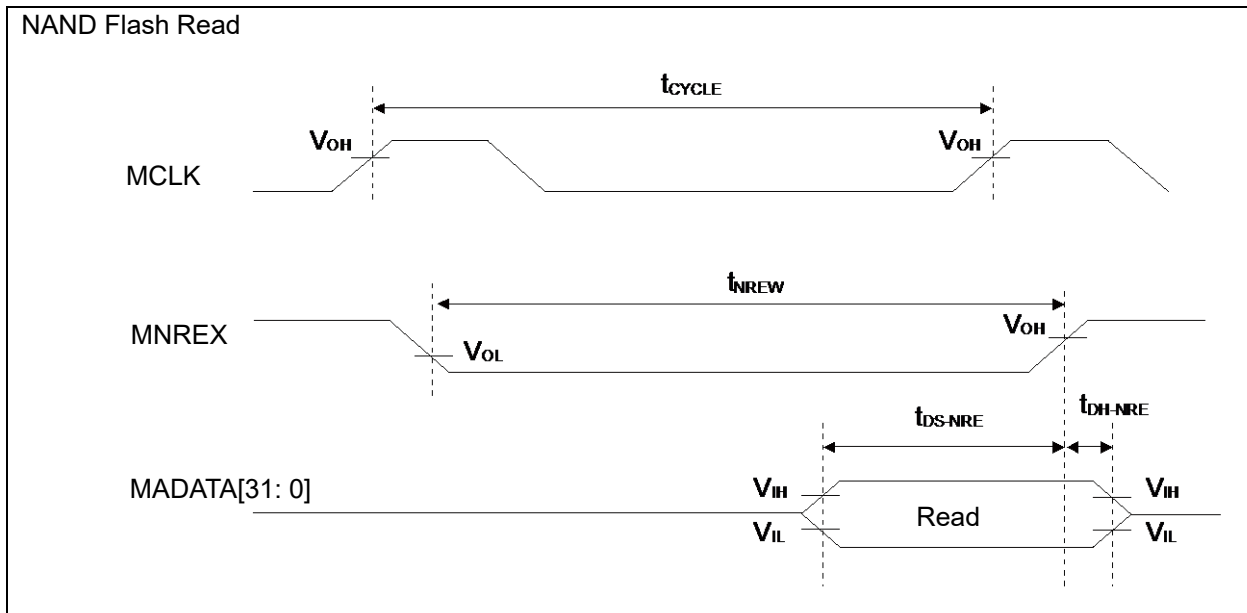
NAND Flash Mode

( $V_{CC} = 2.7\text{ V to } 5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

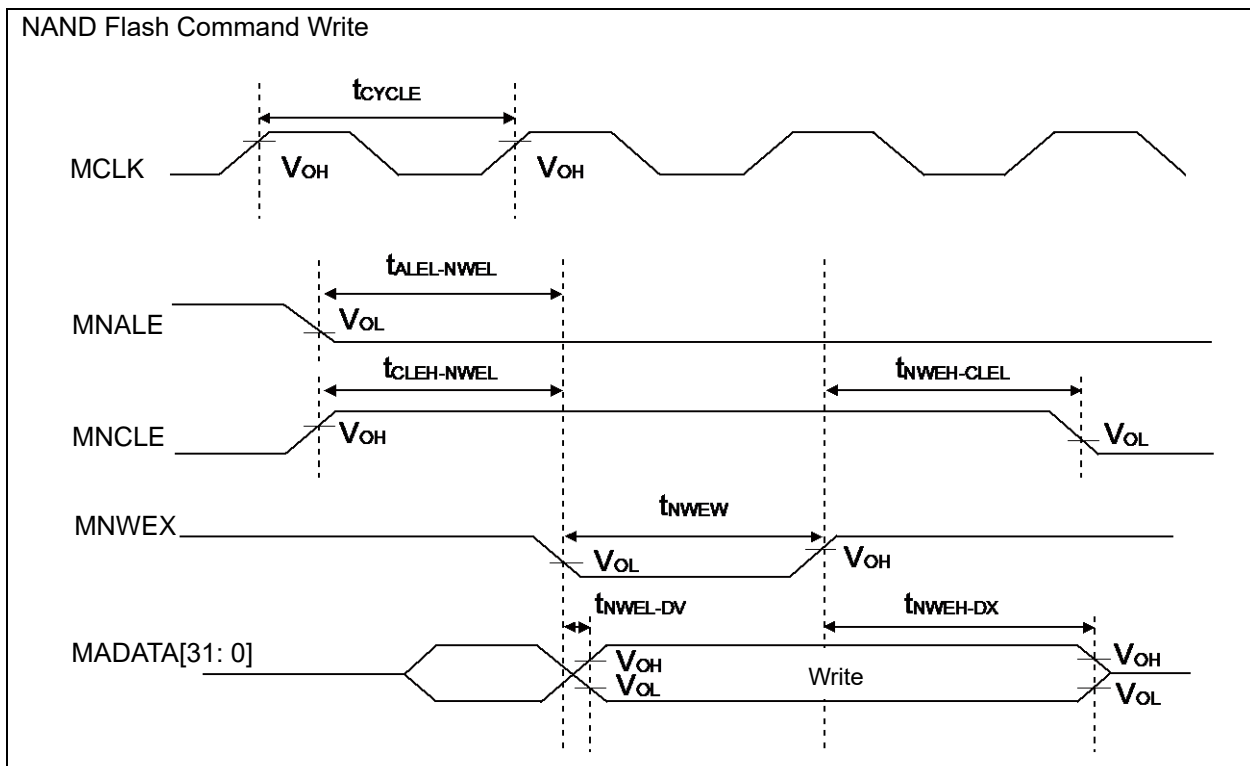
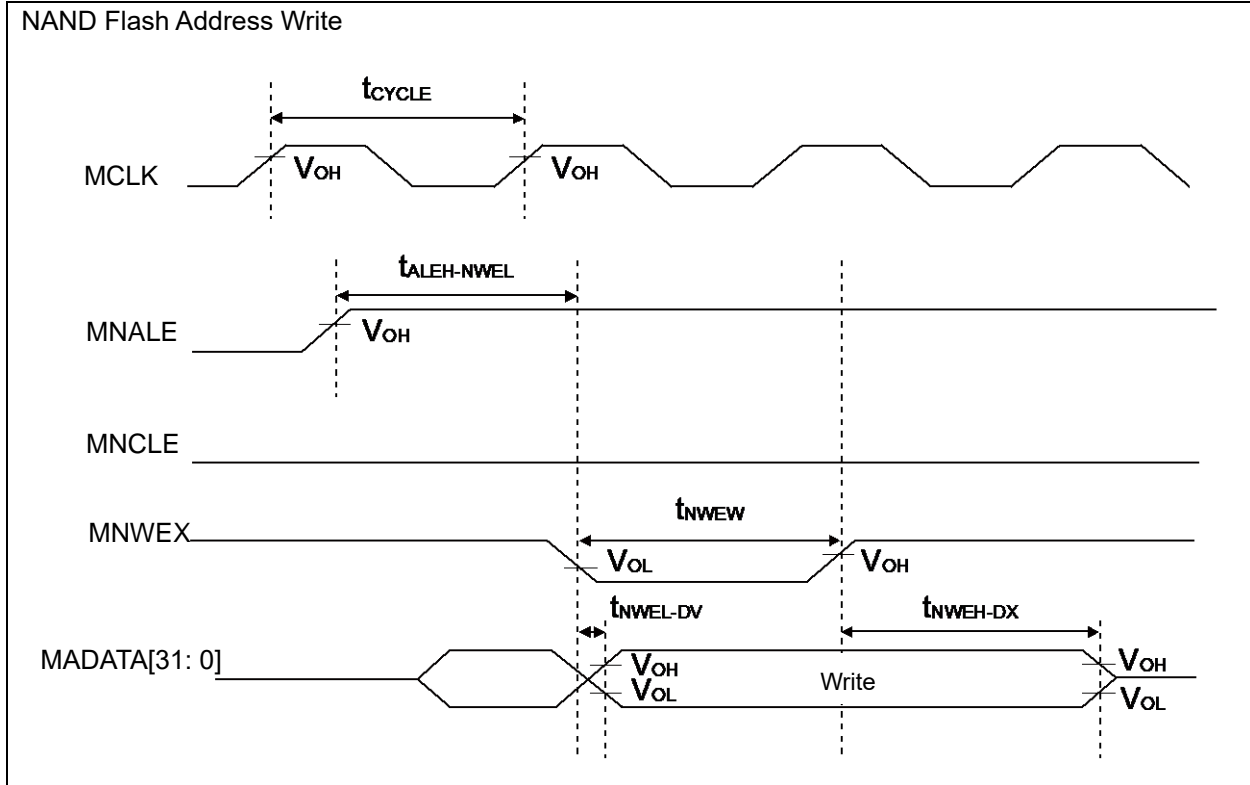
Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
MNREX Min pulse width	$t_{NREW}$	MNREX	-	$MCLK \times n - 3$	-	ns	
Data set up →MNREX ↑ time	$t_{DS-NRE}$	MNREX, MADATA[31: 0]	-	20	-	ns	
MNREX ↑ → Data hold time	$t_{DH-NRE}$	MNREX, MADATA[31: 0]	-	0	-	ns	
MNALE ↑ → MNWEX delay time	$t_{ALEH-NWEL}$	MNALE, MNWEX	-	$MCLK \times m - 9$	$MCLK \times m + 9$	ns	
MNALE ↓ → MNWEX delay time	$t_{ALEL-NWEL}$	MNALE, MNWEX	-	$MCLK \times m - 9$	$MCLK \times m + 9$	ns	
MNCLE ↑ → MNWEX delay time	$t_{CLEH-NWEL}$	MNCLE, MNWEX	-	$MCLK \times m - 9$	$MCLK \times m + 9$	ns	
MNWEH ↑ → MNCLE delay time	$t_{NWEH-CLEL}$	MNCLE, MNWEX	-	0	$MCLK \times m + 9$	ns	
MNWEH Min pulse width	$t_{NWEW}$	MNWEH	-	$MCLK \times n - 3$	-	ns	
MNWEH ↓ → Data output time	$t_{NWEH-DV}$	MNWEH, MADATA[31: 0]	-	-9	9	ns	
MNWEH ↑ → Data hold time	$t_{NWEH-DX}$	MNWEH, MADATA[31: 0]	-	0	$MCLK \times m + 9$	ns	

Note:

- When the external load capacitance  $C_L = 30\text{ pF}$  ( $m = 0\text{ to } 15$ ,  $n = 1\text{ to } 16$ )



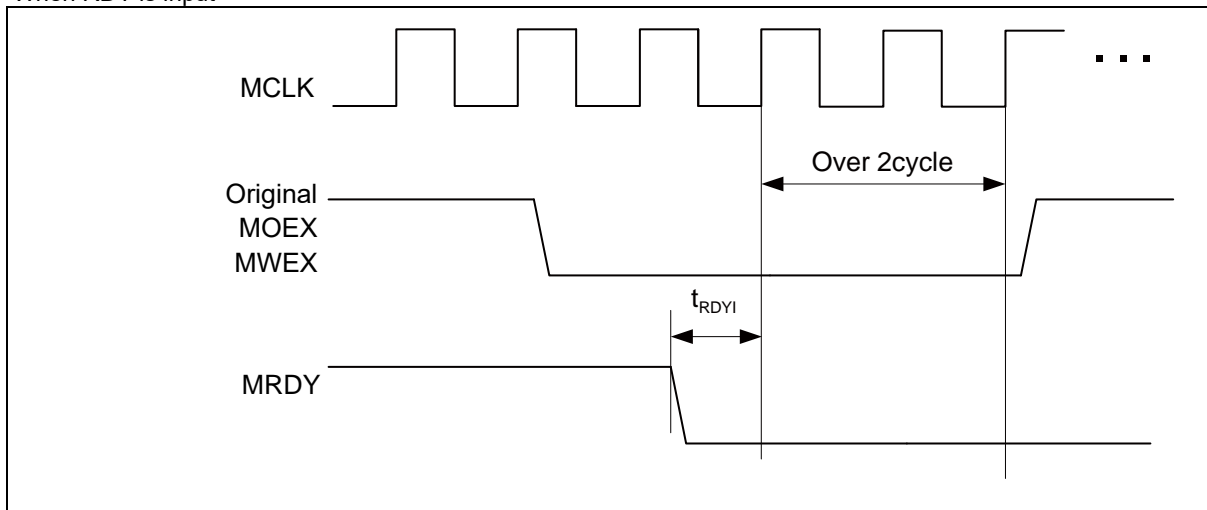
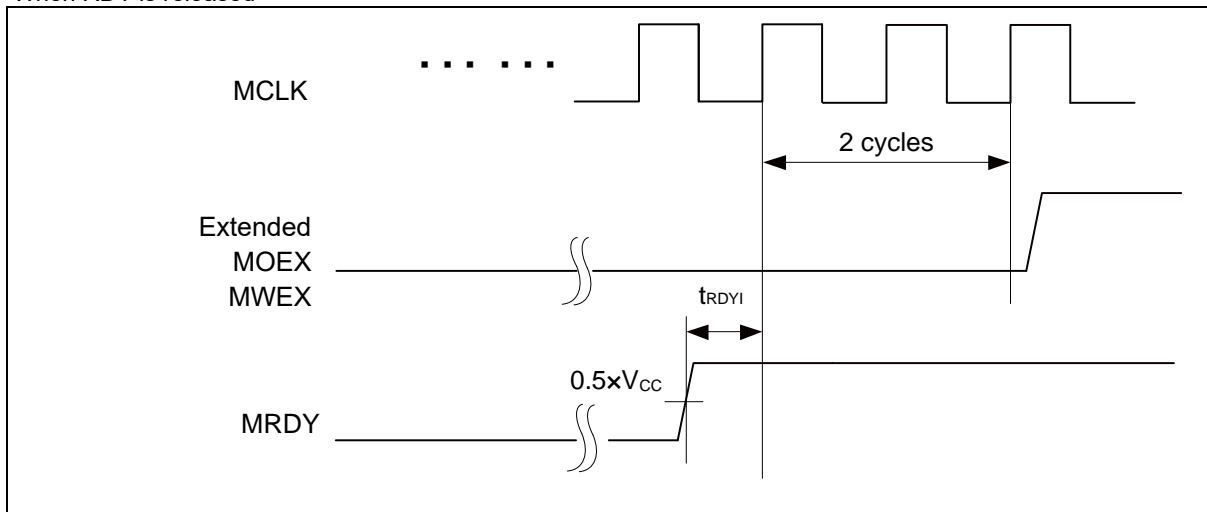




**External Ready Input Timing**

 (V<sub>CC</sub> = 2.7 V to 5.5 V, V<sub>SS</sub> = 0 V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
MCLK↑ MRDY input setup time	t <sub>RDYI</sub>	MCLK, MRDY	-	19	-	ns	

**■ When RDY is input**

**■ When RDY is released**


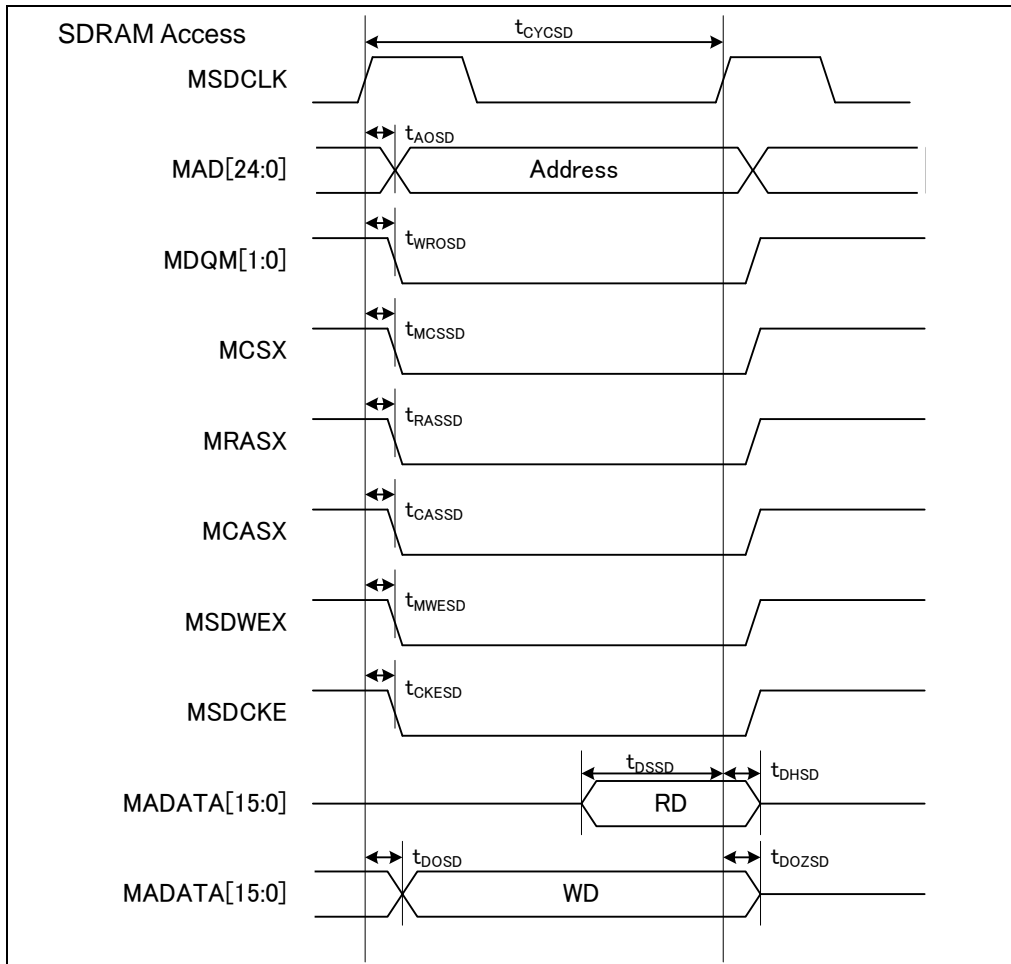
**SDRAM Mode**

 (V<sub>CC</sub> = 2.7 V to 3.6 V, V<sub>SS</sub> = 0 V)

Parameter	Symbol	Pin Name	Value	Unit		Unit	Remarks
				Min	Max		
Output frequency	t <sub>CYCSD</sub>	MSDCLK	-	-	50	MHz	
Address delay time	t <sub>AOSD</sub>	MSDCLK, MAD[15: 0]	-	2	12	ns	
MSDCLK ↑ → Data output delay time	t <sub>DOSD</sub>	MSDCLK, MADATA[31: 0]	-	2	12	ns	
MSDCLK ↑ → Data output Hi-Z time	t <sub>DOZSD</sub>	MSDCLK, MADATA[31: 0]	-	2	19.5	ns	
MDQM[3: 0] delay time	t <sub>WROSD</sub>	MSDCLK, MDQM[1: 0]	-	1	12	ns	
MCSX delay time	t <sub>MCSSD</sub>	MSDCLK, MCSX8	-	2	12	ns	
MRASX delay time	t <sub>RASSD</sub>	MSDCLK, MRASX	-	2	12	ns	
MCASX delay time	t <sub>CASSD</sub>	MSDCLK, MCASX	-	2	12	ns	
MSDWEX delay time	t <sub>MWESD</sub>	MSDCLK, MSDWEX	-	2	12	ns	
MSDCKE delay time	t <sub>CKESD</sub>	MSDCLK, MSDCKE	-	2	12	ns	
Data set up time	t <sub>DSSD</sub>	MSDCLK, MADATA[31: 0]	-	19	-	ns	
Data hold time	t <sub>DHSD</sub>	MSDCLK, MADATA[31: 0]	-	0	-	ns	

**Note:**

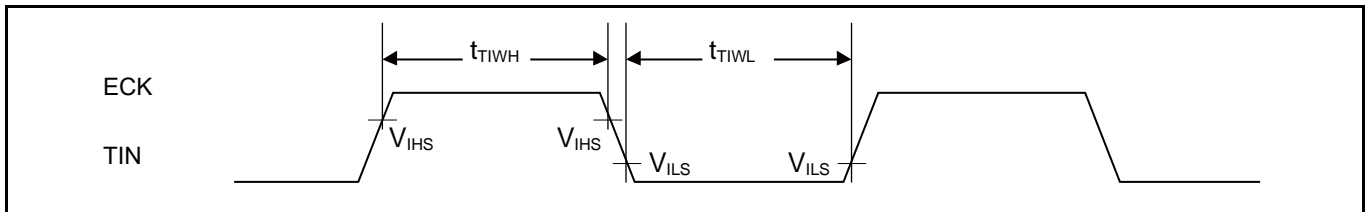
- When the external load capacitance C<sub>L</sub> = 30 pF



**12.4.11 Base Timer Input Timing**
**Timer Input Timing**

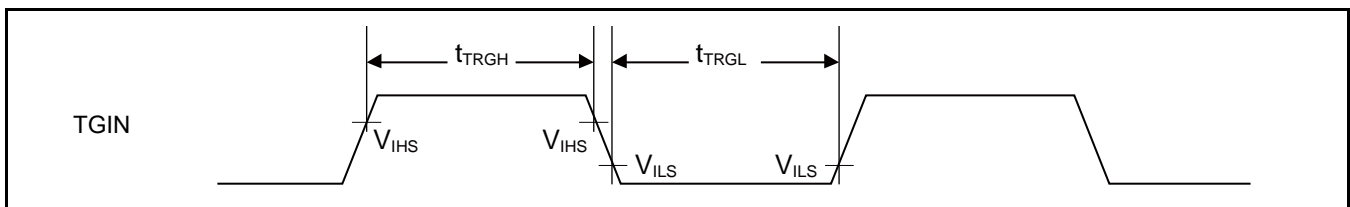
 (V<sub>CC</sub> = 2.7 V to 5.5 V, V<sub>SS</sub> = 0 V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t <sub>TIWH</sub> , t <sub>TIWL</sub>	TIOAn/TIOBn (when using as ECK, TIN)	-	2t <sub>CYCP</sub>	-	ns	


**Trigger Input Timing**

 (V<sub>CC</sub> = 2.7V to 5.5V, V<sub>SS</sub> = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t <sub>TRGH</sub> , t <sub>TRGL</sub>	TIOAn/TIOBn (when using as TGIN)	-	2t <sub>CYCP</sub>	-	ns	


**Note:**

- t<sub>CYCP</sub> indicates the APB bus clock cycle time. For more information about the APB bus number to which the base timer is connected, see 8. Block Diagram in this data sheet.

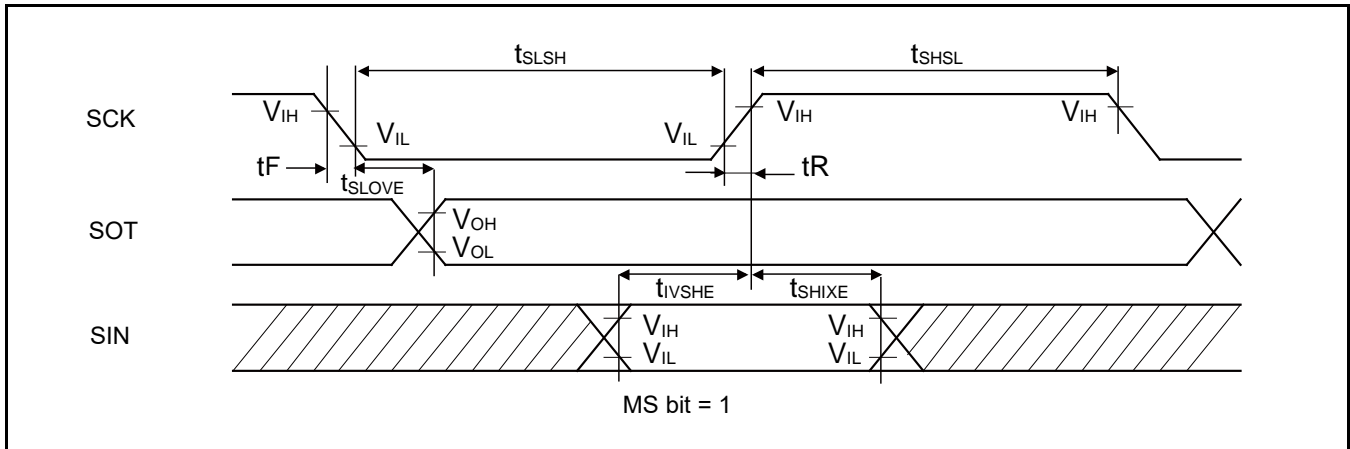
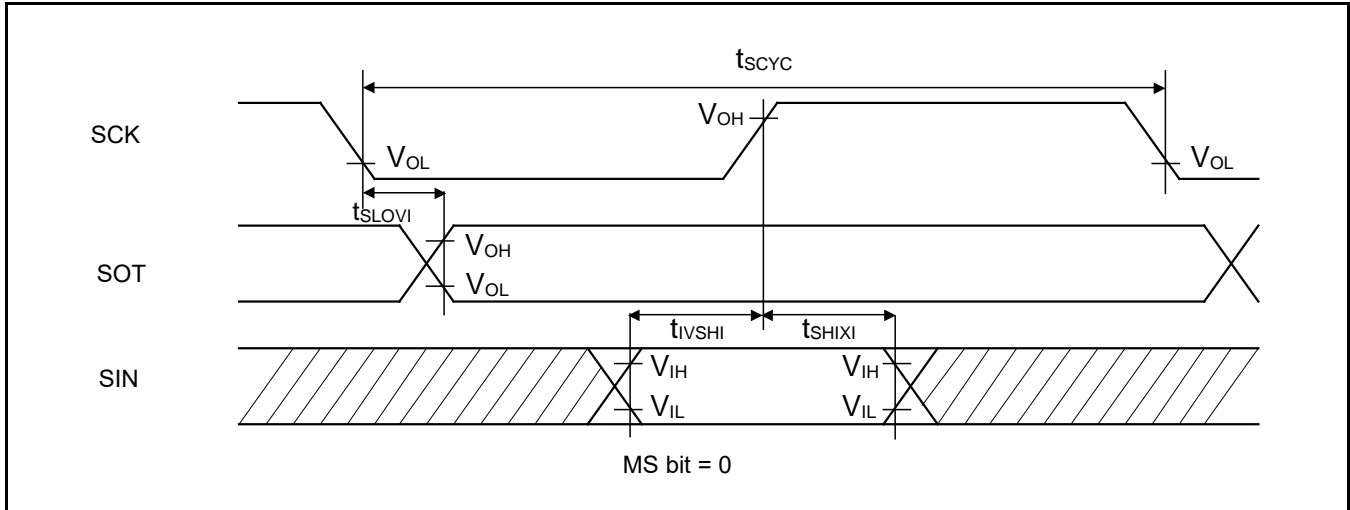
**12.4.12 CSIO (SPI) Timing**
**Synchronous Serial (SPI = 0, SCINV = 0)**

 (V<sub>CC</sub> = 2.7 V to 5.5 V, V<sub>SS</sub> = 0 V)

Parameter	Symbol	Pin Name	Conditions	V <sub>CC</sub> < 4.5 V		V <sub>CC</sub> ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Baud rate	-	-		-	8	-	8	Mbps
Serial clock cycle time	t <sub>SCYC</sub>	SCKx	Internal shift clock operation	4t <sub>CYCP</sub>	-	4t <sub>CYCP</sub>	-	ns
SCK↓→SOT delay time	t <sub>SLOVI</sub>	SCKx, SOTx		-30	+30	-20	+20	ns
SIN→SCK↑ setup time	t <sub>IVSHI</sub>	SCKx, SINx		50	-	30	-	ns
SCK↑→SIN hold time	t <sub>SHIXI</sub>	SCKx, SINx		0	-	0	-	ns
Serial clock L pulse width	t <sub>SLSH</sub>	SCKx		2t <sub>CYCP</sub> - 10	-	2t <sub>CYCP</sub> - 10	-	ns
Serial clock H pulse width	t <sub>SHSL</sub>	SCKx	t <sub>CYCP</sub> + 10	-	t <sub>CYCP</sub> + 10	-	ns	
SCK↓→SOT delay time	t <sub>SLOVE</sub>	SCKx, SOTx	External shift clock operation	-	50	-	30	ns
SIN→SCK↑ setup time	t <sub>IVSHE</sub>	SCKx, SINx		10	-	10	-	ns
SCK↑→SIN hold time	t <sub>SHIXE</sub>	SCKx, SINx		20	-	20	-	ns
SCK fall time	t <sub>F</sub>	SCKx		-	5	-	5	ns
SCK rise time	t <sub>R</sub>	SCKx		-	5	-	5	ns

**Notes:**

- The above characteristics apply to CLK synchronous mode.
- t<sub>CYCP</sub> indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 8. Block Diagram in this data sheet.
- These characteristics only guarantee the same relocate port number; for example, the combination of SCKx\_0 and SOTx\_1 is not guaranteed.
- When the external load capacitance C<sub>L</sub> = 30 pF.



**Synchronous Serial (SPI = 0, SCINV = 1)**

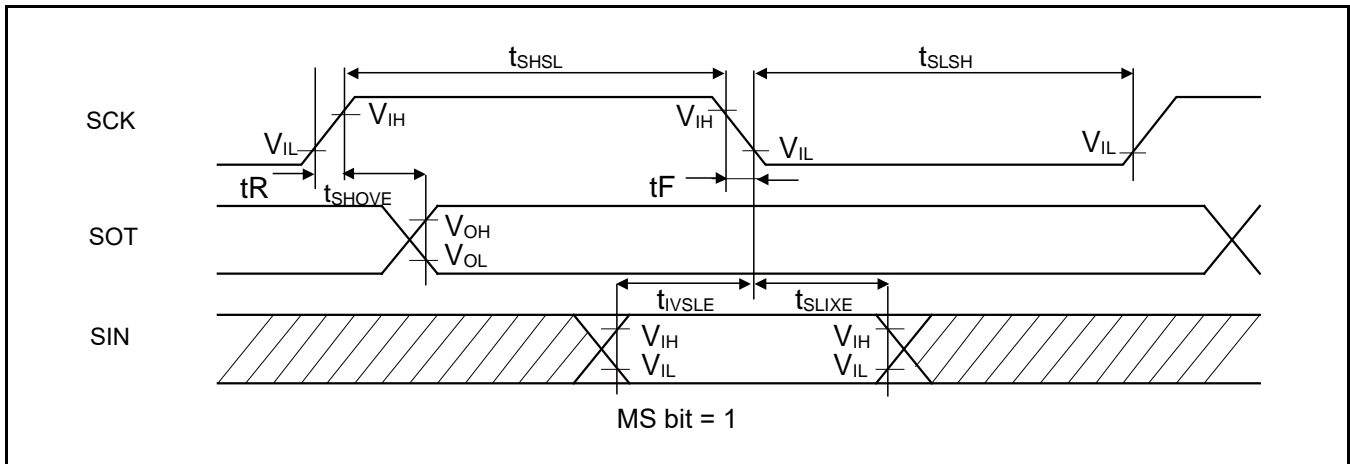
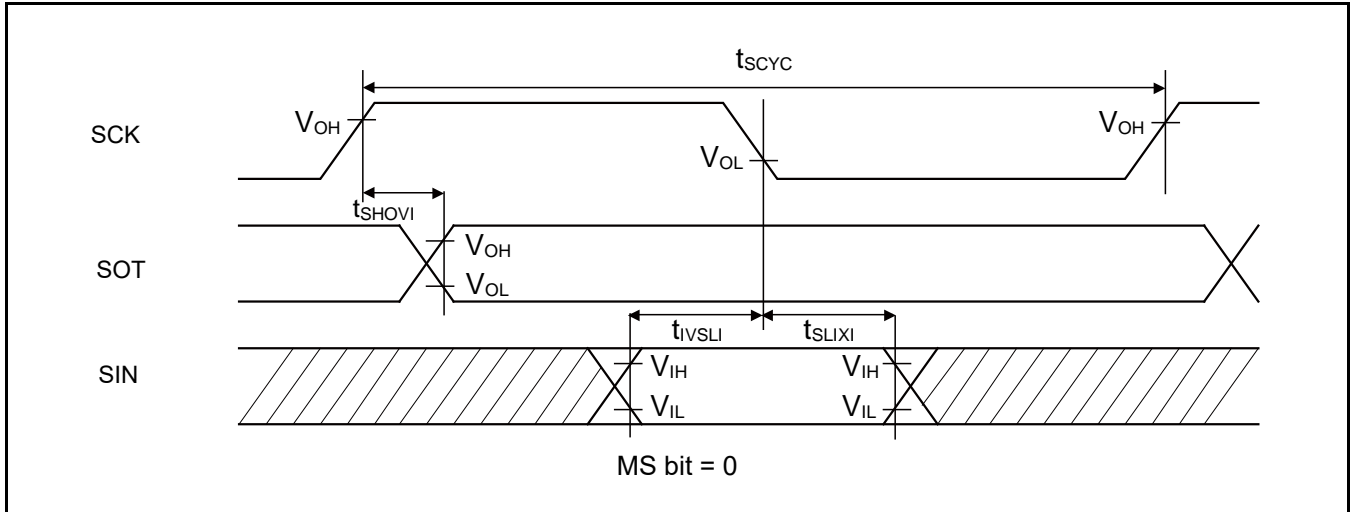
 (V<sub>CC</sub> = 2.7 V to 5.5 V, V<sub>SS</sub> = 0 V)

Parameter	Symbol	Pin Name	Conditions	V <sub>CC</sub> < 4.5 V		V <sub>CC</sub> ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Baud rate	-	-	-	-	8	-	8	Mbps
Serial clock cycle time	t <sub>SCYC</sub>	SCKx	Internal shift clock operation	4t <sub>CYCP</sub>	-	4t <sub>CYCP</sub>	-	ns
SCK↑→SOT delay time	t <sub>SHOVI</sub>	SCKx, SOTx		-30	+30	-20	+20	ns
SIN→SCK↓ setup time	t <sub>IVSLI</sub>	SCKx, SINx		50	-	30	-	ns
SCK↓→SIN hold time	t <sub>SLIXI</sub>	SCKx, SINx		0	-	0	-	ns
Serial clock L pulse width	t <sub>SLSH</sub>	SCKx		2t <sub>CYCP</sub> - 10	-	2t <sub>CYCP</sub> - 10	-	ns
Serial clock H pulse width	t <sub>SHSL</sub>	SCKx	t <sub>CYCP</sub> + 10	-	t <sub>CYCP</sub> + 10	-	ns	
SCK↑→SOT delay time	t <sub>SHOVE</sub>	SCKx, SOTx	External shift clock operation	-	50	-	30	ns
SIN→SCK↓ setup time	t <sub>IVSLE</sub>	SCKx, SINx		10	-	10	-	ns
SCK↓→SIN hold time	t <sub>SLIXE</sub>	SCKx, SINx		20	-	20	-	ns
SCK fall time	t <sub>F</sub>	SCKx		-	5	-	5	ns
SCK rise time	t <sub>R</sub>	SCKx		-	5	-	5	ns

**Notes:**

- The above characteristics apply to CLK synchronous mode.
- t<sub>CYCP</sub> indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 8. Block Diagram in this data sheet.
- These characteristics only guarantee the same relocate port number; for example, the combination of SCKx\_0 and SOTx\_1 is not guaranteed.
- When the external load capacitance C<sub>L</sub> = 30 pF.





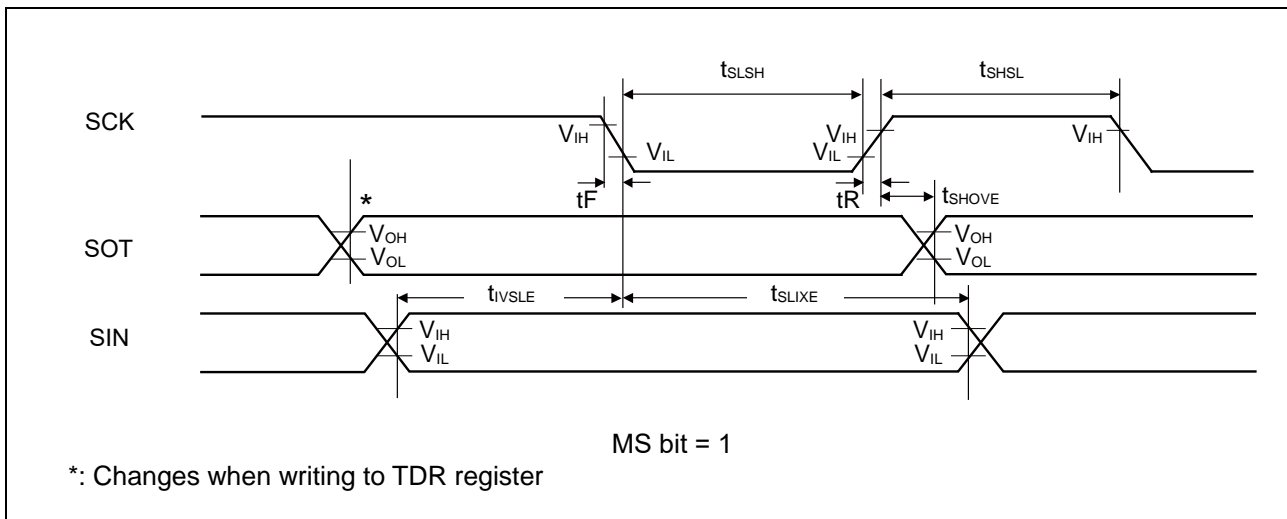
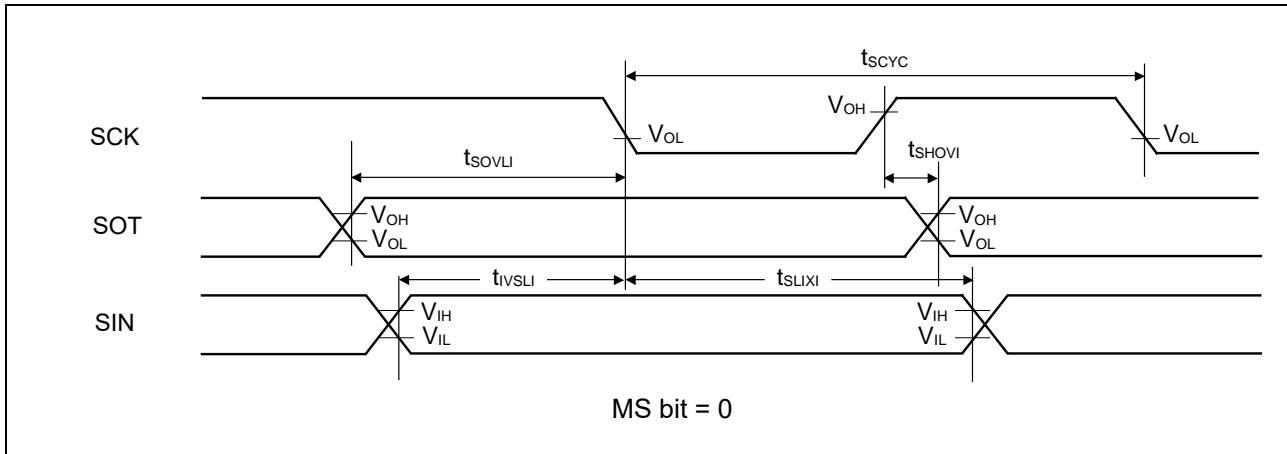
**Synchronous Serial (SPI = 1, SCINV = 0)**

 (V<sub>CC</sub> = 2.7 V to 5.5 V, V<sub>SS</sub> = 0 V)

Parameter	Symbol	Pin Name	Conditions	V <sub>CC</sub> < 4.5 V		V <sub>CC</sub> ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Baud rate	-	-	-	-	8	-	8	Mbps
Serial clock cycle time	t <sub>SCYC</sub>	SCKx	Internal shift clock operation	4t <sub>CYCP</sub>	-	4t <sub>CYCP</sub>	-	ns
SCK↑→SOT delay time	t <sub>SHOVI</sub>	SCKx, SOTx		-30	+30	-20	+20	ns
SIN→SCK↓ setup time	t <sub>IVSLI</sub>	SCKx, SINx		50	-	30	-	ns
SCK↓→SIN hold time	t <sub>SLIXI</sub>	SCKx, SINx		0	-	0	-	ns
SOT→SCK↓ delay time	t <sub>SOVLI</sub>	SCKx, SOTx		2t <sub>CYCP</sub> - 30	-	2t <sub>CYCP</sub> - 30	-	ns
Serial clock L pulse width	t <sub>LSLH</sub>	SCKx		2t <sub>CYCP</sub> - 10	-	2t <sub>CYCP</sub> - 10	-	ns
Serial clock H pulse width	t <sub>SHSL</sub>	SCKx	t <sub>CYCP</sub> + 10	-	t <sub>CYCP</sub> + 10	-	ns	
SCK↑→SOT delay time	t <sub>SHOVE</sub>	SCKx, SOTx	External shift clock operation	-	50	-	30	ns
SIN→SCK↓ setup time	t <sub>IVSLE</sub>	SCKx, SINx		10	-	10	-	ns
SCK↓→SIN hold time	t <sub>SLIXE</sub>	SCKx, SINx		20	-	20	-	ns
SCK fall time	t <sub>F</sub>	SCKx		-	5	-	5	ns
SCK rise time	t <sub>R</sub>	SCKx		-	5	-	5	ns

**Notes:**

- The above characteristics apply to CLK synchronous mode.
- t<sub>CYCP</sub> indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 8. Block Diagram in this data sheet.
- These characteristics only guarantee the same relocate port number; for example, the combination of SCKx\_0 and SOTx\_1 is not guaranteed.
- When the external load capacitance C<sub>L</sub> = 30 pF.



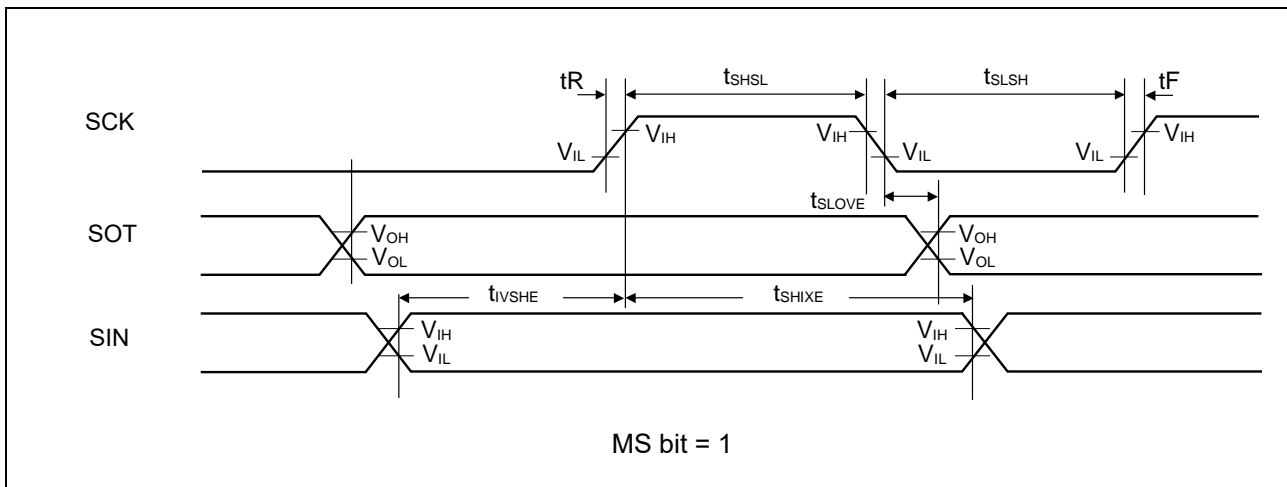
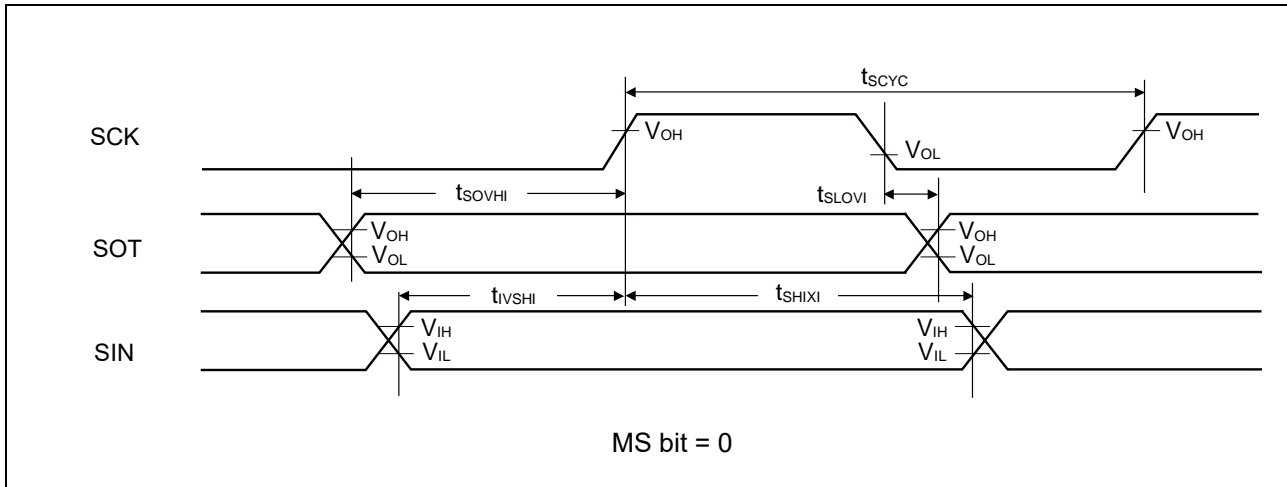
**Synchronous Serial (SPI = 1, SCINV = 1)**

 (V<sub>CC</sub> = 2.7 V to 5.5 V, V<sub>SS</sub> = 0 V)

Parameter	Symbol	Pin Name	Conditions	V <sub>CC</sub> < 4.5 V		V <sub>CC</sub> ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Baud rate	-	-	-	-	8	-	8	Mbps
Serial clock cycle time	t <sub>SCYC</sub>	SCKx	Internal shift clock operation	4t <sub>CYCP</sub>	-	4t <sub>CYCP</sub>	-	ns
SCK↓→SOT delay time	t <sub>SLOVI</sub>	SCKx, SOTx		-30	+30	-20	+20	ns
SIN→SCK↑ setup time	t <sub>VS</sub> HI	SCKx, SINx		50	-	30	-	ns
SCK↑→SIN hold time	t <sub>SHIXI</sub>	SCKx, SINx		0	-	0	-	ns
SOT→SCK↑ delay time	t <sub>SOVHI</sub>	SCKx, SOTx		2t <sub>CYCP</sub> - 30	-	2t <sub>CYCP</sub> - 30	-	ns
Serial clock L pulse width	t <sub>SLSH</sub>	SCKx		2t <sub>CYCP</sub> - 10	-	2t <sub>CYCP</sub> - 10	-	ns
Serial clock H pulse width	t <sub>SHSL</sub>	SCKx	t <sub>CYCP</sub> + 10	-	t <sub>CYCP</sub> + 10	-	ns	
SCK↓→SOT delay time	t <sub>SLOVE</sub>	SCKx, SOTx	External shift clock operation	-	50	-	30	ns
SIN→SCK↑ setup time	t <sub>VS</sub> HE	SCKx, SINx		10	-	10	-	ns
SCK↑→SIN hold time	t <sub>SHIXE</sub>	SCKx, SINx		20	-	20	-	ns
SCK fall time	t <sub>F</sub>	SCKx		-	5	-	5	ns
SCK rise time	t <sub>R</sub>	SCKx		-	5	-	5	ns

**Notes:**

- The above characteristics apply to CLK synchronous mode.
- t<sub>CYCP</sub> indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 8. Block Diagram in this data sheet.
- These characteristics only guarantee the same relocate port number; for example, the combination of SCKx\_0 and SOTx\_1 is not guaranteed.
- When the external load capacitance C<sub>L</sub> = 30 pF.



**When Using Synchronous Serial Chip Select (SCINV = 0, CSLVL = 1)**

 (V<sub>CC</sub> = 2.7 V to 5.5 V, V<sub>SS</sub> = 0 V)

Parameter	Symbol	Conditions	V <sub>CC</sub> < 4.5 V		V <sub>CC</sub> ≥ 4.5 V		Unit
			Min	Max	Min	Max	
SCS↓→SCK↓ setup time	t <sub>CSSI</sub>	Internal shift clock operation	(*1) - 50	(*1) + 0	(*1) - 50	(*1) + 0	ns
SCK↑→SCS↑ hold time	t <sub>CShI</sub>		(*2) + 0	(*2) + 50	(*2) + 0	(*2) + 50	ns
SCS deselect time	t <sub>CSDI</sub>		(*3) - 50 + 5t <sub>CYCP</sub>	(*3) + 50 + 5t <sub>CYCP</sub>	(*3) - 50 + 5t <sub>CYCP</sub>	(*3) + 50 + 5t <sub>CYCP</sub>	ns
SCS↓→SCK↓ setup time	t <sub>CSSE</sub>	External shift clock operation	3t <sub>CYCP</sub> + 30	-	3t <sub>CYCP</sub> + 30	-	ns
SCK↑→SCS↑ hold time	t <sub>CSHE</sub>		0	-	0	-	ns
SCS deselect time	t <sub>CSDE</sub>		3t <sub>CYCP</sub> + 30	-	3t <sub>CYCP</sub> + 30	-	ns
SCS↓→SOT delay time	t <sub>DSE</sub>		-	40	-	40	ns
SCS↑→SOT delay time	t <sub>DSE</sub>		0	-	0	-	ns

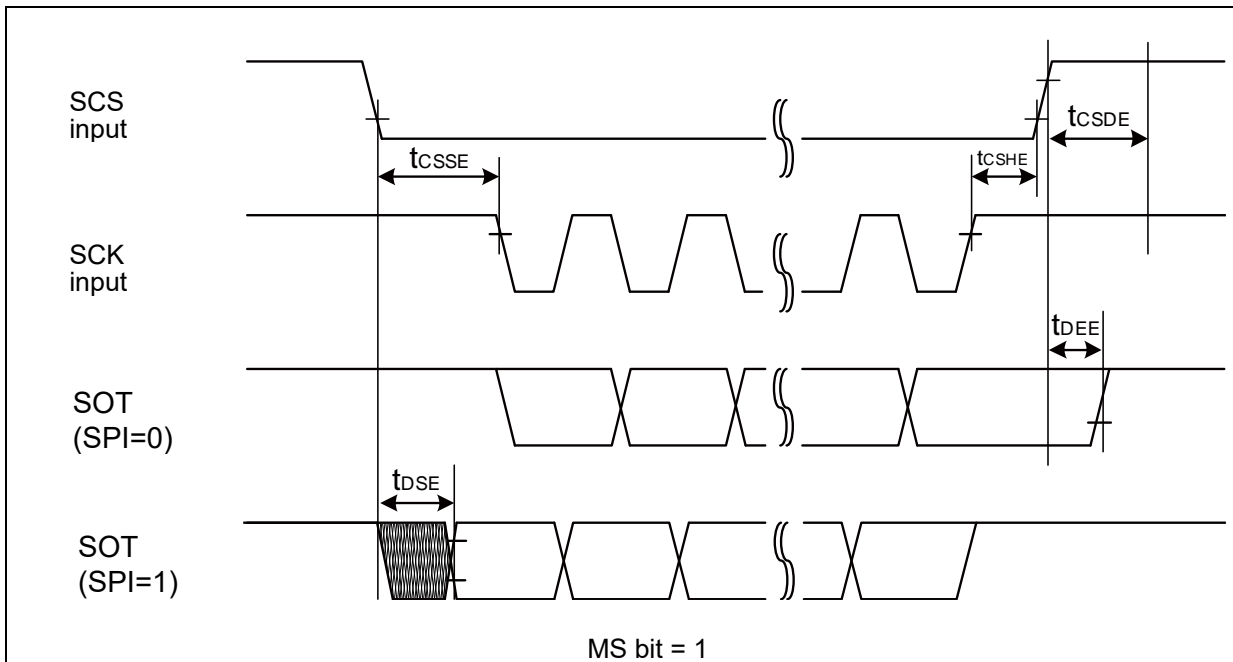
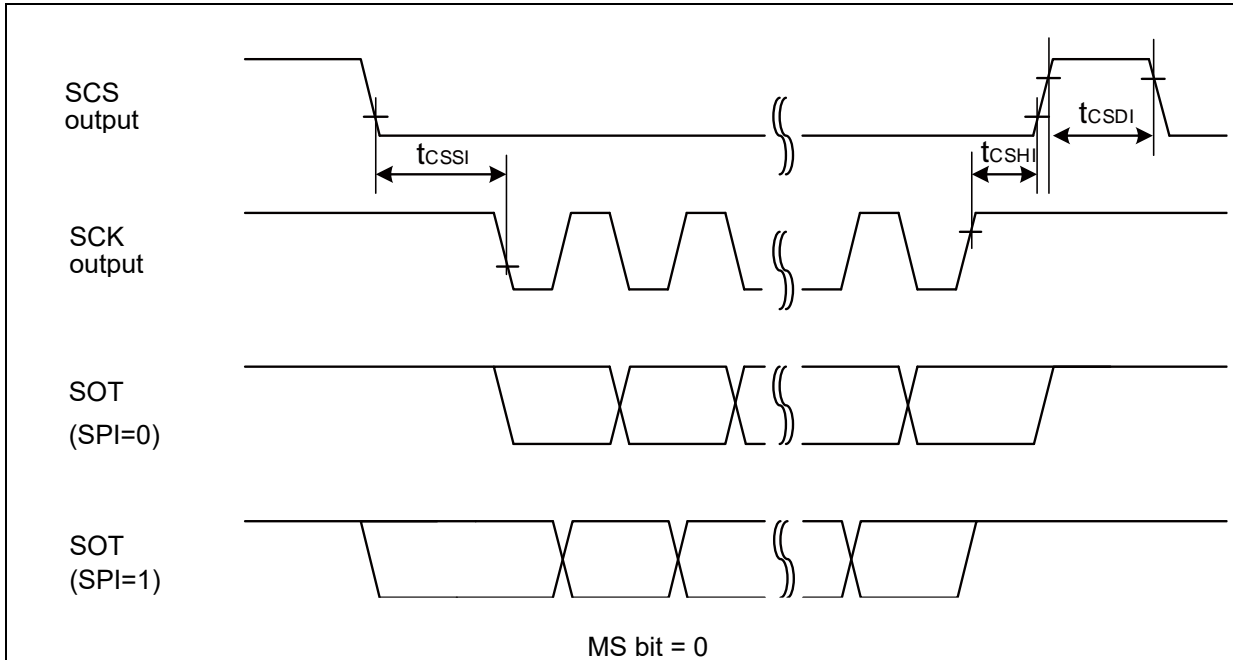
(\*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

(\*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

(\*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

**Notes:**

- t<sub>CYCP</sub> indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 8. Block Diagram in this data sheet.
- For more information about CSSU, CSHD, CSDS, and the serial chip select timing operating clock, see FM4 Family Peripheral Manual Main Part (002-04856).
- When the external load capacitance C<sub>L</sub> = 30 pF.



**When Using Synchronous Serial Chip Select (SCINV = 1, CSLVL = 1)**

 (V<sub>CC</sub> = 2.7 V to 5.5 V, V<sub>SS</sub> = 0 V)

Parameter	Symbol	Conditions	V <sub>CC</sub> < 4.5 V		V <sub>CC</sub> ≥ 4.5 V		Unit
			Min	Max	Min	Max	
SCS↓→SCK↓ setup time	t <sub>CSSI</sub>	Internal shift clock operation	(*1) - 50	(*1) + 0	(*1) - 50	(*1) + 0	ns
SCK↑→SCS↑ hold time	t <sub>CShI</sub>		(*2) + 0	(*2) + 50	(*2) + 0	(*2) + 50	ns
SCS deselect time	t <sub>CSDI</sub>		(*3) - 50 + 5t <sub>CYCP</sub>	(*3) + 50 + 5t <sub>CYCP</sub>	(*3) - 50 + 5t <sub>CYCP</sub>	(*3) + 50 + 5t <sub>CYCP</sub>	ns
SCS↓→SCK↓ setup time	t <sub>CSE</sub>	External shift clock operation	3t <sub>CYCP</sub> + 30	-	3t <sub>CYCP</sub> + 30	-	ns
SCK↑→SCS↑ hold time	t <sub>CSE</sub>		0	-	0	-	ns
SCS deselect time	t <sub>CSE</sub>		3t <sub>CYCP</sub> + 30	-	3t <sub>CYCP</sub> + 30	-	ns
SCS↓→SOT delay time	t <sub>DSE</sub>		-	40	-	40	ns
SCS↑→SOT delay time	t <sub>DEE</sub>		0	-	0	-	ns

(\*1): CSSU bit value × serial chip select timing operating clock cycle [ns]

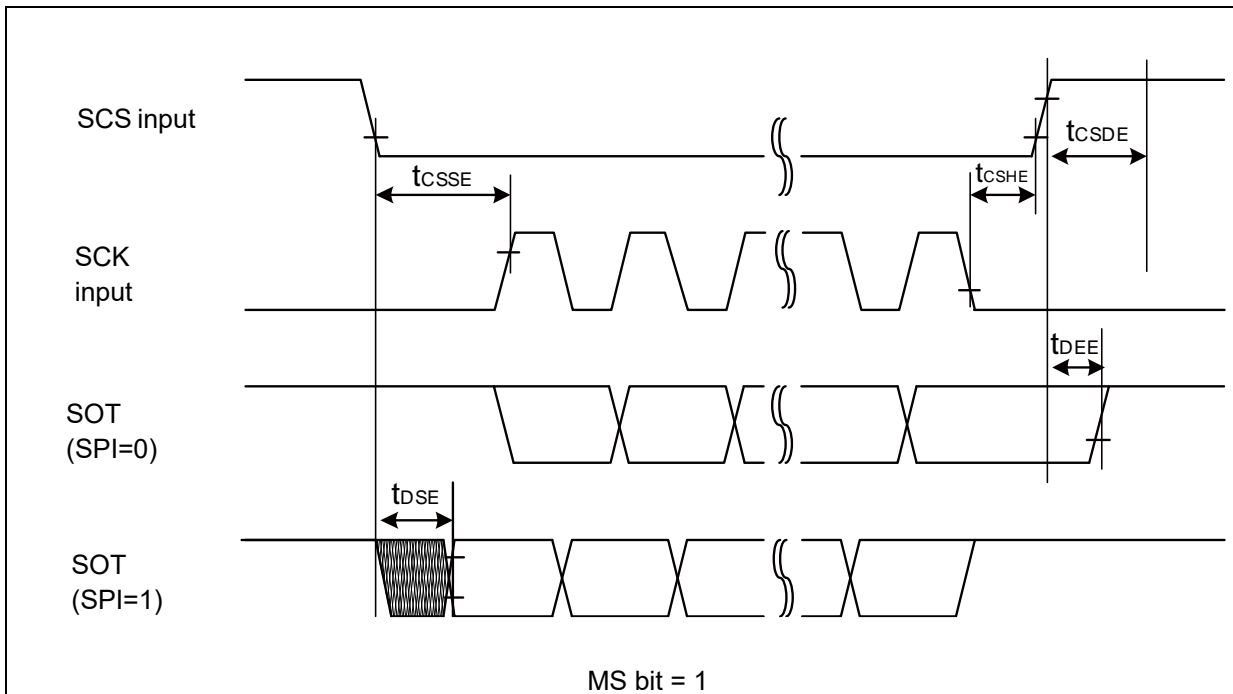
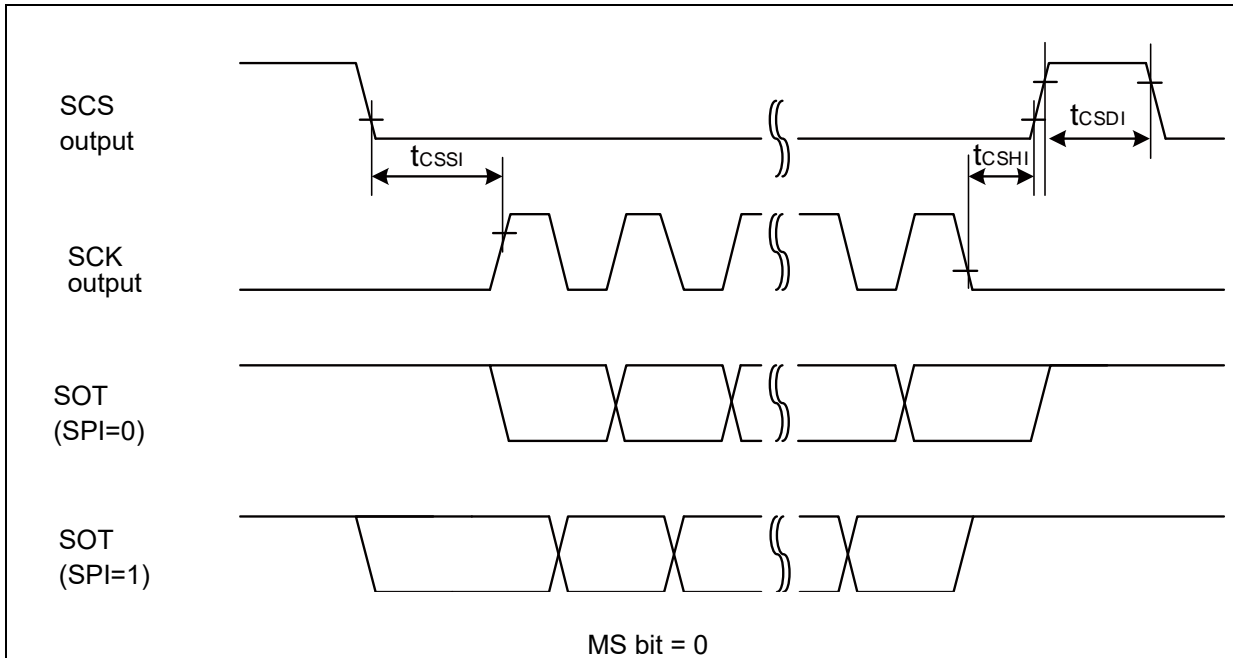
(\*2): CSHD bit value × serial chip select timing operating clock cycle [ns]

(\*3): CSDS bit value × serial chip select timing operating clock cycle [ns]

**Notes:**

- t<sub>CYCP</sub> indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 8. Block Diagram in this data sheet.
- For more information about CSSU, CSHD, CSDS, and the serial chip select timing operating clock, see FM4 Family Peripheral Manual Main Part (002-04856).
- When the external load capacitance C<sub>L</sub> = 30 pF.





## When Using Synchronous Serial Chip Select (SCINV = 0, CSLVL = 0)

(V<sub>CC</sub> = 2.7 V to 5.5 V, V<sub>SS</sub> = 0 V)

Parameter	Symbol	Conditions	V <sub>CC</sub> < 4.5 V		V <sub>CC</sub> ≥ 4.5 V		Unit
			Min	Max	Min	Max	
SCS↑→SCK↓ setup time	t <sub>CSSI</sub>	Internal shift clock operation	(*1) - 50	(*1) + 0	(*1) - 50	(*1) + 0	ns
SCK↑→SCS↓ hold time	t <sub>CSHI</sub>		(*2) + 0	(*2) + 50	(*2) + 0	(*2) + 50	ns
SCS deselect time	t <sub>CSDI</sub>		(*3) - 50 + 5t <sub>CYCP</sub>	(*3) + 50 + 5t <sub>CYCP</sub>	(*3) - 50 + 5t <sub>CYCP</sub>	(*3) + 50 + 5t <sub>CYCP</sub>	ns
SCS↑→SCK↓ setup time	t <sub>CSSE</sub>	External shift clock operation	3t <sub>CYCP</sub> + 30	-	3t <sub>CYCP</sub> + 30	-	ns
SCK↑→SCS↓ hold time	t <sub>CSHE</sub>		0	-	0	-	ns
SCS deselect time	t <sub>CSDE</sub>		3t <sub>CYCP</sub> + 30	-	3t <sub>CYCP</sub> + 30	-	ns
SCS↑→SOT delay time	t <sub>DSE</sub>		-	40	-	40	ns
SCS↓→SOT delay time	t <sub>DEE</sub>		0	-	0	-	ns

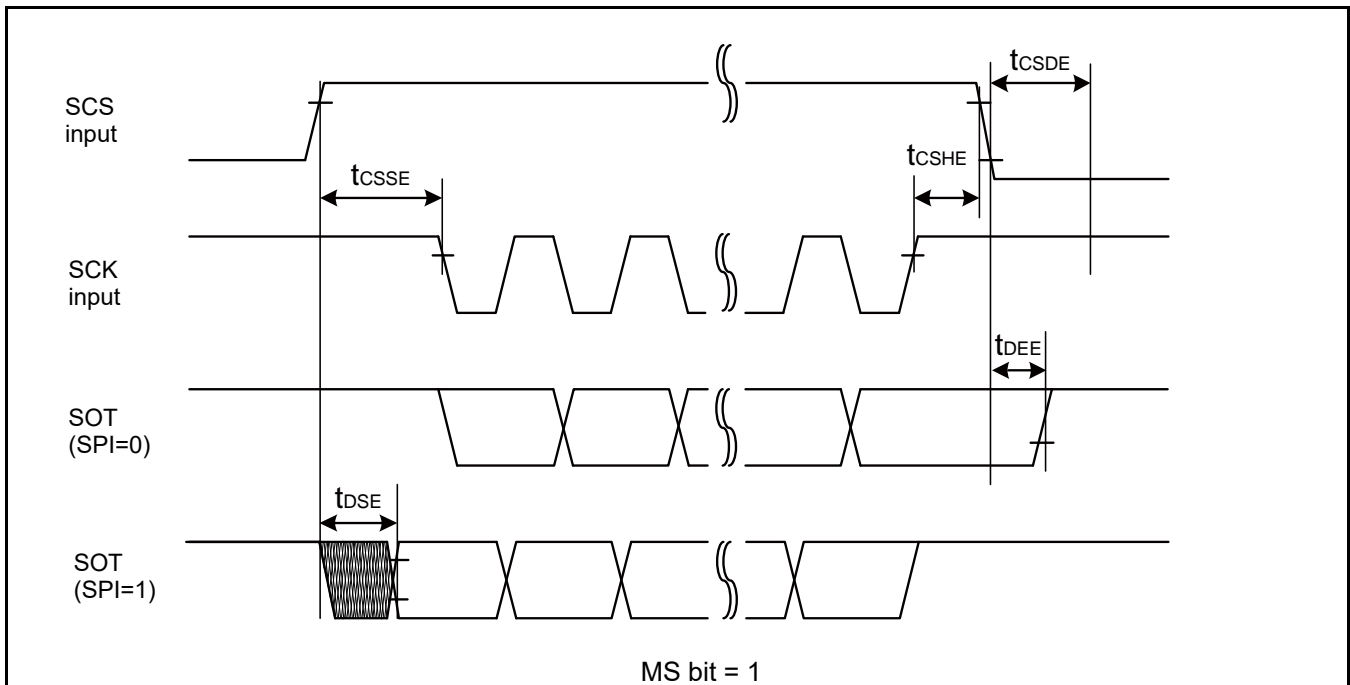
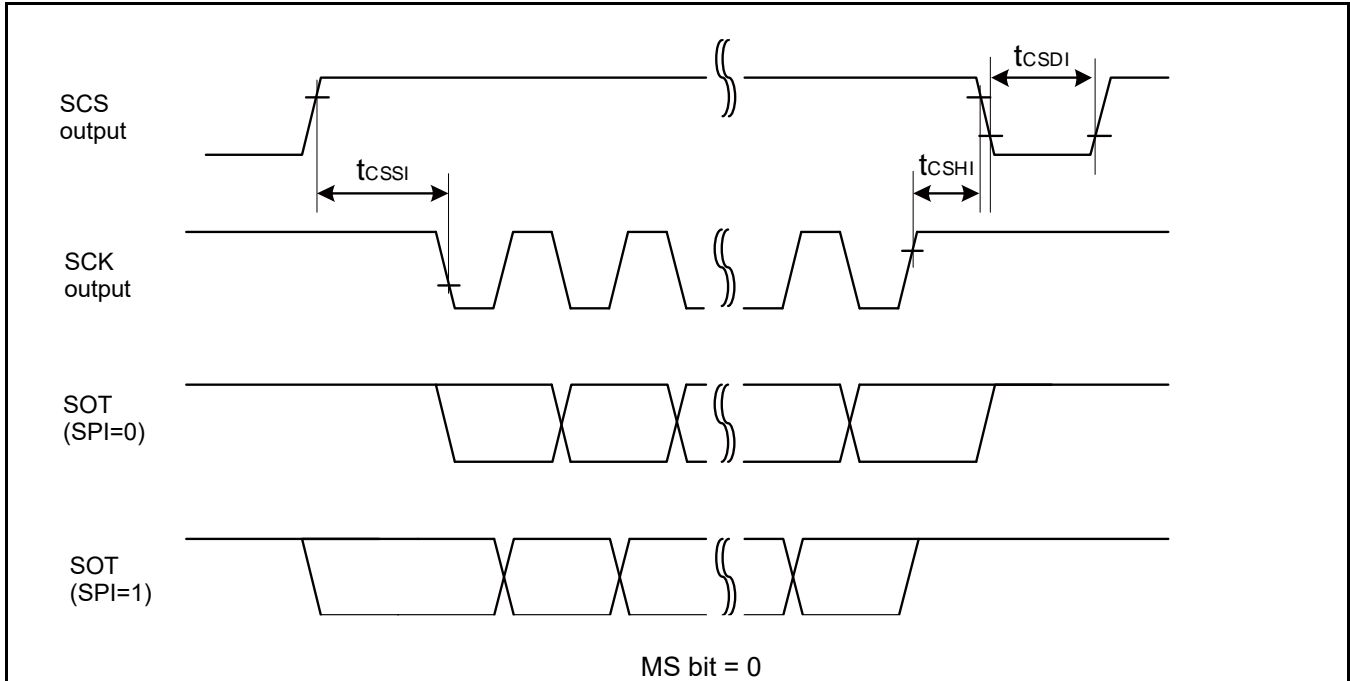
(\*1): CSSU bit value × serial chip select timing operating clock cycle [ns]

(\*2): CSHD bit value × serial chip select timing operating clock cycle [ns]

(\*3): CSDS bit value × serial chip select timing operating clock cycle [ns]

### Notes:

- t<sub>CYCP</sub> indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 8. Block Diagram in this data sheet.
- For more information about CSSU, CSHD, CSDS, and the serial chip select timing operating clock, see FM4 Family Peripheral Manual Main Part (002-04856).
- When the external load capacitance C<sub>L</sub> = 30 pF.



**When Using Synchronous Serial Chip Select (SCINV = 1, CSLVL = 0)**

 (V<sub>CC</sub> = 2.7 V to 5.5 V, V<sub>SS</sub> = 0 V)

Parameter	Symbol	Conditions	V <sub>CC</sub> < 4.5 V		V <sub>CC</sub> ≥ 4.5 V		Units
			Min	Max	Min	Max	
SCS ↑ → SCK ↑ setup time	t <sub>CSSI</sub>	Internal shift clock operation	(*1) - 50	(*1) + 0	(*1) - 50	(*1) + 0	ns
SCK ↓ → SCS ↓ hold time	t <sub>CSHI</sub>		(*2) + 0	(*2) + 50	(*2) + 0	(*2) + 50	ns
SCS deselect time	t <sub>CSDI</sub>		(*3) - 50 + 5t <sub>CYCP</sub>	(*3) + 50 + 5t <sub>CYCP</sub>	(*3) - 50 + 5t <sub>CYCP</sub>	(*3) + 50 + 5t <sub>CYCP</sub>	ns
SCS ↑ → SCK ↑ setup time	t <sub>CSSE</sub>	External shift clock operation	3t <sub>CYCP</sub> + 30	-	3t <sub>CYCP</sub> + 30	-	ns
SCK ↓ → SCS ↓ hold time	t <sub>CSHE</sub>		0	-	0	-	ns
SCS deselect time	t <sub>CSDE</sub>		3t <sub>CYCP</sub> + 30	-	3t <sub>CYCP</sub> + 30	-	ns
SCS ↑ → SOT delay time	t <sub>DSE</sub>		-	40	-	40	ns
SCS ↓ → SOT delay time	t <sub>DEE</sub>		0	-	0	-	ns

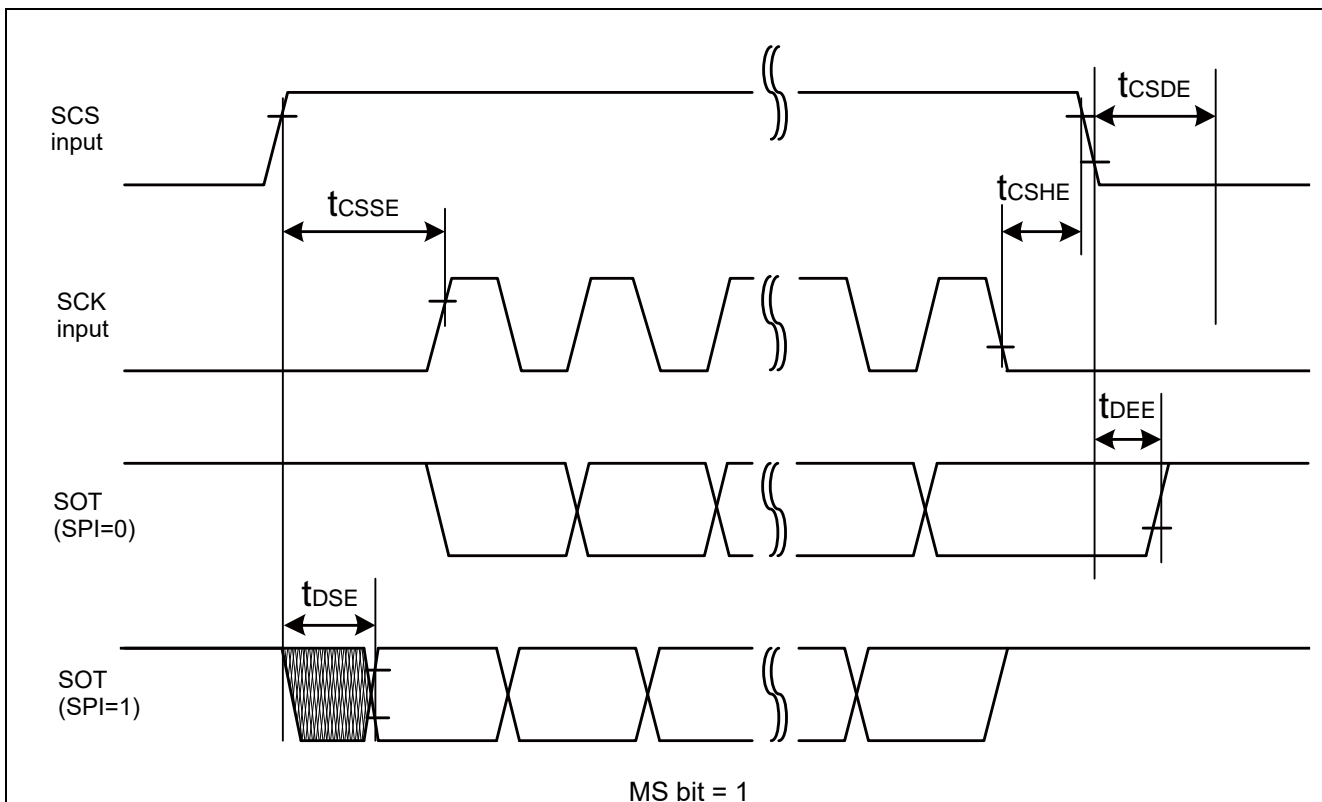
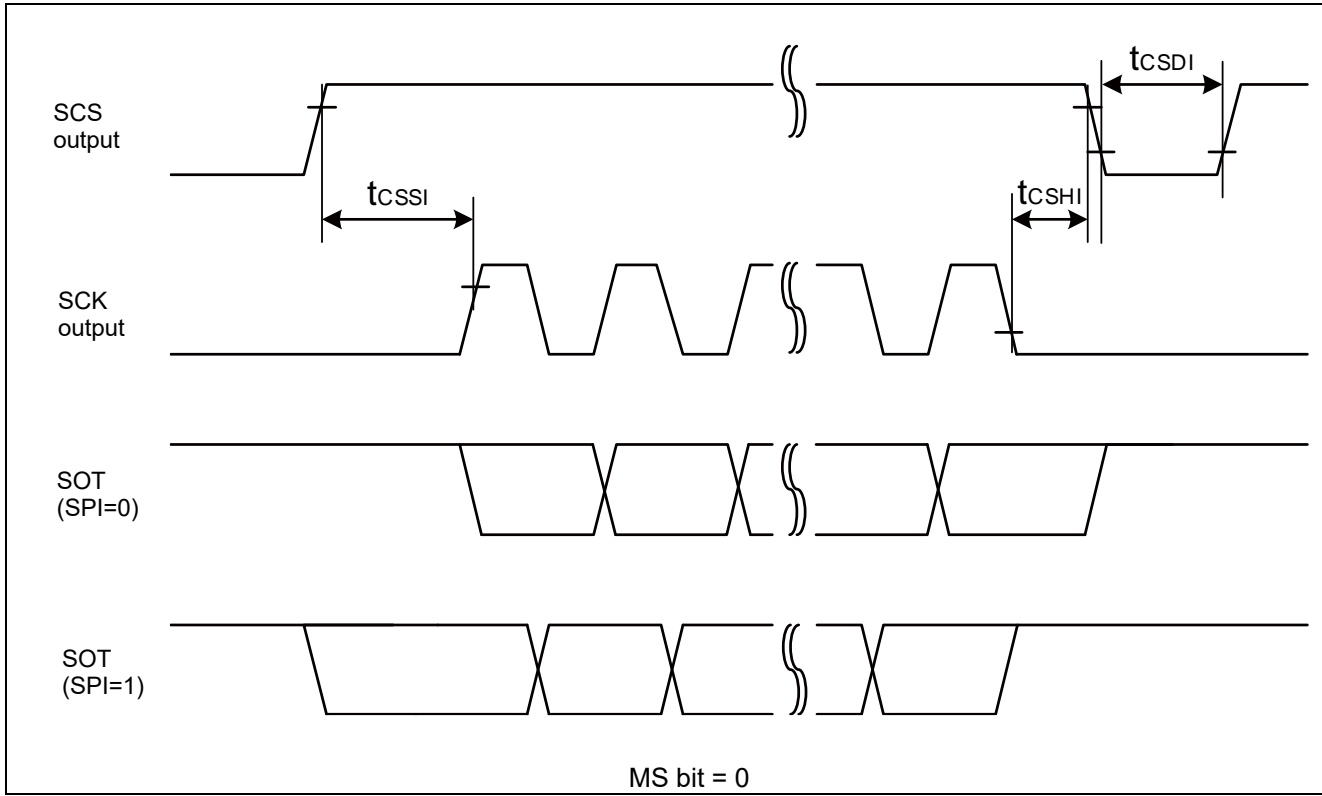
(\*1): CSSU bit value × serial chip select timing operating clock cycle [ns]

(\*2): CSHD bit value × serial chip select timing operating clock cycle [ns]

(\*3): CSDS bit value × serial chip select timing operating clock cycle [ns]

**Notes:**

- t<sub>CYCP</sub> indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 8. Block Diagram in this data sheet.
- For more information about CSSU, CSHD, CSDS, and the serial chip select timing operating clock, see FM4 Family Peripheral Manual Main Part (002-04856).
- When the external load capacitance C<sub>L</sub> = 30 pF.



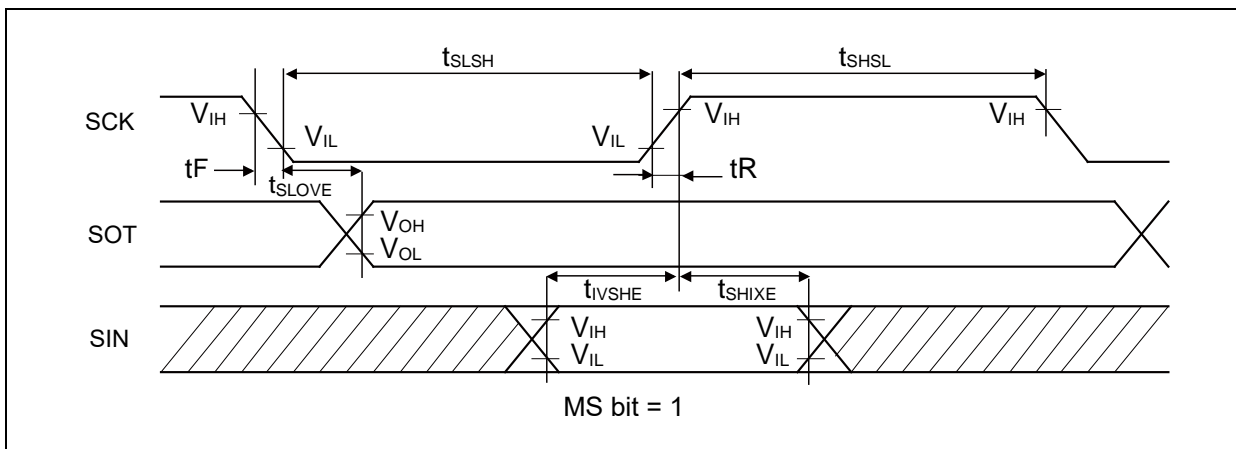
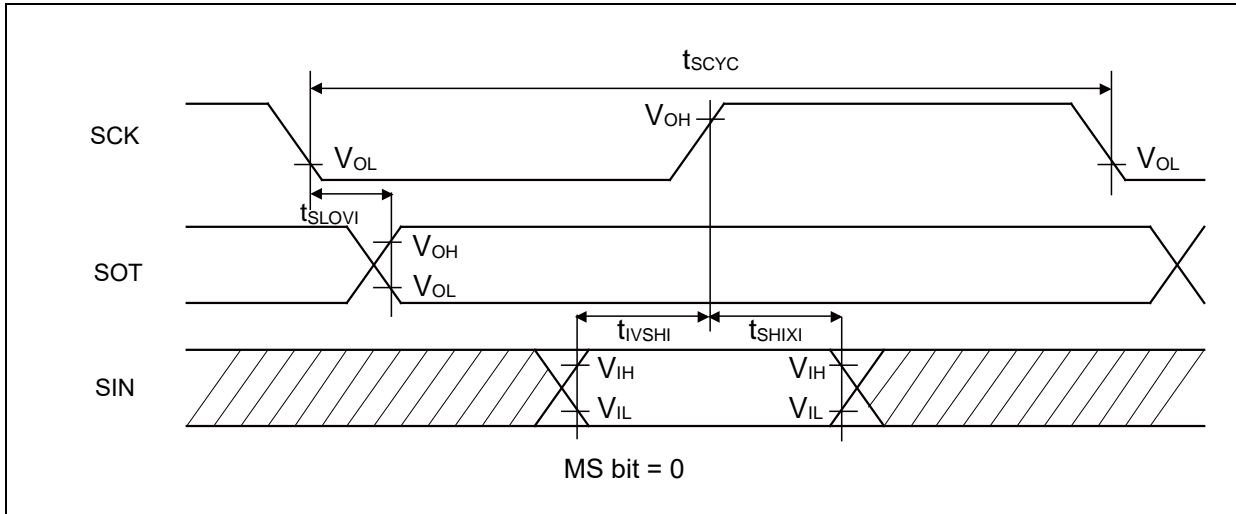
**High-Speed Synchronous Serial (SPI = 0, SCINV = 0)**

 (V<sub>CC</sub> = 2.7 V to 5.5 V, V<sub>SS</sub> = 0 V)

Parameter	Symbol	Pin Name	Conditions	V <sub>CC</sub> < 4.5 V		V <sub>CC</sub> ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t <sub>SCYC</sub>	SCKx	Internal shift clock operation	4t <sub>CYCP</sub>	-	4t <sub>CYCP</sub>	-	ns
SCK <sub>↓</sub> →SOT delay time	t <sub>SLOVI</sub>	SCKx, SOTx		-10	+10	-10	+10	ns
SIN→SCK <sub>↑</sub> setup time	t <sub>VS<sub>HI</sub></sub>	SCKx, SINx		14	-	12.5	-	ns
				12.5*				
SCK <sub>↑</sub> →SIN hold time	t <sub>SHIXI</sub>	SCKx, SINx		5	-	5	-	ns
Serial clock L pulse width	t <sub>SLSH</sub>	SCKx	External shift clock operation	2t <sub>CYCP</sub> - 5	-	2t <sub>CYCP</sub> - 5	-	ns
Serial clock H pulse width	t <sub>SHSL</sub>	SCKx		t <sub>CYCP</sub> + 10	-	t <sub>CYCP</sub> + 10	-	ns
SCK <sub>↓</sub> →SOT delay time	t <sub>SLOVE</sub>	SCKx, SOTx		-	15	-	15	ns
SIN→SCK <sub>↑</sub> setup time	t <sub>VS<sub>HE</sub></sub>	SCKx, SINx		5	-	5	-	ns
SCK <sub>↑</sub> →SIN hold time	t <sub>SHIXE</sub>	SCKx, SINx		5	-	5	-	ns
SCK fall time	t <sub>F</sub>	SCKx		-	5	-	5	ns
SCK rise time	t <sub>R</sub>	SCKx		-	5	-	5	ns

**Notes:**

- The above characteristics apply to CLK synchronous mode.
- t<sub>CYCP</sub> indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 8. Block Diagram in this data sheet.
- These characteristics only guarantee the following pins:
  - No chip select: SIN4\_0, SOT4\_0, SCK4\_0
  - Chip select: SIN6\_0, SOT6\_0, SCK6\_0, SCS60\_0, SCS61\_0, SCS62\_0, SCS63\_0
- When the external load capacitance C<sub>L</sub> = 30 pF. (For \*, when C<sub>L</sub> = 10 pF)



**High-Speed Synchronous Serial (SPI = 0, SCINV = 1)**

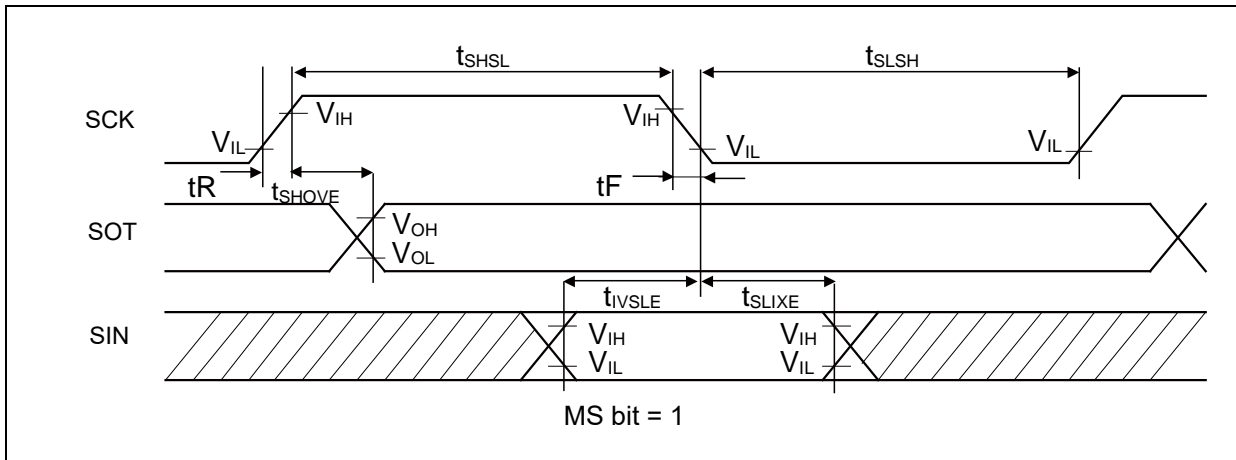
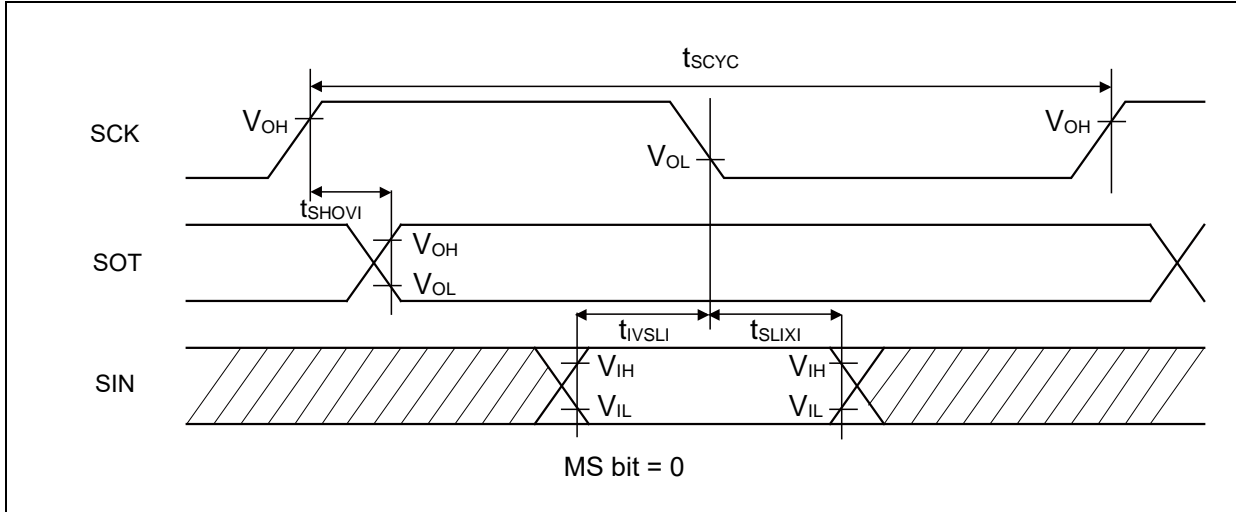
 (V<sub>CC</sub> = 2.7 V to 5.5 V, V<sub>SS</sub> = 0 V)

Parameter	Symbol	Pin Name	Conditions	V <sub>CC</sub> < 4.5 V		V <sub>CC</sub> ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t <sub>SCYC</sub>	SCKx	Internal shift clock operation	4t <sub>CYCP</sub>	-	4t <sub>CYCP</sub>	-	ns
SCK↑→SOT delay time	t <sub>SHOVI</sub>	SCKx, SOTx		-10	+10	-10	+10	ns
SIN→SCK↓ setup time	t <sub>IVSLI</sub>	SCKx, SINx		14	-	12.5	-	ns
				12.5*				
SCK↓→SIN hold time	t <sub>SLIXI</sub>	SCKx, SINx		5	-	5	-	ns
Serial clock L pulse width	t <sub>LSLH</sub>	SCKx	External shift clock operation	2t <sub>CYCP</sub> - 5	-	2t <sub>CYCP</sub> - 5	-	ns
Serial clock H pulse width	t <sub>SHSL</sub>	SCKx		t <sub>CYCP</sub> + 10	-	t <sub>CYCP</sub> + 10	-	ns
SCK↑→SOT delay time	t <sub>SHOVE</sub>	SCKx, SOTx		-	15	-	15	ns
SIN→SCK↓ setup time	t <sub>IVSLE</sub>	SCKx, SINx		5	-	5	-	ns
SCK↓→SIN hold time	t <sub>SLIXE</sub>	SCKx, SINx		5	-	5	-	ns
SCK fall time	t <sub>F</sub>	SCKx		-	5	-	5	ns
SCK rise time	t <sub>R</sub>	SCKx		-	5	-	5	ns

**Notes:**

- The above characteristics apply to CLK synchronous mode.
- t<sub>CYCP</sub> indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 8. Block Diagram in this data sheet.
- These characteristics only guarantee the following pins:  
     No chip select: SIN4\_0, SOT4\_0, SCK4\_0  
     Chip select: SIN6\_0, SOT6\_0, SCK6\_0, SCS60\_0, SCS61\_0, SCS62\_0, SCS63\_0
- When the external load capacitance C<sub>L</sub> = 30 pF. (For \*, when C<sub>L</sub> = 10 pF)





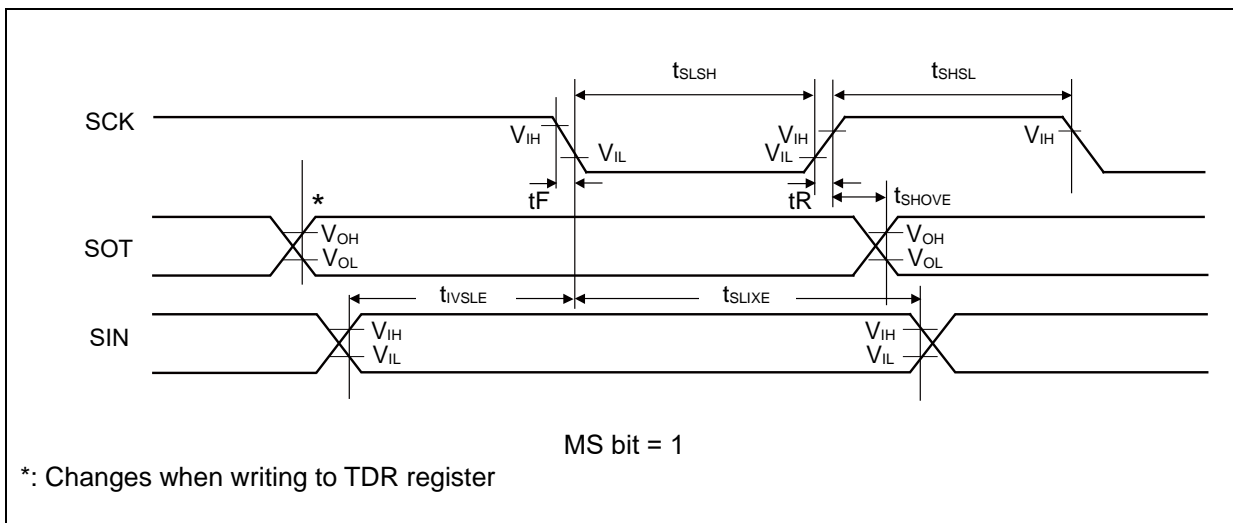
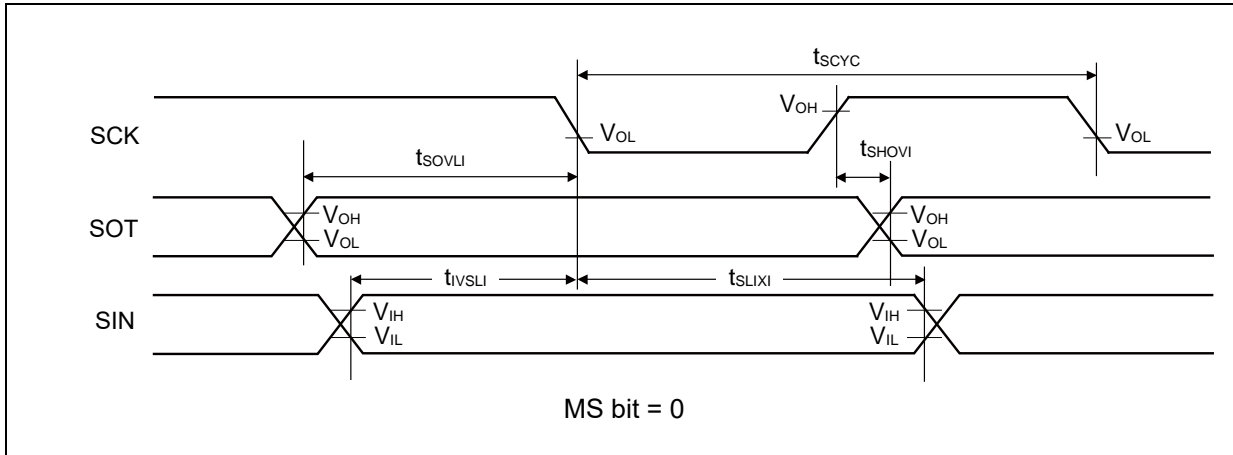
**High-Speed Synchronous Serial (SPI = 1, SCINV = 0)**

 (V<sub>CC</sub> = 2.7 V to 5.5 V, V<sub>SS</sub> = 0 V)

Parameter	Symbol	Pin Name	Conditions	V <sub>CC</sub> < 4.5 V		V <sub>CC</sub> ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t <sub>SCYC</sub>	SCKx	Internal shift clock operation	4t <sub>CYCP</sub>	-	4t <sub>CYCP</sub>	-	ns
SCK↑→SOT delay time	t <sub>SHOVI</sub>	SCKx, SOTx		-10	+10	-10	+10	ns
SIN→SCK↓ setup time	t <sub>IVSLI</sub>	SCKx, SINx		14	-	12.5	-	ns
				12.5*				
SCK↓→SIN hold time	t <sub>SLIXI</sub>	SCKx, SINx		5	-	5	-	ns
SOT→SCK↓ delay time	t <sub>SOVLI</sub>	SCKx, SOTx		2t <sub>CYCP</sub> - 10	-	2t <sub>CYCP</sub> - 10	-	ns
Serial clock L pulse width	t <sub>LSLH</sub>	SCKx	External shift clock operation	2t <sub>CYCP</sub> - 5	-	2t <sub>CYCP</sub> - 5	-	ns
Serial clock H pulse width	t <sub>SHSL</sub>	SCKx		t <sub>CYCP</sub> + 10	-	t <sub>CYCP</sub> + 10	-	ns
SCK↑→SOT delay time	t <sub>SHOVE</sub>	SCKx, SOTx		-	15	-	15	ns
SIN→SCK↓ setup time	t <sub>IVSLE</sub>	SCKx, SINx		5	-	5	-	ns
SCK↓→SIN hold time	t <sub>SLIXE</sub>	SCKx, SINx		5	-	5	-	ns
SCK fall time	t <sub>F</sub>	SCKx		-	5	-	5	ns
SCK rise time	t <sub>R</sub>	SCKx		-	5	-	5	ns

**Notes:**

- The above characteristics apply to CLK synchronous mode.
- t<sub>CYCP</sub> indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 8. Block Diagram in this data sheet.
- These characteristics only guarantee the following pins:  
     No chip select: SIN4\_0, SOT4\_0, SCK4\_0  
     Chip select: SIN6\_0, SOT6\_0, SCK6\_0, SCS60\_0, SCS61\_0, SCS62\_0, SCS63\_0
- When the external load capacitance C<sub>L</sub> = 30 pF. (for \*, when C<sub>L</sub> = 10 pF)



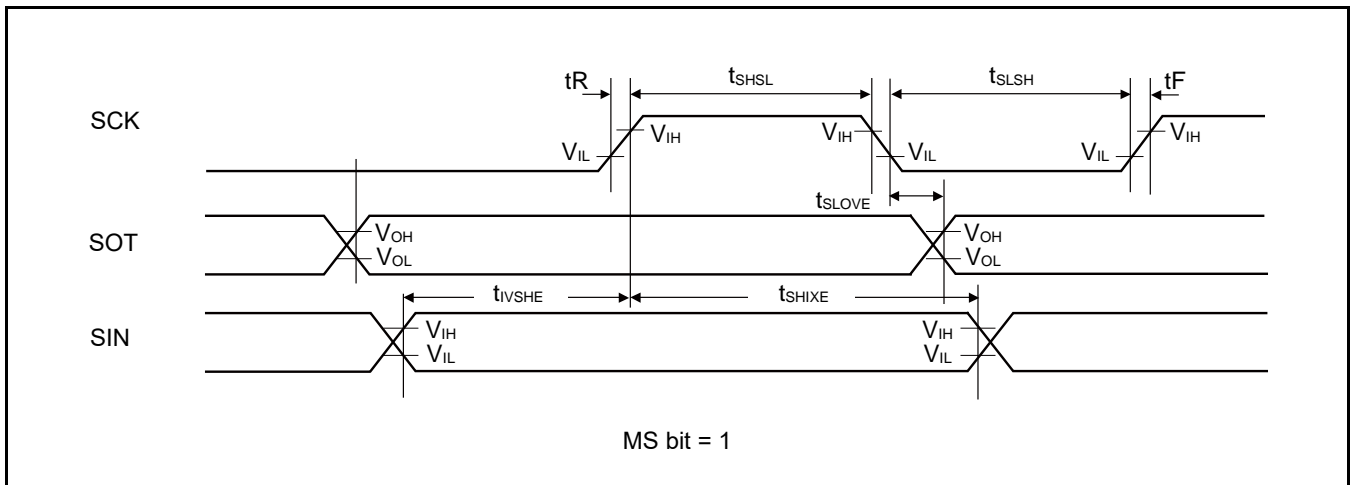
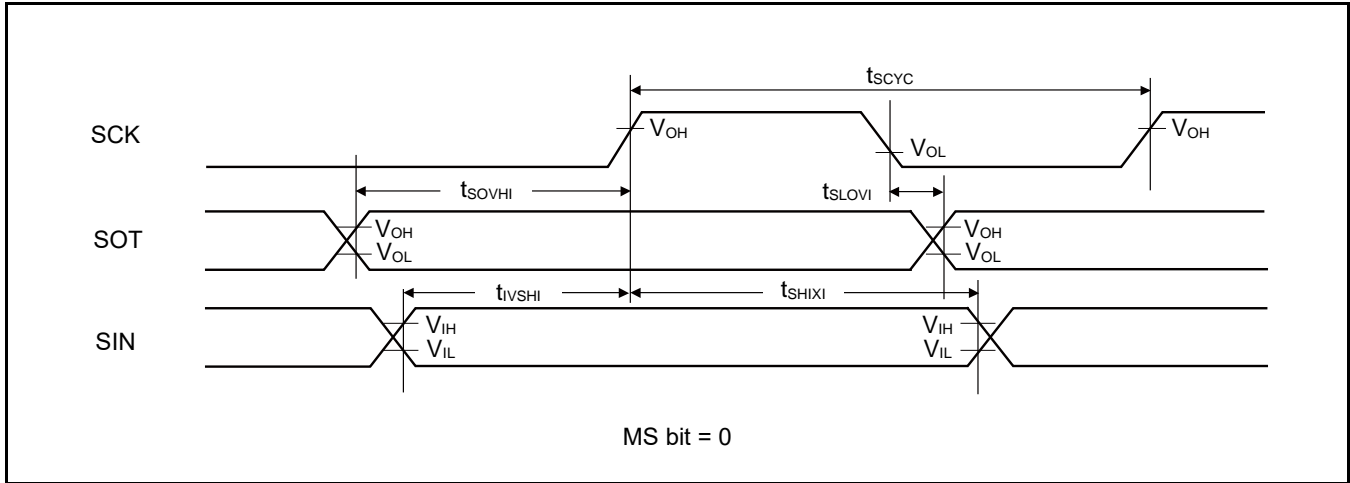
**High-Speed Synchronous Serial (SPI = 1, SCINV = 1)**

 (V<sub>CC</sub> = 2.7 V to 5.5 V, V<sub>SS</sub> = 0 V)

Parameter	Symbol	Pin Name	Conditions	V <sub>CC</sub> < 4.5 V		V <sub>CC</sub> ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t <sub>SCYC</sub>	SCKx	Internal shift clock operation	4t <sub>CYCP</sub>	-	4t <sub>CYCP</sub>	-	ns
SCK↓→SOT delay time	t <sub>SLOVI</sub>	SCKx, SOTx		-10	+10	-10	+10	ns
SIN→SCK↑ setup time	t <sub>VS</sub>	SCKx, SINx		14	-	12.5	-	ns
				12.5*				
SCK↑→SIN hold time	t <sub>SHIXI</sub>	SCKx, SINx		5	-	5	-	ns
SOT→SCK↑ delay time	t <sub>SOVHI</sub>	SCKx, SOTx		2t <sub>CYCP</sub> - 10	-	2t <sub>CYCP</sub> - 10	-	ns
Serial clock L pulse width	t <sub>SLSH</sub>	SCKx	External shift clock operation	2t <sub>CYCP</sub> - 5	-	2t <sub>CYCP</sub> - 5	-	ns
Serial clock H pulse width	t <sub>SHSL</sub>	SCKx		t <sub>CYCP</sub> + 10	-	t <sub>CYCP</sub> + 10	-	ns
SCK↓→SOT delay time	t <sub>SLOVE</sub>	SCKx, SOTx		-	15	-	15	ns
SIN→SCK↑ setup time	t <sub>VS</sub>	SCKx, SINx		5	-	5	-	ns
SCK↑→SIN hold time	t <sub>SHIXE</sub>	SCKx, SINx		5	-	5	-	ns
SCK fall time	t <sub>F</sub>	SCKx		-	5	-	5	ns
SCK rise time	t <sub>R</sub>	SCKx		-	5	-	5	ns

**Notes:**

- The above characteristics apply to CLK synchronous mode.
- t<sub>CYCP</sub> indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 8. Block Diagram in this data sheet.
- These characteristics only guarantee the following pins:  
     No chip select: SIN4\_0, SOT4\_0, SCK4\_0  
     Chip select: SIN6\_0, SOT6\_0, SCK6\_0, SCS60\_0, SCS61\_0, SCS62\_0, SCS63\_0
- When the external load capacitance C<sub>L</sub> = 30 pF. (for \*, when C<sub>L</sub> = 10 pF)



**When Using High-Speed Synchronous Serial Chip Select (SCINV = 0, CSLVL = 1)**

 (V<sub>CC</sub> = 2.7 V to 5.5 V, V<sub>SS</sub> = 0 V)

Parameter	Symbol	Conditions	V <sub>CC</sub> < 4.5 V		V <sub>CC</sub> ≥ 4.5 V		Unit
			Min	Max	Min	Max	
SCS↓→SCK↓ setup time	t <sub>CSSI</sub>	Internal shift clock operation	(*1) - 20	(*1) + 0	(*1) - 20	(*1) + 0	ns
SCK↑→SCS↑ hold time	t <sub>CShI</sub>		(*2) + 0	(*2) + 20	(*2) + 0	(*2) + 20	ns
SCS deselect time	t <sub>CSDI</sub>		(*3) - 20 + 5t <sub>CYCP</sub>	(*3) + 20 + 5t <sub>CYCP</sub>	(*3) - 20 + 5t <sub>CYCP</sub>	(*3) + 20 + 5t <sub>CYCP</sub>	ns
SCS↓→SCK↓ setup time	t <sub>CSE</sub>	External shift clock operation	3t <sub>CYCP</sub> + 15	-	3t <sub>CYCP</sub> + 15	-	ns
SCK↑→SCS↑ hold time	t <sub>CSE</sub>		0	-	0	-	ns
SCS deselect time	t <sub>CSE</sub>		3t <sub>CYCP</sub> + 15	-	3t <sub>CYCP</sub> + 15	-	ns
SCS↓→SOT delay time	t <sub>DSE</sub>		-	25	-	25	ns
SCS↑→SOT delay time	t <sub>DEE</sub>		0	-	0	-	ns

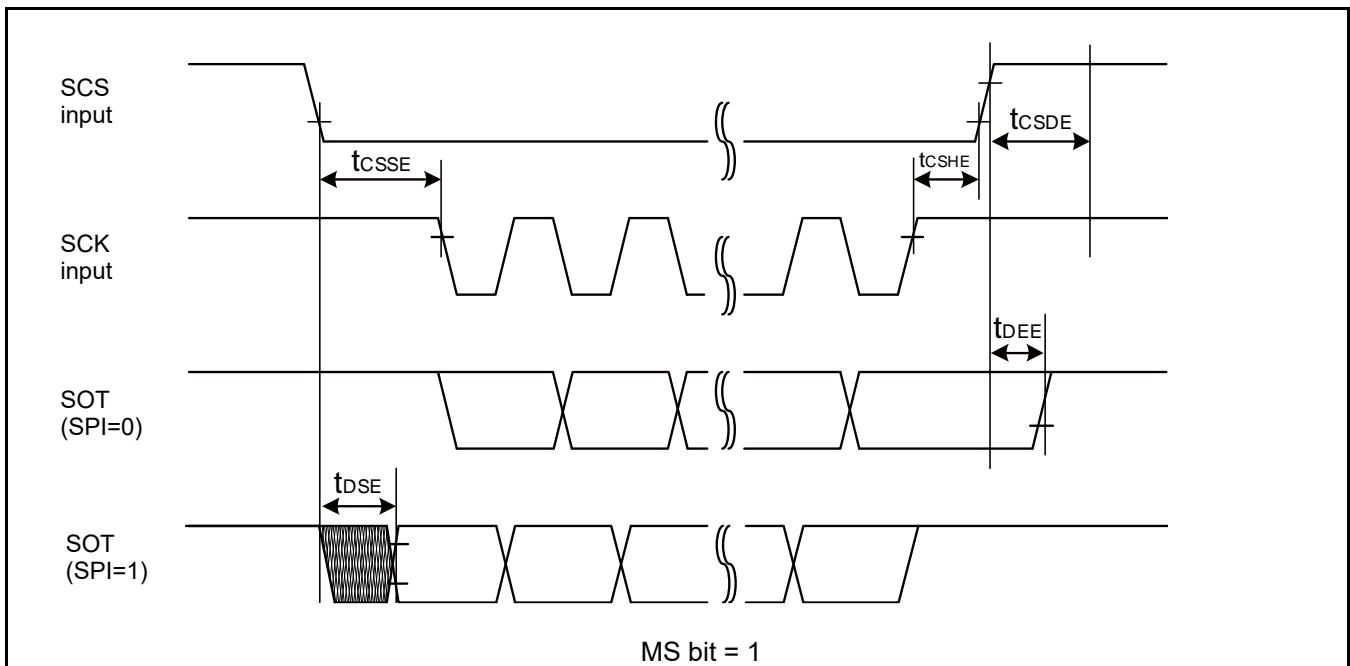
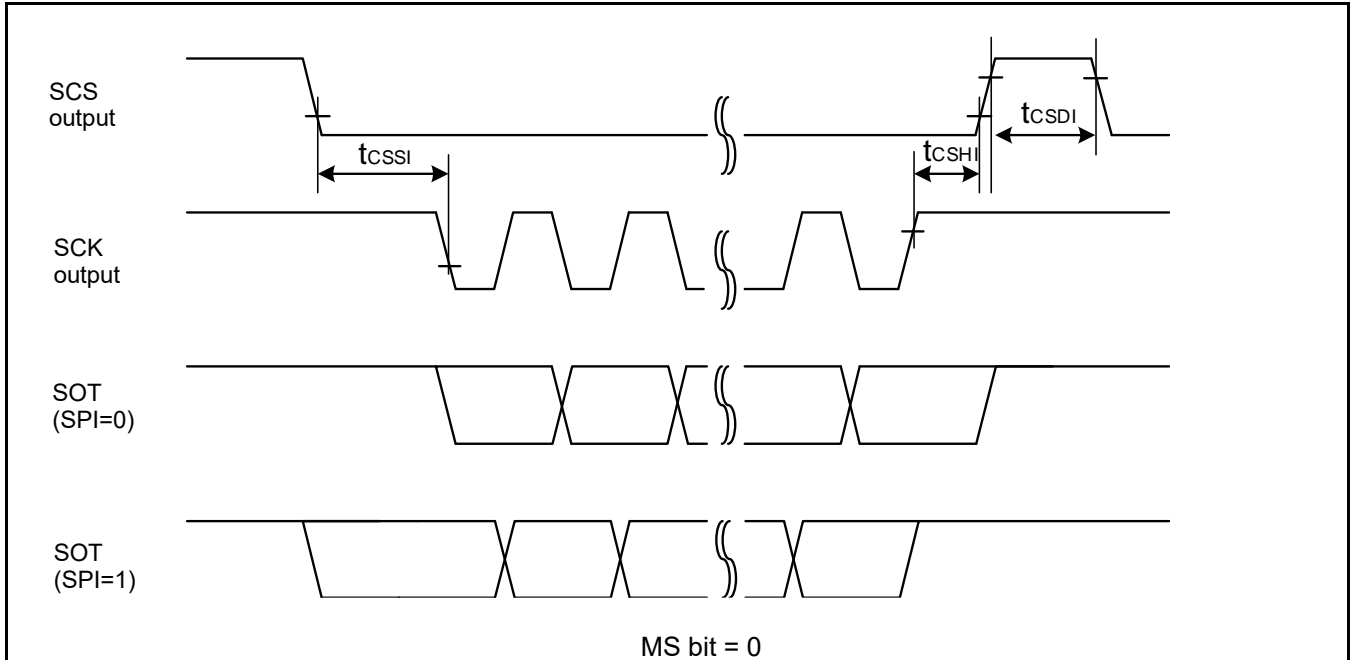
(\*1): CSSU bit value × serial chip select timing operating clock cycle [ns]

(\*2): CSHD bit value × serial chip select timing operating clock cycle [ns]

(\*3): CSDS bit value × serial chip select timing operating clock cycle [ns]

**Notes:**

- t<sub>CYCP</sub> indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 8. Block Diagram in this data sheet.
- For more information about CSSU, CSHD, CSDS, and the serial chip select timing operating clock, see FM4 Family Peripheral Manual Main Part (002-04856).
- When the external load capacitance C<sub>L</sub> = 30 pF.



**When Using High-Speed Synchronous Serial Chip Select (SCINV = 1, CSLVL = 1)**

 (V<sub>CC</sub> = 2.7 V to 5.5 V, V<sub>SS</sub> = 0 V)

Parameter	Symbol	Conditions	V <sub>CC</sub> < 4.5 V		V <sub>CC</sub> ≥ 4.5 V		Unit
			Min	Min	Min	Max	
SCS↓→SCK↓ setup time	t <sub>CSSI</sub>	Internal shift clock operation	(*1) - 20	(*1) + 0	(*1) - 20	(*1) + 0	ns
SCK↑→SCS↑ hold time	t <sub>CShI</sub>		(*2) + 0	(*2) + 20	(*2) + 0	(*2) + 20	ns
SCS deselect time	t <sub>CSDI</sub>		(*3) - 20 + 5t <sub>CYCP</sub>	(*3) + 20 + 5t <sub>CYCP</sub>	(*3) - 20 + 5t <sub>CYCP</sub>	(*3) + 20 + 5t <sub>CYCP</sub>	ns
SCS↓→SCK↑ setup time	t <sub>CSE</sub>	External shift clock operation	3t <sub>CYCP</sub> + 15	-	3t <sub>CYCP</sub> + 15	-	ns
SCK↑→SCS↑ hold time	t <sub>CSE</sub>		0	-	0	-	ns
SCS deselect time	t <sub>CSE</sub>		3t <sub>CYCP</sub> + 15	-	3t <sub>CYCP</sub> + 15	-	ns
SCS↓→SOT delay time	t <sub>DSE</sub>		-	25	-	25	ns
SCS↑→SOT delay time	t <sub>DEE</sub>		0	-	0	-	ns

(\*1): CSSU bit value × serial chip select timing operating clock cycle [ns]

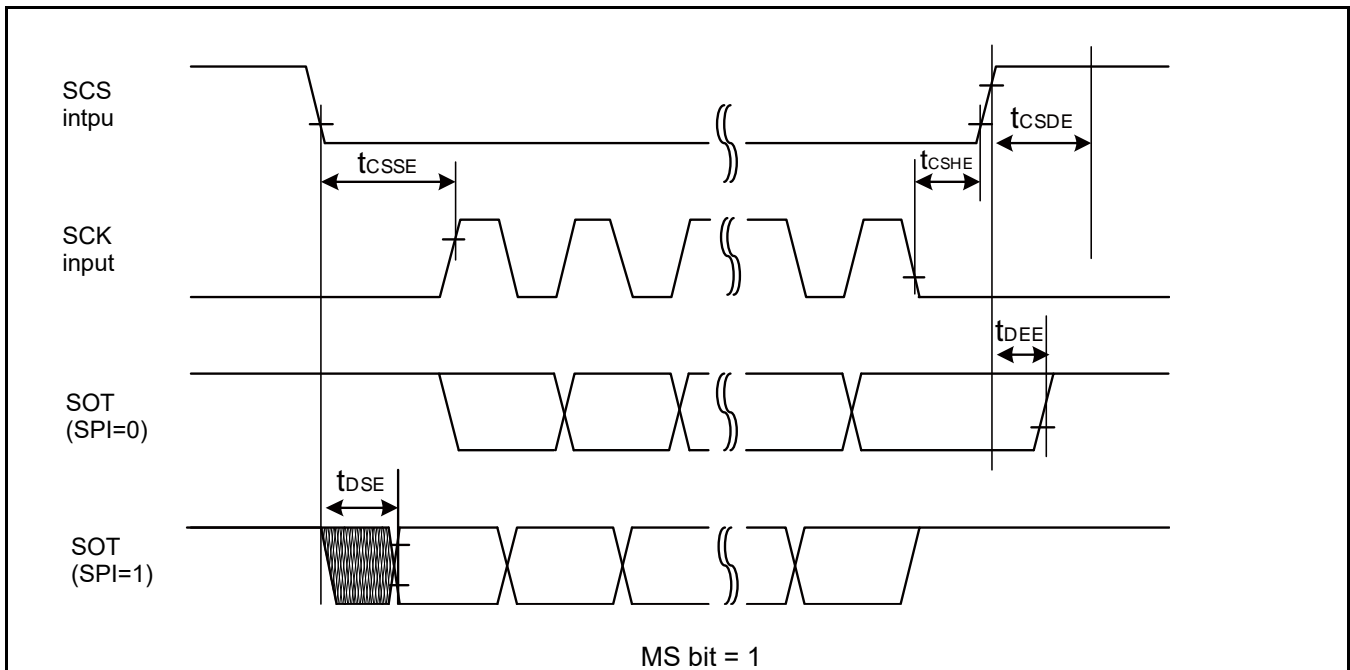
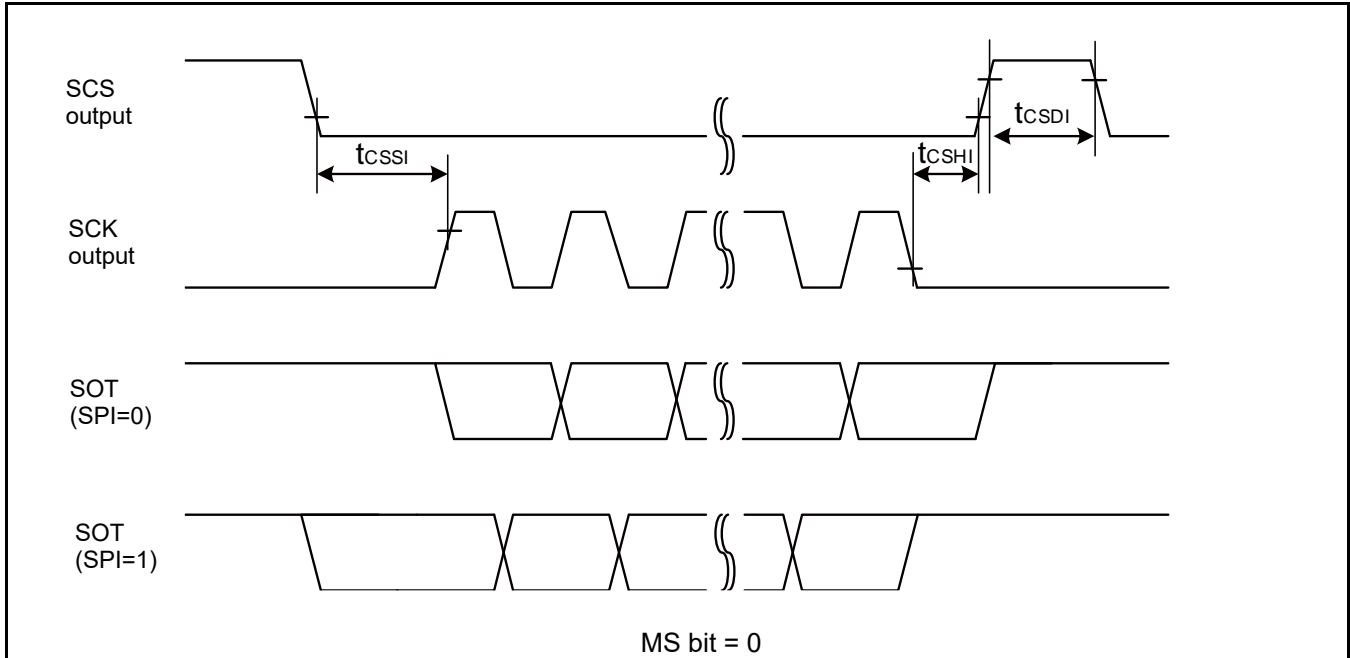
(\*2): CSHD bit value × serial chip select timing operating clock cycle [ns]

(\*3): CSDS bit value × serial chip select timing operating clock cycle [ns]

**Notes:**

- t<sub>CYCP</sub> indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 8. Block Diagram in this data sheet.
- For more information about CSSU, CSHD, CSDS, and the serial chip select timing operating clock, see FM4 Family Peripheral Manual Main Part (002-04856).
- When the external load capacitance C<sub>L</sub> = 30 pF.





**When Using High-Speed Synchronous Serial Chip Select (SCINV = 0, CSLVL = 0)**
 $(V_{CC} = 2.7\text{ V to } 5.5\text{ V}, V_{SS} = 0\text{ V})$ 

Parameter	Symbol	Conditions	$V_{CC} < 4.5\text{ V}$		$V_{CC} \geq 4.5\text{ V}$		Unit
			Min	Max	Min	Max	
SCS $\uparrow$ →SCK $\downarrow$ setup time	$t_{CSSI}$	Internal shift clock operation	(*1)-20	(*1)+0	(*1)-20	(*1)+0	ns
SCK $\uparrow$ →SCS $\downarrow$ hold time	$t_{CSHI}$		(*2)+0	(*2)+20	(*2)+0	(*2)+20	ns
SCS deselect time	$t_{CSDI}$		(*3)-20 +5 $t_{CYCP}$	(*3)+20 +5 $t_{CYCP}$	(*3)-20 +5 $t_{CYCP}$	(*3)+20 +5 $t_{CYCP}$	ns
SCS $\uparrow$ →SCK $\downarrow$ setup time	$t_{CSSE}$	External shift clock operation	3 $t_{CYCP}$ +15	-	3 $t_{CYCP}$ +15	-	ns
SCK $\uparrow$ →SCS $\downarrow$ hold time	$t_{CSHE}$		0	-	0	-	ns
SCS deselect time	$t_{CSDE}$		3 $t_{CYCP}$ +15	-	3 $t_{CYCP}$ +15	-	ns
SCS $\uparrow$ →SOT delay time	$t_{DSE}$		-	25	-	25	ns
SCS $\downarrow$ →SOT delay time	$t_{DEE}$		0	-	0	-	ns

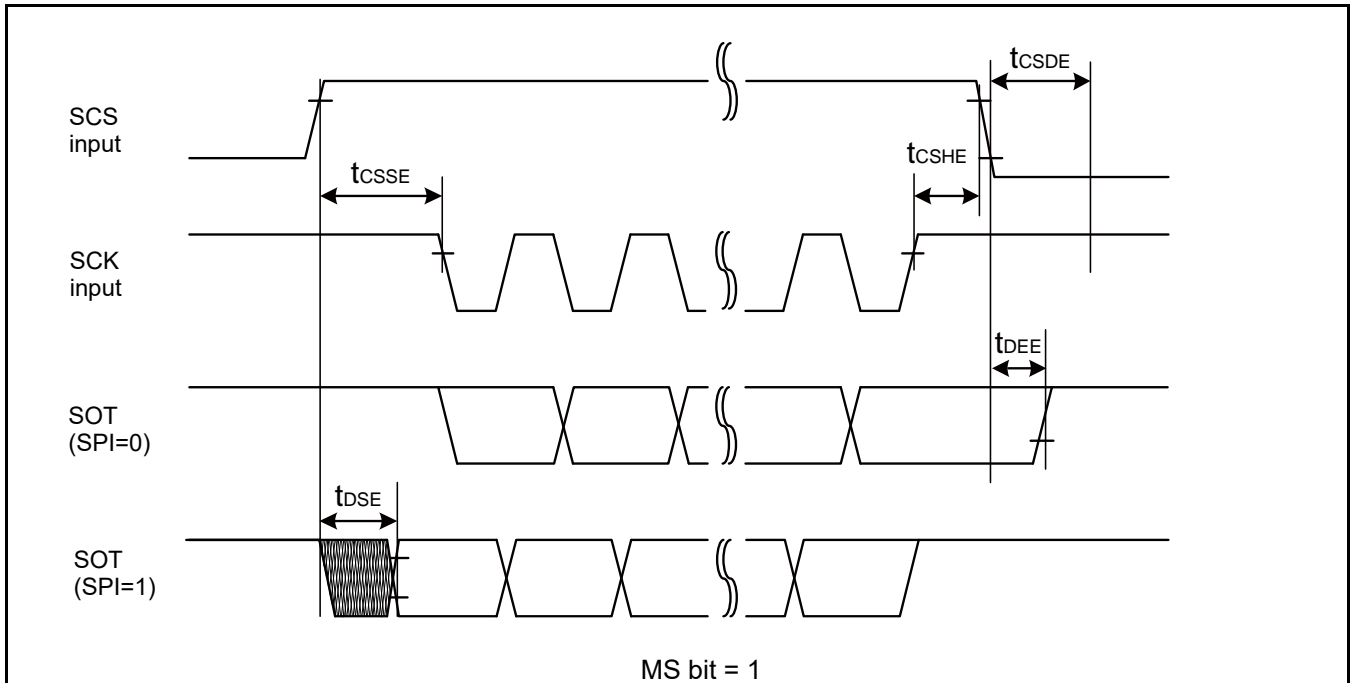
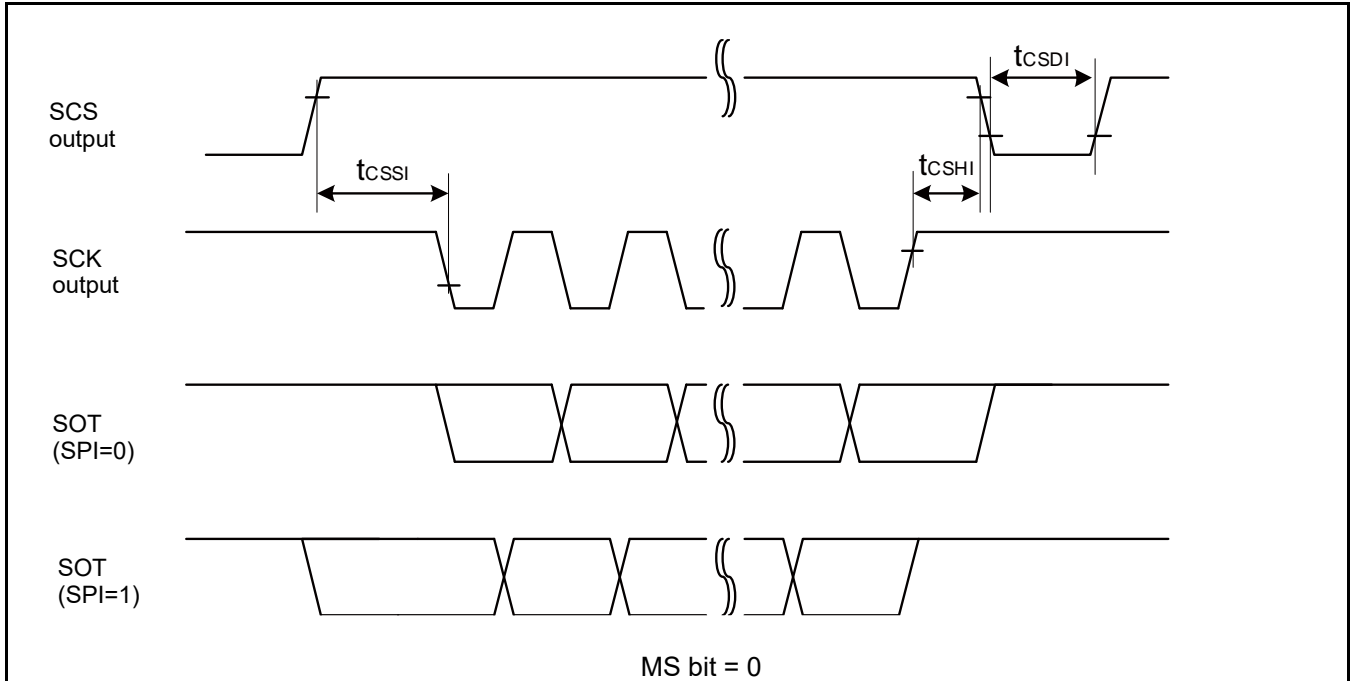
(\*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

(\*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

(\*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

**Notes:**

- $t_{CYCP}$  indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 8. Block Diagram in this data sheet.
- For more information about CSSU, CSHD, CSDS, and the serial chip select timing operating clock, see FM4 Family Peripheral Manual Main Part (002-04856).
- When the external load capacitance  $C_L = 30\text{ pF}$ .



**When Using High-Speed Synchronous Serial Chip Select (SCINV = 1, CSLVL = 0)**

 (V<sub>CC</sub> = 2.7 V to 5.5 V, V<sub>SS</sub> = 0 V)

Parameter	Symbol	Conditions	V <sub>CC</sub> < 4.5 V		V <sub>CC</sub> ≥ 4.5 V		Unit
			Min	Max	Min	Max	
SCS↓→SCK↓ setup time	t <sub>CSSI</sub>	Internal shift clock operation	(*1)-20	(*1)+0	(*1)-20	(*1)+0	ns
SCK↑→SCS↓ hold time	t <sub>CShI</sub>		(*2)+0	(*2)+20	(*2)+0	(*2)+20	ns
SCS deselect time	t <sub>CSDI</sub>		(*3)-20 +5t <sub>CYCP</sub>	(*3)+20 +5t <sub>CYCP</sub>	(*3)-20 +5t <sub>CYCP</sub>	(*3)+20 +5t <sub>CYCP</sub>	ns
SCS↑→SCK↑ setup time	t <sub>CSSE</sub>	External shift clock operation	3t <sub>CYCP</sub> +15	-	3t <sub>CYCP</sub> +15	-	ns
SCK↓→SCS↓ hold time	t <sub>CSHE</sub>		0	-	0	-	ns
SCS deselect time	t <sub>CSDE</sub>		3t <sub>CYCP</sub> +15	-	3t <sub>CYCP</sub> +15	-	ns
SCS↑→SOT delay time	t <sub>DSE</sub>		-	40	-	40	ns
SCS↓→SOT delay time	t <sub>DEE</sub>		0	-	0	-	ns

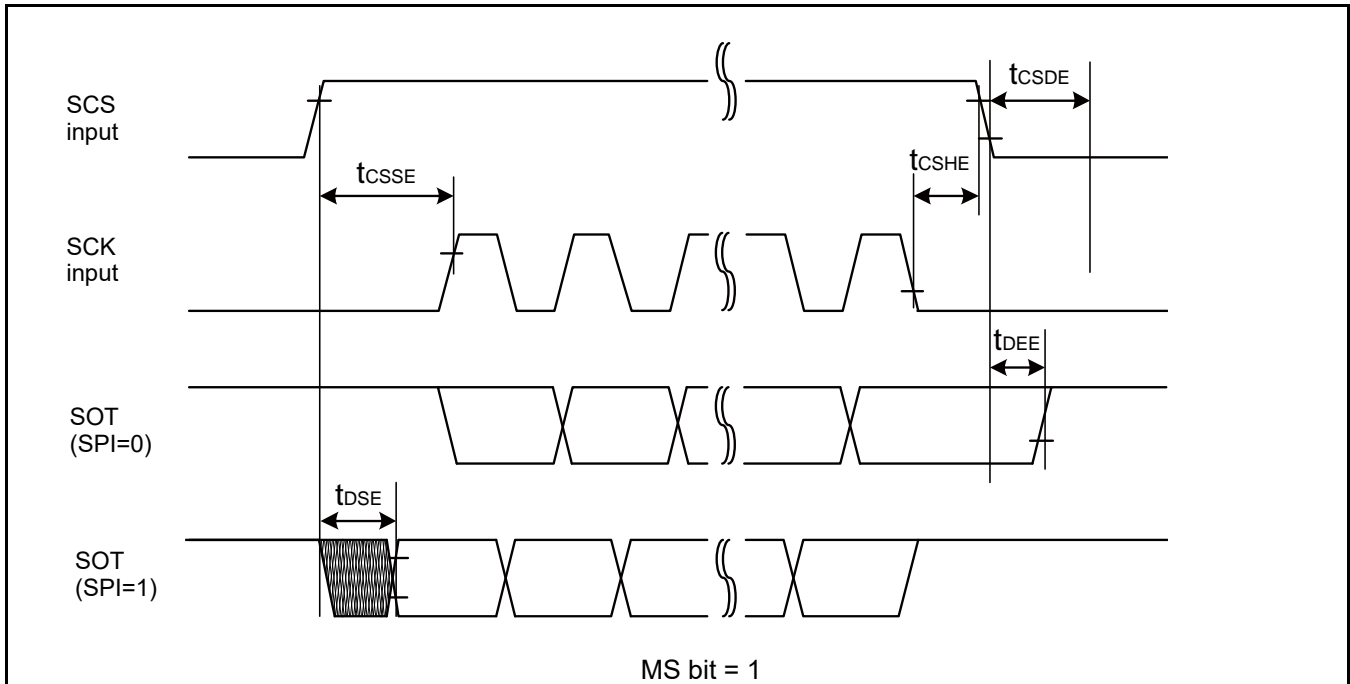
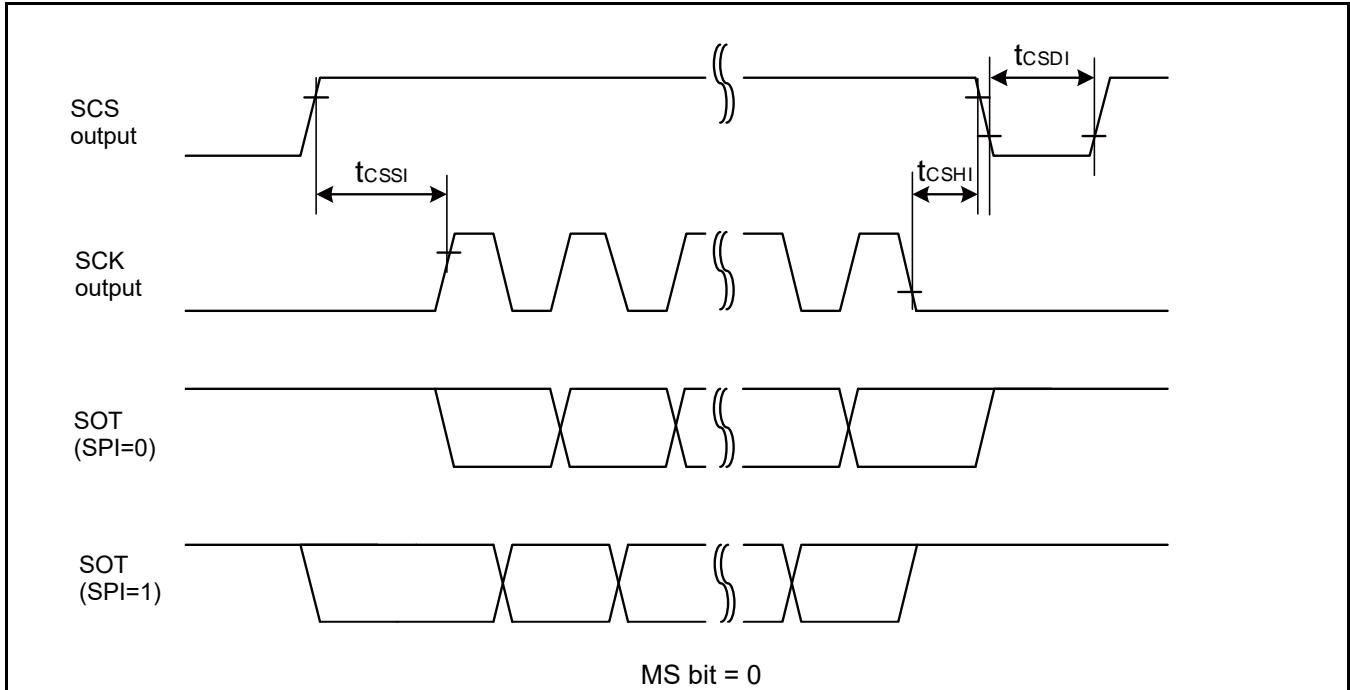
(\*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

(\*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

(\*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

**Notes:**

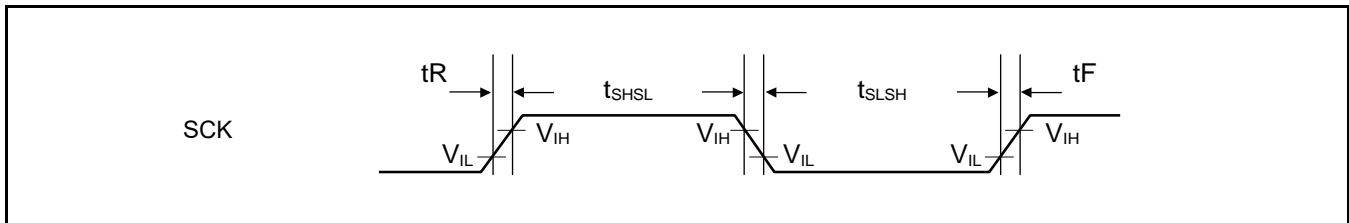
- t<sub>CYCP</sub> indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 8. Block Diagram in this data sheet.
- For more information about CSSU, CSHD, CSDS, and the serial chip select timing operating clock, see FM4 Family Peripheral Manual Main Part (002-04856).
- When the external load capacitance C<sub>L</sub> = 30 pF.



**External clock (EXT = 1): When in Asynchronous Mode Only**

 ( $V_{CC} = 2.7\text{ V to }5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min	Max		
Serial clock L pulse width	$t_{SLSH}$	$C_L = 30\text{ pF}$	$t_{CYCP} + 10$	-	ns	
Serial clock H pulse width	$t_{SHSL}$		$t_{CYCP} + 10$	-	ns	
SCK fall time	$t_F$		-	5	ns	
SCK rise time	$t_R$		-	5	ns	

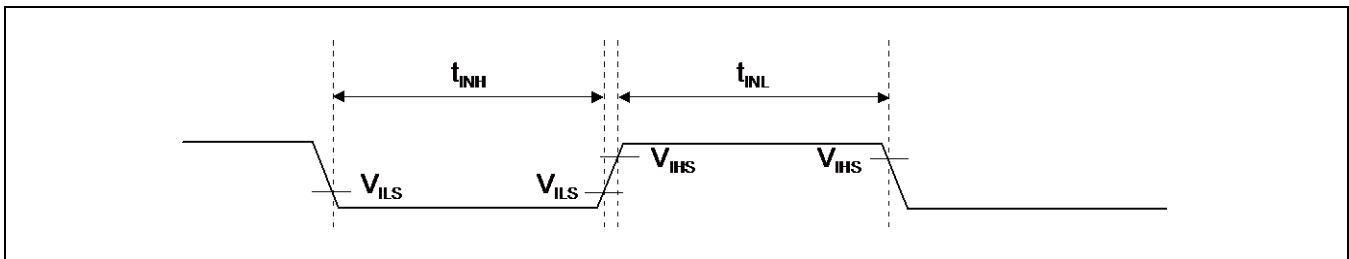


12.4.13 External Input Timing

(V<sub>CC</sub> = 2.7 V to 5.5 V, V<sub>SS</sub> = 0 V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t <sub>INH</sub> , t <sub>INL</sub>	ADTGx	-	2t <sub>CYCP</sub> <sup>*1</sup>	-	ns	A/D converter trigger input
		FRCKx					Free-run timer input clock
		ICxx					Input capture
		DTTixX	-	2t <sub>CYCP</sub> <sup>*1</sup>	-	ns	Waveform generator
		INT00 to INT31, NMIX	-	2t <sub>CYCP</sub> + 100 <sup>*1</sup>	-	ns	External interrupt, NMI
		500 <sup>*2</sup>		-	ns		
WKUPx	-	500 <sup>*3</sup>	-	ns	Deep standby wake up		

- 1: t<sub>CYCP</sub> indicates the APB bus clock cycle time except stop when in Stop mode, in Timer mode. For more information about the APB bus number to which the A/D converter, multi-function timer, and external interrupt are connected, see 8. Block Diagram in this data sheet.
- 2: When in Stop mode, in Timer mode
- 3: When in Deep Standby RTC mode, in Deep Standby Stop mode

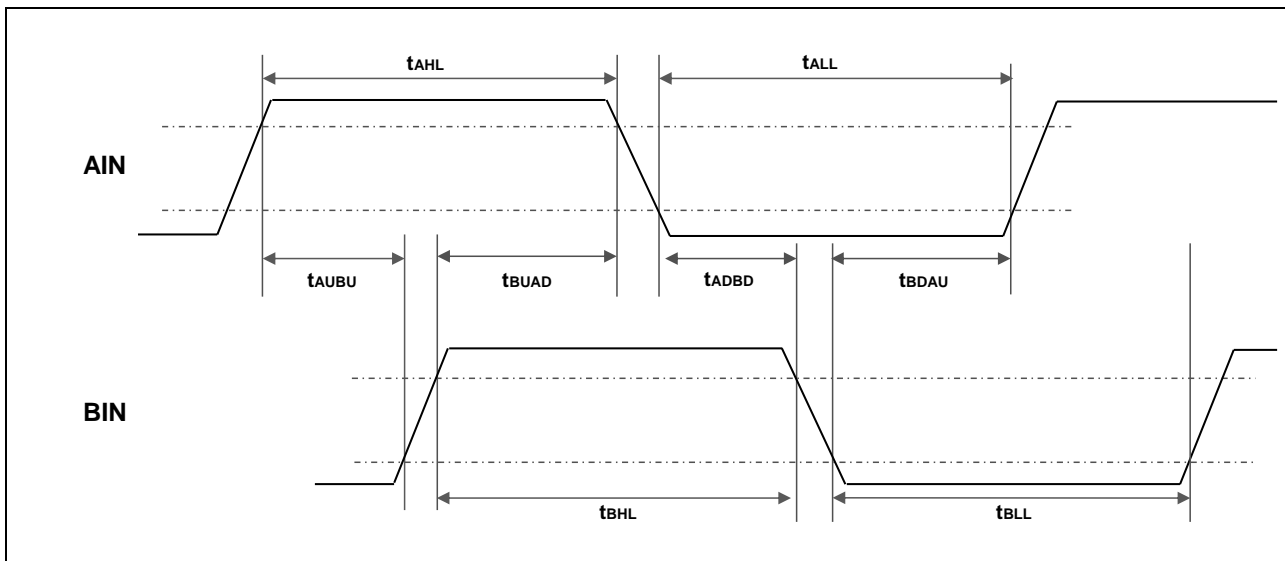


**12.4.14 Quadrature Position/Revolution Counter Timing**

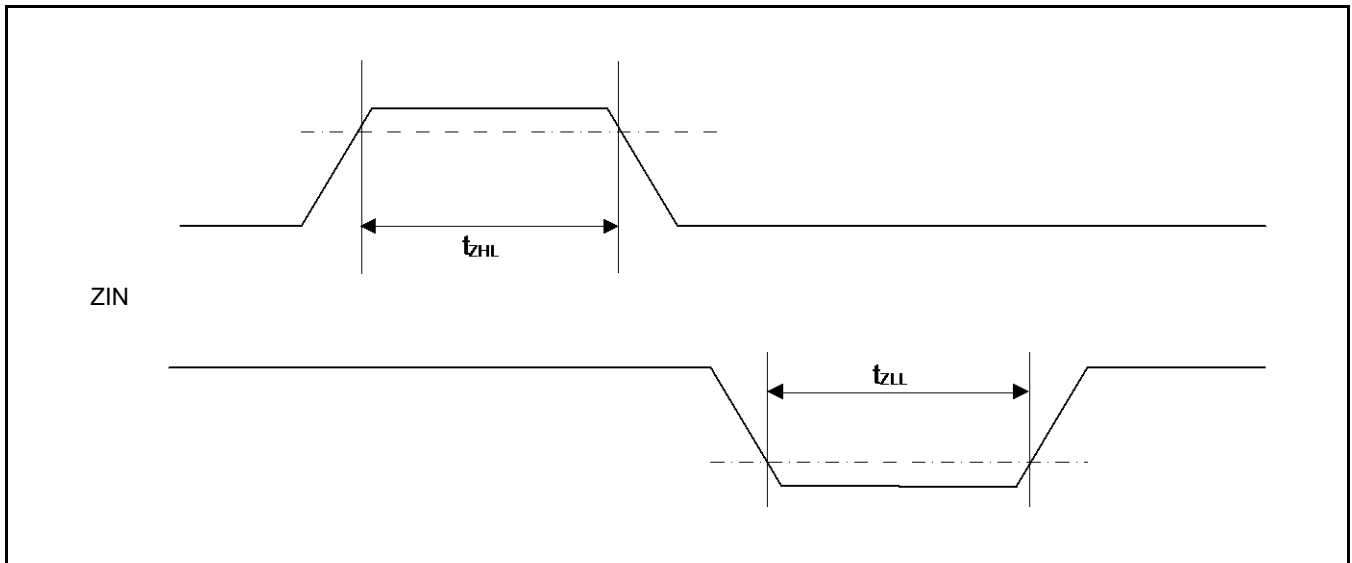
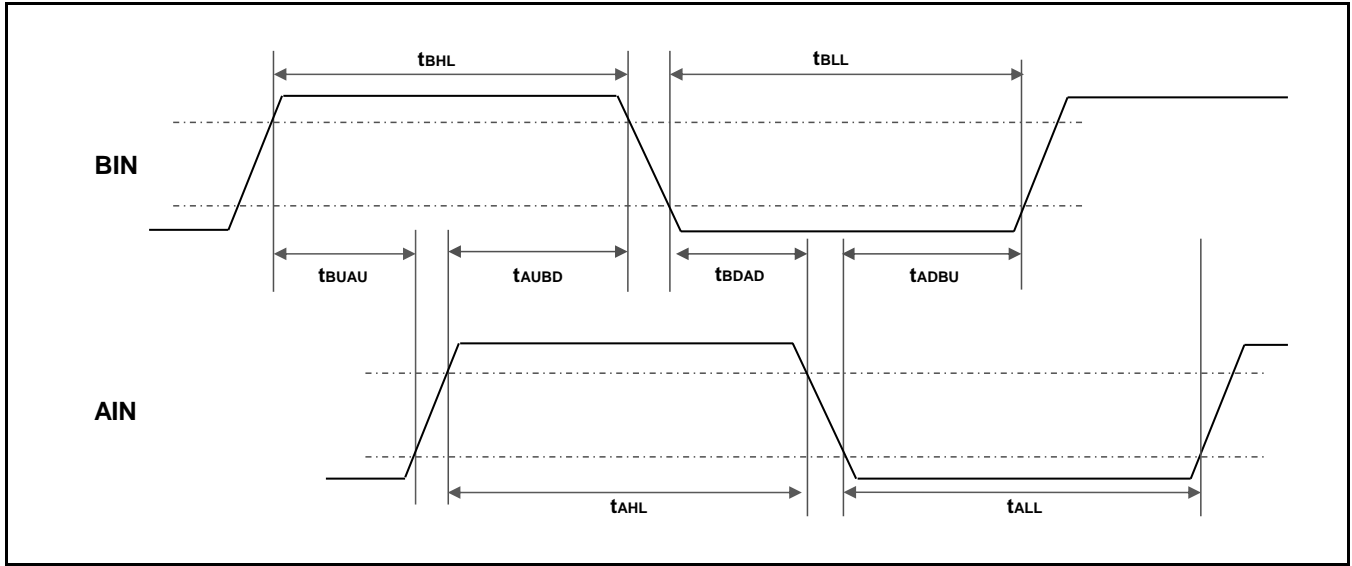
 (V<sub>CC</sub> = AV<sub>CC</sub> = 2.7 V to 5.5 V, V<sub>SS</sub> = AV<sub>SS</sub> = 0 V, T<sub>A</sub> = -40 °C to +105 °C)

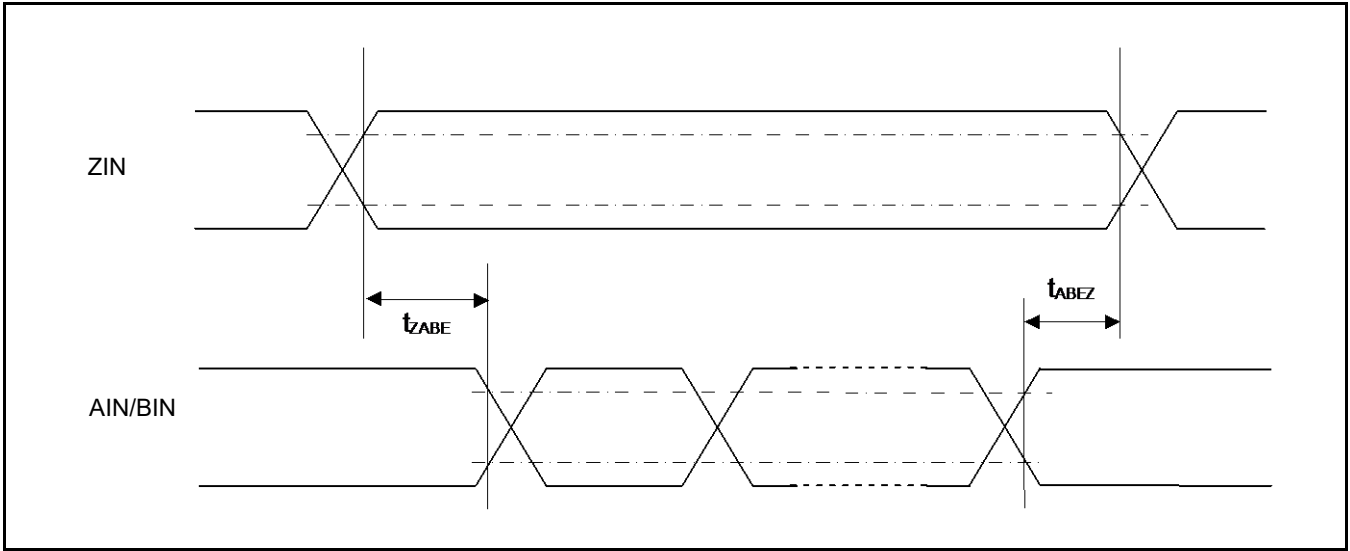
Parameter	Symbol	Conditions	Value		Unit
			Min	Max	
AIN pin H width	t <sub>AHL</sub>	-	2t <sub>CYCP</sub> *	-	ns
AIN pin L width	t <sub>ALL</sub>	-			
BIN pin H width	t <sub>BHL</sub>	-			
BIN pin L width	t <sub>BLL</sub>	-			
BIN rise time from AIN pin H level	t <sub>AUBU</sub>	PC_Mode2 or PC_Mode3			
AIN fall time from BIN pin H level	t <sub>BUAD</sub>	PC_Mode2 or PC_Mode3			
BIN fall time from AIN pin L level	t <sub>ADBD</sub>	PC_Mode2 or PC_Mode3			
AIN rise time from BIN pin L level	t <sub>BDAU</sub>	PC_Mode2 or PC_Mode3			
AIN rise time from BIN pin H level	t <sub>BUAU</sub>	PC_Mode2 or PC_Mode3			
BIN fall time from AIN pin H level	t <sub>AUBD</sub>	PC_Mode2 or PC_Mode3			
AIN fall time from BIN pin L level	t <sub>BDAD</sub>	PC_Mode2 or PC_Mode3			
BIN rise time from AIN pin L level	t <sub>ADBU</sub>	PC_Mode2 or PC_Mode3			
ZIN pin H width	t <sub>ZHL</sub>	QCR: CGSC = 0			
ZIN pin L width	t <sub>ZLL</sub>	QCR: CGSC = 0			
AIN/BIN rise and fall time from determined ZIN level	t <sub>ZABE</sub>	QCR: CGSC = 1			
Determined ZIN level from AIN/BIN rise and fall time	t <sub>ABEZ</sub>	QCR: CGSC = 1			

\*: t<sub>CYCP</sub> indicates the APB bus clock cycle time except when in Stop mode, in Timer mode. For more information about the APB bus number to which the quadrature position/revolution counter is connected, see "8. Block Diagram" in this data sheet.









**12.4.15 I<sup>2</sup>C Timing**
**Standard-mode, Fast-mode**

 (V<sub>CC</sub> = 2.7 V to 5.5 V, V<sub>SS</sub> = 0 V)

Parameter	Symbol	Conditions	Standard-mode		Fast-mode		Unit	Remarks
			Min	Max	Min	Max		
SCL clock frequency	f <sub>SCL</sub>	C <sub>L</sub> = 30 pF, R = (V <sub>p</sub> /I <sub>OL</sub> ) <sup>*1</sup>	0	100	0	400	kHz	
(Repeated) START condition hold time SDA ↓ → SCL ↓	t <sub>HDSTA</sub>		4.0	-	0.6	-	μs	
SCL clock L width	t <sub>LOW</sub>		4.7	-	1.3	-	μs	
SCL clock H width	t <sub>HIGH</sub>		4.0	-	0.6	-	μs	
(Repeated) START condition setup time SCL ↑ → SDA ↓	t <sub>SUSTA</sub>		4.7	-	0.6	-	μs	
Data hold time SCL ↓ → SDA ↓ ↑	t <sub>HDDAT</sub>		0	3.45 <sup>*2</sup>	0	0.9 <sup>*3</sup>	μs	
Data setup time SDA ↓ ↑ → SCL ↑	t <sub>SUDAT</sub>		250	-	100	-	ns	
Stop condition setup time SCL ↑ → SDA ↑	t <sub>SUSTO</sub>		4.0	-	0.6	-	μs	
Bus free time between "Stop condition" and "START condition"	t <sub>BUF</sub>		4.7	-	1.3	-	μs	
Noise filter	t <sub>SP</sub>		2 MHz ≤ t <sub>CYCP</sub> < 40 MHz	2 t <sub>CYCP</sub> <sup>*4</sup>	-	2 t <sub>CYCP</sub> <sup>*4</sup>	-	ns
		40 MHz ≤ t <sub>CYCP</sub> < 60 MHz	4 t <sub>CYCP</sub> <sup>*4</sup>	-	4 t <sub>CYCP</sub> <sup>*4</sup>	-	ns	
		60 MHz ≤ t <sub>CYCP</sub> < 80 MHz	6 t <sub>CYCP</sub> <sup>*4</sup>	-	6 t <sub>CYCP</sub> <sup>*4</sup>	-	ns	
		80 MHz ≤ t <sub>CYCP</sub> ≤ 100 MHz	8 t <sub>CYCP</sub> <sup>*4</sup>	-	8 t <sub>CYCP</sub> <sup>*4</sup>	-	ns	

\*1: R and C<sub>L</sub> represent the pull-up resistance and load capacitance of the SCL and SDA lines, respectively. V<sub>p</sub> indicates the power supply voltage of the pull-up resistance and I<sub>OL</sub> indicates V<sub>OL</sub> guaranteed current.

\*2: The maximum t<sub>HDDT</sub> must not extend beyond the low period (t<sub>LOW</sub>) of the device's SCL signal.

\*3: Fast-mode I<sup>2</sup>C bus device can be used on a Standard-mode I<sup>2</sup>C bus system as long as the device satisfies the requirement of "t<sub>SUDAT</sub> ≥ 250 ns."

\*4: t<sub>CYCP</sub> is the APB bus clock cycle time. For more information about the APB bus number to which the I<sup>2</sup>C is connected, see "8.Block Diagram" in this data sheet.

When using Standard-mode, the peripheral bus clock must be set more than 2 MHz.

When using Fast-mode, the peripheral bus clock must be set more than 8 MHz.

\*5: The noise filter time can be changed by register settings. Change the number of the noise filter steps according to the APB bus clock frequency.

## Fast Mode Plus (Fm+)

( $V_{CC} = 2.7\text{ V to }5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

Parameter	Symbol	Conditions	Fast Mode Plus (Fm+)*6		Unit	Remarks
			Min	Max		
SCL clock frequency	$f_{SCL}$	$C_L = 30\text{ pF}$ , $R = (V_p/I_{OL})^{*1}$	0	1000	kHz	
(Repeated) START condition hold time SDA ↓ → SCL ↓	$t_{HDSTA}$		0.26	-	$\mu\text{s}$	
SCL clock L width	$t_{LOW}$		0.5	-	$\mu\text{s}$	
SCL clock H width	$t_{HIGH}$		0.26	-	$\mu\text{s}$	
SCL clock frequency	$f_{SUSTA}$		0.26	-	$\mu\text{s}$	
(Repeated) START condition hold time SDA ↓ → SCL ↓	$t_{HDDAT}$		0	$0.45^{*2, *3}$	$\mu\text{s}$	
Data setup time SDA ↓ ↑ → SCL ↑	$t_{SUDAT}$		50	-	ns	
Stop condition setup time SCL ↑ → SDA ↑	$t_{SUSTO}$		0.26	-	$\mu\text{s}$	
Bus free time between "Stop condition" and "START condition"	$t_{BUF}$		0.5	-	$\mu\text{s}$	
Noise filter	$t_{SP}$		$60\text{ MHz} \leq t_{CYCP} < 80\text{ MHz}$	$6 t_{CYCP}^{*4}$	-	ns
		$80\text{ MHz} \leq t_{CYCP} \leq 100\text{ MHz}$	$8 t_{CYCP}^{*4}$	-	ns	

\*1: R and  $C_L$  represent the pull-up resistance and load capacitance of the SCL and SDA lines, respectively.  $V_p$  indicates the power supply voltage of the pull-up resistance and  $I_{OL}$  indicates  $V_{OL}$  guaranteed current.

\*2: The maximum  $t_{HDDT}$  must not extend beyond the low period ( $t_{LOW}$ ) of the device's SCL signal.

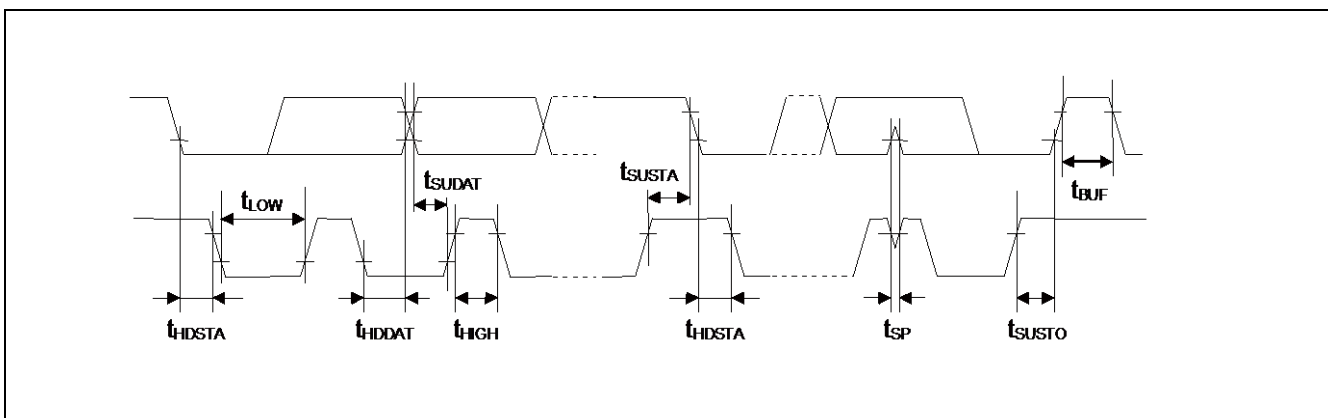
\*3: The Fast mode I<sup>2</sup>C bus device can be used on a Standard-mode I<sup>2</sup>C bus system as long as the device satisfies the requirement of " $t_{SUDAT} \geq 250\text{ ns}$ ."

\*4:  $t_{CYCP}$  is the APB bus clock cycle time. For more information about the APB bus number to which the I<sup>2</sup>C is connected, see "8.Block Diagram" in this data sheet.

To use fast mode plus (Fm+), set the peripheral bus clock at 64 MHz or more.

\*5: The noise filter time can be changed by register settings. Change the number of the noise filter steps according to the APB bus clock frequency.

\*6: When using fast mode plus (Fm+), set the I/O pin to the mode corresponding to I<sup>2</sup>C Fm+ in the EPFR register. See Chapter12: I/O PORT in FM4 Family Peripheral Manual Main Part (002-04856) for the details.



12.4.16 SD Card Interface Timing

Default-Speed Mode

■ Clock CLK (All values are referenced to  $V_{IH}$  and  $V_{IL}$  transition points)

( $V_{CC} = 2.7\text{ V to }3.6\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

Parameter	Symbol	Pin Name	Conditions	Value		Remarks
				Min	Max	
Clock frequency Data Transfer Mode	$f_{PP}$	S_CLK	$C_{CARD} \leq 10\text{ pF}$ (1card)	0	25	MHz
Clock frequency Identification Mode	$f_{OD}$	S_CLK		0/100	400	kHz
Clock low time	$t_{WL}$	S_CLK		10	-	ns
Clock high time	$t_{WH}$	S_CLK		10	-	ns
Clock rise time	$t_{TLH}$	S_CLK		-	10	ns
Clock fall time	$t_{THL}$	S_CLK		-	10	ns

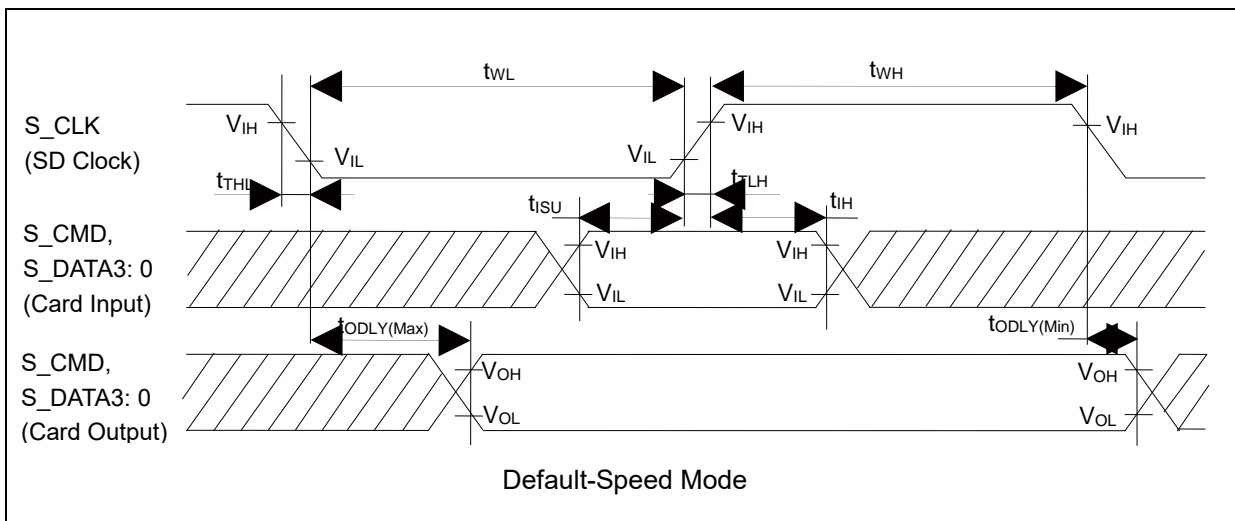
\* 0 Hz means to stop the clock. The given minimum frequency range is for cases where a continuous clock is required.

■ Card Inputs CMD, DAT (referenced to Clock CLK)

Parameter	Symbol	Pin Name	Conditions	Value		Remarks
				Min	Max	
Input set-up time	$t_{ISU}$	S_CMD, S_DATA3: 0	$C_{CARD} \leq 10\text{ pF}$ (1card)	5	-	ns
Input hold time	$t_{IH}$	S_CMD, S_DATA3: 0		5	-	ns

■ Card Outputs CMD, DAT (referenced to Clock CLK)

Parameter	Symbol	Pin Name	Conditions	Value		Remarks
				Min	Max	
Output Delay time during Data Transfer Mode	$t_{ODLY}$	S_CMD, S_DATA3: 0	$C_{CARD} \leq 40\text{ pF}$ (1card)	0	14	ns
Output Delay time during Identification Mode	$t_{ODLY}$	S_CMD, S_DATA3: 0		0	50	ns



Notes:

- The Card Input corresponds to the Host Output and the Card Output corresponds to the Host Input because this model is the Host.
- For more information about clock frequency ( $f_{PP}$ ), see Chapter 15: SD card Interface in FM4 Family Peripheral Manual Main Part (002-04856).

### High-Speed Mode

■ Clock CLK (All values are referred to  $V_{IH}$  and  $V_{IL}$ )

( $V_{CC} = 2.7\text{ V to }3.6\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

Parameter	Symbol	Pin Name	Conditions	Value		Remarks
				Min	Max	
Clock frequency Data Transfer Mode	$f_{PP}$	S_CLK	$C_{CARD} \leq 10\text{ pF}$ (1 card)	0	50	MHz
Clock low time	$t_{WL}$	S_CLK		7	-	ns
Clock high time	$t_{WH}$	S_CLK		7	-	ns
Clock rise time	$t_{TLH}$	S_CLK		-	3	ns
Clock fall time	$t_{THL}$	S_CLK		-	3	ns

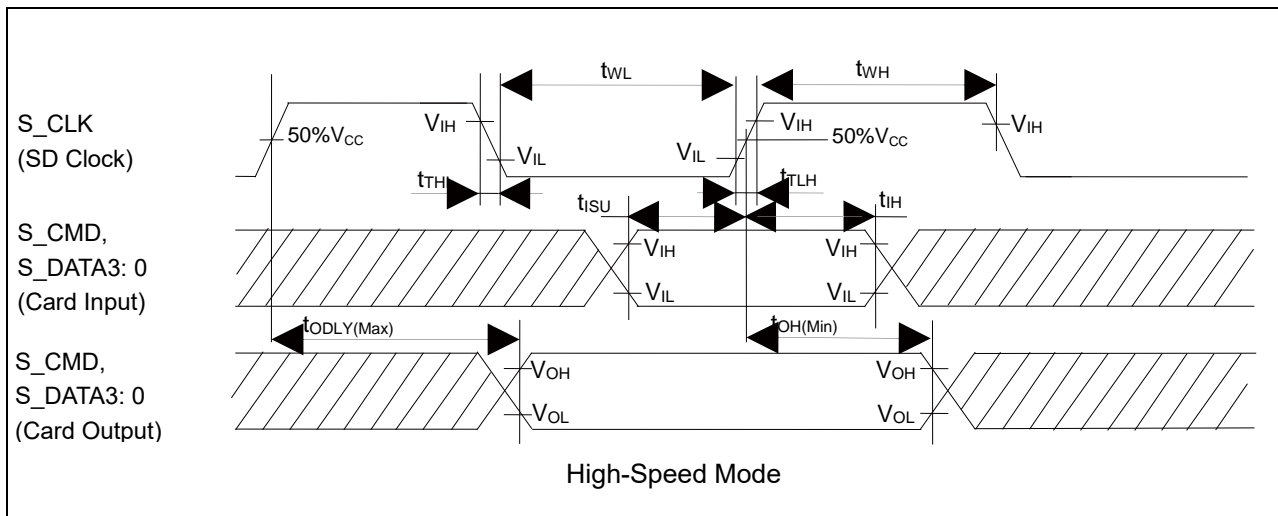
■ Card Inputs CMD, DAT (referenced to Clock CLK)

Parameter	Symbol	Pin Name	Conditions	Value		Remarks
				Min	Max	
Input set-up time	$t_{ISU}$	S_CMD, S_DATA3: 0	$C_{CARD} \leq 10\text{ pF}$ (1 card)	6	-	ns
Input hold time	$t_{IH}$	S_CMD, S_DATA3: 0		2	-	ns

■ Card Outputs CMD, DAT (referenced to Clock CLK)

Parameter	Symbol	Pin Name	Conditions	Value		Remarks
				Min	Max	
Output delay time during data transfer mode	$t_{ODLY}$	S_CMD, S_DATA3: 0	$C_L \leq 40\text{ pF}$ (1 card)	0	14	ns
Output hold time	$t_{OH}$	S_CMD, S_DATA3: 0	$C_L \geq 15\text{ pF}$ (1 card)	2.5	-	ns
Total system capacitance for each line*	$C_L$	-	1 card	-	40	pF

\*: In order to satisfy severe timing, host shall drive only one card.



**Notes:**

- The Card Input corresponds to the Host Output and the Card Output corresponds to the Host Input because this model is the Host.
- For more information about clock frequency ( $f_{PP}$ ), see Chapter 15: SD card Interface in FM4 Family Peripheral Manual Main Part (002-04856).

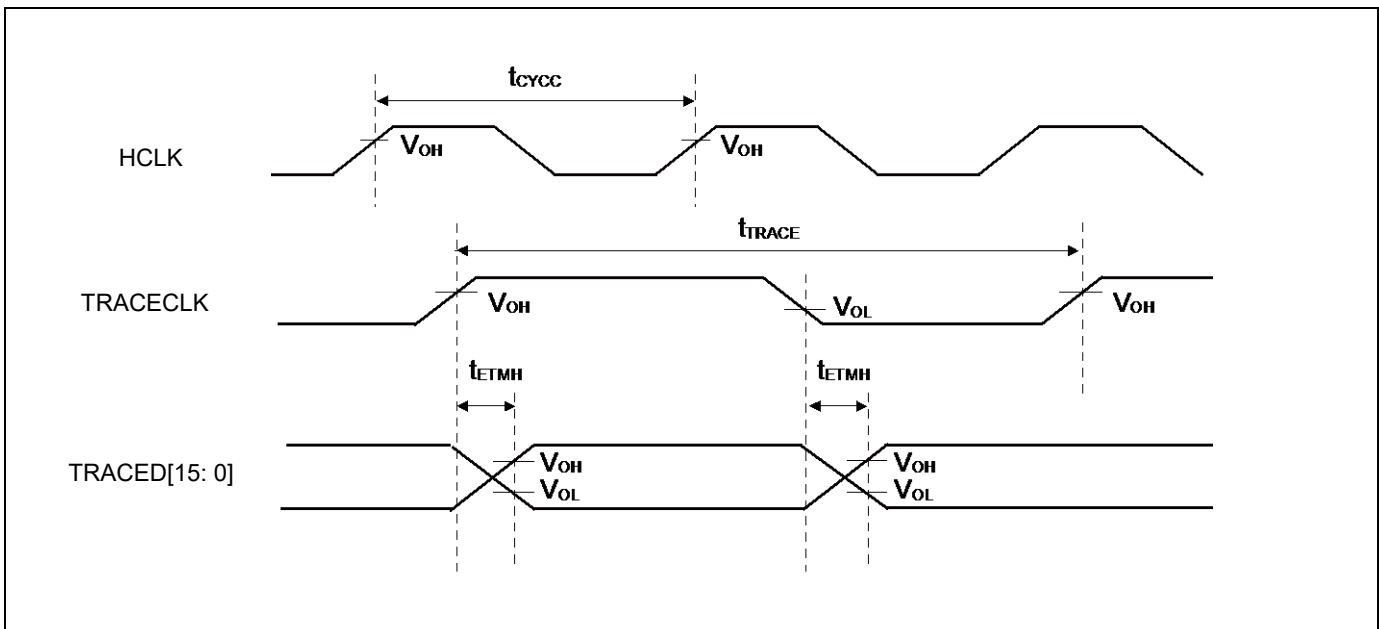
**12.4.17 ETM/ HTM Timing**

 (V<sub>CC</sub> = 2.7 V to 5.5 V, V<sub>SS</sub> = 0 V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Data hold	t <sub>ETMH</sub>	TRACECLK, TRACED[15: 0]	V <sub>CC</sub> ≥ 4.5 V	2	9	ns	
			V <sub>CC</sub> < 4.5 V	2	15		
TRACECLK frequency	1/t <sub>TRACE</sub>	TRACECLK	V <sub>CC</sub> ≥ 4.5 V		50	MHz	
			V <sub>CC</sub> < 4.5 V		32	MHz	
TRACECLK clock cycle	t <sub>TRACE</sub>		V <sub>CC</sub> ≥ 4.5 V	20	-	ns	
			V <sub>CC</sub> < 4.5 V	31.25	-	ns	

**Note:**

- When the external load capacitance C<sub>L</sub> = 30 pF.



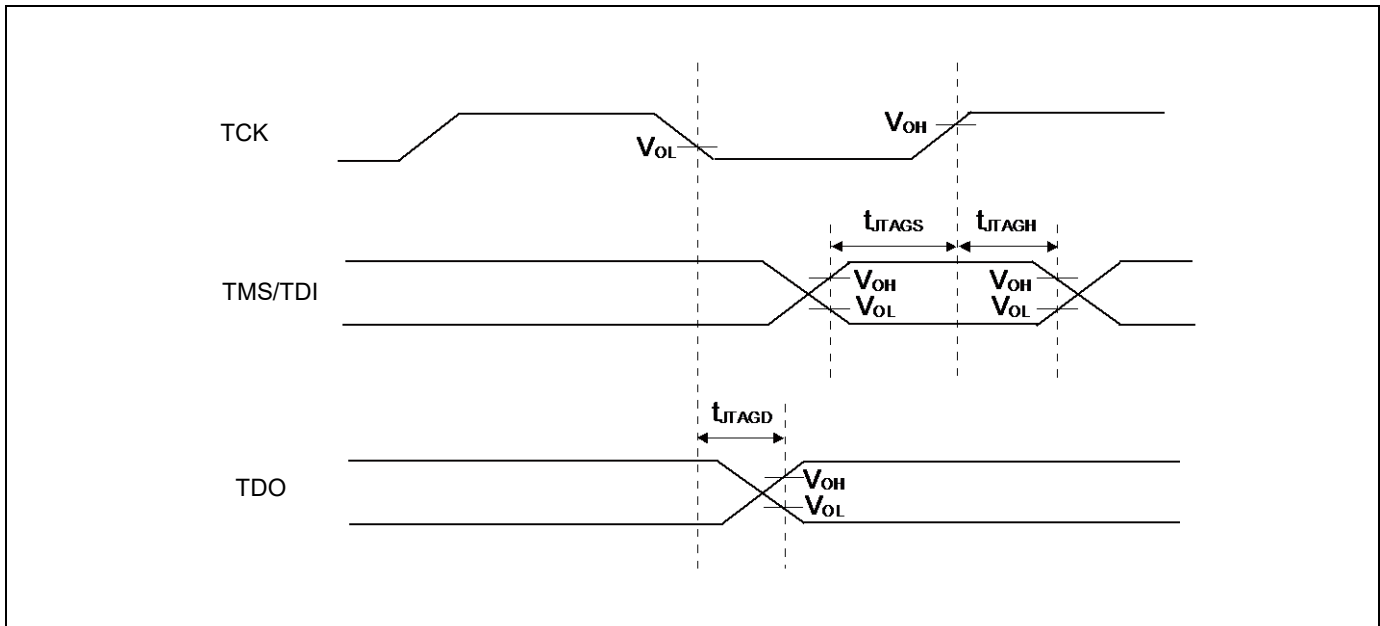
**12.4.18 JTAG Timing**

 (V<sub>CC</sub> = 2.7 V to 5.5 V, V<sub>SS</sub> = 0 V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
TMS, TDI setup time	t <sub>JTAGS</sub>	TCK, TMS, TDI	V <sub>CC</sub> ≥ 4.5 V	15	-	ns	
			V <sub>CC</sub> < 4.5 V				
TMS, TDI hold time	t <sub>JTAGH</sub>	TCK, TMS, TDI	V <sub>CC</sub> ≥ 4.5 V	15	-	ns	
			V <sub>CC</sub> < 4.5 V				
TDO delay time	t <sub>JTAGD</sub>	TCK, TDO	V <sub>CC</sub> ≥ 4.5 V	-	25	ns	
			V <sub>CC</sub> < 4.5 V	-	45		

**Note:**

- When the external load capacitance C<sub>L</sub> = 30 pF.





**12.4.19 I<sup>2</sup>S Timing**
**Master Mode Timing**

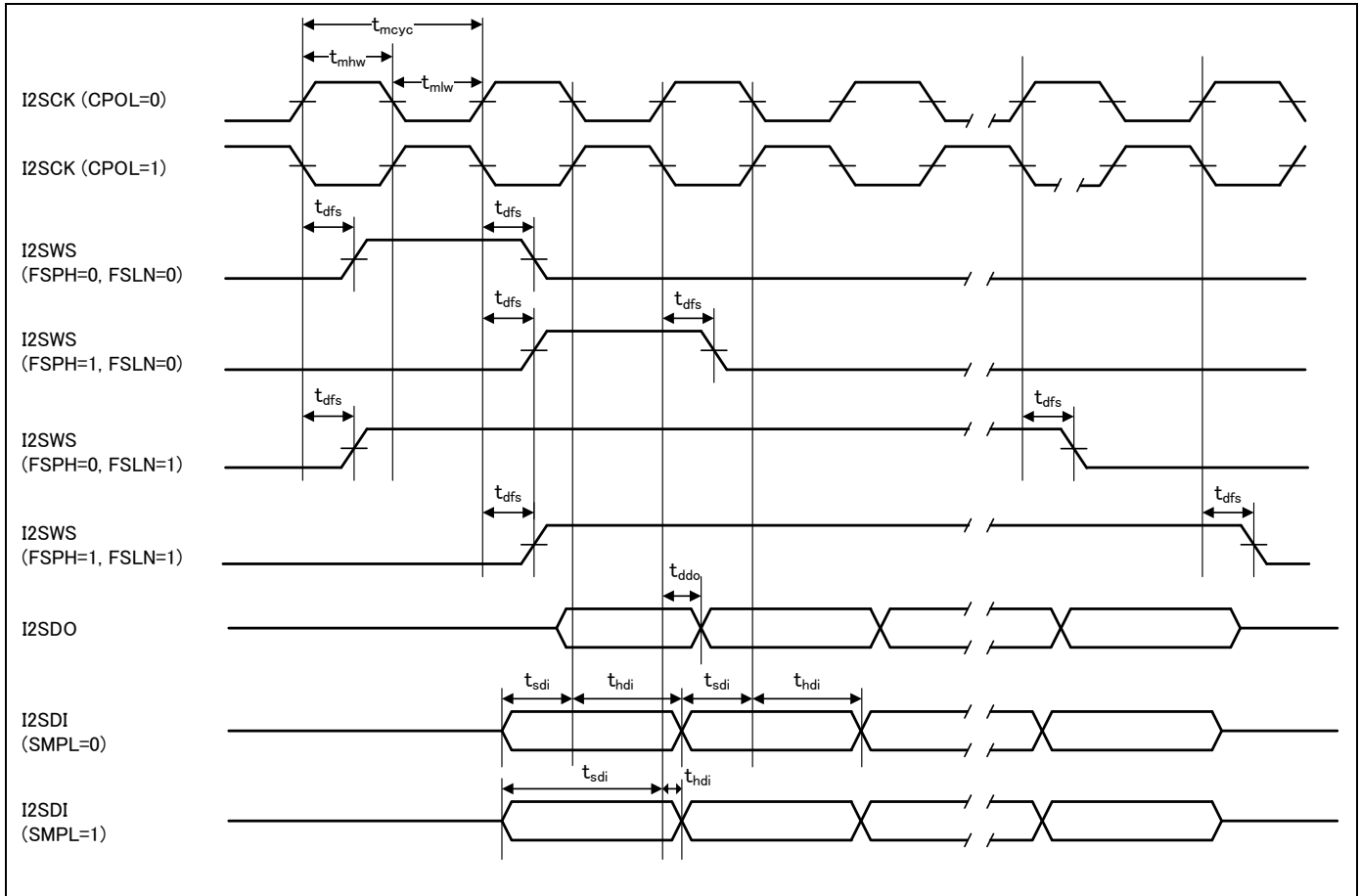
 (V<sub>CC</sub> = 2.7 V to 5.5 V, V<sub>SS</sub> = 0 V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Output frequency	f <sub>M CYC</sub>	I2SCK	-	-	12.288	MHz	
Output clock pulse width	t <sub>M HW</sub>	I2SCK	-	45	55	%	
	t <sub>M LW</sub>			45	55	%	
I2SCK→I2SWS delay time	t <sub>D FS</sub>	I2SCK, I2SWS	-	0	24.0	ns	
I2SCK→I2SDO delay time*	t <sub>D DO</sub>	I2SCK, I2SDO	-	0	24.0	ns	
I2SDI→I2SCK setup time	t <sub>H SDI</sub>	I2SCK, I2SDI	-	25.0	-	ns	
I2SDI→I2SCK hold time	t <sub>H DI</sub>		-	0	-	ns	
Input signal rise time	t <sub>F I</sub>	I2SDI	-	-	5	ns	
Input signal fall time	t <sub>F I</sub>		-	-	5	ns	

\*: Except for the first bit of transmission frame

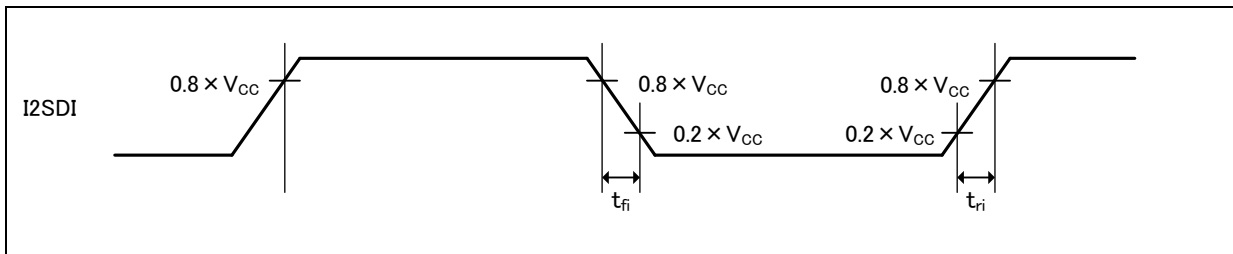
**Notes:**

- When the external load capacitance C<sub>L</sub> = 20 pF
- When I2SWS = 48 kHz, I2MCLK = 256 × I2SWS  
 Frame synchronization signal (I2SWS) is settable to 48 kHz, 32 kHz, 16 kHz.  
 See Chapter7-2: I<sup>2</sup>S (Inter-IC Sound bus) Interface in FM4 Family Peripheral Manual Communication Macro Part (002-04862) for the details.



**Note:**

- See Chapter7-2: I<sup>2</sup>S (Inter-IC Sound bus) Interface in FM4 Family Peripheral Manual Communication Macro Part (002-04862) for the details of CPOL, FSPH, FSLIN, and SMPL.



**Slave Mode Timing**

 (V<sub>CC</sub> = 2.7 V to 5.5 V, V<sub>SS</sub> = 0 V)

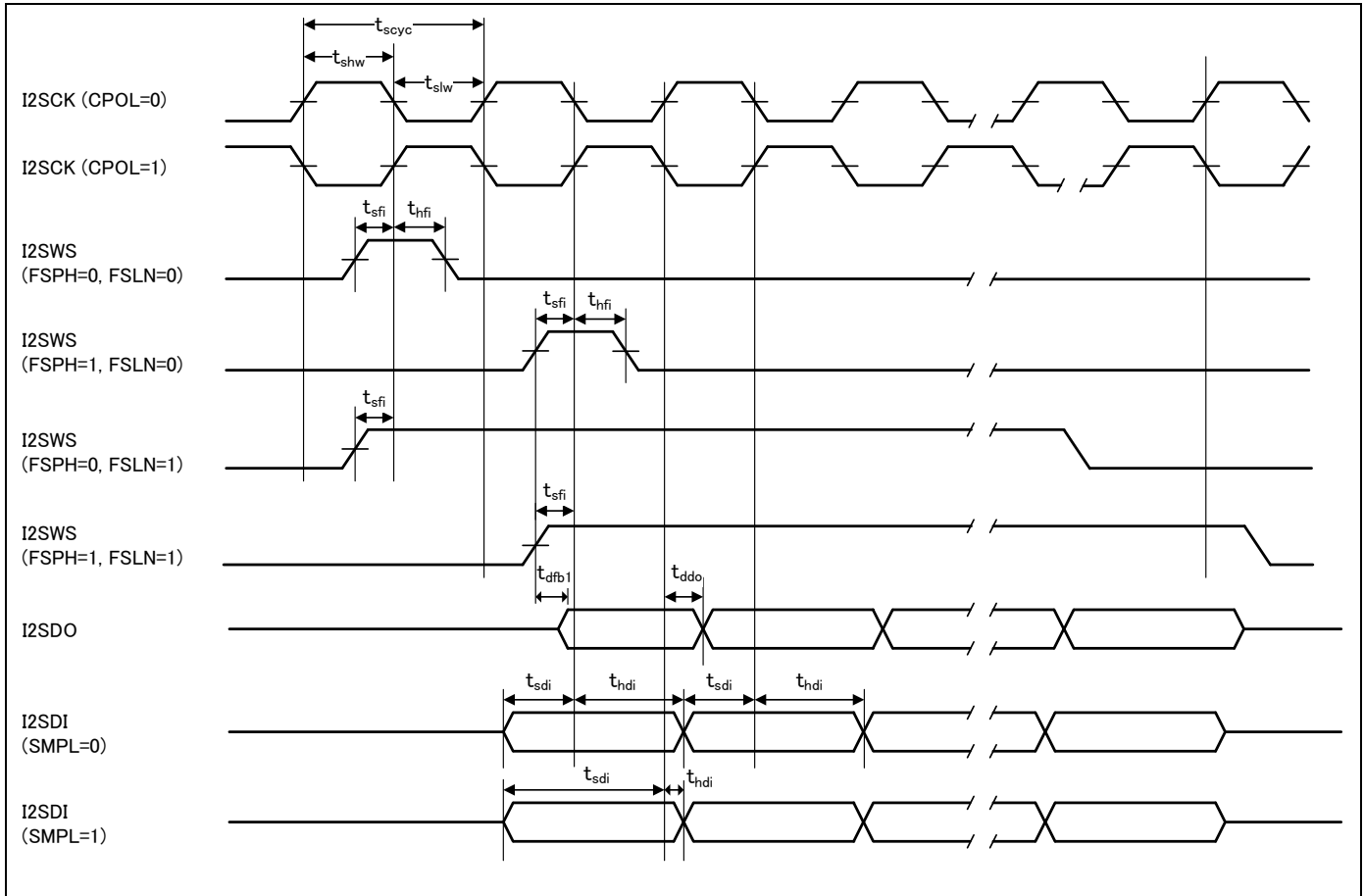
Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input frequency	f <sub>SCYC</sub>	I2SCK	-	-	12.288	MHz	
Input clock pulse width	t <sub>SHW</sub>	I2SCK	-	45	55	%	
	t <sub>SLW</sub>			45	55	%	
I2SWS → I2SCK Setup time	t <sub>SFI</sub>	I2SCK, I2SWS	-	8	-	ns	
I2SWS → I2SCK Hold time	t <sub>HFI</sub>	I2SCK, I2SWS	-	0	-	ns	
I2SCK ↑ → I2SDO Delay time* <sup>1</sup>	t <sub>DDO</sub>	I2SCK, I2SDO	-	0	32	ns	
I2SCK ↑ → I2SDO Delay time* <sup>2</sup>	t <sub>DFB1</sub>		-	0	32	ns	
I2SDI → I2SCK ↓ Setup time	t <sub>SDI</sub>	I2SCK, I2SDI	-	8	-	ns	
I2SDI → I2SCK ↓ Hold time	t <sub>HDI</sub>		-	0	-	ns	
Input signal rise time	t <sub>FI</sub>	I2SCK, I2SWS, I2SDI	-	-	5	ns	
Input signal fall time	t <sub>FI</sub>		-	-	5	ns	

\*1: Except for the first bit of transmission frame

\*2: When FSPH bit = 1.

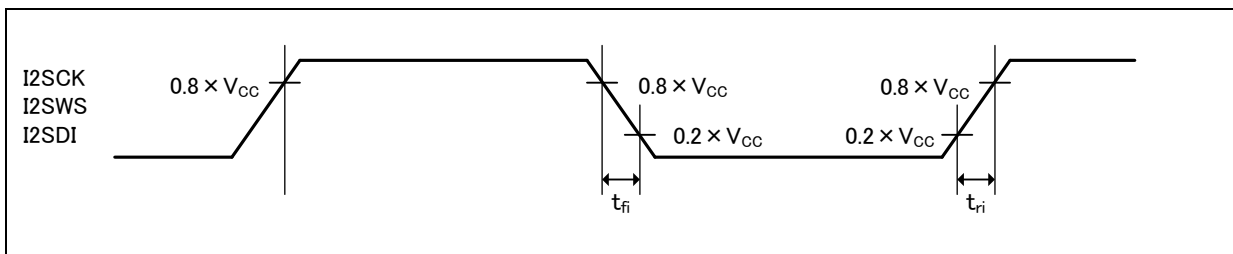
**Notes:**

- When the external load capacitance C<sub>L</sub> = 20 pF
- When I2SWS = 48 kHz, I2MCLK = 256 × I2SWS  
 Frame synchronization signal (I2SWS) is settable to 48 kHz, 32 kHz, 16 kHz. See Chapter 7-2: I<sup>2</sup>S (Inter-IC Sound bus) Interface in FM4 Family Peripheral Manual Communication Macro Part (002-04862) for the details.



**Notes:**

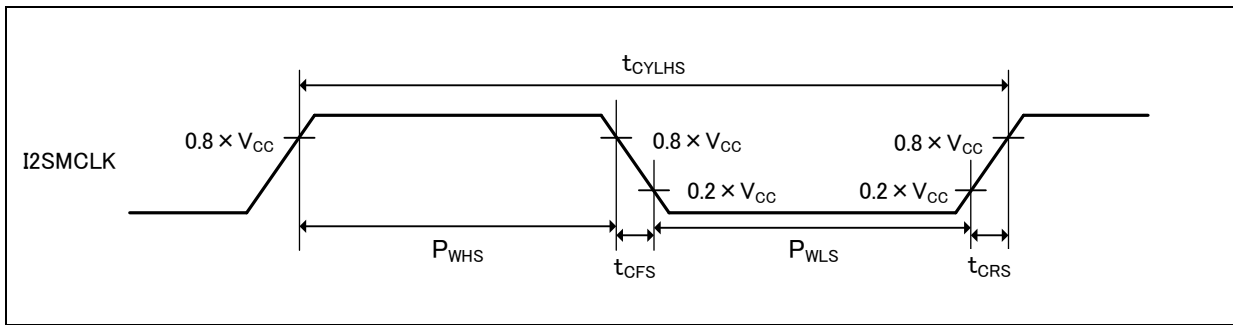
- See Chapter7-2: I<sup>2</sup>S (Inter-IC Sound bus) Interface in FM4 Family Peripheral Manual Communication Macro Part (002-04862) for the details of FSPH, FSLN, SMPL
- I2SCK input is selectable polarity by CPOL bit of CNTREG register



I2SMCLK Input Characteristics

( $V_{CC} = 2.7\text{ V to }5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input frequency	$f_{CHS}$	I2SMCK	-	-	25	MHz	
Input clock cycle	$t_{CYLHS}$	-	-	40	-	ns	
Input clock pulse width	-	-	$P_{WHS}/t_{CYLHS}$ $P_{WLS}/t_{CYLHS}$	45	55	%	When using external clock
Input clock rise time and fall time	$t_{CFS}$ $t_{CRS}$	-	-	-	5	ns	When using external clock



I2SMCLK Output Characteristics

( $V_{CC} = 2.7\text{ V to }5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Output frequency	$f_{CHS}$	I2SMCK	-	-	12.288	MHz	

**12.4.20 High-Speed Quad SPI Timing**

 (V<sub>CC</sub> = 2.7 V to 3.6 V, V<sub>SS</sub> = 0 V)

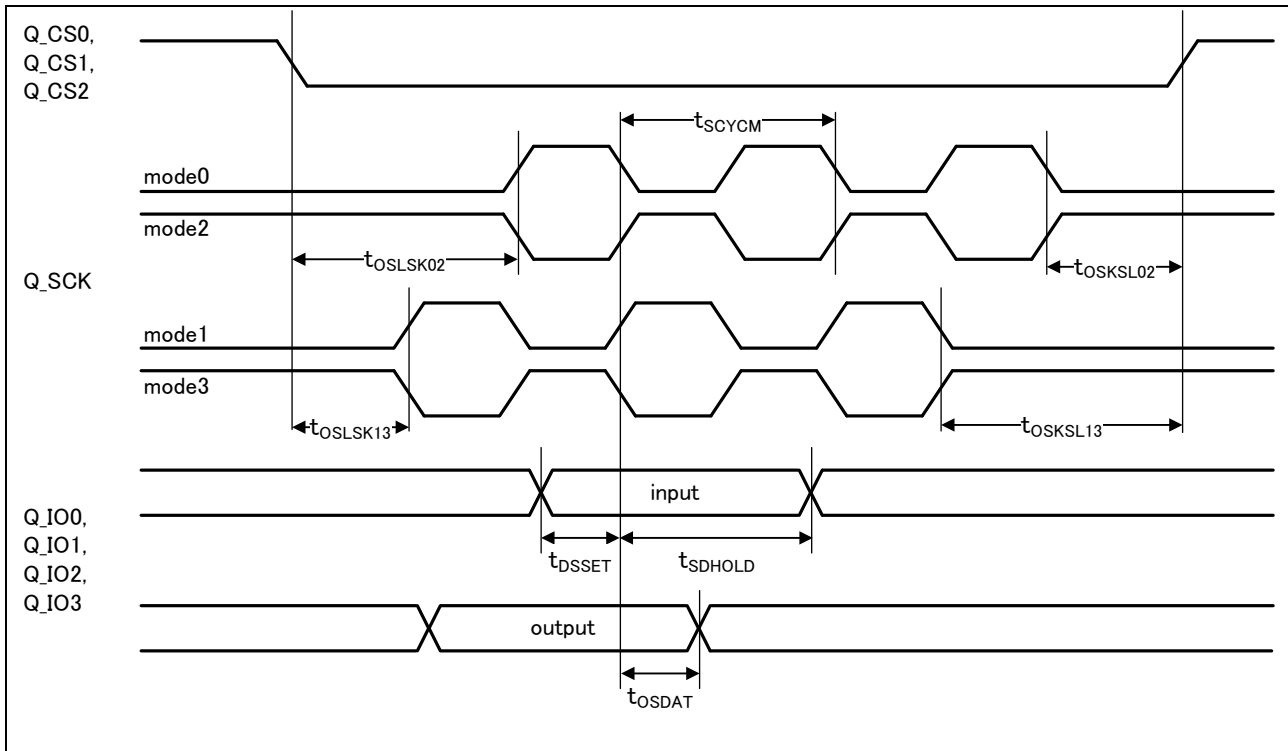
Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock frequency	t <sub>SCYCM</sub>	Q_SCK_0	C <sub>L</sub> = 15 pF, V <sub>CC</sub> = 3.0 to 3.6V	-	66	MHz	*1
			C <sub>L</sub> = 30 pF	-	50	MHz	*2
Enabled CS→ CLK Starting Time (mode0/mode2)	t <sub>OSLSK02</sub>	Q_SCK_0, Q_CS0_0, Q_CS1_0, Q_CS2_0	C <sub>L</sub> = 30 pF	1.5 × t <sub>SCYCM</sub> - 5	-	ns	
Enabled CS→ CLK Starting Time (mode1/mode3)	t <sub>OSLSK13</sub>			t <sub>SCYCM</sub> - 5	-	ns	
CLK Last→ Disabled CS Time (mode0/mode2)	t <sub>OSKSL02</sub>			t <sub>SCYCM</sub>	-	ns	
CLK Last→ Disabled CS Time (mode1/mode3)	t <sub>OSKSL13</sub>			1.5 × t <sub>SCYCM</sub>	-	ns	
SIO Data output time	t <sub>OSDAT</sub>	Q_SCK_0, Q_IO0_0, Q_IO1_0, Q_IO2_0, Q_IO3_0	C <sub>L</sub> = 15 pF, V <sub>CC</sub> = 3.0 to 3.6V	0	5	ns	
			C <sub>L</sub> = 30 pF	0	5		
SIO Setup	t <sub>DSSET</sub>	Q_SCK_0, Q_IO0_0, Q_IO1_0, Q_IO2_0, Q_IO3_0	C <sub>L</sub> = 30 pF	3	-	ns	*1
				10	-		*2
SIO Hold	t <sub>SDHOLD</sub>		C <sub>L</sub> = 30 pF	0.5 × t <sub>SCYCM</sub>	-	ns	

\*1: When RTM = 1 and mode = 0, 1, 3

\*2: When RTM = 1 and mode = 2 or RTM = 0 and mode = 0, 1, 2, 3

**Notes:**

- See Chapter8-3: High-Speed Quad SPI controller in FM4 Family Peripheral Manual Communication Macro Part (002-04862) for the detail of RTM mode.
- When using High-Speed Quad SPI, please set PDSR register to set the pin drive capability for V<sub>CC</sub> = 3 V. See Chapter12: I/O Port in FM4 Family Peripheral Manual Main Part (002-04856) for the details.



**12.5 12-bit A/D Converter**
**Electrical Characteristics for the A/D Converter**

 (V<sub>CC</sub> = AV<sub>CC</sub> = 2.7 V to 5.5 V, V<sub>SS</sub> = AV<sub>SS</sub> = AV<sub>RL</sub> = 0 V)

Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	12	bit	
Integral nonlinearity	-	-	- 4.5	-	+ 4.5	LSB	AVRH = 2.7 V to 5.5 V
Differential nonlinearity	-	-	- 2.5	-	+ 2.5	LSB	
Zero transition voltage	V <sub>ZT</sub>	ANxx	- 15	-	+ 15	mV	
Full-scale transition voltage	V <sub>FST</sub>	ANxx	AVRH - 15	-	AVRH + 15	mV	
			AV <sub>CC</sub> - 15	-	AV <sub>CC</sub> + 15	mV	
Conversion time	-	-	0.5 <sup>*1</sup>	-	-	μs	AV <sub>CC</sub> ≥ 4.5 V
Sampling time *2	T <sub>s</sub>	-	0.15	-	10	μs	AV <sub>CC</sub> ≥ 4.5 V
			0.3	-			AV <sub>CC</sub> < 4.5 V
Compare clock cycle *3	T <sub>ck</sub>	-	25	-	1000	ns	AV <sub>CC</sub> ≥ 4.5 V
			50	-			AV <sub>CC</sub> < 4.5 V
State transition time to operation permission	T <sub>stt</sub>	-	-	-	1.0	μs	
Power supply current (analog + digital)	-	AV <sub>CC</sub>	-	0.69	0.92	mA	A/D 1 unit operation
			-	1.3	22	μA	When A/D stop
Reference power supply current (AVRH)	-	AVRH	-	1.1	1.97	mA	A/D 1 unit operation AVRH = 5.5 V
			-	0.3	6.3	μA	When A/D stop
Analog input capacity	C <sub>AIN</sub>	-	-	-	12.05	pF	
Analog input resistance	R <sub>AIN</sub>	-	-	-	1.2	kΩ	AV <sub>CC</sub> ≥ 4.5 V
					1.8		AV <sub>CC</sub> < 4.5 V
Interchannel disparity	-	-	-	-	4	LSB	
Analog port input leak current	-	ANxx	-	-	5	μA	
Analog input voltage	-	ANxx	AV <sub>SS</sub>	-	AVRH	V	
			AV <sub>SS</sub>	-	AV <sub>CC</sub>	V	
Reference voltage	-	AVRH	4.5	-	AV <sub>CC</sub>	V	T <sub>ck</sub> < 50 ns
			2.7	-	AV <sub>CC</sub>		T <sub>ck</sub> ≥ 50 ns
	-	AVRL	AV <sub>SS</sub>	-	AV <sub>SS</sub>	V	

\*1: The conversion time is the value of sampling time (T<sub>s</sub>) + compare time (T<sub>c</sub>).

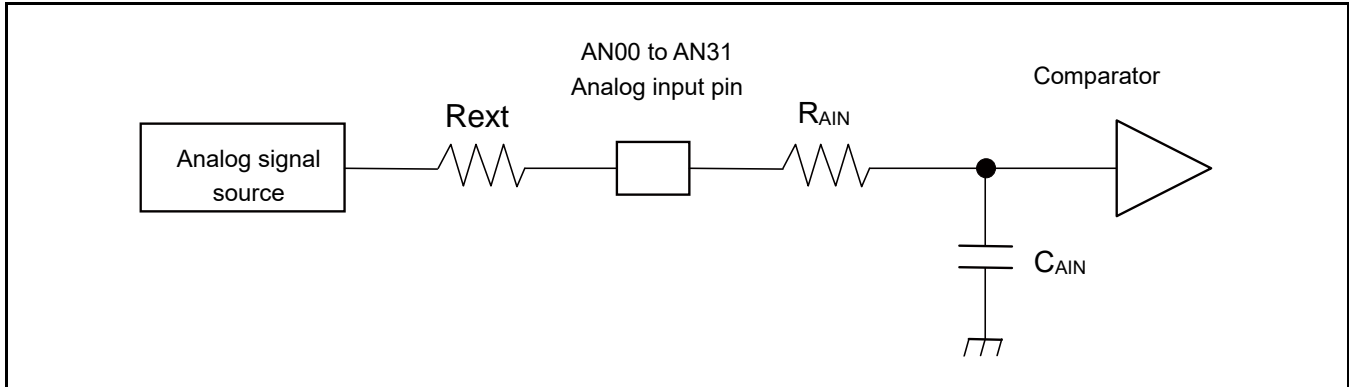
The condition of the minimum conversion time is when the value of T<sub>s</sub> = 150 ns and T<sub>c</sub> = 350 ns (AV<sub>CC</sub> ≥ 4.5V). Ensure that it satisfies the value of sampling time (T<sub>s</sub>) and compare clock cycle (T<sub>ck</sub>). For setting of sampling time and compare clock cycle, see Chapter 1-1: A/D Converter in FM4 Family Peripheral Manual Analog Macro Part (002-04860). The register setting of the A/D converter is reflected by the APB bus clock timing. For more information about the APB bus number to which the A/D converter is connected, see 8. Block Diagram in this data sheet.

The sampling and compare clock are set at base clock (HCLK).

\*2: A necessary sampling time changes by external impedance. Ensure that it sets the sampling time to satisfy (Equation 1).

\*3: The compare time (T<sub>c</sub>) is the value of (Equation 2).





(Equation 1)  $T_s \geq (R_{AIN} + R_{ext}) \times C_{AIN} \times 9$

$T_s$ : Sampling time

$R_{AIN}$ : Input resistance of A/D = 1.2 k $\Omega$  at 4.5 V  $\leq AV_{CC} \leq$  5.5 V

Input resistance of A/D = 1.8 k $\Omega$  at 2.7 V  $\leq AV_{CC} <$  4.5 V

$C_{AIN}$ : Input capacity of A/D = 12.05 pF at 2.7 V  $\leq AV_{CC} \leq$  5.5 V

$R_{ext}$ : Output impedance of external circuit

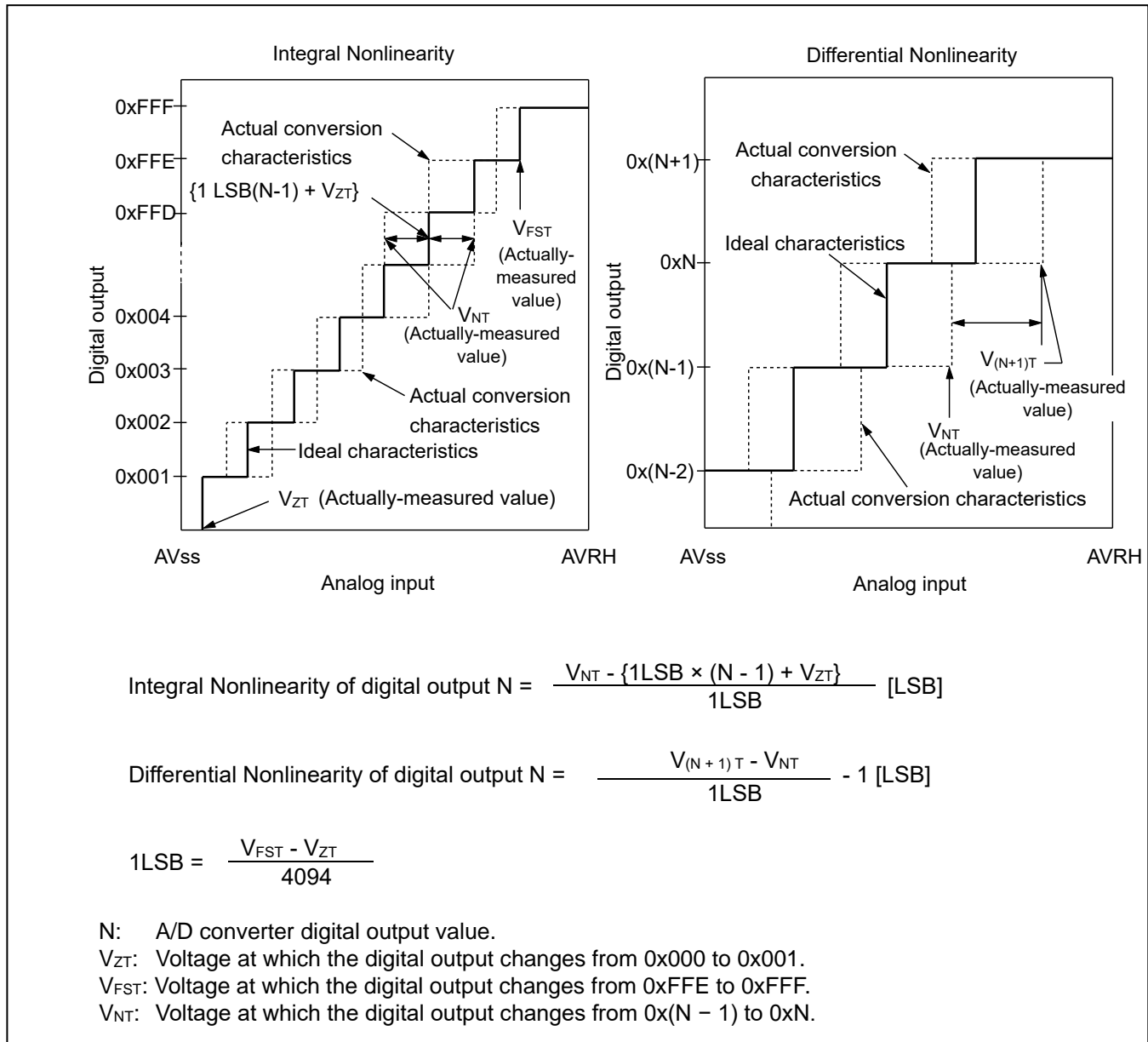
(Equation 2)  $T_c = T_{cck} \times 14$

$T_c$ : Compare time

$T_{cck}$ : Compare clock cycle

**Definition of 12-bit A/D Converter Terms**

- Resolution: Analog variation that is recognized by an A/D converter.
- Integral Nonlinearity: Deviation of the line between the zero-transition point (0b000000000000 ↔ 0b000000000001) and the full-scale transition point (0b111111111110 ↔ 0b111111111111) from the actual conversion characteristics.
- Differential Nonlinearity: Deviation from the ideal value of the input voltage that is required to change the output code by 1 LSB.



**12.6 12-bit D/A Converter**
**Electrical Characteristics for the D/A Converter**

 (V<sub>CC</sub> = AV<sub>CC</sub> = 2.7 V to 5.5 V, V<sub>SS</sub> = AV<sub>SS</sub> = 0 V)

Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	DAx	-	-	12	bit	
Conversion time	t <sub>C20</sub>		0.56	0.69	0.81	μs	Load 20 pF
	t <sub>C100</sub>		2.79	3.42	4.06	μs	Load 100 pF
Integral nonlinearity *	INL		- 16	-	+ 16	LSB	
Differential nonlinearity *	DNL		- 0.98	-	+ 1.5	LSB	
Output voltage offset	V <sub>OFF</sub>		-	-	+ 10	mV	When setting 0x000
			- 20.0	-	+ 1.4	mV	When setting 0xFFFF
Analog output impedance	R <sub>O</sub>	3.10	3.80	4.50	kΩ	D/A operation	
		2.0	-	-	MΩ	When D/A stop	
Power supply current *	IDDA	AVCC	260	330	410	μs	D/A 1ch operation AV <sub>CC</sub> = 3.3 V
			400	510	620	μs	D/A 1ch operation AV <sub>CC</sub> = 5.0 V
	IDSA		-	-	14	μs	When D/A stop

\*: During no load

12.7 USB Characteristics

(V<sub>CC</sub> = AV<sub>CC</sub> = 2.7 V to 5.5 V, USBV<sub>CC0</sub> = USBV<sub>CC1</sub> = 3.0 V to 3.6 V, V<sub>SS</sub> = AV<sub>SS</sub> = 0 V)

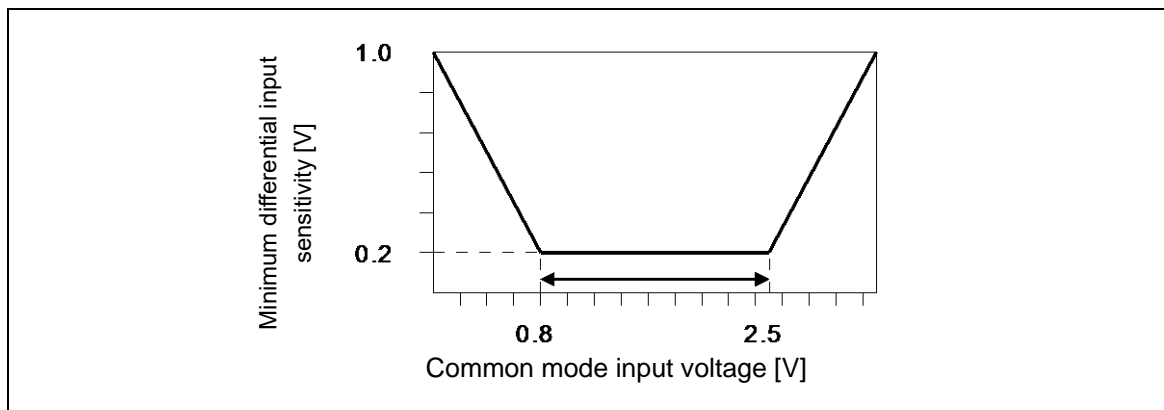
Parameter		Symbol	Pin Name	Conditions	Value		Unit	Remarks
					Min	Max		
Input characteristics	Input H level voltage	V <sub>IH</sub>	UDP0/ UDM0, UDP1/ UDM1	-	2.0	USBV <sub>CC</sub> + 0.3	V	*1
	Input L level voltage	V <sub>IL</sub>		-	V <sub>SS</sub> - 0.3	0.8	V	*1
	Differential input sensitivity	V <sub>DI</sub>		-	0.2	-	V	*2
	Different common mode range	V <sub>CM</sub>		-	0.8	2.5	V	*2
Output characteristics	Output H level voltage	V <sub>OH</sub>		External pull-down resistance = 15 kΩ	2.8	3.6	V	*3
	Output L level voltage	V <sub>OL</sub>		External pull-up resistance = 1.5 kΩ	0.0	0.3	V	*3
	Crossover voltage	V <sub>CRS</sub>		-	1.3	2.0	V	*4
	Rise time	t <sub>FR</sub>		Full-Speed	4	20	ns	*5
	Fall time	t <sub>FF</sub>		Full-Speed	4	20	ns	*5
	Rise/fall time matching	t <sub>FRFM</sub>		Full-Speed	90	111.11	%	*5
	Output impedance	Z <sub>DRV</sub>	Full-Speed	28	44	Ω	*6	
	Rise time	t <sub>LR</sub>	Low-Speed	75	300	ns	*7	
	Fall time	t <sub>LF</sub>	Low-Speed	75	300	ns	*7	
	Rise/fall time matching	t <sub>LRFM</sub>	Low-Speed	80	125	%	*7	

\*1: The switching threshold voltage of the single-end-receiver of USB I/O buffer is set as within V<sub>IL</sub> (Max) = 0.8 V, V<sub>IH</sub> (Min) = 2.0 V (TTL input standard).

There is some hysteresis applied to lower noise sensitivity.

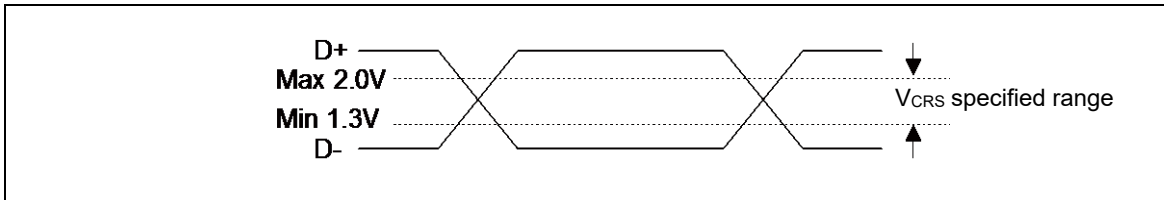
\*2: Use differential-receiver to receive USB differential data signal. Differential-receiver has 200 mV of differential input sensitivity when the differential data input is within 0.8 V to 2.5 V to the local ground reference level.

Above voltage range is the common mode input voltage range.

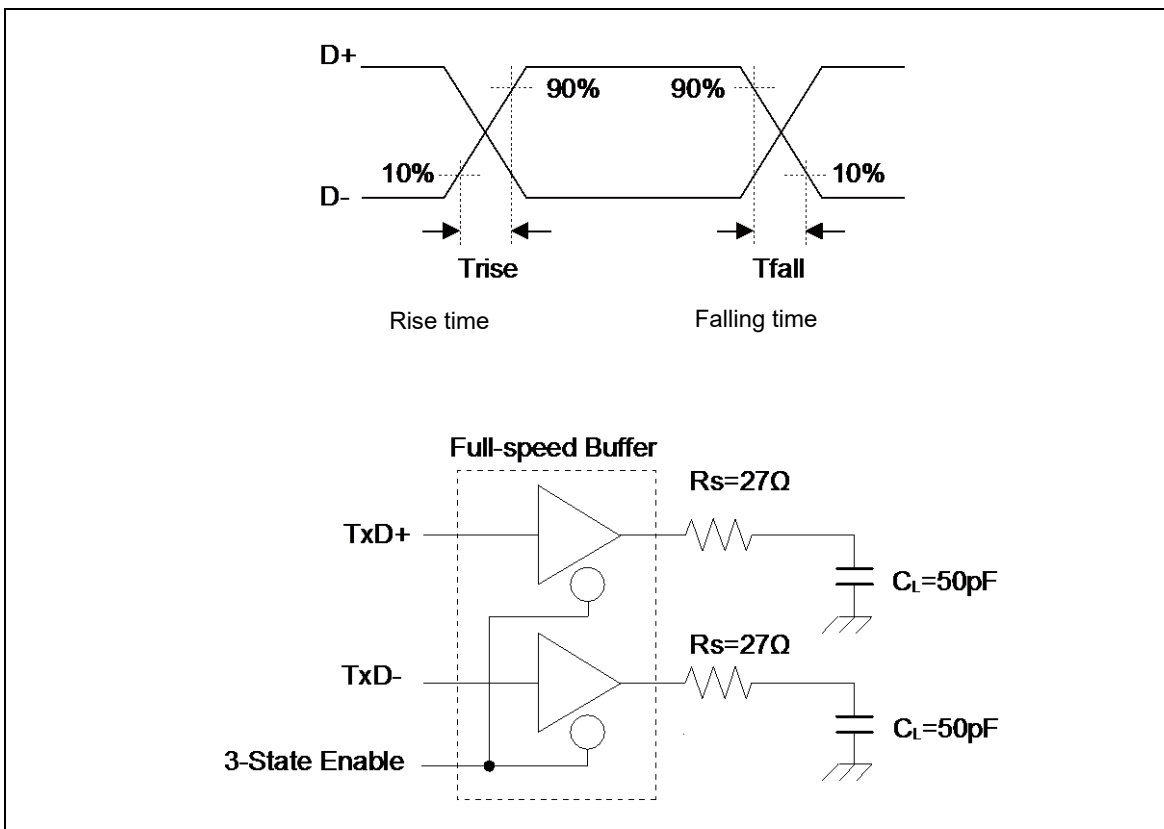


\*3: The output drive capability of the driver is below 0.3 V at low state ( $V_{OL}$ ) (to 3.6 V and 1.5 k $\Omega$  load), and 2.8 V or above (to the VSS and 1.5 k $\Omega$  load) at high state ( $V_{OH}$ ).

\*4: The cross voltage of the external differential output signal (D +/D -) of USB I/O buffer is within 1.3 V to 2.0 V.

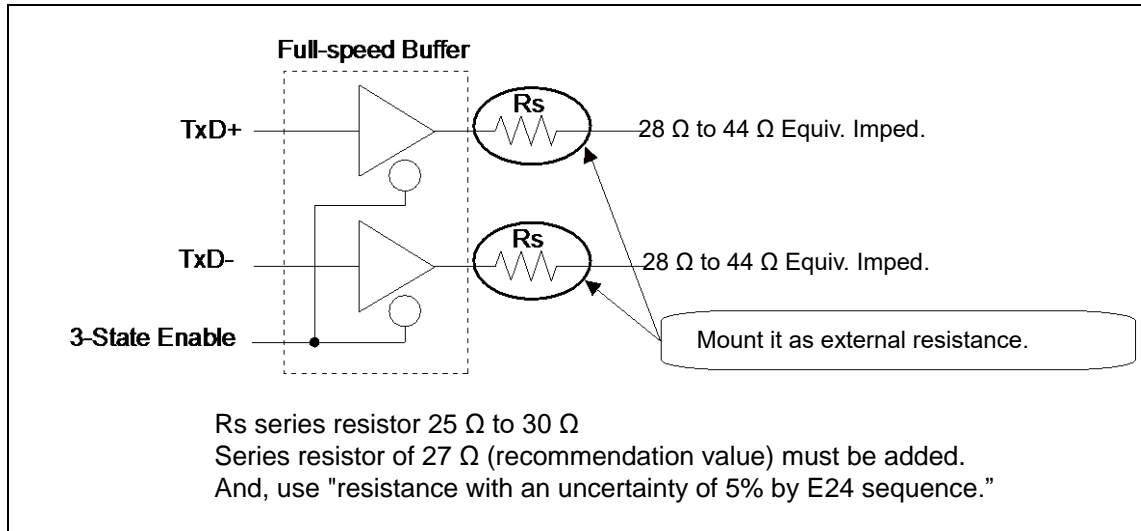


\*5: They indicate rise time ( $T_{rise}$ ) and fall time ( $T_{fall}$ ) of the full-speed differential data signal. They are defined by the time between 10% and 90% of the output signal voltage. For full-speed buffer,  $T_r/T_f$  ratio is regulated as within  $\pm 10\%$  to minimize RFI emission.

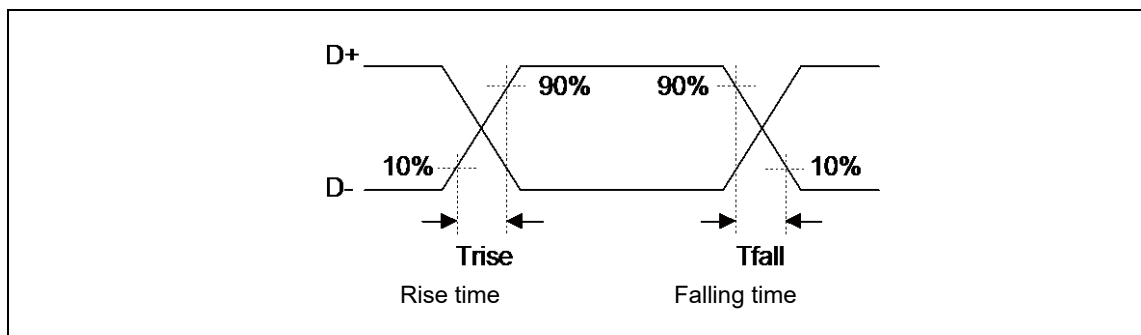


\*6: USB Full-speed connection is performed via twisted-pair cable shield with  $90 \Omega \pm 15\%$  characteristic impedance (differential mode).

USB standard defines that the output impedance of the USB driver must be in the range from  $28 \Omega$  to  $44 \Omega$ . So, a discrete series resistor ( $R_s$ ) addition is defined in order to satisfy the above definition and keep balance. When using this USB I/O, use it with  $25 \Omega$  to  $30 \Omega$  (recommended value  $27 \Omega$ ) series resistor  $R_s$ .



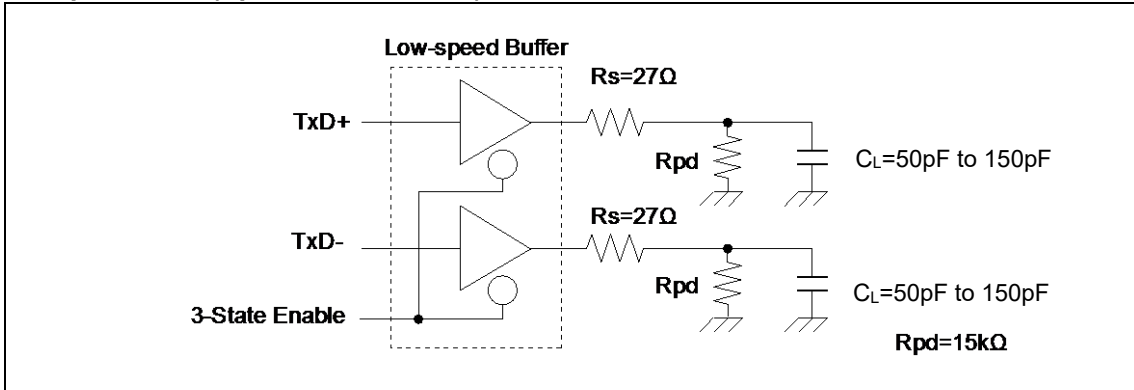
\*7: They indicate rise time ( $T_{rise}$ ) and fall time ( $T_{fall}$ ) of the low-speed differential data signal. They are defined by the time between 10% and 90% of the output signal voltage.



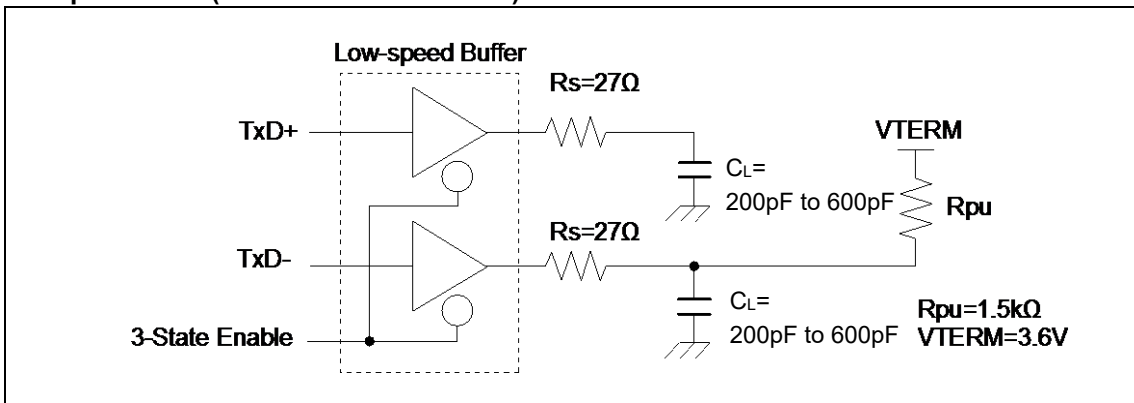
**Note:**

- See *Low-Speed Load (Compliance Load)* for conditions of external load.

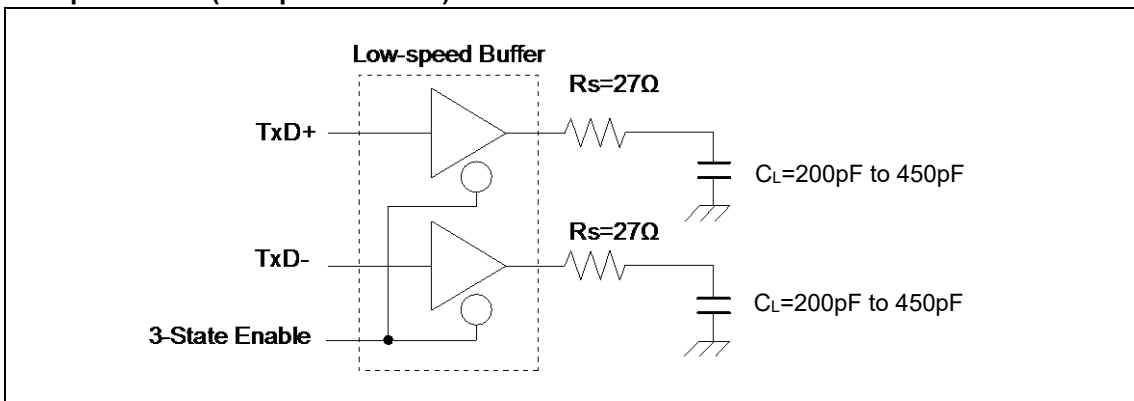
Low-Speed Load (Upstream Port Load) - Reference 1



Low-Speed Load (Downstream Port Load) - Reference 2



Low-Speed Load (Compliance Load)



## 12.8 Low-Voltage Detection Characteristics

### 12.8.1 Low-Voltage Detection Reset

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	-	2.46	2.55	2.64	V	When voltage drops
Released voltage	VDH	-	2.51	2.60	2.69	V	When voltage rises

### 12.8.2 Interrupt of Low-Voltage Detection

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	SVHI = 00111	2.80	2.90	3.00	V	When voltage drops
Released voltage	VDH		2.90	3.00	3.11	V	When voltage rises
Detected voltage	VDL	SVHI = 00100	2.99	3.10	3.21	V	When voltage drops
Released voltage	VDH		3.09	3.20	3.31	V	When voltage rises
Detected voltage	VDL	SVHI = 01100	3.18	3.30	3.42	V	When voltage drops
Released voltage	VDH		3.28	3.40	3.52	V	When voltage rises
Detected voltage	VDL	SVHI = 01111	3.67	3.80	3.93	V	When voltage drops
Released voltage	VDH		3.76	3.90	4.04	V	When voltage rises
Detected voltage	VDL	SVHI = 01110	3.76	3.90	4.04	V	When voltage drops
Released voltage	VDH		3.86	4.00	4.14	V	When voltage rises
Detected voltage	VDL	SVHI = 01001	4.05	4.20	4.35	V	When voltage drops
Released voltage	VDH		4.15	4.30	4.45	V	When voltage rises
Detected voltage	VDL	SVHI = 01000	4.15	4.30	4.45	V	When voltage drops
Released voltage	VDH		4.25	4.40	4.55	V	When voltage rises
Detected voltage	VDL	SVHI = 11000	4.25	4.40	4.55	V	When voltage drops
Released voltage	VDH		4.34	4.50	4.66	V	When voltage rises
LVD stabilization wait time	T <sub>LVDW</sub>	-	-	-	6000 × t <sub>CYCP</sub> *	μs	

\*: t<sub>CYCP</sub> indicates the APB2 bus clock cycle time.



**12.9 MainFlash Memory Write/Erase Characteristics**

 (V<sub>CC</sub> = 2.7 V to 5.5 V)

Parameter		Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	Large Sector	-	0.7	3.7	s	Includes write time prior to internal erase
	Small Sector	-	0.3	1.1	s	
Half word (16-bit) write time	Write cycles ≤ 100 times	-	12	100	μs	Not including system-level overhead time
	Write cycles > 100 times			200		
Chip erase time*		-	13.6	68	s	Includes write time prior to internal erase

\*: It indicates the chip erase time of 1 MB MainFlash memory

For devices with 1.5 MB or 2 MB of MainFlash memory, two erase cycles are required.

See 3.2.2 Command Operating Explanations and 3.3.3 Flash Erase Operation in this product's Flash Programming Manual for the detail.

**Write Cycles and Data Retention Time**

Erase/Write Cycles (Cycle)	Data Retention Time (Year)
1,000	20*
10,000	10*
100,000	5*

\*: This value comes from the technology qualification (using Arrhenius equation to translate high temperature acceleration test result into average temperature value at + 85°C).

**12.10 Dual Flash Memory Write/Erase Characteristics**

It is the same write/erase characteristics as the MainFlash memory.

See 3.6 Dual flash mode in this product's Flash Programming Manual for the detail of dual flash mode.

### 12.11 Standby Recovery Time

#### 12.11.1 Recovery cause: Interrupt/WKUP

The time from the interrupt occurring to the time of program operation start is shown.

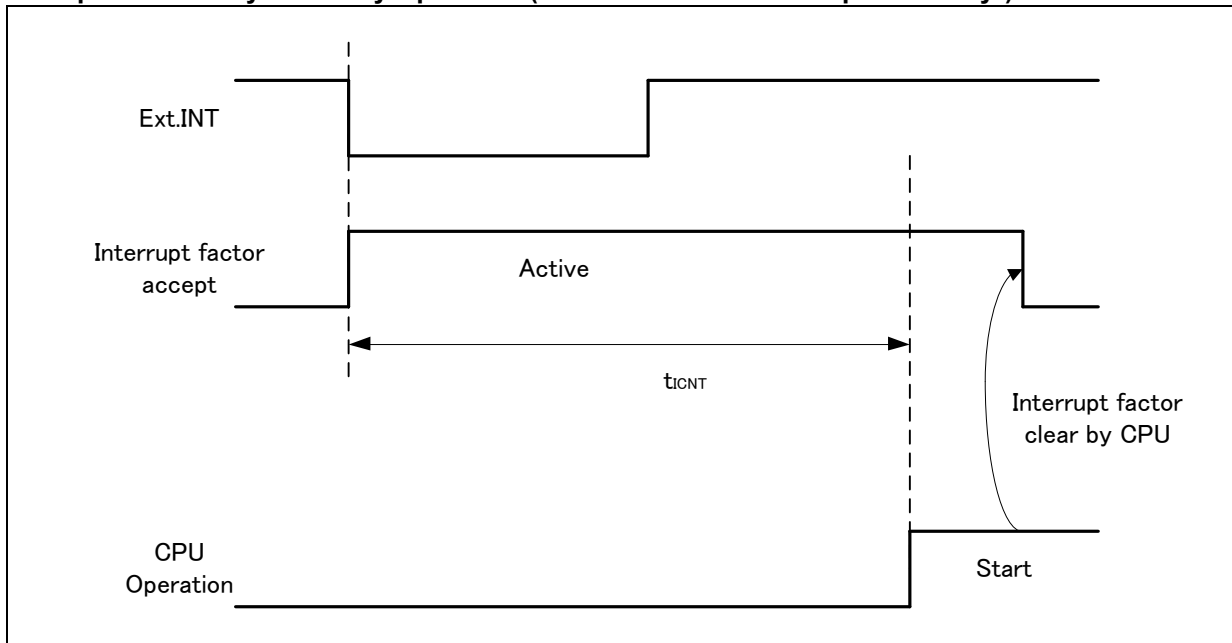
#### Recovery Count Time

(V<sub>CC</sub> = 2.7 V to 5.5 V, V<sub>SS</sub> = 0 V)

Parameter	Symbol	Value		Unit	Remarks
		Typ	Max*		
Sleep mode	t <sub>ICNT</sub>	HCLK×1		μs	
High-speed CR Timer mode Main Timer mode PLL Timer mode		40	80	μs	
Low-speed CR Timer mode		450	900	μs	
Sub Timer mode		896	1136	μs	
RTC mode Stop mode (High-speed CR/Main/PLL Run mode return)		316	581	μs	
RTC mode Stop mode (Low-speed CR/sub Run mode return)		270	540	μs	
Deep Standby RTC mode with RAM retention		365	667	μs	without RAM retention
Deep Standby Stop mode with RAM retention		365	667	μs	with RAM retention

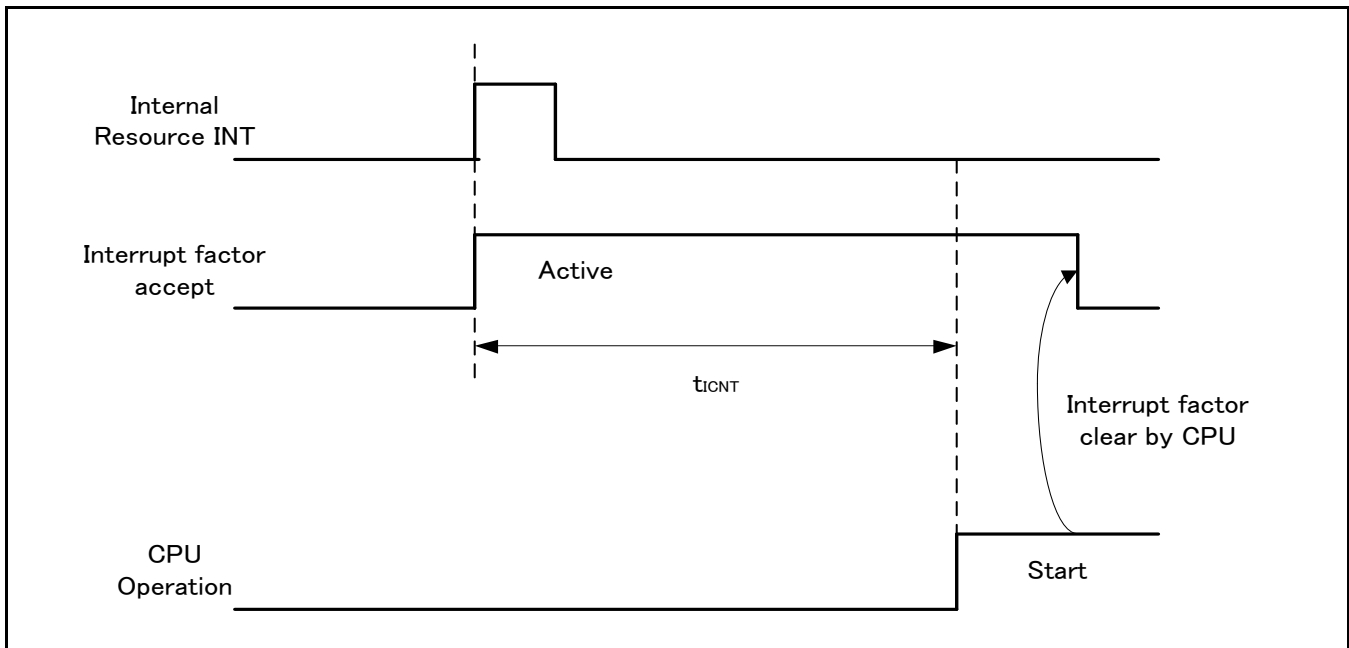
\*: The maximum value depends on the built-in CR accuracy.

#### Example of Standby Recovery Operation (when in External Interrupt Recovery\*)



\*: External interrupt is set to detecting fall edge.

**Example of Standby Recovery Operation (when in Internal Resource Interrupt Recovery\*)**



\*: Depending on the standby mode, interrupt from the internal resource is not included in the recovery cause.

**Notes:**

- The return factor is different in each low-power consumption mode. See Chapter 6: Low Power Consumption Mode and Operations of Standby Modes in FM4 Family Peripheral Manual Main Part (002-04856).
- The recovery process is unique for each operating mode. See Chapter 6: Low Power Consumption Mode in FM4 Family Peripheral Manual Main Part (002-04856).

**12.11.2 Recovery Cause: Reset**

The time from reset release to the program operation start is shown.

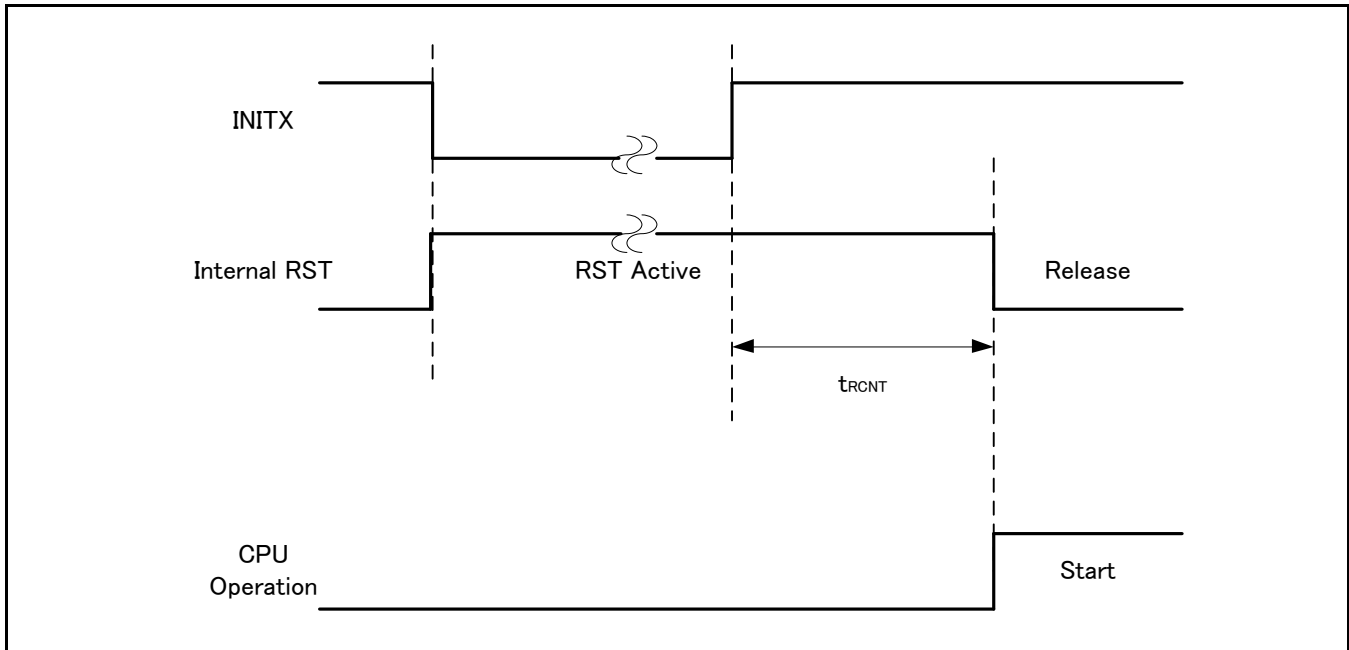
**Recovery Count Time**

(V<sub>CC</sub> = 2.7 V to 5.5 V, V<sub>SS</sub> = 0 V)

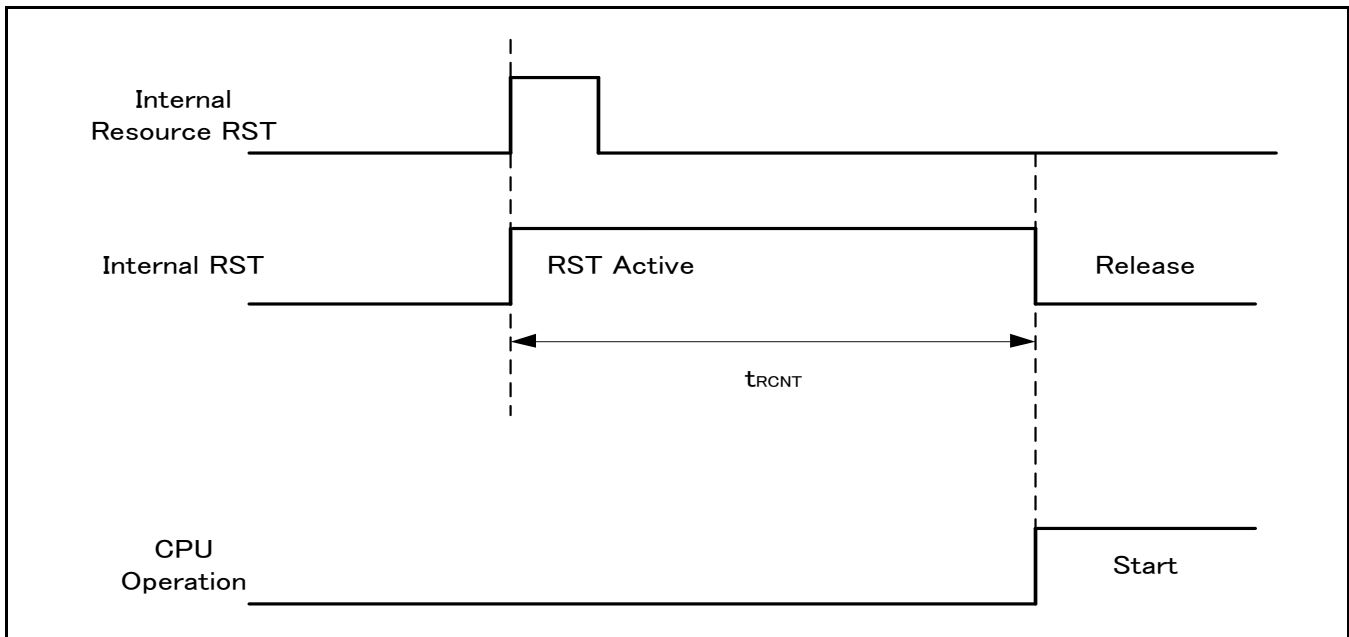
Parameter	Symbol	Value		Unit	Remarks
		Typ	Max*		
Sleep mode	t <sub>RCNT</sub>	155	266	μs	
High-speed CR Timer mode Main Timer mode PLL Timer mode		155	266	μs	
Low-speed CR Timer mode		315	567	μs	
Sub Timer mode		315	567	μs	
RTC mode Stop mode		315	567	μs	
Deep Standby RTC mode with RAM retention Deep Standby Stop mode with RAM retention		336	667	μs	without RAM retention
		336	667	μs	with RAM retention

\*: The maximum value depends on the built-in CR accuracy.

**Example of Standby Recovery Operation (when in INITX Recovery)**



Example of Standby Recovery Operation (when in Internal Resource Reset Recovery\*)



\*: Depending on the low-power consumption mode, the reset issue from the internal resource is not included in the recovery cause.

**Notes:**

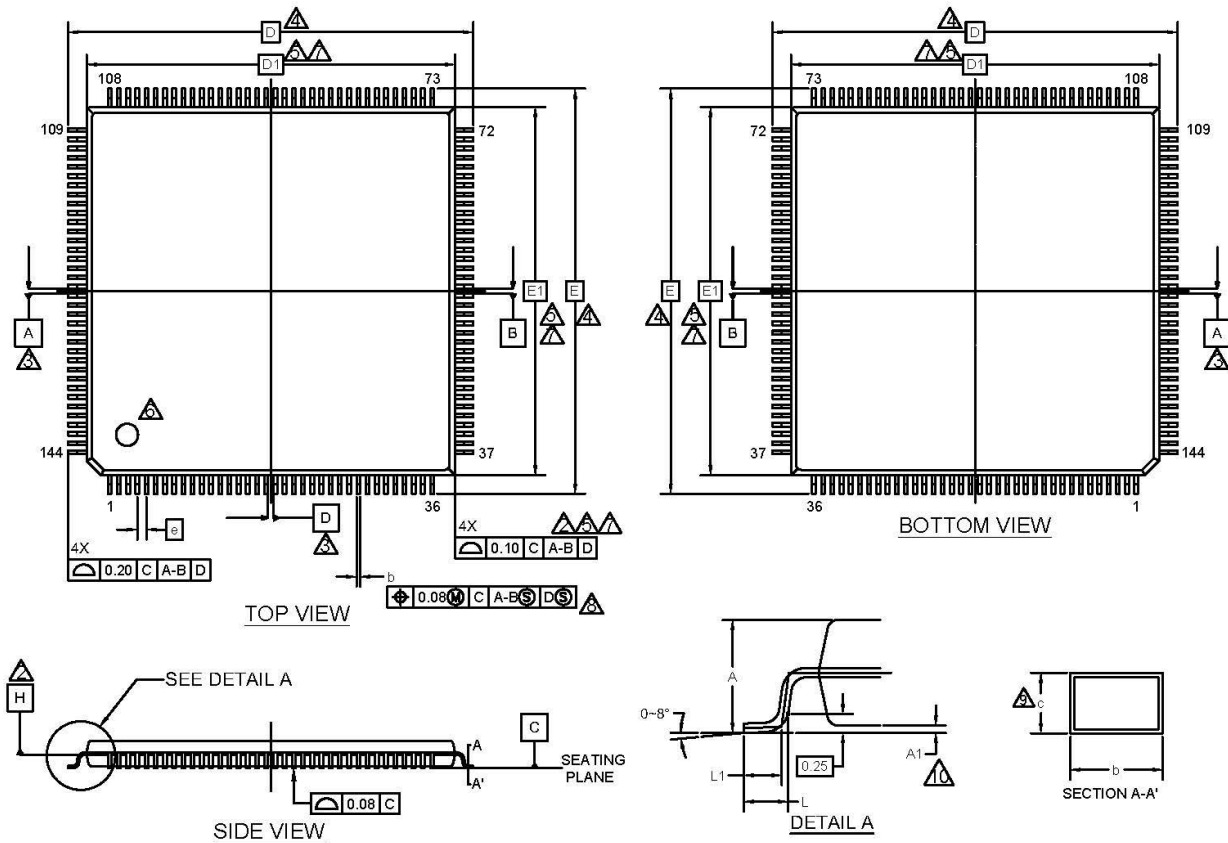
- The return factor is different in each low power consumption mode. See Chapter 6: Low Power Consumption Mode and Operations of Standby Modes in FM4 Family Peripheral Manual Main Part (002-04856).
- The recovery process is unique for each operating mode. See Chapter 6: Low Power Consumption Mode in FM4 Family Peripheral Manual Main Part (002-04856).
- When the power-on reset/low-voltage detection reset, they are not included in the return factor. See 12.4.8 Power-On Reset Timing.
- In recovering from reset, CPU changes to High-speed Run mode. In the case of using the main clock and PLL clock, they need further main clock oscillation stabilization wait time and oscillation stabilization wait time of Main PLL clock.
- Internal resource reset indicates Watchdog reset and CSV reset.

**13. Ordering Information**

Part number	Flash	RAM	Crypto	Package
S6E2C38H0AGV2000A	1 MB	128 KB	N/A	Plastic • LQFP (0.5-mm pitch), 144 pin (LQS144)
S6E2C39H0AGV2000A	1.5 MB	192 KB	N/A	
S6E2C3AH0AGV2000A	2 MB	256 KB	N/A	
S6E2C38J0AGV2000A	1 MB	128 KB	N/A	Plastic • LQFP (0.65-mm pitch), 176 pin (LQP176)
S6E2C39J0AGV2000A	1.5 MB	192 KB	N/A	
S6E2C3AJ0AGV2000A	2 MB	256 KB	N/A	
S6E2C38J0AGB1000A	1 MB	128 KB	N/A	Plastic • LQFP (0.8-mm pitch), 192 pin (LBE192)
S6E2C39J0AGB1000A	1.5 MB	192 KB	N/A	
S6E2C3AJ0AGB1000A	2 MB	256 KB	N/A	
S6E2C38L0AGL2000A	1 MB	128 KB	N/A	Plastic • LQFP (0.4-mm pitch), 216 pin (LQQ216)
S6E2C39L0AGL2000A	1.5 MB	192 KB	N/A	
S6E2C3AL0AGL2000A	2 MB	256 KB	N/A	

14. Package Diagrams

Package Type	Package Code
LQFP 144	LQS 144

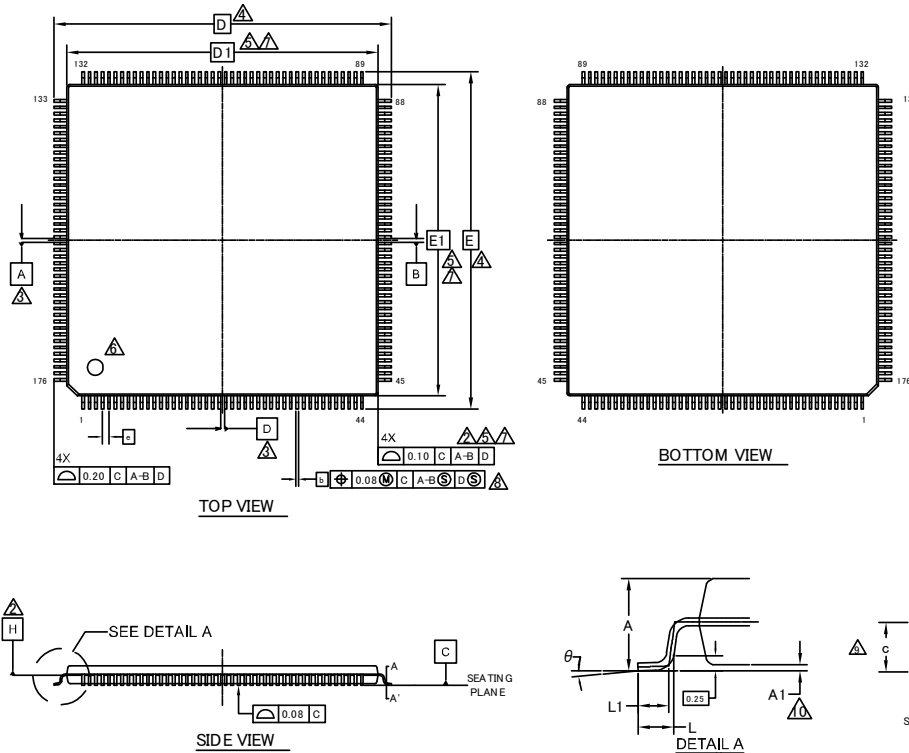


SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.05	—	0.15
b	0.17	0.22	0.27
c	0.09	—	0.20
D	22.00 BSC		
D1	20.00 BSC		
e	0.50 BSC		
E	22.00 BSC		
E1	20.00 BSC		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70

NOTES

- ALL DIMENSIONS ARE IN MILLIMETERS
- DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
- DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
- DATUMS C AND E TO BE DETERMINED AT SEATING PLANE C.
- DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE.
- DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
- DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
- REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
- DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
- THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
- A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

Package Type	Package Code
LQFP 176	LQP 176



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.05	—	0.15
b	0.17	0.22	0.27
c	0.09	—	0.20
D	26.00 BSC		
D1	24.00 BSC		
e	0.50 BSC		
E	26.00 BSC		
E1	24.00 BSC		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
$\theta$	0°	—	8°

**NOTES**

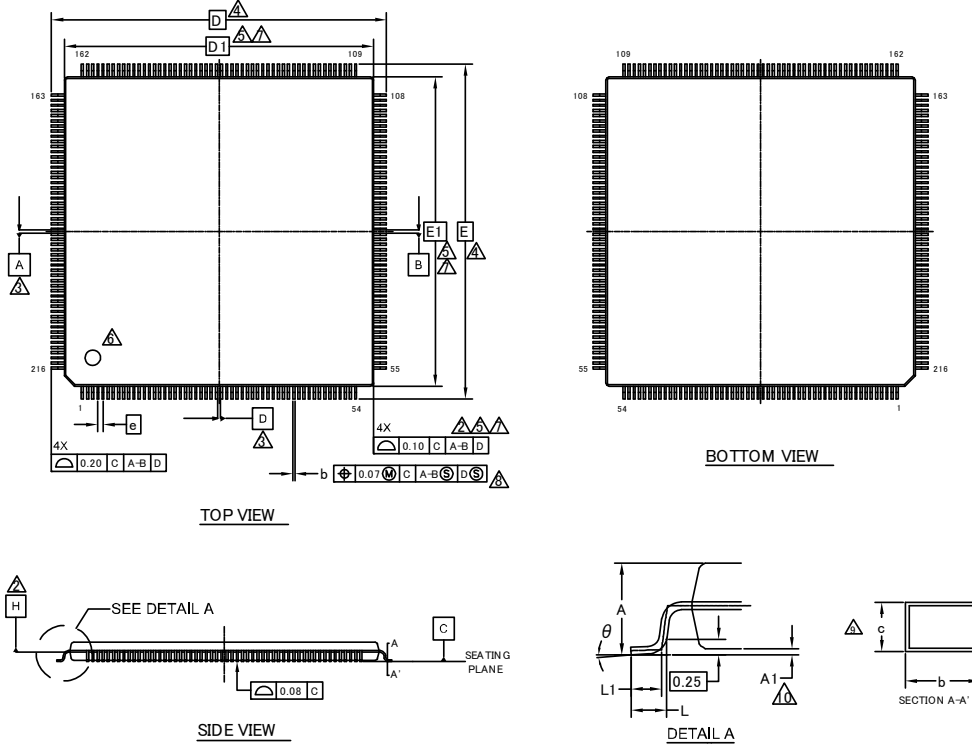
- ALL DIMENSIONS ARE IN MILLIMETERS.
  - DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
  - DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
  - TO BE DETERMINED AT SEATING PLANE C.
  - DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
  - DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
  - REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS, DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS, BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
  - DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBER PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
  - THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
  - A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-15150 \*\*

 PACKAGE OUTLINE, 176 LEAD LQFP  
 24.0X24.0X1.7 MM LQP176 REV\*\*



<b>Package Type</b>	<b>Package Code</b>
LQFP 216	LQQ 216



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.05	—	0.15
b	0.13	0.18	0.23
c	0.09	—	0.20
D	26.00 BSC.		
D1	24.00 BSC.		
e	0.40 BSC.		
E	26.00 BSC.		
E1	24.00 BSC.		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
$\theta$	0°	—	8°

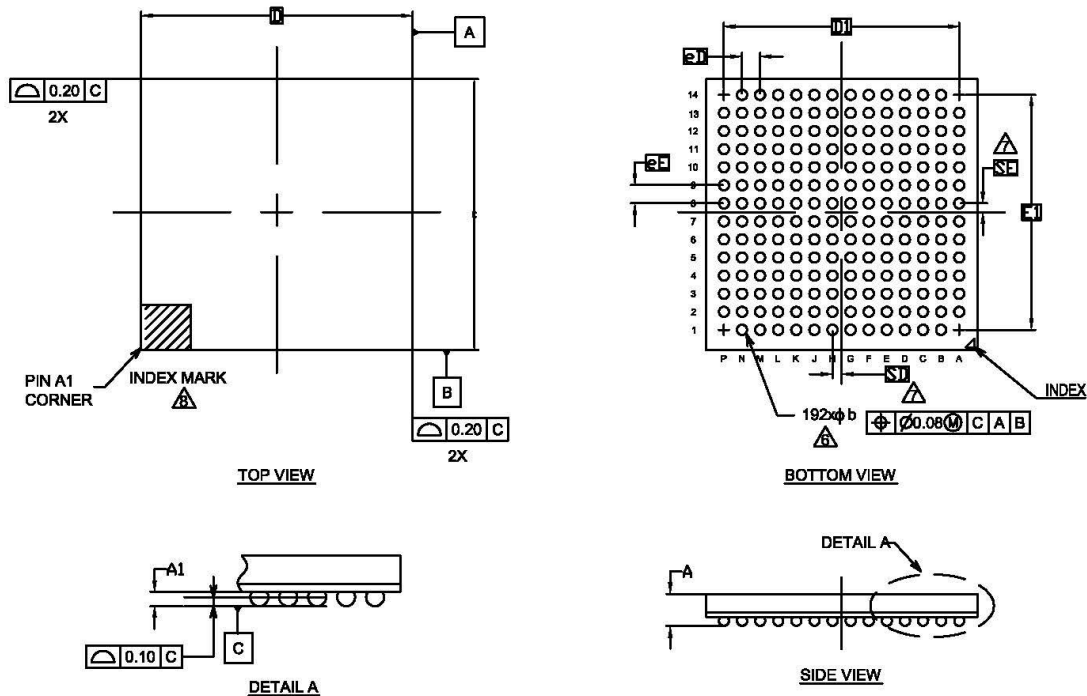
**NOTES**

- ALL DIMENSIONS ARE IN MILLIMETERS.
- DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
- DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
- DATUMS A-B AND D TO BE DETERMINED AT SEATING PLANE C.
- DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
- DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
- REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS, DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS, BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
- DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
- THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
- A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-15153 \*\*

 PACKAGE OUTLINE, 216 LEAD LQFP  
 24.0X24.0X1.7 MM LQQ216 REV\*\*

Package Type	Package Code
PFBGA 192	LBE 192



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.45
A1	0.25	0.35	0.45
D	12.00 BSC		
E	12.00 BSC		
D1	10.40 BSC		
E1	10.40 BSC		
MD	14		
ME	14		
n	192		
φb	0.35	0.45	0.55
eD	0.80 BSC		
eE	0.80 BSC		
SD/SE	0.40 BSC		

**NOTES**

- ALL DIMENSIONS ARE IN MILLIMETERS.
- DIMENSIONS AND TOLERANCES METHODS PER ASME Y14.5-2009. THIS OUTLINE CONFORMS TO JEP95, SECTION 4.5.
- BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-010.
- "e" REPRESENTS THE SOLDER BALL GRID PITCH.
- SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION. SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION. n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
- DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
- "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW. WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" OR "SE" = 0. WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
- A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK. METALLIZED MARK INDENTATION OR OTHER MEANS.
- "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.

002-13493 \*A

## 15. Major Changes

Spansion Publication Number: S6E2C3\_DS709-00012

Page	Section	Change Results
Revision 0.1		
-	-	Initial release
Revision 1.0		
11 13 87 88	2. Features 3. Product Lineup 10. Block Diagram 12. Memory Map	Deleted HDM-CEC/Remote Control Receiver.
16-18	5. Pin Assignments	Deleted the pins of HDM-CEC/Remote Control Receiver.(CEC0,CEC1) Revised the pin name of I2S. (MI2S*_0→MI2S*0_0) Deleted the pin of IGTRG0_0.
20-71	6. Pin Descriptions	Deleted the pins of HDM-CEC/Remote Control Receiver.(CEC0,CEC1) Revised the pin name of I2S. (MI2S*_0→MI2S*0_0) Revised the pin number of PF7 in LQFP216.(91→90) revised the pin number of X1. (73, 58, 50, P5→107, 87, 71, P13) Revised the pin number of X0A. (107, 87, 71, P13→73, 58, 50, P5)
72-79	7. I/O Circuit Type	Revised IOH/IOL of Type S.(IOH=-12mA→-10mA, IOL=12mA→10mA) Added the case of using I2C in Type E, F, G, L, N, S.
94-101	13. Pin Status In Each CPU State	Deleted X and Y in Pin Status Type.
102-103	14.1. Absolute Maximum Ratings	Added 10mA type.
104-107	14.2. Recommended Operating Conditions	Added AVRL in Analog reference voltage. Revised the leakage current in Maximum leakage current at operating
108-117	14.3.1. Current Rating	Revised the maximum current of each category.
118-119	14.3.2. Pin Characteristics	Added the characteristic of external bus in H level input voltage (hysteresis input). Added the characteristic of 10 mA type.
122	14.4.5. Operating Conditions of USB PLL · I2S PLL (in the case of using main clock for input clock of PLL)	Revised the maximum of I2S PLL macro oscillation clock frequency. (307.2 MHz→384 MHz)
186	14.5.12-bit A/D Converter	Revised the minimum of Sampling time. Revised the characteristic of State transition time to operation permission Added AVRL in Analog reference voltage.
194	14.8.2. Interrupt of Low-Voltage Detection	Revised the SVHI values in Conditions

**NOTE: Please see “Document History” about later revised information.**

## Document History

Document Title: S6E2C3 Series 32-bit ARM® Cortex®-M4F, FM4 Microcontroller

Document Number: 002-04988

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	-	AKIH	04/22/2015	New Spec.
*A	5126421	HITK	02/05/2016	Company name and layout design change. Added the note of TAP pin. Updated Package Code and Dimensions (LQFP-144, LQFP-176, LQFP-216).
*B	5634625	YSKA	02/20/2017	Deleted CAN in communications interfaces. (Page 1) Deleted CAN(RX0_2, TX0_2) in LQ216 pin assignments (Page 12) Deleted RX2_0 in P7D in "4. Pin Descriptions" (Page 20) Updated 12.4.8 Power-On Reset Timing. Changed parameter from "Power Supply rise time( $t_{VCCR}$ )[ms]" to "Power ramp rate(dV/dt)[mV/us]" and add some comments. (Page 113) Modified CSIO timing typo (12.4.12 CSIO(SPI) Timing) Deleted "SPI=1, MS=0" in the titles and added MS=0,1 in the schematic (Page 134-141, 150-157) Modified RTC description(Features, Real-Time Clock(RTC) ) Deleted "second , or day of the week" in the Interrupt function.(Page 3) Modifications related to the VBAT in the following chapter. "7. Handling Devices" Notes on Power-on (Page 76) "11. Pin Status in Each CPU State" List of VBAT Domain Pin Status (Page 90) "12.3.1 Current Rating" Table12-9. Typical and Maximum Current Consumption in Deep Standby STOP Mode, Deep Standby RTC Mode and VBAT (Page 105) Deleted MPNs below from "13. Ordering Information" (Page 190) S6E2C38H0AGV20000, S6E2C38J0AGB10000, S6E2C38J0AGV20000, S6E2C38L0AGL20000, S6E2C39H0AGV20000, S6E2C39J0AGB10000, S6E2C39J0AGV20000, S6E2C39L0AGL20000, S6E2C3AH0AGV20000, S6E2C3AJ0AGB10000, S6E2C3AJ0AGV20000, S6E2C3AL0AGL20000 Added MPNs below to "13. Ordering Information" (Page 190) S6E2C38H0AGV2000A, S6E2C38J0AGB1000A, S6E2C38J0AGV2000A, S6E2C38L0AGL2000A, S6E2C39H0AGV2000A, S6E2C39J0AGB1000A, S6E2C39J0AGV2000A, S6E2C39L0AGL2000A, S6E2C3AH0AGV2000A, S6E2C3AJ0AGB1000A, S6E2C3AJ0AGV2000A, S6E2C3AL0AGL2000A Deleted Baud rate spec for High-Speed Synchronous Serial in "12.4.12 CSIO(SPI) Timing"(Page 142-148) Modified the expression of the "Built-in CR" and add Note in the "1. Product Lineup"(Page 8) Modified typo(SCLKx_0 -> SCKx_0)(Page 126, 128, 130, 132) Change the name from "USB Function" to "USB Device" (Page 1, 8, 58) Added Maximum Access size in "Features"(Page 1) Updated IO circuit (type A) (Page 62)

*C	6095085	HUAL	03/12/2018	Updated Package Diagrams: Spec 002-13015 – Changed revision from ** to *A. Spec 002-13493 – Changed revision from ** to *A. Updated to new template. Completing Sunset Review.
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