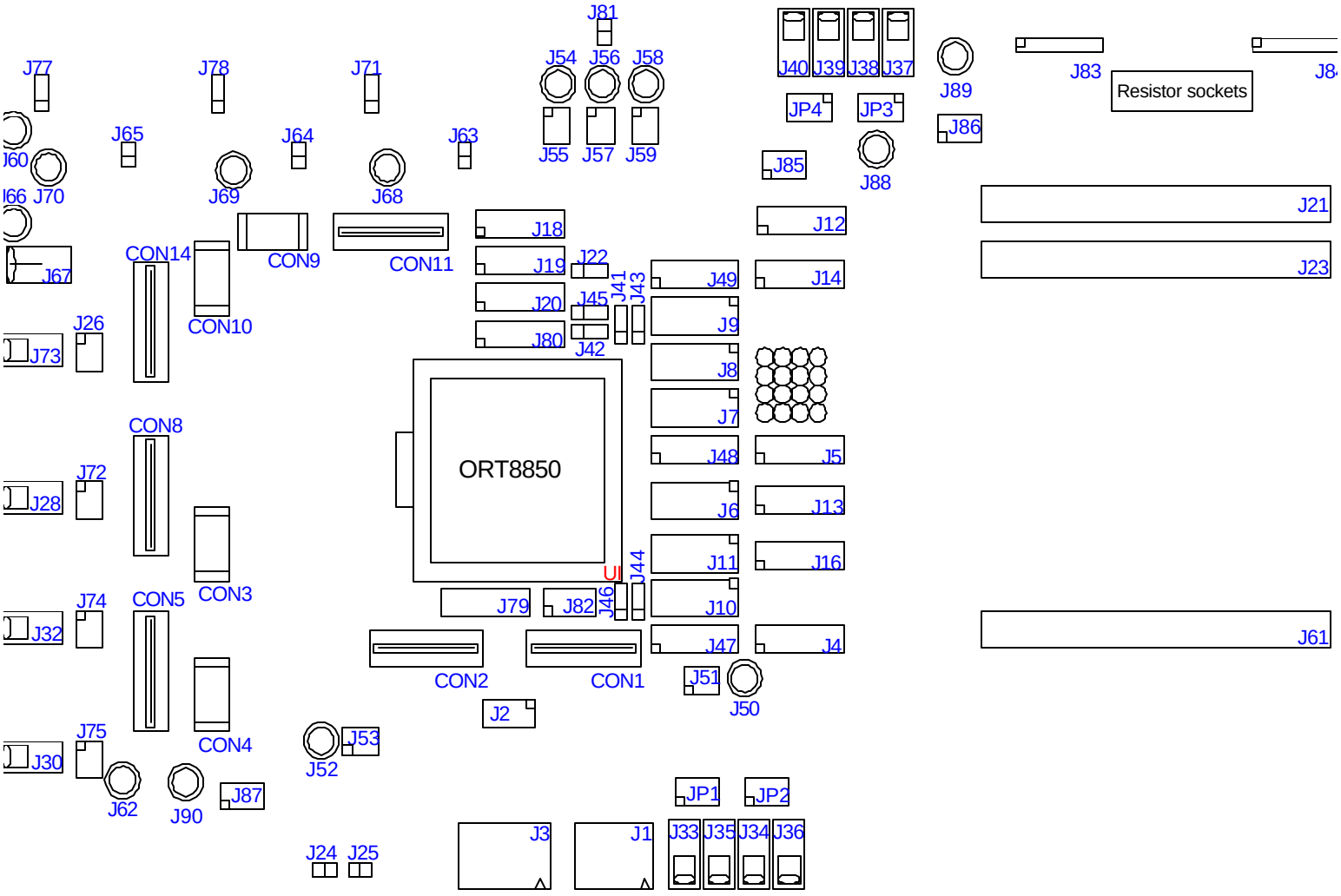
ORT8850
Evaluation Board
User Manual



Rough layout of ORT8850 board.

Pin outs and references of the connectors on the ORT8850 board (rev 1.5).

J1

Schematic page 2

A 7-pin serial connector used for configuration. An arrow, as well as the company's logo indicates pin one.

Serial Connector	
Pin 1	Vdd
Pin 2	cclk
Pin 3	D0
Pin 4	Done
Pin 5	Prog
Pin 6	nc
Pin 7	GND

J2

Schematic page 2

Ten-pin header used with an adapter to program the device via a parallel cable. **J2** is numbered as a standard header. Looking at it from above, pin one would be the top left pin. Pin two is to the right of pin one. Pin three is under pin one. Pin four is to the right of pin three, etc. This is what I consider a *standard* pin-out for a header, and I will refer back to this again.

JTAG Parallel Adapter	
Pin 1	Vdd
Pin 2	Done
Pin 3	Prgrm_n
Pin 4	TDI
Pin 5	Reset_n
Pin 6	TMS
Pin 7	Init_n
Pin 8	TCK
Pin 9	GND
Pin 10	Rd_Data_Tdo

J3

Schematic page 2

J3 is an 8-pin JTAG connector. It is physically similar to **J1**; an arrow indicates pin 1.

JTAG Connector	
Pin 1	Vdd
Pin 2	TDI
Pin 3	TMS
Pin 4	TCK
Pin 5	TDO
Pin 6	Rd_Cfg_n
Pin 7	Init_n
Pin 8	GND

Header Connections

Standard 0.100 headers are provided for interconnecting points on the board. This can be accomplished with 0.100 IDC connectors and ribbon cable for bus connections or 0.025 pin socket patch cords(such as Pomona Electronics #5948 www.pomonelectronics.com)

J4

Schematic page 2

This is a *standard* header. Pin one is at the top left. Pin numbers increment from left to right. The pins on this header correspond to dip switches. One column of the header (pins 1,3,5,7…) connect to **SW3**, with: J4.1 connecting to SW3.1, J4.3 connecting to SW3.2, J4.5 connecting to SW3.3, etc. The other column of the header (pins 2,4,6,8…) connect to **SW2**, with: J4.2 connecting to SW2.8, J4.4 connecting to SW2.7, J4.6 connecting to SW2.6, etc.
J4 is in line with **J16**. They can be connected via a ribbon cable or individual 0.025 Pin Socket patch cords to provide input for the ORT8850.

J4			
Pin 1	SW3.1	Pin 2	SW2.8
Pin 3	SW3.2	Pin 4	SW2.7
Pin 5	SW3.3	Pin 6	SW2.6
Pin 7	SW3.4	Pin 8	SW2.5
Pin 9	SW3.5	Pin 10	SW2.4
Pin 11	SW3.6	Pin 12	SW2.3
Pin 13	SW3.7	Pin 14	SW2.2
Pin 15	SW3.8	Pin 16	SW2.1
Pin 17	NC	Pin 18	NC
Pin 19	NC	Pin 20	NC

J5

Schematic page 4

This is a standard header as described above. This header connects to LEDs. When a jumper cable is used, output from the ORT8850 can drive these LEDs to display a pattern. The connections are:

J5	
Pin 1	red LED
Pin 3	red LED
Pin 5	red LED
Pin 7	red LED
Pin 9	yellow LED
Pin 11	yellow LED
Pin 13	yellow LED
Pin 15	yellow LED
Pin 2	green LED
Pin 4	green LED
Pin 6	green LED
Pin 8	green LED
Pin 10	red LED
Pin 12	red LED
Pin 14	red LED
Pin 16	red LED
Pin 17-20	N.C.

J5 is positioned in line with **J13**. They can be connected with a ribbon cable to provide a visual output for the ORT8850.

J6-J11

Schematic pages 5 and 6

These are 3 by 10 headers that provide differential output from the ORT8850. The first column (pins 1, 4, 7, 10, etc.) connect to the true side of the pair. Ground is connected to the middle column (pins 2, 5, 8, 11, etc.). And, the third column (pins 3, 6, 9, 12, etc.) are connected to the complement side of the pair.

J6					
Pin 1	3.3V	Pin 2	GND	Pin 3	3.3V
Pin 4	PL7C	Pin 5	GND	Pin 6	PL7D
Pin 7	PL11C	Pin 8	GND	Pin 9	PL11D
Pin 10	PL15C	Pin 11	GND	Pin 12	PL15D
Pin 13	PL17C	Pin 14	GND	Pin 15	PL17D
Pin 16	PL20C	Pin 17	GND	Pin 18	PL20D
Pin 19	PL22C	Pin 20	GND	Pin 21	PL22D
Pin 22	PL22A	Pin 23	GND	Pin 24	PL22B
Pin 25	PL23A	Pin 26	GND	Pin 27	PL23B
Pin 28	2.5V	Pin 29	GND	Pin 30	2.5V

J7					
Pin 1	3.3V	Pin 2	GND	Pin 3	3.3V
Pin 4	PL24A	Pin 5	GND	Pin 6	PL24B
Pin 7	PL25A	Pin 8	GND	Pin 9	PL25B
Pin 10	PL27C	Pin 11	GND	Pin 12	PL27D
Pin 13	PL33C	Pin 14	GND	Pin 15	PL33D
Pin 16	PL41C	Pin 17	GND	Pin 18	PL41D
Pin 19	PL43C	Pin 20	GND	Pin 21	PL43D
Pin 22	PL47A	Pin 23	GND	Pin 24	PL47B
Pin 25	3.3V	Pin 26	GND	Pin 27	3.3V
Pin 28	2.5V	Pin 29	GND	Pin 30	2.5V

J8					
Pin 1	3.3V	Pin 2	GND	Pin 3	3.3V
Pin 4	PB3C	Pin 5	GND	Pin 6	PB3D
Pin 7	PB5C	Pin 8	GND	Pin 9	PB5D
Pin 10	PB7C	Pin 11	GND	Pin 12	PB7D
Pin 13	PB13A	Pin 14	GND	Pin 15	PB13B
Pin 16	PB14A	Pin 17	GND	Pin 18	PB14B
Pin 19	PB15C	Pin 20	GND	Pin 21	PB15D
Pin 22	PB17C	Pin 23	GND	Pin 24	PB17D
Pin 25	PB21C	Pin 26	GND	Pin 27	PB21D
Pin 28	PB23A	Pin 29	GND	Pin 30	PB23B

J9					
Pin 1	3.3V	Pin 2	GND	Pin 3	3.3V
Pin 4	PB24A	Pin 5	GND	Pin 6	PB24B
Pin 7	PB25C	Pin 8	GND	Pin 9	PB25D
Pin 10	PB27C	Pin 11	GND	Pin 12	PB27D
Pin 13	PB29C	Pin 14	GND	Pin 15	PB29D
Pin 16	PB31C	Pin 17	GND	Pin 18	PB31D
Pin 19	PB33C	Pin 20	GND	Pin 21	PB33D
Pin 22	PB34C	Pin 23	GND	Pin 24	PB34D
Pin 25	PB36C	Pin 26	GND	Pin 27	PB36D
Pin 28	2.5V	Pin 29	GND	Pin 30	2.5V

J10					
Pin 1	3.3V	Pin 2	GND	Pin 3	3.3V
Pin 4	PT35C	Pin 5	GND	Pin 6	PT35D
Pin 7	PT35A	Pin 8	GND	Pin 9	PT35B
Pin 10	PT33C	Pin 11	GND	Pin 12	PT33D
Pin 13	PT31C	Pin 14	GND	Pin 15	PT31D
Pin 16	PT30C	Pin 17	GND	Pin 18	PT30D
Pin 19	PT28C	Pin 20	GND	Pin 21	PT28D
Pin 22	PT27C	Pin 23	GND	Pin 24	PT27D
Pin 25	PT26C	Pin 26	GND	Pin 27	PT26D
Pin 28	2.5V	Pin 29	GND	Pin 30	2.5V

J11					
Pin 1	3.3V	Pin 2	GND	Pin 3	3.3V
Pin 4	PT25C	Pin 5	GND	Pin 6	PT25D
Pin 7	PT24A	Pin 8	GND	Pin 9	PT24B
Pin 10	PT23A	Pin 11	GND	Pin 12	PT23B
Pin 13	PT20C	Pin 14	GND	Pin 15	PT20D
Pin 16	PT12C	Pin 17	GND	Pin 18	PT12D
Pin 19	PT4A	Pin 20	GND	Pin 21	PT4B
Pin 22	PT3A	Pin 23	GND	Pin 24	PT3B
Pin 25	PT2A	Pin 26	GND	Pin 27	PT2B
Pin 28	2.5V	Pin 29	GND	Pin 30	2.5V

J12

Schematic page 3

J12 is a standard header used for test. This 2X10 header outputs bits 0 to 19 of the 860's address bus. This can be used along with **J14** to debug the 860 interface.

J13

Schematic page 7

This is a standard header that is physically located next to **J5**. By using a ribbon cable as a jumper, one can use the output signals on **J13** to control the LEDs through **J5**. Only the first 16 pins are used for this purpose. The header can also be used as basic input/output.

J13			
Pin 1	PL3D	Pin 2	PL31D
Pin 3	PL5D	Pin 4	PL35A
Pin 5	PL8D	Pin 6	PL37A
Pin 7	PL11A	Pin 8	PL38A
Pin 9	PL13A	Pin 10	PL40D
Pin 11	PL20A	Pin 12	PL44B
Pin 13	PL21A	Pin 14	PL45D
Pin 15	PL27A	Pin 16	PL45A
Pin 17	PL28A	Pin 18	PL46D
Pin 19	PL29A	Pin 20	PL46A

J14

Schematic page 3

This is a 2X10 standard header used for test. It is similar to **J12**. The header outputs bits 20 through 31 of the 860's address bus. Bit 20 corresponds to pin 1, 21 corresponds to pin 2, and 22 corresponds to pin 3, all the way up to bit 31 and pin 12. Pins 13 to 20 are not used.

J16

Schematic page 7

This is a standard header physically located next to **J4**. By connecting the two headers with a ribbon cable, one can use the jumpers to input signals to the ORT8850. Only the first 16 pins are used for this purpose. The header can also be used as basic input/output.

J16			
Pin 1	PT34C	Pin 2	PT20A
Pin 3	PT32D	Pin 4	PT19D
Pin 5	PT29D	Pin 6	PT19A
Pin 7	PT29A	Pin 8	PT17D
Pin 9	PT28A	Pin 10	PT12A
Pin 11	PT27A	Pin 12	PT11C
Pin 13	PT24D	Pin 14	PT11A
Pin 15	PT22A	Pin 16	PT7C
Pin 17	PT21C	Pin 18	PT5D
Pin 19	PT21A	Pin 20	PT3D

J18-J20

Schematic page 8

These are extra I/O headers. They are 2X10 headers with standard numbering. One side of the header (pins 1, 3, 5, 7, etc.) has signals, and the other side (pins 2, 4, 6, 8, etc.) has grounds. **J18** has all ten of the signal pins connected. **J19** has six signals pins connected. And, **J20** has five signal pins connected.

J18			
Pin 1	PB2B	Pin 2	GND
Pin 3	PB3A	Pin 4	GND
Pin 5	PB9A	Pin 6	GND
Pin 7	PB10A	Pin 8	GND
Pin 9	PB11A	Pin 10	GND
Pin 11	PB12A	Pin 12	GND
Pin 13	PB19A	Pin 14	GND
Pin 15	PB20A	Pin 16	GND
Pin 17	PB21A	Pin 18	GND
Pin 19	PB22A	Pin 20	GND

J19			
Pin 1	PB22D	Pin 2	GND
Pin 3	PB24D	Pin 4	GND
Pin 5	PB26C	Pin 6	GND
Pin 7	PB27A	Pin 8	GND
Pin 9	PB28A	Pin 10	GND
Pin 11	PB29A	Pin 12	GND
Pin 13	NC	Pin 14	GND
Pin 15	NC	Pin 16	GND
Pin 17	NC	Pin 18	GND
Pin 19	NC	Pin 20	GND

J20			
Pin 1	PB30A	Pin 2	GND
Pin 3	PB30C	Pin 4	GND
Pin 5	PB32C	Pin 6	GND
Pin 7	PB35A	Pin 8	GND
Pin 9	PB35C	Pin 10	GND
Pin 11	NC	Pin 12	GND
Pin 13	NC	Pin 14	GND
Pin 15	NC	Pin 16	GND
Pin 17	NC	Pin 18	GND
Pin 19	NC	Pin 20	GND

J21

Schematic page 15

This header fits with the 860 bus to communicate to a Windriver (www.windriver.com)MPC860 development board.
h

J22

Schematic page 15

This jumper selects the data 0 bit between the 860 bus communications and the 7-pin serial connector (**J1**). Jumping pins 1 and 2 selects the serial communication. Jumping pins 2 and 3 selects the 860 bus.

J23

Schematic page 16

This header is designed fit the 860 bus to communicate with the Windriver(EST) MPC860 development board.

J24, J25

Schematic page 16

These headers are the chip select controls. The default is selected when no jumpers are present.

J26

Schematic page 17

This is the system clock jumper. The pins are numbered from left to right. Placing a jumper across pins 1 and 2 selects oscillator Y1 as input clock (sys_clk). Placing a jumper across pins 3 and 4 selects the SMA connector **J73** as the input clock. Placing a jumper across pins 5 and 6 selects the oscillator Y2 as the input clock. This oscillator has feedback from pin AP27 to serve as a VXCO.

J28

Schematic page 17

This is a SMA connector that inputs to **J72**. If selected with a jumper, it could serve as the g_clk input.

J30, J32

Schematic page 18

This SMA connector outputs the clock signal fro m Y3 or Y4 based on jumper placement in header **J75**.

J33-J40

Schematic page 19

These SMA connectors provide differential input to the PLL clocks. The pairs are:

J33	-	PLL_CLK1C
J35	-	PLL_CLK1T
J34	-	PLL_CLK0C
J36	-	PLL_CLK0T
J37	-	PLL_CLK7C
J38	-	PLL_CLK7T
J39	-	PLL_CLK6C
J40	-	PLL_CLK6T

J41-J46

Schematic page 20

These are three pin headers for the differential clock input. Pin one is complement, pin two is ground, and pin three is true.

J47-J49

Schematic page 22

These are 2X10 reference voltage headers. The extra pins are unconnected.

J50, J52, J54, J56, J58

Schematic page 23

These banana jacks may be selected through jumpers **J51**, **J53**, **J55**, **J57**, and **J59**, respectively, as input for the VddI/O.

J51, J53, J55, J57, J59

Schematic page 23

These jumpers select the input for the VddI/O voltage. See the schematic for a drawing of the jumper connections.

J60, J62

Schematic page 24

These banana jacks are connected to the ground plane of the board.

J61

Schematic page 24

This 96 pin header is used to provide support for the physical connection to the Power PC daughter card.

J63-J65

Schematic page 24

Three two-pin headers are provided to bring out 3.3V (**J63**), 2.5V (**J64**) and 1.5V (**J65**) with a ground pin.

J66

Schematic page 24

This banana jack connects to 5V.

J67

Schematic page 24

This power jack takes 5V from the wall adapter.

J68-J70

Schematic page 25

These banana jacks may be selected to provide power to the board through jumpers **J71**, **J77** and **J78**.

J71, J77, J78

Schematic page 25

These jumpers select if the board is powered from the regulators or from the banana jacks. **J71** selects the source for 3.3V. **J78** selects the 2.5V source, and **J77** selects the 1.5V source.

J72

Schematic page 17

This is the g clock jumper. Placing a jumper across pins 1 and 2 selects oscillator Y1 as g clock (g_clk). Placing a jumper across pins 3 and 4 selects the SMA connector **J28** as the g clock. Placing a jumper across pins 5 and 6 selects the oscillator Y2 as the input clock. This oscillator has feedback from pin AP27 to serve as a VXCO. Note the two on-board oscillators are shared with the system clock (**J26**).

J73

Schematic page 17

This SMA connector may be selected to provide input to the system clock.

J74

Schematic page 18

This jumper selects between a built in 15 MHz oscillator and an oscillator socket. Adding a jumper to pins 1 and 3 selects the socket. Pins 3 and 5 select the 15 MHz oscillator. The connector has a column of ground pins (pins 2, 4, and 6) so that the clock can be sent from the header via a twisted pair.

J75

Schematic page 18

This jumper selects between a built in 66 MHz oscillator and an oscillator socket. Adding a jumper to pins 1 and 3 selects the socket. Pins 3 and 5 select the 66 MHz oscillator. The connector has a column of ground pins (pins 2, 4, and 6) so that the clock can be sent from the header via a twisted pair.

J79

Schematic page 3

This header brings out the dedicated test pins from the ORT8850. These include TSTMUX0S to TSTMUX9S as well as the SCAN_TSTMD, SCANEN and RST_N. The RST_N is pulled up via **R169**. It can be pulled down by **R171,** which is not populated by default. The extra pins (pins 14 to 20) are connected to ground.

J79	
Pin 1	TSTMUX0S
Pin 2	TSTMUX1S
Pin 3	TSTMUX2S
Pin 4	TSTMUX3S
Pin 5	TSTMUX4S
Pin 6	TSTMUX5S
Pin 7	TSTMUX6S
Pin 8	TSTMUX7S
Pin 9	TSTMUX8S
Pin 10	TSTMUX9S
Pin 11	SCAN_TSTMD
Pin 12	SCANEN
Pin 13	RST_N
Pin 14	GND
Pin 15	GND
Pin 16	GND
Pin 17	GND
Pin 18	GND
Pin 19	GND
Pin 20	GND

J80

Schematic page 3

This header brings out additional dedicated test pins from the ORT8850. Extra pins (pins 10 to 20) are connected to ground.

J80	
Pin 1	DAUTREC
Pin 2	TSTCLK
Pin 3	TESTRST
Pin 4	TSTSHFTLD
Pin 5	RESETTX
Pin 6	ETOGGLE
Pin 7	ECSEL
Pin 8	EXDNUP
Pin 9	MRESET
Pin 10	GND
Pin 11	GND
Pin 12	GND
Pin 13	GND
Pin 14	GND
Pin 15	GND
Pin 16	GND
Pin 17	GND
Pin 18	GND
Pin 19	GND
Pin 20	GND

J81

Schematic page 3

This two-pin header is used to output the PTEMP signal from the ORT8850. Pin 2 is connected to ground.

J82

Schematic page 2

J82 is a ten-pin header for additional dedicated signals from the ORT8850. One column of the header (pins 1, 3, 5, etc) is connected to ground.

J82			
Pin 1	GND	Pin 2	HDC
Pin 3	GND	Pin 4	LDC_N
Pin 5	GND	Pin 6	DOUT
Pin 7	GND	Pin 8	RDY_BUSY_N_RCLK
Pin 9	GND	Pin 10	LVDS_R

J83, J84

Schematic page 26

These two 1 X 8 headers connect to the resistor sockets. The table shows the pin connections to the specific sockets.

J83	J84	Resistor
Pin 1	Pin 1	R181
Pin 2	Pin 2	R182
Pin 3	Pin 3	R183
Pin 4	Pin 4	R184
Pin 5	Pin 5	R185
Pin 6	Pin 6	R186
Pin 7	Pin 7	R187
Pin 8	Pin 8	R188

J85-J87

Schematic page 26

These headers are connected to banana jacks **J88**, **J89**, and **J90**.

J88-J90

Schematic page 26

These banana jacks are connected to headers **J85**, **J86**, and **J87**.

JP1-JP4

Schematic page 19

JP1 to **JP4** are eight-pin headers (2X4) that control the termination of **J33** to **J40**.

CON 1

Schematic page 9

This Amp Micro-strip connector has 47 pins. Check the datasheet from www.amp.com (part number 536255-1) for pin number information.

CON 1	
Pin 1	GND
Pin 2	GND
Pin 3	GND
Pin 4	GND
Pin 5	GND
Pin 6	GND
Pin 7	TXSOC_A_N
Pin 8	TXCLK_A_N
Pin 9	TXSOC_A_P
Pin 10	TXCLK_A_P
Pin 11	GND
Pin 12	GND
Pin 13	TXD_A0_N
Pin 14	TXD_A1_N
Pin 15	TXD_A0_P
Pin 16	TXD_A1_P
Pin 17	GND
Pin 18	GND
Pin 19	TXD_A2_N
Pin 20	TXD_A3_N
Pin 21	TXD_A2_P
Pin 22	TXD_A3_P
Pin 23	GND
Pin 24	GND
Pin 25	TXD_A4_N
Pin 26	TXD_A5_N
Pin 27	TXD_A4_P
Pin 28	TXD_A5_P
Pin 29	GND
Pin 30	GND
Pin 31	TXD_A6_N
Pin 32	TXD_A7_N
Pin 33	TXD_A6_P
Pin 34	TXD_A7_P
Pin 35	GND
Pin 36	GND
Pin 37	GND
Pin 38	GND
Pin 39	GND
Pin 40	GND

CON 2

Schematic page 10

Amp Micro-strip connector.

CON2	
Pin 1	GND
Pin 2	GND
Pin 3	GND
Pin 4	GND
Pin 5	GND
Pin 6	GND
Pin 7	RXSOC_A_N
Pin 8	RXCLK_A_N
Pin 9	RXSOC_A_P
Pin 10	RXCLK_A_P
Pin 11	GND
Pin 12	GND
Pin 13	RXD_A0_N
Pin 14	RXD_A1_N
Pin 15	RXD_A0_P
Pin 16	RXD_A1_P
Pin 17	GND
Pin 18	GND
Pin 19	RXD_A2_N
Pin 20	RXD_A3_N
Pin 21	RXD_A2_P
Pin 22	RXD_A3_P
Pin 23	GND
Pin 24	GND
Pin 25	RXD_A4_N
Pin 26	RXD_A5_N
Pin 27	RXD_A4_P
Pin 28	RXD_A5_P
Pin 29	GND
Pin 30	GND
Pin 31	RXD_A6_N
Pin 32	RXD_A7_N
Pin 33	RXD_A6_P
Pin 34	RXD_A7_P
Pin 35	GND
Pin 36	GND
Pin 37	GND
Pin 38	GND
Pin 39	GND
Pin 40	GND

CON 3, CON 4

Schematic pages 11 and 12

This connector type is an Amp Z-Pack 2mm header. A and B pins are connected to the receive pins of the ORT8850 and D and E pins are connected to the transmit pins of the ORT8850. A cable similar to one from W.L Gore (http://www.wlgore.com/) P/N 2MMA3143-01 adapts the 2mm Z-Pack to individual SMA connectors and is useful to observe the LVDS channels or connect to other test devices.

CON3									
Pin A1	RXD_B0_P	Pin B1	RXD_B0_N	Pin C1	GND	Pin D1	TXD_B0_N	Pin E1	TXD_B0_P
Pin A2	RXD_B1_P	Pin B2	RXD_B1_N	Pin C2	GND	Pin D2	TXD_B1_N	Pin E2	TXD_B1_P
Pin A3	RXD_B2_P	Pin B3	RXD_B2_N	Pin C3	GND	Pin D3	TXD_B2_N	Pin E3	TXD_B2_P
Pin A4	RXD_B3_P	Pin B4	RXD_B3_N	Pin C4	GND	Pin D4	TXD_B3_N	Pin E4	TXD_B3_P

CON4									
Pin A1	RXD_B4_P	Pin B1	RXD_B4_N	Pin C1	GND	Pin D1	TXD_B4_N	Pin E1	TXD_B4_P
Pin A2	RXD_B5_P	Pin B2	RXD_B5_N	Pin C2	GND	Pin D2	TXD_B5_N	Pin E2	TXD_B5_P
Pin A3	RXD_B6_P	Pin B3	RXD_B6_N	Pin C3	GND	Pin D3	TXD_B6_N	Pin E3	TXD_B6_P
Pin A4	RXD_B7_P	Pin B4	RXD_B7_N	Pin C4	GND	Pin D4	TXD_B7_N	Pin E4	TXD_B7_P

CON 5

Schematic page 11

This Amp Micro-strip connector is connected to the transit pins of the ORT8850. Transmit signals can be sent to this connector, or **CON 3** and **CON 4** by selecting via DIP switches (**SW6** to **SW9** and **SW22** to **SW25**).

CON5	
Pin 1	GND
Pin 2	GND
Pin 3	GND
Pin 4	GND
Pin 5	GND
Pin 6	GND
Pin 7	TXSOC_B_N
Pin 8	TXCLK_B_N
Pin 9	TXSOC_B_P
Pin 10	TXCLK_B_P
Pin 11	GND
Pin 12	GND
Pin 13	TXD_B0_P
Pin 14	TXD_B1_P
Pin 15	TXD_B0_N
Pin 16	TXD_B1_N
Pin 17	GND
Pin 18	GND
Pin 19	TXD_B2_P
Pin 20	TXD_B3_P
Pin 21	TXD_B2_N
Pin 22	TXD_B3_N
Pin 23	GND
Pin 24	GND
Pin 25	TXD_B4_P
Pin 26	TXD_B5_P
Pin 27	TXD_B4_N
Pin 28	TXD_B5_N
Pin 29	GND
Pin 30	GND
Pin 31	TXD_B6_P
Pin 32	TXD_B7_P
Pin 33	TXD_B6_N
Pin 34	TXD_B7_N
Pin 35	GND
Pin 36	GND
Pin 37	GND
Pin 38	GND
Pin 39	GND
Pin 40	GND

CON 8

Schematic page 12

This Amp Micro-strip connector is connected to the receive pins of the ORT8850. Receive signals can be sent through this connector, or **CON 3** and **CON 4** by selecting via DIP switches (**SW10** to **SW13** and **SW26** to **SW29**).

CON8	
Pin 1	GND
Pin 2	GND
Pin 3	GND
Pin 4	GND
Pin 5	GND
Pin 6	GND
Pin 7	RXSOC_B_N
Pin 8	RXCLK_B_N
Pin 9	RXSOC_B_P
Pin 10	RXCLK_B_P
Pin 11	GND
Pin 12	GND
Pin 13	RXD_B0_P
Pin 14	RXD_B1_P
Pin 15	RXD_B0_N
Pin 16	RXD_B1_N
Pin 17	GND
Pin 18	GND
Pin 19	RXD_B2_P
Pin 20	RXD_B3_P
Pin 21	RXD_B2_N
Pin 22	RXD_B3_N
Pin 23	GND
Pin 24	GND
Pin 25	RXD_B4_P
Pin 26	RXD_B5_P
Pin 27	RXD_B4_N
Pin 28	RXD_B5_N
Pin 29	GND
Pin 30	GND
Pin 31	RXD_B6_P
Pin 32	RXD_B7_P
Pin 33	RXD_B6_N
Pin 34	RXD_B7_N
Pin 35	GND
Pin 36	GND
Pin 37	GND
Pin 38	GND
Pin 39	GND
Pin 40	GND

CON 9, CON 10

Schematic pages 13 and 14

This connector type is an Amp Z-Pack 2mm header. A and B pins are connected to the receive pins of the ORT8850 and D and E pins are connected to the transmit pins of the ORT8850. A cable similar to one from W.L Gore (http://www.wlgore.com/) P/N 2MMA3143-01 adapts the 2mm Z-Pack to individual SMA connectors and is useful to observe the LVDS channels or connect to other test devices.

CON9									
Pin A1	RXD_C0_P	Pin B1	RXD_C0_N	Pin C1	GND	Pin D1	TXD_C0_N	Pin E1	TXD_C0_P
Pin A2	RXD_C1_P	Pin B2	RXD_C1_N	Pin C2	GND	Pin D2	TXD_C1_N	Pin E2	TXD_C1_P
Pin A3	RXD_C2_P	Pin B3	RXD_C2_N	Pin C3	GND	Pin D3	TXD_C2_N	Pin E3	TXD_C2_P
Pin A4	RXD_C3_P	Pin B4	RXD_C3_N	Pin C4	GND	Pin D4	TXD_C3_N	Pin E4	TXD_C3_P

CON10									
Pin A1	RXD_C4_P	Pin B1	RXD_C4_N	Pin C1	GND	Pin D1	TXD_C4_N	Pin E1	TXD_C4_P
Pin A2	RXD_C5_P	Pin B2	RXD_C5_N	Pin C2	GND	Pin D2	TXD_C5_N	Pin E2	TXD_C5_P
Pin A3	RXD_C6_P	Pin B3	RXD_C6_N	Pin C3	GND	Pin D3	TXD_C6_N	Pin E3	TXD_C6_P
Pin A4	RXD_C7_P	Pin B4	RXD_C7_N	Pin C4	GND	Pin D4	TXD_C7_N	Pin E4	TXD_C7_P

CON 11

Schematic page 13

This Amp Micro-strip connector is connected to the transit pins of the ORT8850. Transmit signals can be sent to this connector, or **CON 9** and **CON 10** by selecting via DIP switches (**SW14** to **SW17** and **SW30** to **SW33**).

CON11	
Pin 1	GND
Pin 2	GND
Pin 3	GND
Pin 4	GND
Pin 5	GND
Pin 6	GND
Pin 7	TXSOC_C_N
Pin 8	TXCLK_C_N
Pin 9	TXSOC_C_P
Pin 10	TXCLK_C_P
Pin 11	GND
Pin 12	GND
Pin 13	TXD_C0_P
Pin 14	TXD_C1_P
Pin 15	TXD_C0_N
Pin 16	TXD_C1_N
Pin 17	GND
Pin 18	GND
Pin 19	TXD_C2_P
Pin 20	TXD_C3_P
Pin 21	TXD_C2_N
Pin 22	TXD_C3_N
Pin 23	GND
Pin 24	GND
Pin 25	TXD_C4_P
Pin 26	TXD_C5_P
Pin 27	TXD_C4_N
Pin 28	TXD_C5_N
Pin 29	GND
Pin 30	GND
Pin 31	TXD_C6_P
Pin 32	TXD_C7_P
Pin 33	TXD_C6_N
Pin 34	TXD_C7_N
Pin 35	GND
Pin 36	GND
Pin 37	GND
Pin 38	GND
Pin 39	GND
Pin 40	GND

CON 14

Schematic page 14

This Amp Micro-strip connector is connected to the receive pins of the ORT8850. Receive signals can be sent through this connector, or **CON 9** and **CON 10** by selecting via DIP switches (**SW18** to **SW21** and **SW34** to **SW37**).

CON14	
Pin 1	GND
Pin 2	GND
Pin 3	GND
Pin 4	GND
Pin 5	GND
Pin 6	GND
Pin 7	RXSOC_C_N
Pin 8	RXCLK_C_N
Pin 9	RXSOC_C_P
Pin 10	RXCLK_C_P
Pin 11	GND
Pin 12	GND
Pin 13	RXD_C0_P
Pin 14	RXD_C1_P
Pin 15	RXD_C0_N
Pin 16	RXD_C1_N
Pin 17	GND
Pin 18	GND
Pin 19	RXD_C2_P
Pin 20	RXD_C3_P
Pin 21	RXD_C2_N
Pin 22	RXD_C3_N
Pin 23	GND
Pin 24	GND
Pin 25	RXD_C4_P
Pin 26	RXD_C5_P
Pin 27	RXD_C4_N
Pin 28	RXD_C5_N
Pin 29	GND
Pin 30	GND
Pin 31	RXD_C6_P
Pin 32	RXD_C7_P
Pin 33	RXD_C6_N
Pin 34	RXD_C7_N
Pin 35	GND
Pin 36	GND
Pin 37	GND
Pin 38	GND
Pin 39	GND
Pin 40	GND

R174

Schematic page 22

This adjustable resistor is used along with test point (reference **TP10**) to set the 1.4 Volts reference for the ORT8850.

R175

Schematic page 22

This adjustable resistor is used along with test point (reference **TP9**) to set the 1.0 Volts reference for the ORT8850.

Board Revisions

The connectivity of the ORT8850H microprocessor interface pins to the MPC680 bus is incorrect. The actual connections between the ORCA device and PowerPC for J21 and J23 should follow the table listed below rather than the connections depicted in the schematic. Included with this kit is an intermediate PCB which will map the connections correctly for use with the Windriver MPC860 development board.

PPC Address Pin	ORCA Address Pin	PPC Data Pin	ORCA Data Pin
31	17	0	0
30	16	1	1
29	15	2	2
28	14	3	3
27	13	4	4
26	12	5	5
25	11	6	6
24	10	7	7
23	9	8	8
22	8	9	9
21	7	10	10
20	6	11	11
19	5	12	12
18	4	13	13
17	3	14	14
16	2	15	15
15	1	16	16
14	0	17	17
13	NC	18	18
12	NC	19	19
11	NC	20	20
10	NC	21	21
9	NC	22	22
8	NC	23	23
7	NC	24	24
6	NC	25	25
5	NC	26	26
4	NC	27	27
3	NC	28	28
2	NC	29	29
1	NC	30	30
0	NC	31	31

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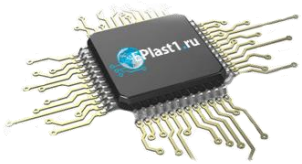
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

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