PCA9540B

2-channel I²C-bus multiplexer

Rev. 04 — 3 September 2009 Product data sheet

1. General description

The PCA9540B is a 1-of-2 bidirectional translating multiplexer, controlled via the I²C-bus. The SCL/SDA upstream pair fans out to two SCx/SDx downstream pairs, or channels. Only one SCx/SDx channel is selected at a time, determined by the contents of the programmable control register.

A power-on reset function puts the registers in their default state and initializes the I²C-bus state machine with no channels selected.

The pass gates of the multiplexer are constructed such that the V_{DD} pin can be used to limit the maximum high voltage that will be passed by the PCA9540B. This allows the use of different bus voltages on each SCx/SDx pair, so that 1.8 V, 2.5 V or 3.3 V parts can communicate with 5 V parts without any additional protection. External pull-up resistors can pull the bus up to the desired voltage level for this channel. All I/O pins are 5 V tolerant.

2. Features

- 1-of-2 bidirectional translating multiplexer
- I²C-bus interface logic; compatible with SMBus standards
- Channel selection via I²C-bus
- Power up with all multiplexer channels deselected
- Low R_{on} switches
- Allows voltage level translation between 1.8 V, 2.5 V, 3.3 V and 5 V buses
- No glitch on power-up
- Supports hot insertion
- Low standby current
- Operating power supply voltage range of 2.3 V to 5.5 V
- 5 V tolerant inputs
- 0 Hz to 400 kHz clock frequency
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD2-A115 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Packages offered: SO8, TSSOP8, XSON8U

3. Ordering information

Table 1. Ordering information

T_{amb} = −40 °C to +85 °C

Type number	Topside mark	Package		
		Name	Description	Version
PCA9540BD	PA9540B	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1
PCA9540BDP	9540B	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm	SOT505-1
PCA9540BGD	40B	XSON8U	plastic extremely thin small outline package; no leads; 8 terminals; UTLP based; body 3 × 2 × 0.5 mm	SOT996-2

4. Block diagram

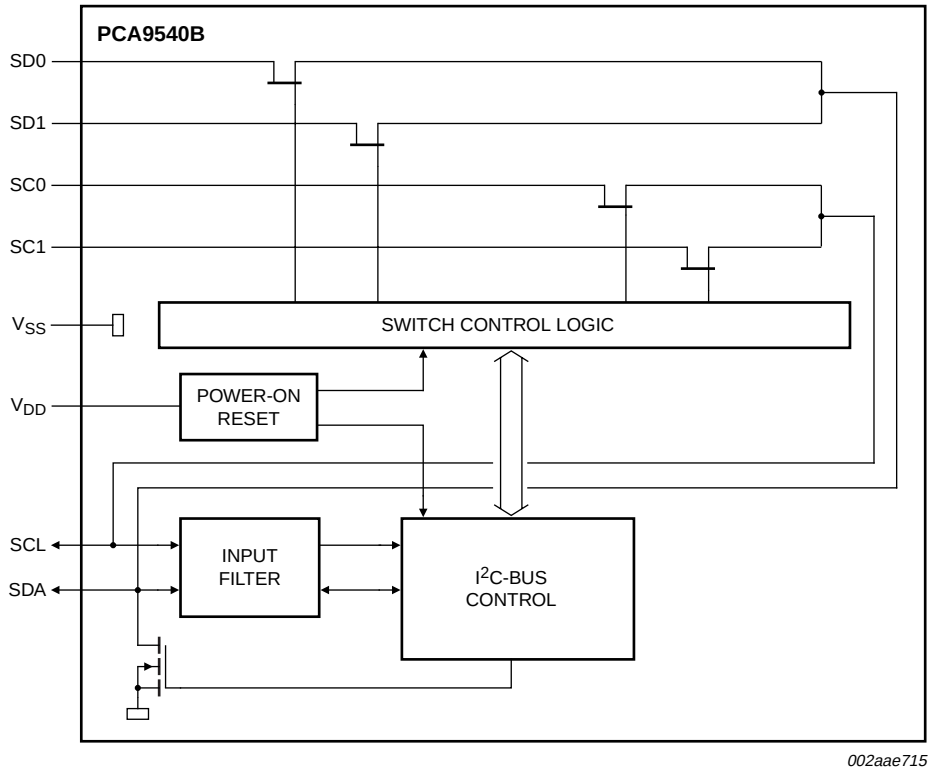


Fig 1. Block diagram of PCA9540B

5. Pinning information

5.1 Pinning

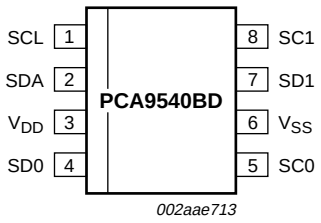


Fig 2. Pin configuration for SO8

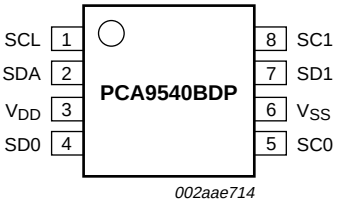
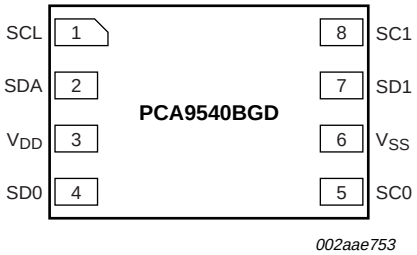


Fig 3. Pin configuration for TSSOP8



Transparent top view

Fig 4. Pin configuration for XSON8U

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
SCL	1	serial clock line
SDA	2	serial data line
V_{DD}	3	supply voltage
SD0	4	serial data 0
SC0	5	serial clock 0
V_{SS}	6	supply ground
SD1	7	serial data 1
SC1	8	serial clock 1

6. Functional description

Refer to Figure 1 “Block diagram of PCA9540B”.

6.1 Device addressing

Following a START condition the bus master must output the address of the slave it is accessing. The address of the PCA9540B is shown in Figure 5.

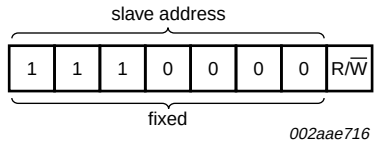


Fig 5. Slave address

The last bit of the slave address defines the operation to be performed. When set to logic 1 a read is selected, while a logic 0 selects a write operation.

6.2 Control register

Following the successful acknowledgement of the slave address, the bus master will send a byte to the PCA9540B which will be stored in the Control register. If multiple bytes are received by the PCA9540B, it will save the last byte received. This register can be written and read via the I²C-bus.

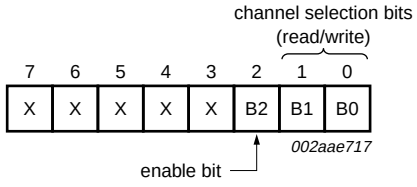


Fig 6. Control register

6.2.1 Control register definition

A SCx/SDx downstream pair, or channel, is selected by the contents of the Control register. This register is written after the PCA9540B has been addressed. The 2 LSBs of the control byte are used to determine which channel is to be selected. When a channel is selected, it will become active after a STOP condition has been placed on the I²C-bus. This ensures that all SCx/SDx lines will be in a HIGH state when the channel is made active, so that no false conditions are generated at the time of connection.

Table 3. Control register: Write—channel selection; Read—channel status

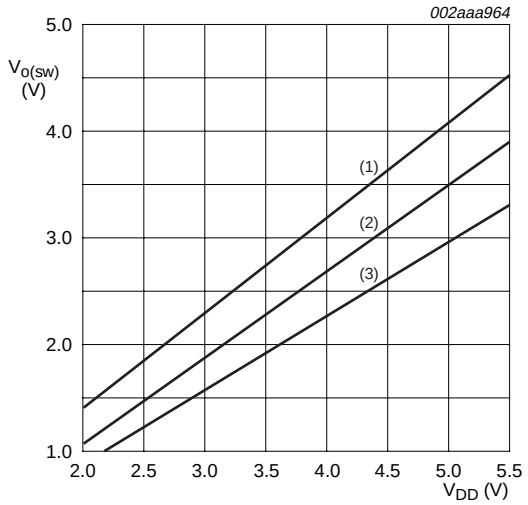
D7	D6	D5	D4	D3	B2	B1	B0	Command
X	X	X	X	X	0	X	X	no channel selected
X	X	X	X	X	1	0	0	channel 0 enabled
X	X	X	X	X	1	0	1	channel 1 enabled
X	X	X	X	X	1	1	X	no channel selected
0	0	0	0	0	0	0	0	no channel selected; power-up default state

6.3 Power-on reset

When power is applied to V_{DD}, an internal Power-On Reset (POR) holds the PCA9540B in a reset condition until V_{DD} has reached V_{POR}. At this point, the reset condition is released and the PCA9540B registers and I²C-bus state machine are initialized to their default states (all zeroes), causing all the channels to be deselected. Thereafter, V_{DD} must be lowered below 0.2 V to reset the device.

6.4 Voltage translation

The pass gate transistors of the PCA9540B are constructed such that the V_{DD} voltage can be used to limit the maximum voltage that will be passed from one I²C-bus to another.



(1) maximum
(2) typical
(3) minimum

Fig 7. Pass gate voltage versus supply voltage

Figure 7 shows the voltage characteristics of the pass gate transistors (note that the graph was generated using the data specified in Section 10 “Static characteristics” of this data sheet). In order for the PCA9540B to act as a voltage translator, the $V_{o(sw)}$ voltage should be equal to, or lower than the lowest bus voltage. For example, if the main bus was running at 5 V, and the downstream buses were 3.3 V and 2.7 V, then $V_{o(sw)}$ should be equal to or below 2.7 V to effectively clamp the downstream bus voltages. Looking at

Figure 7, we see that $V_{o(sw)(max)}$ will be at 2.7 V when the PCA9540B supply voltage is 3.5 V or lower so the PCA9540B supply voltage could be set to 3.3 V. Pull-up resistors can then be used to bring the bus voltages to their appropriate levels (see Figure 14).

More Information can be found in application note *AN262, "PCA954X family of I²C/SMBus multiplexers and switches"*.

7. Characteristics of the I²C-bus

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

7.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals (see Figure 8).

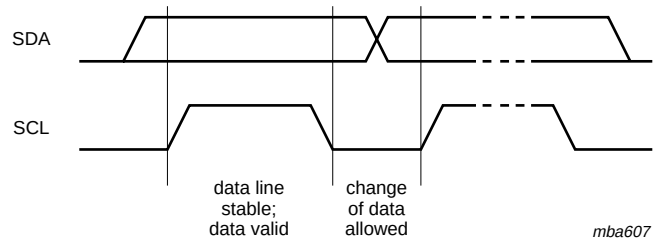


Fig 8. Bit transfer

7.2 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P) (see Figure 9).

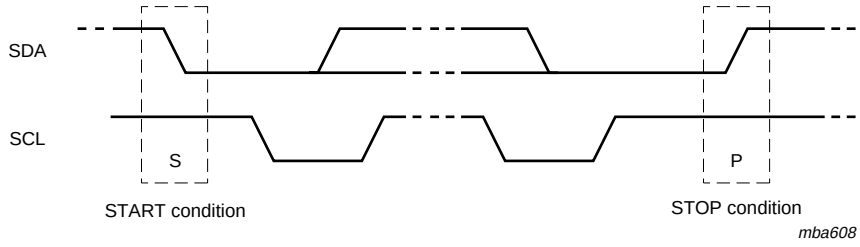


Fig 9. Definition of START and STOP conditions

7.3 System configuration

A device generating a message is a ‘transmitter’, a device receiving is the ‘receiver’. The device that controls the message is the ‘master’ and the devices which are controlled by the master are the ‘slaves’ (see Figure 10).

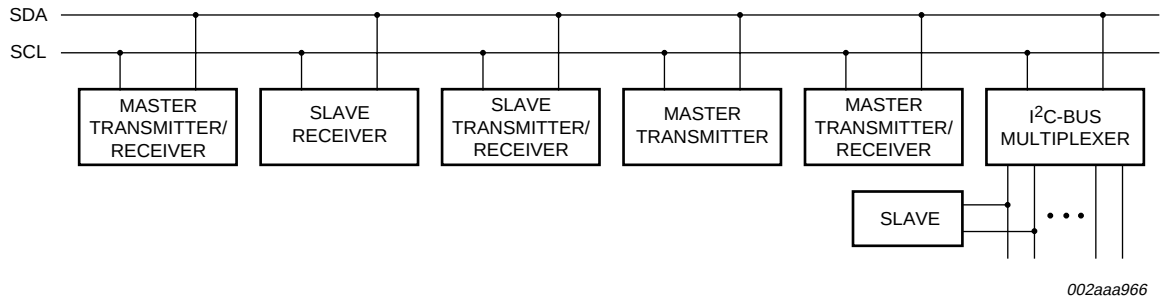


Fig 10. System configuration

7.4 Acknowledge

The number of data bytes transferred between the START and the STOP conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter, whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also, a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse; set-up and hold times must be taken into account.

A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

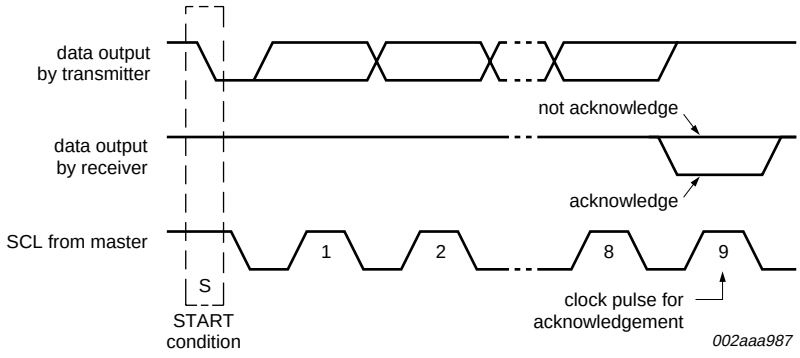


Fig 11. Acknowledgement on the I²C-bus

7.5 Bus transactions

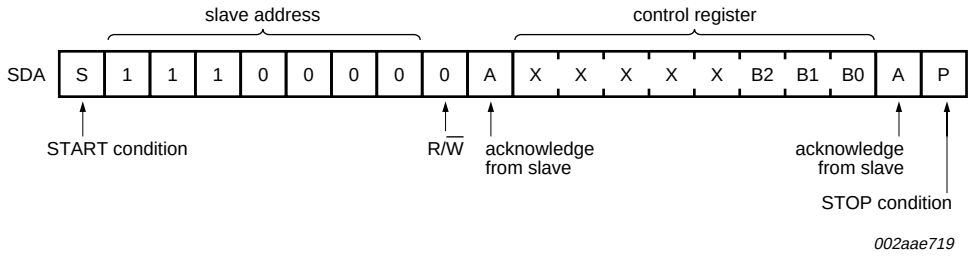


Fig 12. Write control register

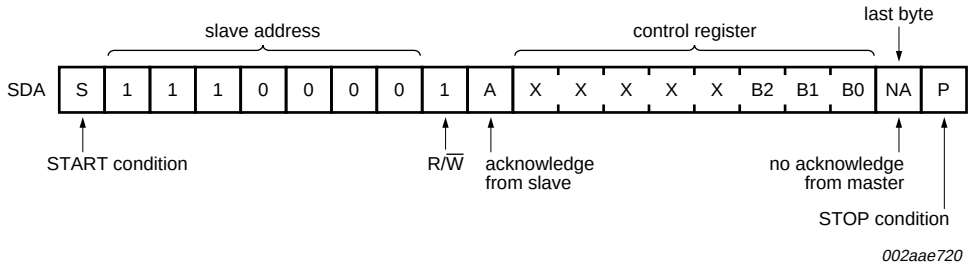


Fig 13. Read control register

8. Application design-in information

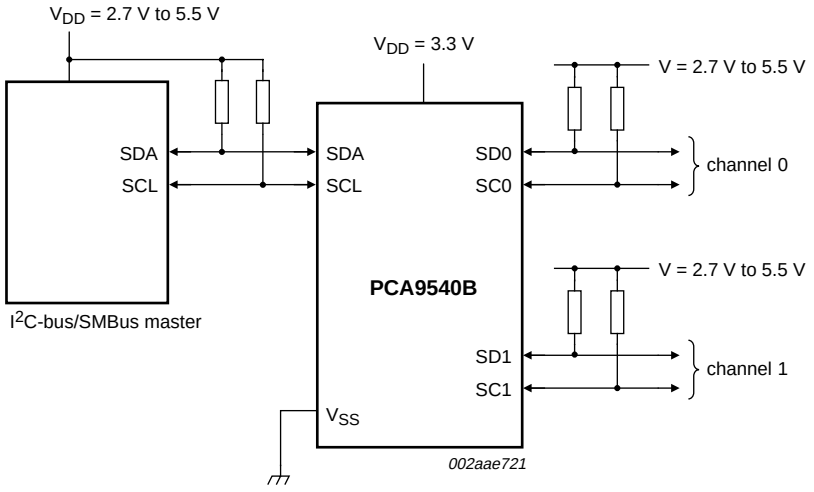


Fig 14. Typical application

9. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to ground (V_{SS} = 0 V).[1]

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		–0.5	+7.0	V
V_I	input voltage		–0.5	+7.0	V
I_I	input current		-	±20	mA
I_O	output current		-	±25	mA
I_{DD}	supply current		-	±100	mA
I_{SS}	ground supply current		-	±100	mA
P_{tot}	total power dissipation		-	400	mW
T_{stg}	storage temperature		–60	+150	°C
T_{amb}	ambient temperature	operating	–40	+85	°C

[1] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 125 °C.

10. Static characteristics

Table 5. Static characteristics at V_{DD} = 2.3 V to 3.6 V

V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
See Table 6 for V_{DD} = 3.6 V to 5.5 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supply							
V_{DD}	supply voltage			2.3	-	3.6	V
I_{DD}	supply current	operating mode; V_{DD} = 3.6 V; no load; V_I = V_{DD} or V_{SS}; f_{SCL} = 100 kHz		-	20	50	µA
I_{stb}	standby current	standby mode; V_{DD} = 3.6 V; no load; V_I = V_{DD} or V_{SS}; f_{SCL} = 0 kHz		-	0.1	1	µA
V_{POR}	power-on reset voltage	no load; V_I = V_{DD} or V_{SS}	[1]	-	1.6	2.1	V
Input SCL; input/output SDA							
V_{IL}	LOW-level input voltage			−0.5	-	+0.3V_{DD}	V
V_{IH}	HIGH-level input voltage			0.7V_{DD}	-	6	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V		3	-	-	mA
		V_{OL} = 0.6 V		6	-	-	mA
I_L	leakage current	V_I = V_{DD} or V_{SS}		−1	-	+1	µA
C_i	input capacitance	V_I = V_{SS}		-	7	8	pF
Pass gate							
R_{on}	ON-state resistance	V_{DD} = 3.0 V to 3.6 V; V_O = 0.4 V; I_O = 15 mA		5	11	31	Ω
		V_{DD} = 2.3 V to 2.7 V; V_O = 0.4 V; I_O = 10 mA		7	16	55	Ω
$V_{o(sw)}$	switch output voltage	$V_{i(sw)}$ = V_{DD} = 3.3 V; $I_{o(sw)}$ = −100 µA		-	1.9	-	V
		$V_{i(sw)}$ = V_{DD} = 3.0 V to 3.6 V; $I_{o(sw)}$ = −100 µA		1.6	-	2.8	V
		$V_{i(sw)}$ = V_{DD} = 2.5 V; $I_{o(sw)}$ = −100 µA		-	1.5	-	V
		$V_{i(sw)}$ = V_{DD} = 2.3 V to 2.7 V; $I_{o(sw)}$ = −100 µA		1.1	-	2.0	V
I_L	leakage current	V_I = V_{DD} or V_{SS}		−1	-	+1	µA
C_{io}	input/output capacitance	V_I = V_{SS}		-	2.5	5	pF

[1] V_{DD} must be lowered to 0.2 V in order to reset part.

Table 6. Static characteristics at V_{DD} = 3.6 V to 5.5 V

V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
See Table 5 for V_{DD} = 2.3 V to 3.6 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supply							
V_{DD}	supply voltage			3.6	-	5.5	V
I_{DD}	supply current	operating mode; V_{DD} = 5.5 V; no load; V_I = V_{DD} or V_{SS}; f_{SCL} = 100 kHz		-	65	100	µA
I_{stb}	standby current	standby mode; V_{DD} = 5.5 V; no load; V_I = V_{DD} or V_{SS}		-	0.3	1	µA
V_{POR}	power-on reset voltage	no load; V_I = V_{DD} or V_{SS}	[1]	-	1.6	2.1	V
Input SCL; input/output SDA							
V_{IL}	LOW-level input voltage			−0.5	-	+0.3V_{DD}	V
V_{IH}	HIGH-level input voltage			0.7V_{DD}	-	6	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V		3	-	-	mA
		V_{OL} = 0.6 V		6	-	-	mA
I_{IL}	LOW-level input current	V_I = V_{SS}		−1	-	+1	µA
I_{IH}	HIGH-level input current	V_I = V_{DD}		−1	-	+1	µA
C_i	input capacitance	V_I = V_{SS}		-	6	8	pF
Pass gate							
R_{on}	ON-state resistance	V_{DD} = 4.5 V to 5.5 V; V_O = 0.4 V; I_O = 15 mA		4	9	24	Ω
$V_{o(sw)}$	switch output voltage	$V_{i(sw)}$ = V_{DD} = 5.0 V; $I_{o(sw)}$ = −100 µA		-	3.6	-	V
		$V_{i(sw)}$ = V_{DD} = 4.5 V to 5.5 V; $I_{o(sw)}$ = −100 µA		2.6	-	4.5	V
I_L	leakage current	V_I = V_{DD} or V_{SS}		−1	-	+1	µA
C_{io}	input/output capacitance	V_I = V_{SS}		-	2.5	5	pF

[1] V_{DD} must be lowered to 0.2 V in order to reset part.

11. Dynamic characteristics

Table 7. Dynamic characteristics

Symbol	Parameter	Conditions		Standard-mode I²C-bus		Fast-mode I²C-bus		Unit
				Min	Max	Min	Max	
t_{PD}	propagation delay	from SDA to SDx, or SCL to SCx		-	0.3[1]	-	0.3[1]	ns
f_{SCL}	SCL clock frequency			0	100	0	400	kHz
t_{BUF}	bus free time between a STOP and START condition			4.7	-	1.3	-	µs
$t_{HD;STA}$	hold time (repeated) START condition		[2]	4.0	-	0.6	-	µs
t_{LOW}	LOW period of the SCL clock			4.7	-	1.3	-	µs
t_{HIGH}	HIGH period of the SCL clock			4.0	-	0.6	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition			4.7	-	0.6	-	µs
$t_{SU;STO}$	set-up time for STOP condition			4.0	-	0.6	-	µs
$t_{HD;DAT}$	data hold time			0[3]	3.45	0[3]	0.9	µs
$t_{SU;DAT}$	data set-up time			250	-	100	-	ns
t_r	rise time of both SDA and SCL signals			-	1000	$20 + 0.1C_b$[4]	300	ns
t_f	fall time of both SDA and SCL signals			-	300	$20 + 0.1C_b$[4]	300	ns
C_b	capacitive load for each bus line			-	400	-	400	pF
t_{SP}	pulse width of spikes that must be suppressed by the input filter			-	50	-	50	ns
$t_{VD;DAT}$	data valid time	HIGH-to-LOW	[5]	-	1	-	1	µs
		LOW-to-HIGH	[5]	-	0.6	-	0.6	µs
$t_{VD;ACK}$	data valid acknowledge time			-	1	-	1	µs

[1] Pass gate propagation delay is calculated from the 20 Ω typical R_{on} and the 15 pF load capacitance.

[2] After this period, the first clock pulse is generated.

[3] A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the $V_{IH(min)}$ of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.

[4] C_b = total capacitance of one bus line in pF.

[5] Measurements taken with 1 kΩ pull-up resistor and 50 pF load.

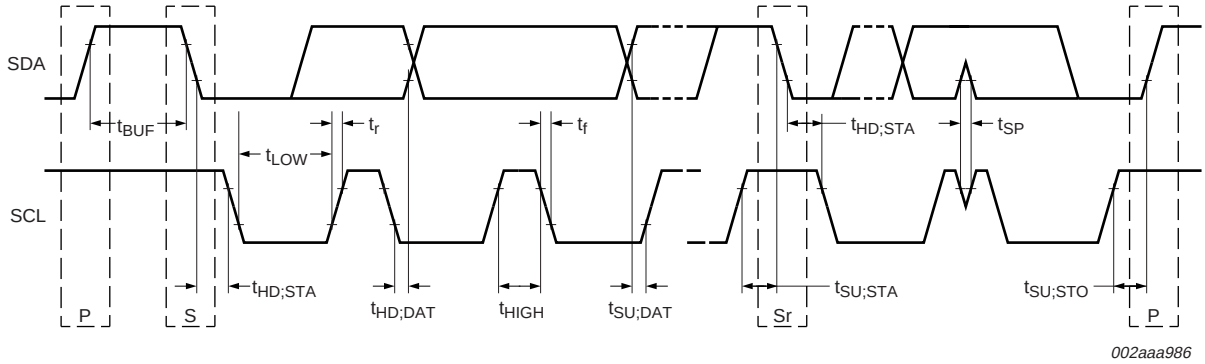
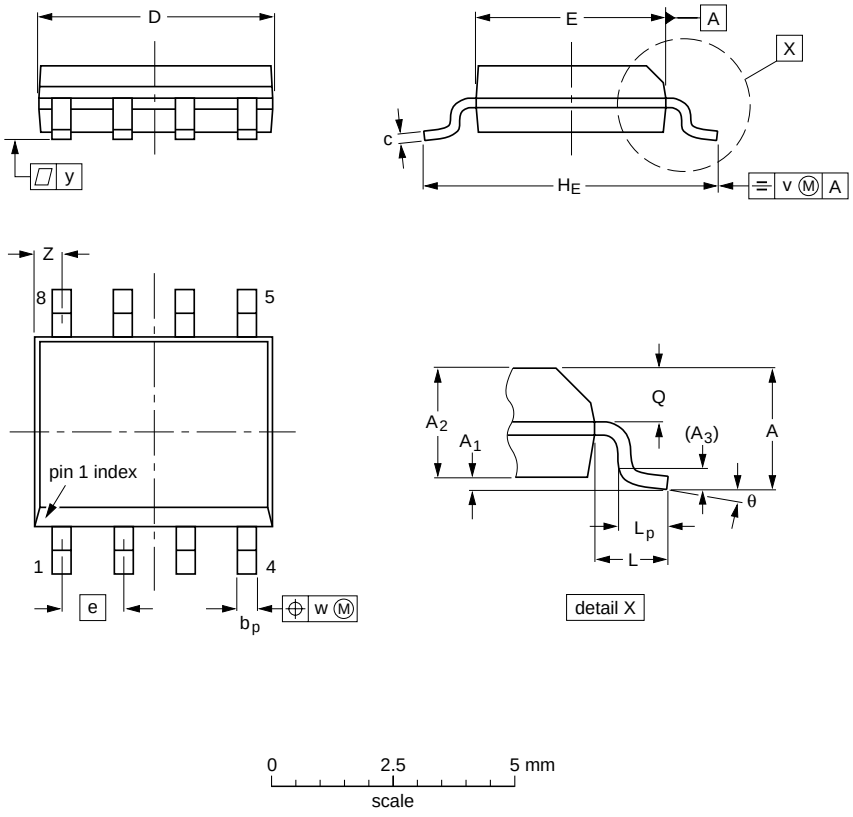


Fig 15. Definition of timing on the I²C-bus

12. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

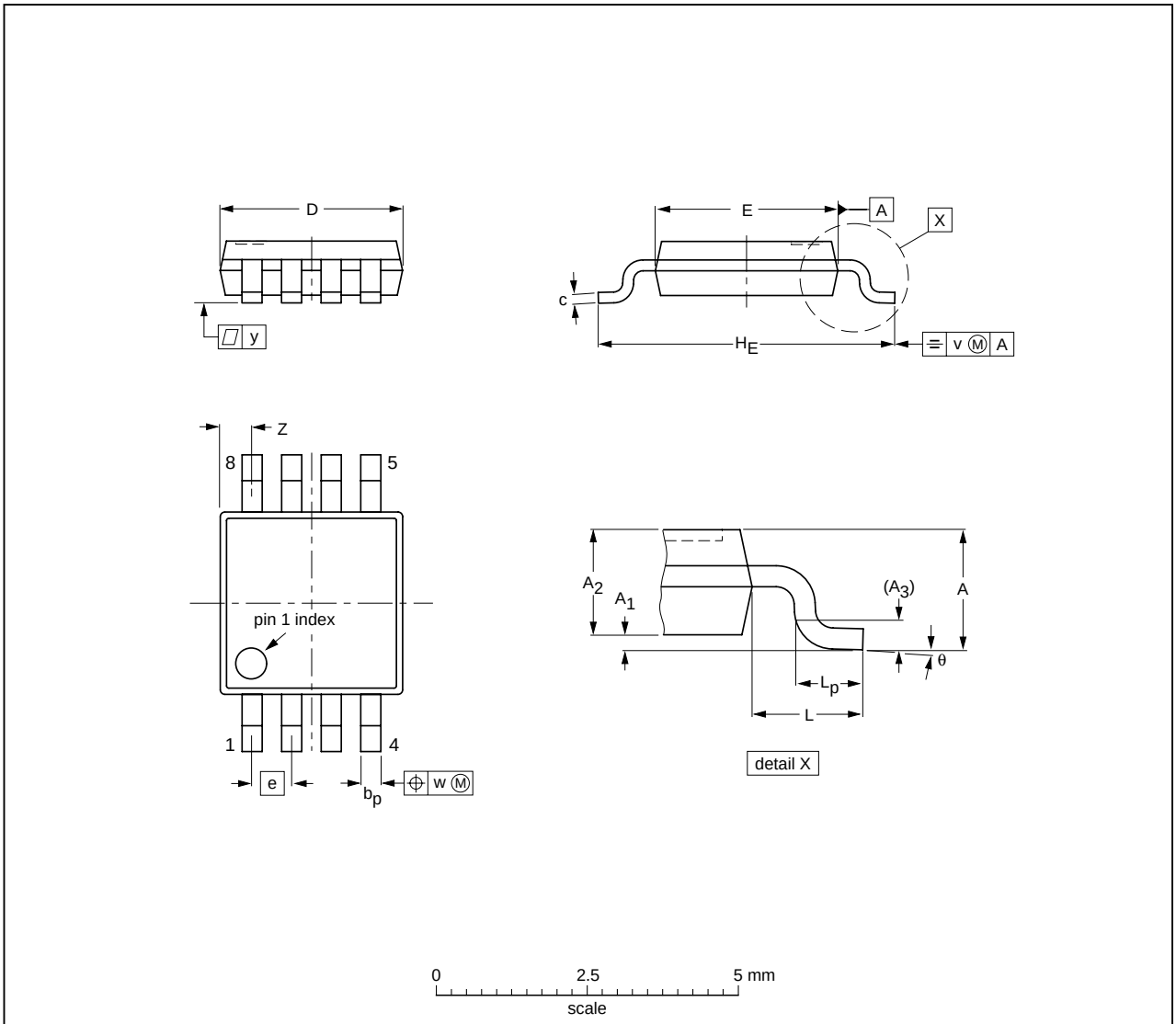
Notes

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT96-1	076E03	MS-012				~~99-12-27~~ 03-02-18

Fig 16. Package outline SOT96-1 (SO8)

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm **SOT505-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.45 0.25	0.28 0.15	3.1 2.9	3.1 2.9	0.65	5.1 4.7	0.94	0.7 0.4	0.1	0.1	0.1	0.70 0.35	6° 0°

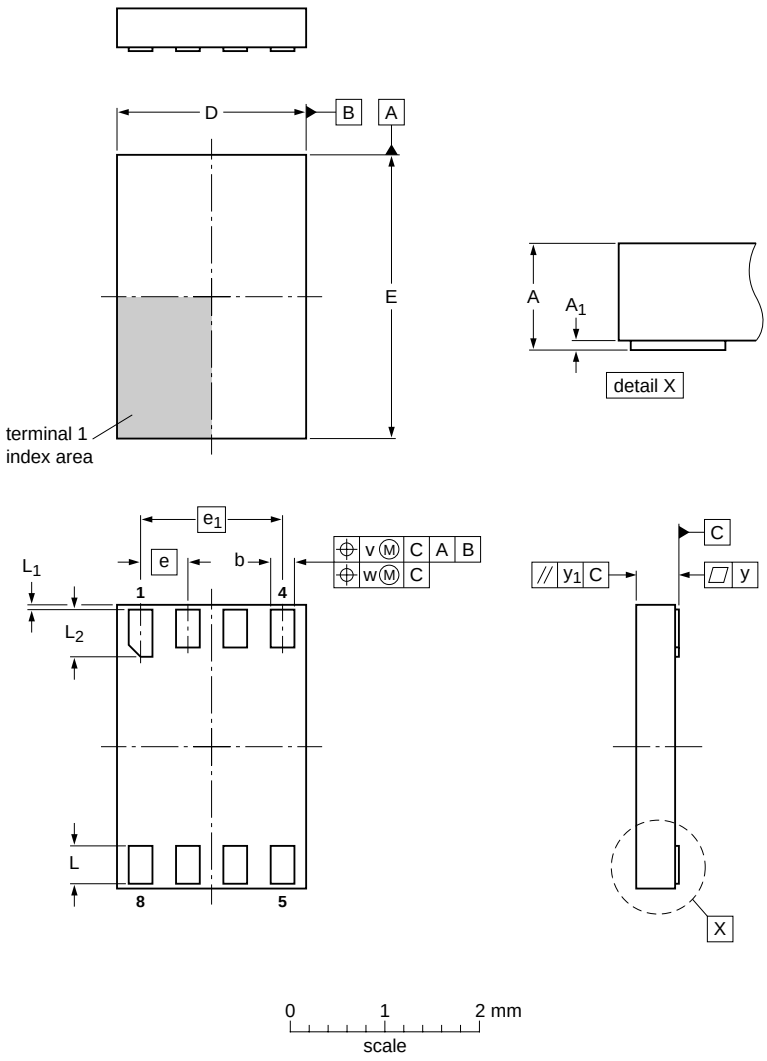
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT505-1						~~99-04-09~~ 03-02-18

Fig 17. Package outline SOT505-1 (TSSOP8)

XSON8U: plastic extremely thin small outline package; no leads; 8 terminals; UTLP based; body 3 x 2 x 0.5 mm **SOT996-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max	A_1	b	D	E	e	e_1	L	L_1	L_2	v	w	y	y_1
mm	0.5	0.05 0.00	0.35 0.15	2.1 1.9	3.1 2.9	0.5	1.5	0.5 0.3	0.15 0.05	0.6 0.4	0.1	0.05	0.05	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT996-2	- - -		- - -			~~07-12-18~~ 07-12-21

Fig 18. Package outline SOT996-2 (XSON8U)

13. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

13.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

13.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

13.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

13.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 19) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 8 and 9

Table 8. SnPb eutectic process (from J-STD-020C)

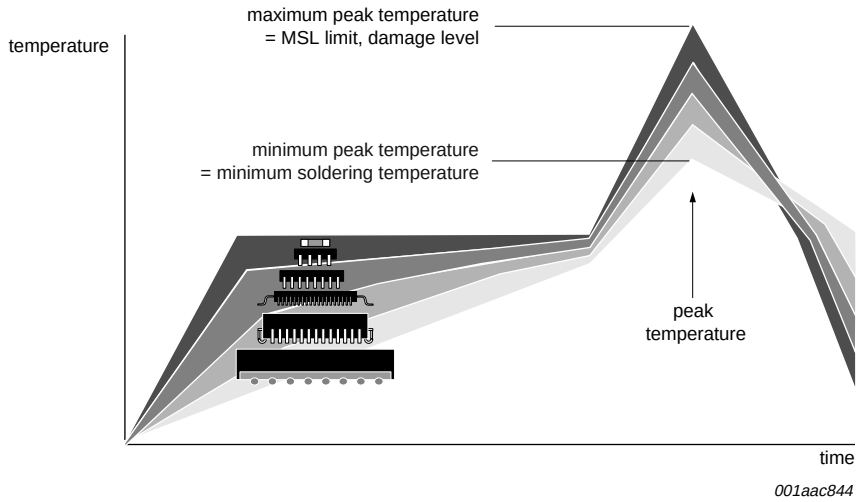
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 9. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 19.



MSL: Moisture Sensitivity Level

Fig 19. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

14. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged-Device Model
ESD	ElectroStatic Discharge
HBM	Human Body Model
I²C-bus	Inter-Integrated Circuit bus
I/O	Input/Output
IC	Integrated Circuit
LSB	Least Significant Bit
MM	Machine Model
POR	Power-On Reset
SMBus	System Management Bus

15. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA9540B_4	20090903	Product data sheet	-	PCA9540B_3
Modifications:	• Added XSON8U package offering (affects Section 2 “Features” last bullet item, Table 1 “Ordering information”, Section 5.1 “Pinning”, and Section 12 “Package outline”).			
PCA9540B_3	20090528	Product data sheet	-	PCA9540B_2
PCA9540B_2 (9397 750 13731)	20040929	Product data sheet	-	PCA9540B_1
PCA9540B_1 (9397 750 12918)	20040413	Product data	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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18. Contents

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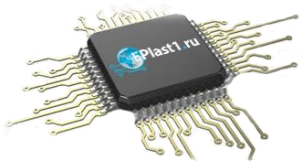

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