

## Power MOSFET

PRODUCT SUMMARY		
$V_{DS}$ (V)	- 60	
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = - 10$ V	0.14
$Q_g$ (Max.) (nC)	34	
$Q_{gs}$ (nC)	9.9	
$Q_{gd}$ (nC)	16	
Configuration	Single	

### FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- Advanced Process Technology
- Surface Mount (IRF9Z34S, SiHF9Z34S)
- Low-Profile Through-Hole (IRF9Z34L, SiHF9Z34L)
- 175 °C Operating Temperature
- Fast Switching
- P-Channel
- Fully Avalanche Rated
- Compliant to RoHS Directive 2002/95/EC



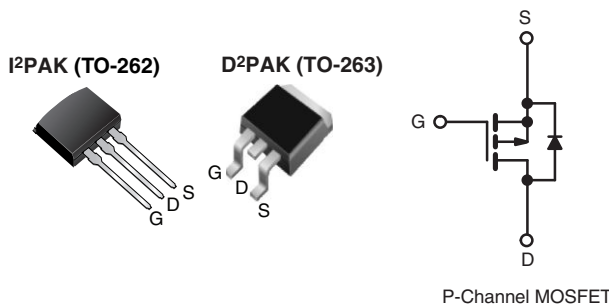
**RoHS\***  
COMPLIANT  
HALOGEN  
**FREE**  
Available

### DESCRIPTION

Third generation Power MOSFETs from Vishay utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The D<sup>2</sup>PAK is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D<sup>2</sup>PAK is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0 W in a typical surface mount application.

The through-hole version (IRF9Z34L, SiHF9Z34L) is available for low-profile applications.



ORDERING INFORMATION				
Package	D <sup>2</sup> PAK (TO-263)	D <sup>2</sup> PAK (TO-263)	D <sup>2</sup> PAK (TO-263)	I <sup>2</sup> PAK (TO-262)
Lead (Pb)-free and Halogen-free	SiHF9Z34S-GE3	SiHF9Z34STRL-GE3 <sup>a</sup>	SiHF9Z34STRR-GE3 <sup>a</sup>	-
Lead (Pb)-free	IRF9Z34SPbF	IRF9Z34STRLPbF <sup>a</sup>	IRF9Z34STRRPbF <sup>a</sup>	IRF9Z34LPbF
	SiHF9Z34S-E3	SiHF9Z34STL-E3 <sup>a</sup>	SiHF9Z34STR-E3 <sup>a</sup>	SiHF9Z34L-E3

#### Note

a. See device orientation.

ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)					
PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			$V_{DS}$	- 60	V
Gate-Source Voltage			$V_{GS}$	$\pm 20$	
Continuous Drain Current	$V_{GS}$ at - 10 V	$T_C = 25$ °C	$I_D$	- 18	A
		$T_C = 100$ °C		- 13	
Pulsed Drain Current <sup>a, e</sup>			$I_{DM}$	- 72	
Linear Derating Factor				0.59	W/°C
Single Pulse Avalanche Energy <sup>b, e</sup>			$E_{AS}$	370	mJ
Avalanche Current <sup>a</sup>			$I_{AR}$	- 18	A
Repetitive Avalanche Energy <sup>a</sup>			$E_{AR}$	8.8	mJ
Maximum Power Dissipation	$T_C = 25$ °C		$P_D$	88	W
	$T_A = 25$ °C			3.7	
Peak Diode Recovery $dV/dt$ <sup>c, e</sup>			$dV/dt$	- 4.5	V/ns
Operating Junction and Storage Temperature Range			$T_J, T_{stg}$	- 55 to + 175	°C
Soldering Recommendations (Peak Temperature)	for 10 s			300 <sup>d</sup>	

#### Notes


- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = - 25$  V, starting  $T_J = 25$  °C,  $L = 1.3$  mH,  $R_g = 25$   $\Omega$ ,  $I_{AS} = - 18$  A (see fig. 12).
- $I_{SD} \leq - 18$  A,  $dI/dt \leq 170$  A/ $\mu$ s,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 175$  °C.
- 1.6 mm from case.
- Uses IRF9Z34, SiHF9Z34 data and test conditions.

\* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient (PCB Mounted, steady-state) <sup>a</sup>	$R_{thJA}$	-	40	°C/W
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	1.7	

### Note

a. When mounted on 1" square PCB (FR-4 or G-10 material).

SPECIFICATIONS ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
<b>Static</b>							
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$		-60	-	-	V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$ , $I_D = -1\text{ mA}^c$		-	-0.06	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$		-2.0	-	-4.0	V
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 20\text{ V}$		-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -60\text{ V}, V_{GS} = 0\text{ V}$		-	-	-100	$\mu\text{A}$
		$V_{DS} = -48\text{ V}, V_{GS} = 0\text{ V}, T_J = 150\text{ }^\circ\text{C}$		-	-	-500	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = -10\text{ V}$	$I_D = -11\text{ A}^b$	-	-	0.14	$\Omega$
Forward Transconductance	$g_{fs}$	$V_{DS} = -25\text{ V}, I_D = -11\text{ A}^c$		5.9	-	-	S
<b>Dynamic</b>							
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, V_{DS} = -25\text{ V}, f = 1.0\text{ MHz}$ , see fig. 5 <sup>c</sup>		-	1100	-	$\mu\text{F}$
Output Capacitance	$C_{oss}$			-	620	-	
Reverse Transfer Capacitance	$C_{rss}$			-	100	-	
Total Gate Charge	$Q_g$	$V_{GS} = -10\text{ V}$	$I_D = -18\text{ A}, V_{DS} = -48\text{ V}$ , see fig. 6 and 13 <sup>b, c</sup>	-	-	34	nC
Gate-Source Charge	$Q_{gs}$			-	-	9.9	
Gate-Drain Charge	$Q_{gd}$			-	-	16	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -30\text{ V}, I_D = -18\text{ A}, R_g = 12\text{ }\Omega, R_D = 1.5\text{ }\Omega$ , see fig. 10 <sup>b, c</sup>		-	18	-	ns
Rise Time	$t_r$			-	120	-	
Turn-Off Delay Time	$t_{d(off)}$			-	20	-	
Fall Time	$t_f$			-	58	-	
<b>Drain-Source Body Diode Characteristics</b>							
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p-n junction diode 		-	-	-18	A
Pulsed Diode Forward Current <sup>a</sup>	$I_{SM}$			-	-	-72	
Body Diode Voltage	$V_{SD}$	$T_J = 25\text{ }^\circ\text{C}, I_S = -18\text{ A}, V_{GS} = 0\text{ V}^b$		-	-	-6.3	V
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}, I_F = -18\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}^b, c$		-	100	200	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$			-	280	520	nC
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )					

### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- Uses IRF9Z34, SiHF9Z34 data and test conditions.

## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

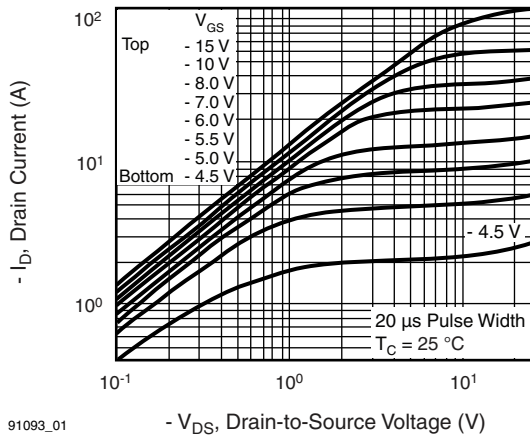


Fig. 1 - Typical Output Characteristics

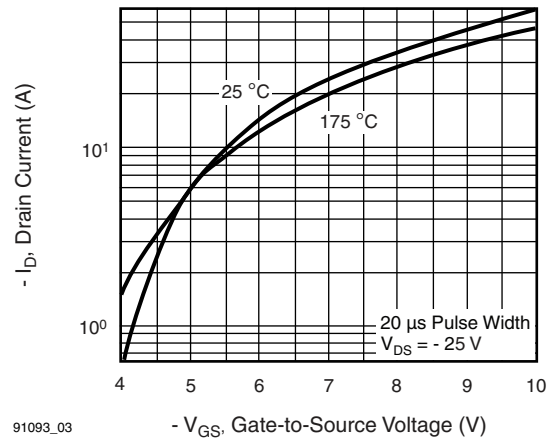


Fig. 3 - Typical Transfer Characteristics

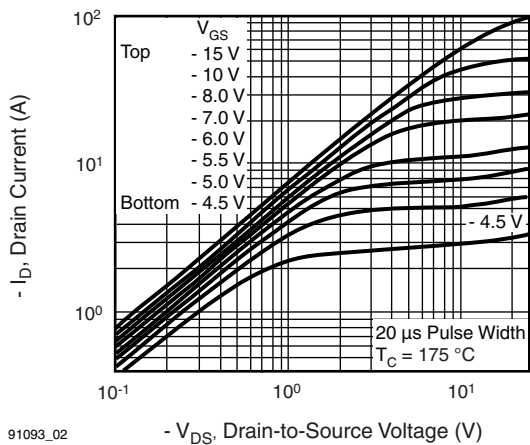


Fig. 2 - Typical Output Characteristics

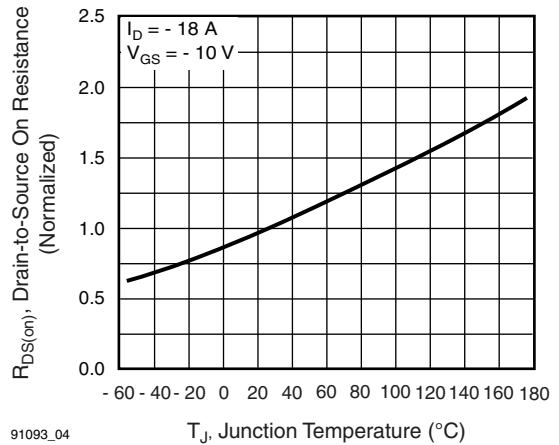


Fig. 4 - Normalized On-Resistance vs. Temperature

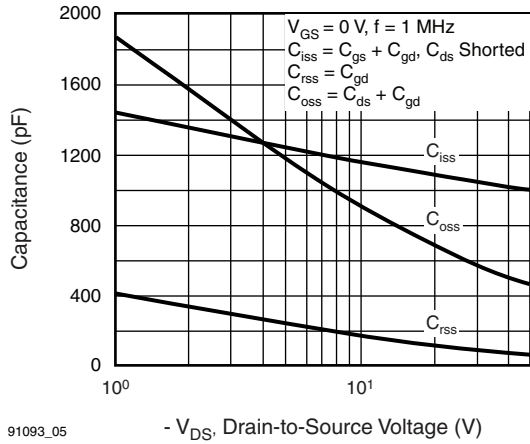


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

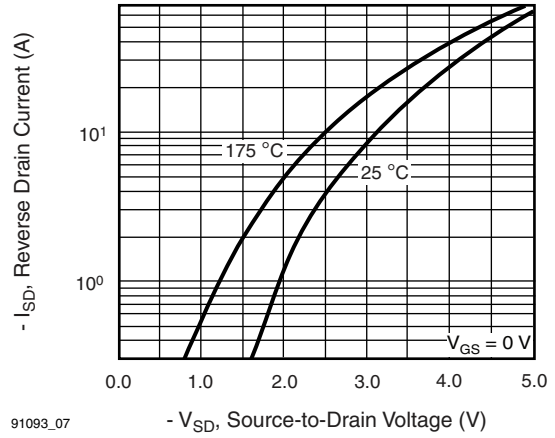


Fig. 7 - Typical Source-Drain Diode Forward Voltage

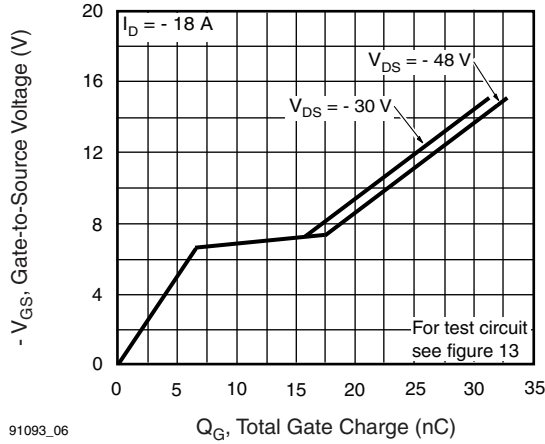


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

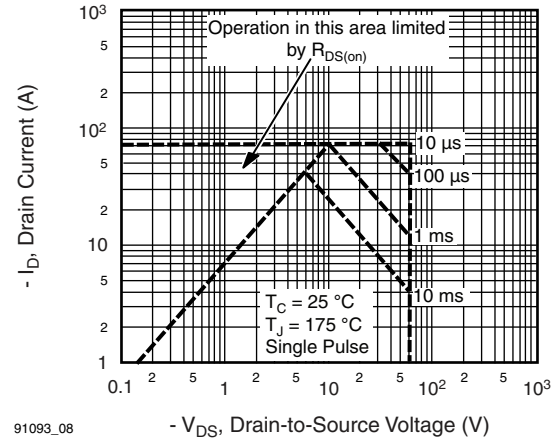


Fig. 8 - Maximum Safe Operating Area

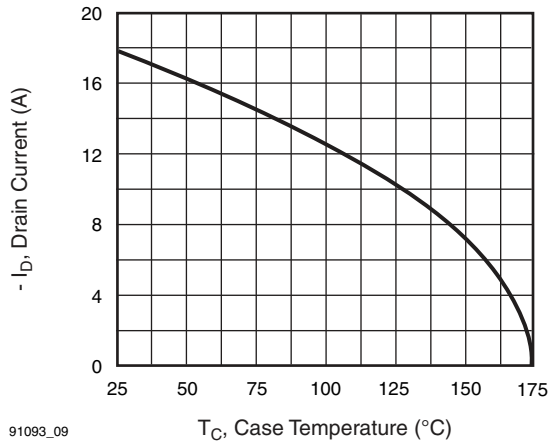


Fig. 9 - Maximum Drain Current vs. Case Temperature

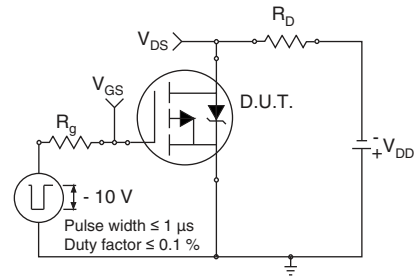


Fig. 10a - Switching Time Test Circuit

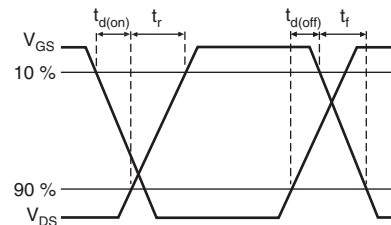


Fig. 10b - Switching Time Waveforms

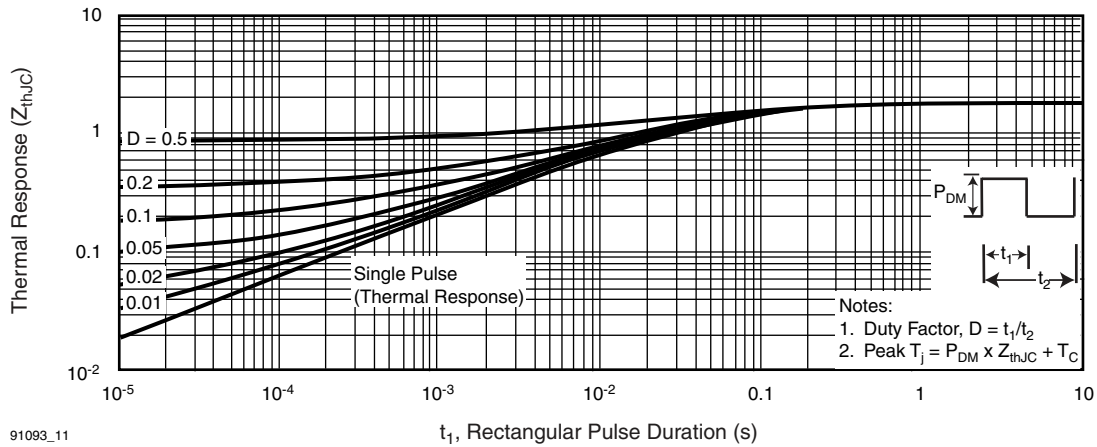


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

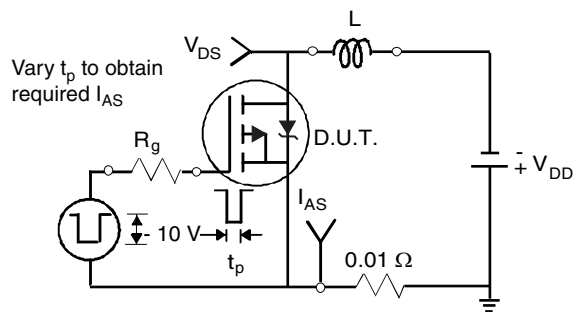


Fig. 12a - Unclamped Inductive Test Circuit

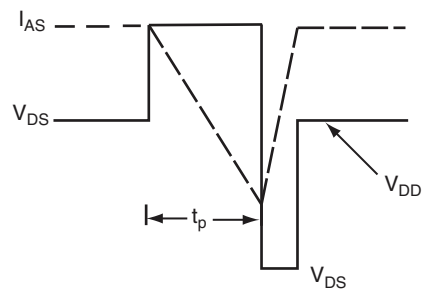


Fig. 12b - Unclamped Inductive Waveforms

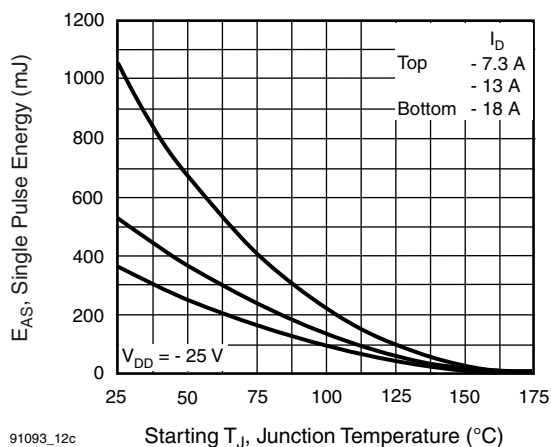


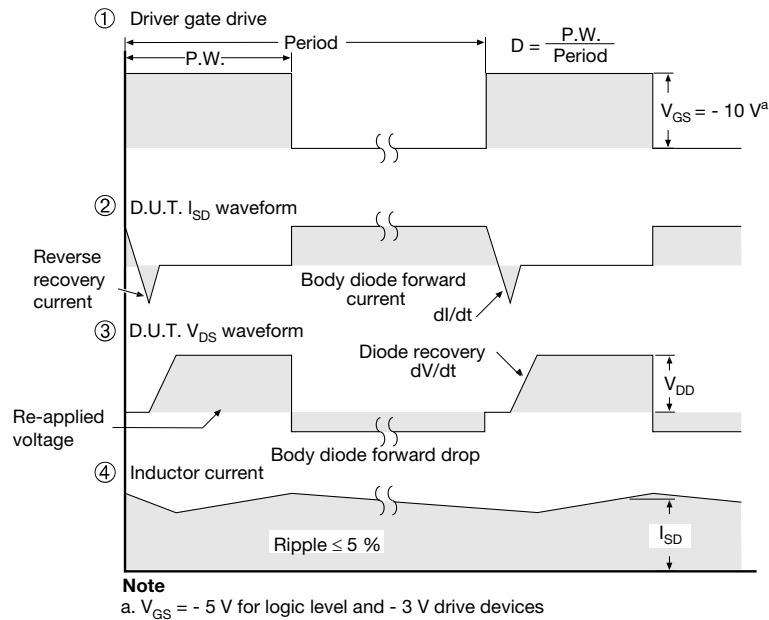
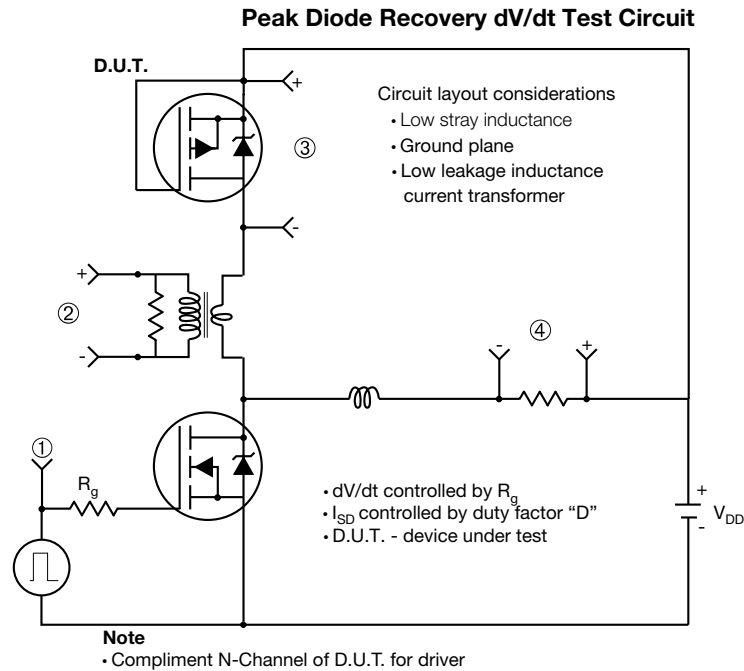
Fig. 12c - Maximum Avalanche Energy vs. Drain Current



Fig. 13a - Maximum Avalanche Energy vs. Drain Current



Fig. 13b - Gate Charge Test Circuit



**Fig. 14 - For P-Channel**

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### TO-263AB (HIGH VOLTAGE)



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.06	4.83	0.160	0.190
A1	0.00	0.25	0.000	0.010
b	0.51	0.99	0.020	0.039
b1	0.51	0.89	0.020	0.035
b2	1.14	1.78	0.045	0.070
b3	1.14	1.73	0.045	0.068
c	0.38	0.74	0.015	0.029
c1	0.38	0.58	0.015	0.023
c2	1.14	1.65	0.045	0.065
D	8.38	9.65	0.330	0.380

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D1	6.86	-	0.270	-
E	9.65	10.67	0.380	0.420
E1	6.22	-	0.245	-
e	2.54 BSC		0.100 BSC	
H	14.61	15.88	0.575	0.625
L	1.78	2.79	0.070	0.110
L1	-	1.65	-	0.066
L2	-	1.78	-	0.070
L3	0.25 BSC		0.010 BSC	
L4	4.78	5.28	0.188	0.208

ECN: S-82110-Rev. A, 15-Sep-08  
DWG: 5970

#### Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions are shown in millimeters (inches).
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body at datum A.
4. Thermal PAD contour optional within dimension E, L1, D1 and E1.
5. Dimension b1 and c1 apply to base metal only.
6. Datum A and B to be determined at datum plane H.
7. Outline conforms to JEDEC outline to TO-263AB.



**RECOMMENDED MINIMUM PADS FOR D<sup>2</sup>PAK: 3-Lead**



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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