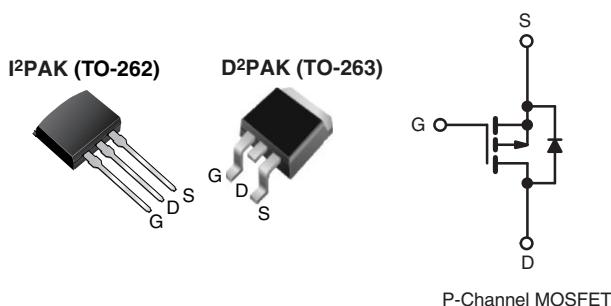


Power MOSFET

PRODUCT SUMMARY		
V _{DS} (V)	- 60	
R _{DS(on)} (Ω)	V _{GS} = - 10 V	0.14
Q _g (Max.) (nC)		34
Q _{gs} (nC)		9.9
Q _{gd} (nC)		16
Configuration		Single

FEATURES

- Halogen-free According to IEC 61249-2-21
- Definition
- Advanced Process Technology
- Surface Mount (IRF9Z34S, SiHF9Z34S)
- Low-Profile Through-Hole (IRF9Z34L, SiHF9Z34L)
- 175 °C Operating Temperature
- Fast Switching
- P-Channel
- Fully Avalanche Rated
- Compliant to RoHS Directive 2002/95/EC



DESCRIPTION

Third generation Power MOSFETs from Vishay utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The D²PAK is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D²PAK is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0 W in a typical surface mount application.

The through-hole version (IRF9Z34L, SiHF9Z34L) is available for low-profile applications.

ORDERING INFORMATION

Package	D ² PAK (TO-263)	D ² PAK (TO-263)	D ² PAK (TO-263)	I ² PAK (TO-262)
Lead (Pb)-free and Halogen-free	SiHF9Z34S-GE3	SiHF9Z34STR-GE3 ^a	SiHF9Z34STRR-GE3 ^a	-
Lead (Pb)-free	IRF9Z34SPbF	IRF9Z34STRLPbF ^a	IRF9Z34STRRPbF ^a	IRF9Z34LPbF
	SiHF9Z34S-E3	SiHF9Z34STL-E3 ^a	SiHF9Z34STR-E3 ^a	SiHF9Z34L-E3

Note

a. See device orientation.

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V _{DS}	- 60	V
Gate-Source Voltage	V _{GS}	± 20	
Continuous Drain Current	V _{GS} at - 10 V	I _D	A
		- 18	
Pulsed Drain Current ^{a, e}	T _C = 25 °C	- 13	A
		- 72	
Linear Derating Factor		0.59	W/°C
Single Pulse Avalanche Energy ^{b, e}	E _{AS}	370	mJ
Avalanche Current ^a	I _{AR}	- 18	A
Repetitive Avalanche Energy ^a	E _{AR}	8.8	mJ
Maximum Power Dissipation	T _C = 25 °C	P _D	W
		3.7	
Peak Diode Recovery dV/dt ^{c, e}	dV/dt	- 4.5	V/ns
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to + 175	°C
Soldering Recommendations (Peak Temperature)	for 10 s	300 ^d	

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

b. V_{DD} = - 25 V, starting T_J = 25 °C, L = 1.3 mH, R_G = 25 Ω, I_{AS} = - 18 A (see fig. 12).

c. I_{SD} ≤ - 18 A, dI/dt ≤ 170 A/μs, V_{DD} ≤ V_{DS}, T_J ≤ 175 °C.

d. 1.6 mm from case.

e. Uses IRF9Z34, SiHF9Z34 data and test conditions.

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient (PCB Mounted, steady-state) ^a	R _{thJA}	-	40	°C/W
Maximum Junction-to-Case (Drain)	R _{thJC}	-	1.7	

Note

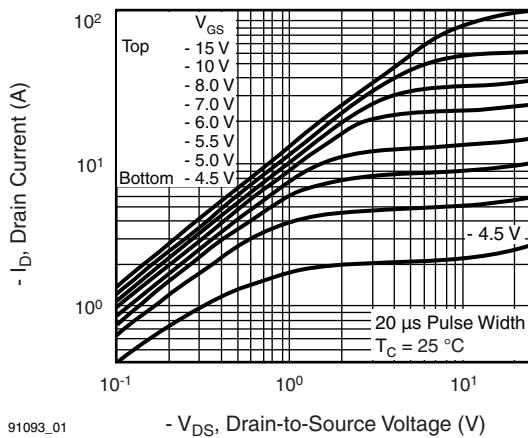
- a. When mounted on 1" square PCB (FR-4 or G-10 material).

SPECIFICATIONS ($T_J = 25$ °C, unless otherwise noted)

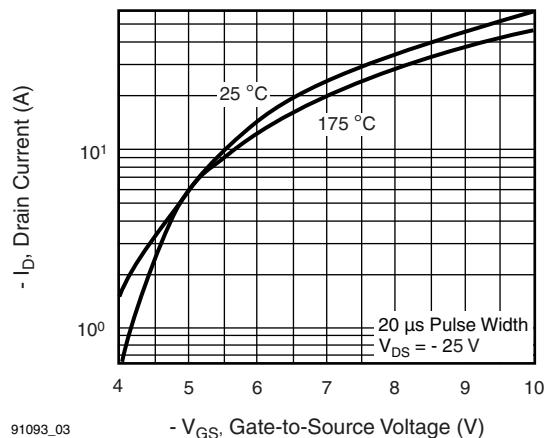
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = - 250 μA		- 60	-	-	V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = - 1 mA ^c		-	- 0.06	-	V/°C
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = - 250 μA		- 2.0	-	- 4.0	V
Gate-Source Leakage	I _{GSS}	V _{GS} = ± 20 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DS}	V _{DS} = - 60 V, V _{GS} = 0 V		-	-	- 100	μA
		V _{DS} = - 48 V, V _{GS} = 0 V, T _J = 150 °C		-	-	- 500	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = - 10 V	I _D = - 11 A ^b	-	-	0.14	Ω
Forward Transconductance	g _{fs}	V _{DS} = - 25 V, I _D = - 11 A ^c		5.9	-	-	S
Dynamic							
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = - 25 V, f = 1.0 MHz, see fig. 5 ^c		-	1100	-	pF
Output Capacitance	C _{oss}			-	620	-	
Reverse Transfer Capacitance	C _{rss}			-	100	-	
Total Gate Charge	Q _g	V _{GS} = - 10 V I _D = - 18 A, V _{DS} = - 48 V, see fig. 6 and 13 ^{b, c}		-	-	34	nC
Gate-Source Charge	Q _{gs}			-	-	9.9	
Gate-Drain Charge	Q _{gd}			-	-	16	
Turn-On Delay Time	t _{d(on)}			-	18	-	ns
Rise Time	t _r	V _{DD} = - 30 V, I _D = - 18 A, R _g = 12 Ω, R _D = 1.5 Ω, see fig. 10 ^{b, c}		-	120	-	
Turn-Off Delay Time	t _{d(off)}			-	20	-	
Fall Time	t _f			-	58	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	- 18	A
Pulsed Diode Forward Current ^a	I _{SM}			-	-	- 72	
Body Diode Voltage	V _{SD}	T _J = 25 °C, I _S = - 18 A, V _{GS} = 0 V ^b		-	-	- 6.3	V
Body Diode Reverse Recovery Time	t _{rr}	T _J = 25 °C, I _F = - 18 A, dI/dt = 100 A/μs ^{b, c}		-	100	200	ns
Body Diode Reverse Recovery Charge	Q _{rr}			-	280	520	nC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)					

Notes

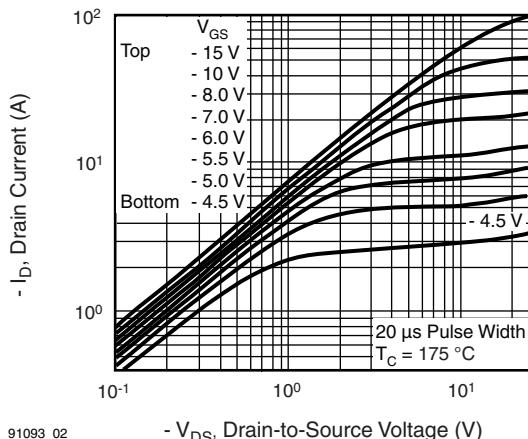
- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Pulse width ≤ 300 μs; duty cycle ≤ 2 %.
c. Uses IRF9Z34, SiHF9Z34 data and test conditions.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)


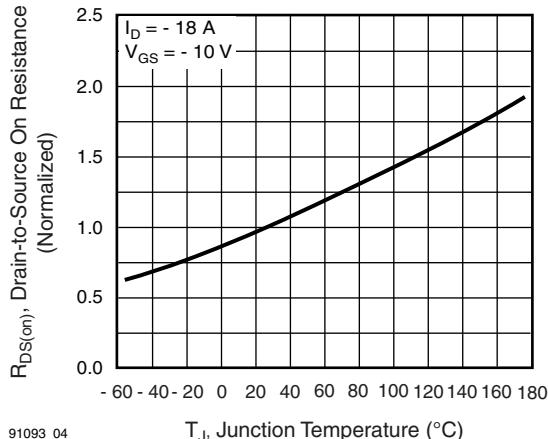
91093_01

- V_{DS} , Drain-to-Source Voltage (V)

91093_03

- V_{GS} , Gate-to-Source Voltage (V)**Fig. 1 - Typical Output Characteristics****Fig. 3 - Typical Transfer Characteristics**

91093_02

- V_{DS} , Drain-to-Source Voltage (V)

91093_04

- T_J , Junction Temperature (°C)**Fig. 2 - Typical Output Characteristics****Fig. 4 - Normalized On-Resistance vs. Temperature**

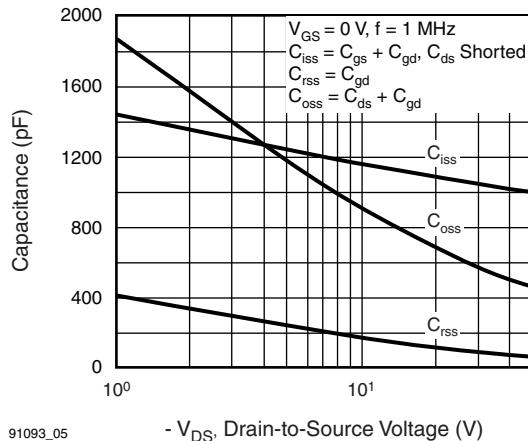


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

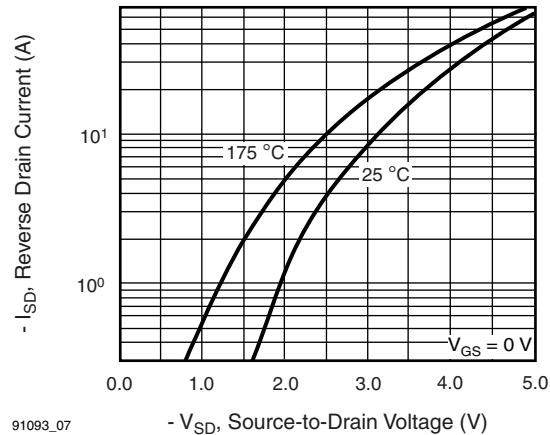


Fig. 7 - Typical Source-Drain Diode Forward Voltage

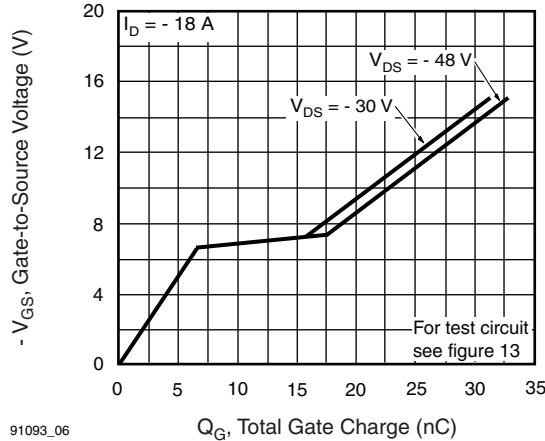


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

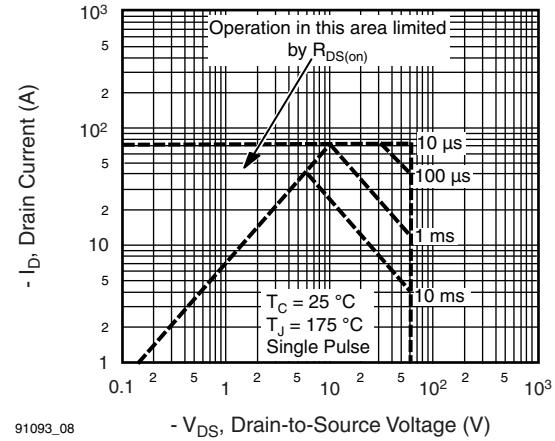
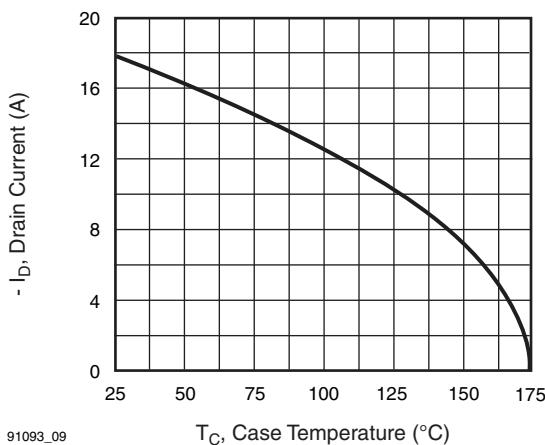


Fig. 8 - Maximum Safe Operating Area



91093_09

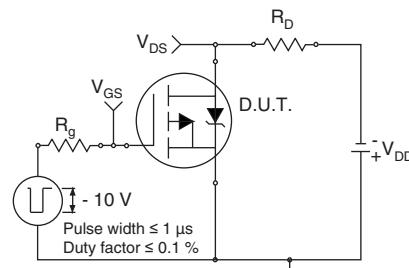


Fig. 10a - Switching Time Test Circuit

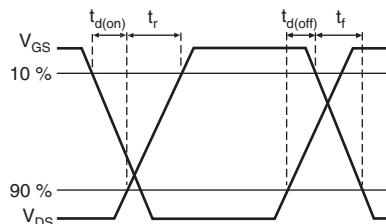
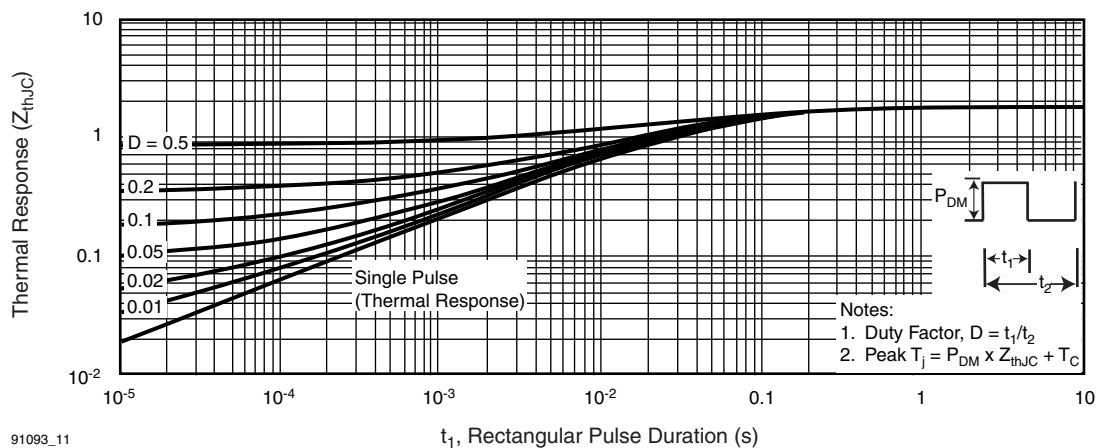


Fig. 10b - Switching Time Waveforms



91093_11

Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

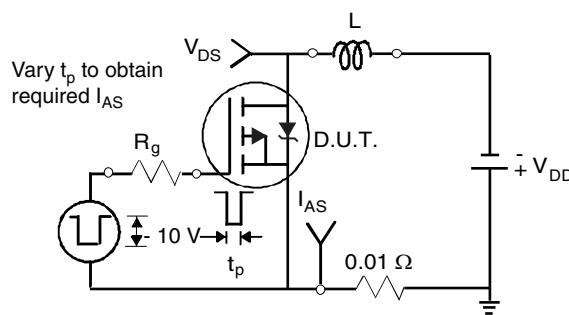


Fig. 12a - Unclamped Inductive Test Circuit

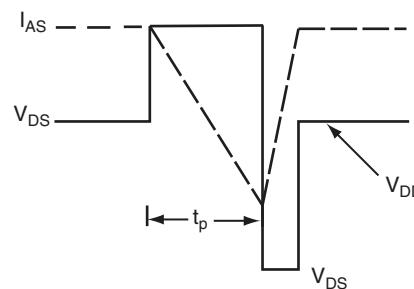


Fig. 12b - Unclamped Inductive Waveforms

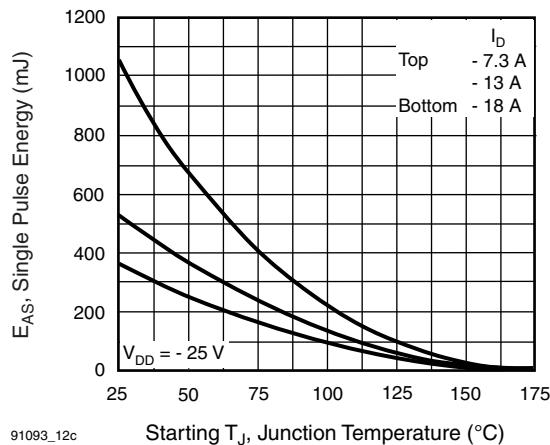


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

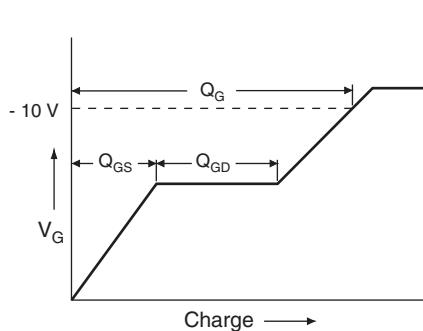


Fig. 13a - Maximum Avalanche Energy vs. Drain Current

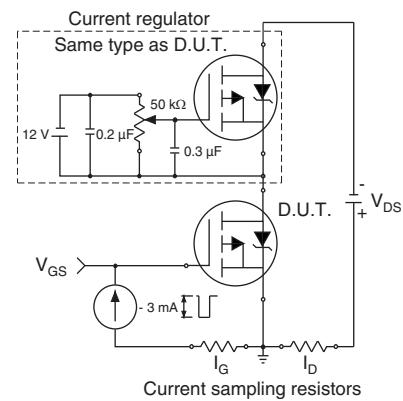
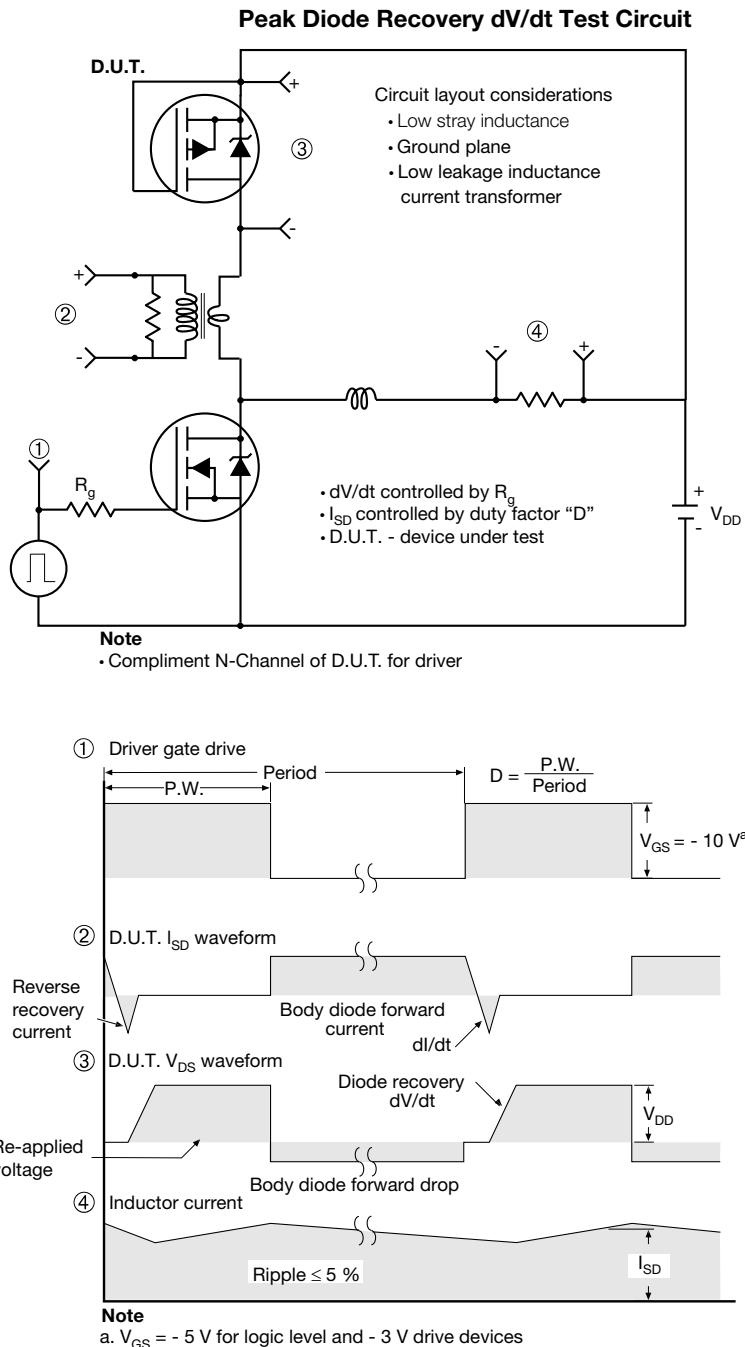


Fig. 13b - Gate Charge Test Circuit


Fig. 14 - For P-Channel

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data see www.vishay.com/ppg?291093.

TO-263AB (HIGH VOLTAGE)



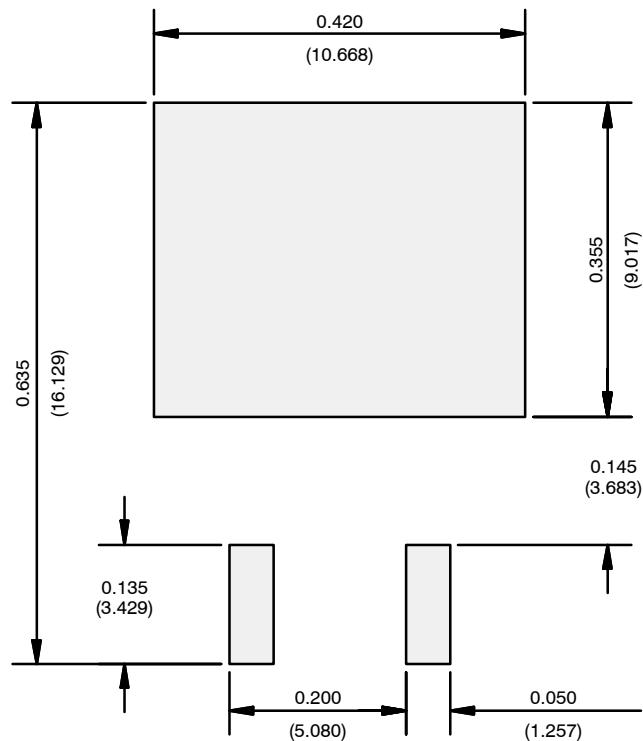
DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.06	4.83	0.160	0.190
A1	0.00	0.25	0.000	0.010
b	0.51	0.99	0.020	0.039
b1	0.51	0.89	0.020	0.035
b2	1.14	1.78	0.045	0.070
b3	1.14	1.73	0.045	0.068
c	0.38	0.74	0.015	0.029
c1	0.38	0.58	0.015	0.023
c2	1.14	1.65	0.045	0.065
D	8.38	9.65	0.330	0.380

ECN: S-82110-Rev. A, 15-Sep-08
DWG: 5970

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D1	6.86	-	0.270	-
E	9.65	10.67	0.380	0.420
E1	6.22	-	0.245	-
e	2.54 BSC		0.100 BSC	
H	14.61	15.88	0.575	0.625
L	1.78	2.79	0.070	0.110
L1	-	1.65	-	0.066
L2	-	1.78	-	0.070
L3	0.25 BSC		0.010 BSC	
L4	4.78	5.28	0.188	0.208

Notes

- Dimensioning and tolerancing per ASME Y14.5M-1994.
- Dimensions are shown in millimeters (inches).
- Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body at datum A.
- Thermal PAD contour optional within dimension E, L1, D1 and E1.
- Dimension b1 and c1 apply to base metal only.
- Datum A and B to be determined at datum plane H.
- Outline conforms to JEDEC outline to TO-263AB.

RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead

Recommended Minimum Pads
Dimensions in Inches/(mm)

[Return to Index](#)



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Please note that some Vishay documentation may still make reference to RoHS Directive 2002/95/EC. We confirm that all the products identified as being compliant to Directive 2002/95/EC conform to Directive 2011/65/EU.

Vishay Intertechnology, Inc. hereby certifies that all its products that are identified as Halogen-Free follow Halogen-Free requirements as per JEDEC JS709A standards. Please note that some Vishay documentation may still make reference to the IEC 61249-2-21 definition. We confirm that all the products identified as being compliant to IEC 61249-2-21 conform to JEDEC JS709A standards.



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- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
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- Техническая поддержка проекта, помошь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

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- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



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