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GaAs PHEMT MMIC POWER AMPLIFIER, DC - 15 GHz

Typical Applications

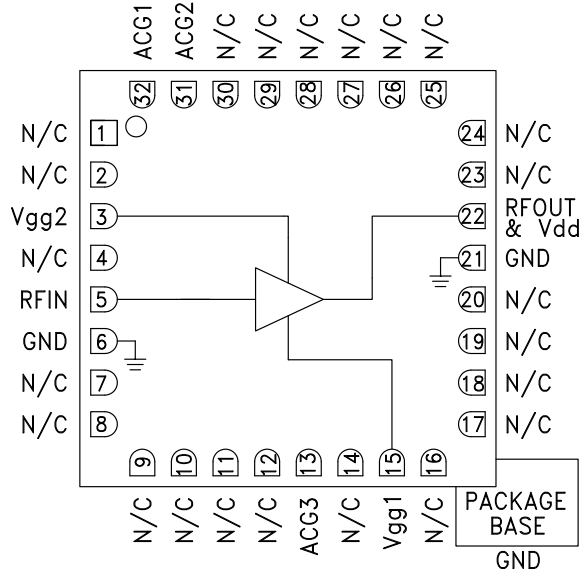
The HMC659LC5 wideband PA is ideal for:

- Telecom Infrastructure
- Microwave Radio & VSAT
- Military & Space
- Test Instrumentation
- Fiber Optics

Features

- P1dB Output Power: +27.5 dBm
- Gain: 19 dB
- Output IP3: +35 dBm
- Supply Voltage: +8V @ 300 mA
- 50 Ohm Matched Input/Output
- 32 Lead Ceramic 5 x 5 mm SMT Package: 25 mm²

Functional Diagram



General Description

The HMC659LC5 is a GaAs MMIC pHEMT Distributed Power Amplifier which is housed in a leadless 5 x 5 mm RoHS compliant ceramic SMT package operating between DC and 15 GHz. The amplifier provides 19 dB of gain, +35 dBm output IP3 and +27.5 dBm of output power at 1 dB gain compression, while requiring 300mA from a +8V supply. Gain flatness is excellent at ± 1.4 dB from DC - 15 GHz making the HMC659LC5 ideal for EW, ECM, Radar and test equipment applications. The HMC659LC5 amplifier I/Os are internally matched to 50 Ohms with no external components. The HMC659LC5 is compatible with high volume surface mount manufacturing techniques.

Electrical Specifications, $T_A = +25^\circ\text{C}$, $V_{dd} = +8\text{V}$, $V_{gg2} = +3\text{V}$, $I_{dd} = 300\text{ mA}$ *

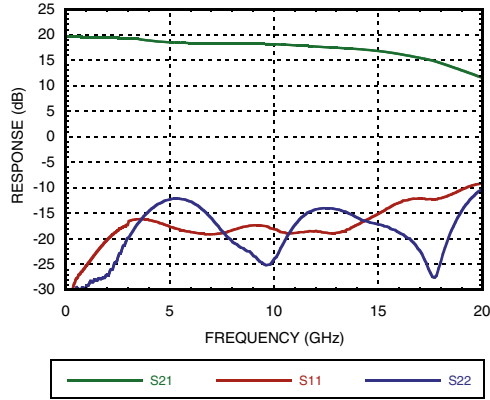
| Parameter | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | Units |
|---|--------|-----------|------|--------|-----------|------|---------|-----------|------|-------|
| Frequency Range | DC - 6 | | | 6 - 11 | | | 11 - 15 | | | GHz |
| Gain | 16 | 19 | | 15 | 18 | | 14 | 17 | | dB |
| Gain Flatness | | ± 0.7 | | | ± 0.4 | | | ± 0.7 | | dB |
| Gain Variation Over Temperature | | 0.015 | | | 0.019 | | | 0.022 | | dB/°C |
| Input Return Loss | | 20 | | | 18 | | | 17 | | dB |
| Output Return Loss | | 19 | | | 20 | | | 15 | | dB |
| Output Power for 1 dB Compression (P1dB) | 23.5 | 26.5 | | 24.5 | 27.5 | | 23.5 | 26.5 | | dBm |
| Saturated Output Power (P _{sat}) | | 28.0 | | | 28.5 | | | 27.5 | | dBm |
| Output Third Order Intercept (IP3) | | 35 | | | 32 | | | 29 | | dBm |
| Noise Figure | | 3.0 | | | 2.5 | | | 3.5 | | dB |
| Supply Current (I _{dd}) (V _{dd} = 8V, V _{gg1} = -0.8V Typ.) | | 300 | | | 300 | | | 300 | | mA |

*Adjust V_{gg1} between -2 to 0V to achieve I_{dd}= 300 mA typical.

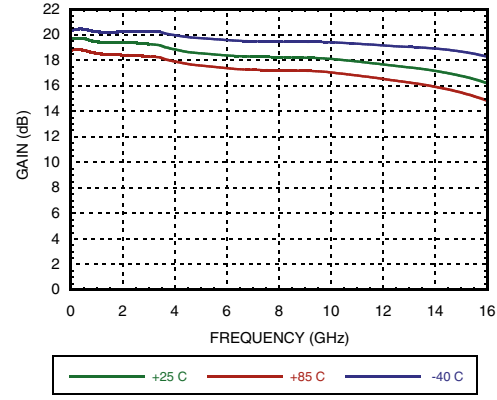


**GaAs PHEMT MMIC
POWER AMPLIFIER, DC - 15 GHz**

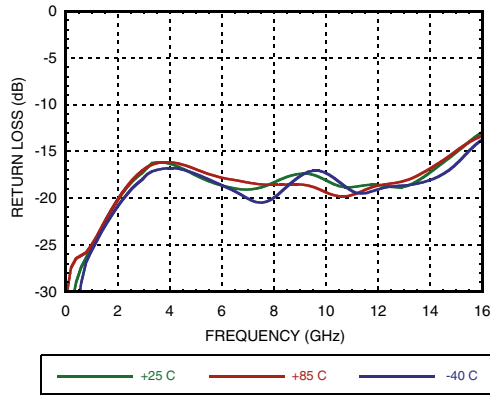
Gain & Return Loss



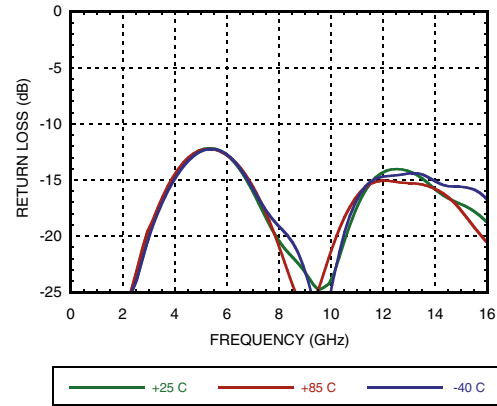
Gain vs. Temperature



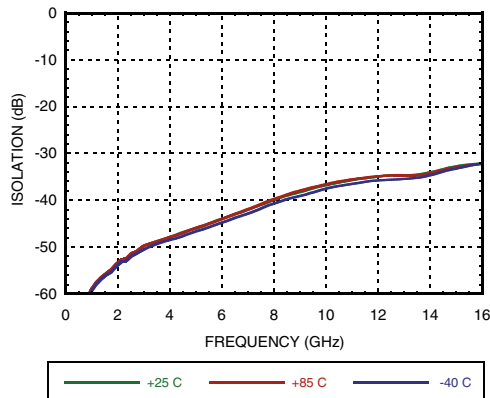
Input Return Loss vs. Temperature



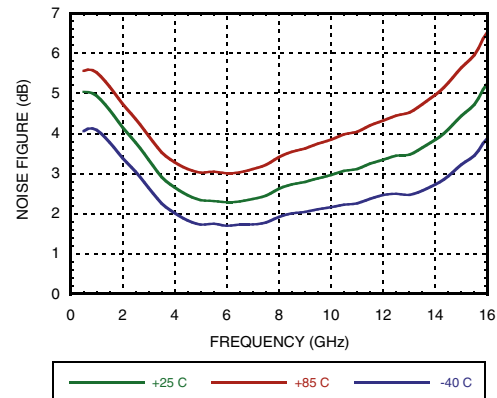
Output Return Loss vs. Temperature



Reverse Isolation vs. Temperature



Noise Figure vs. Temperature

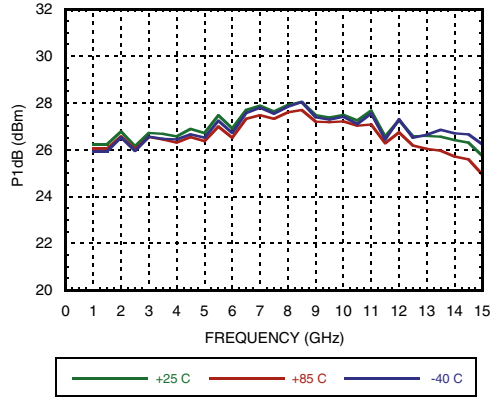




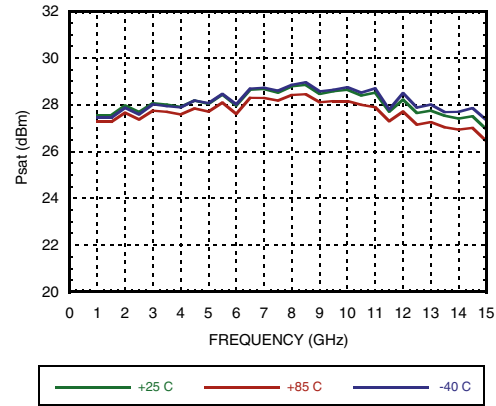
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LINEAR & POWER AMPLIFIERS - SMT

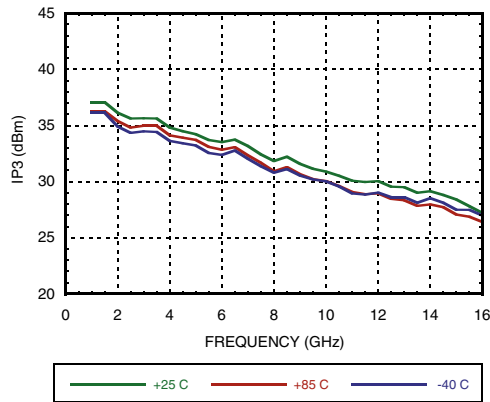
Output P1dB vs. Temperature



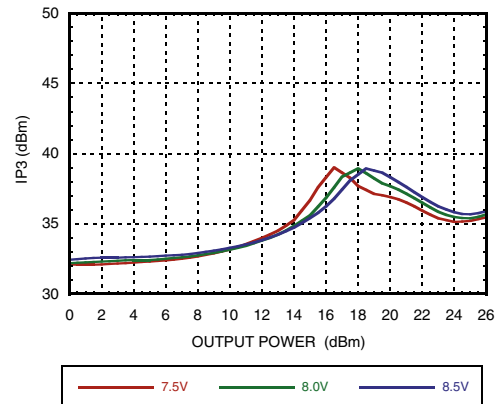
Psat vs. Temperature



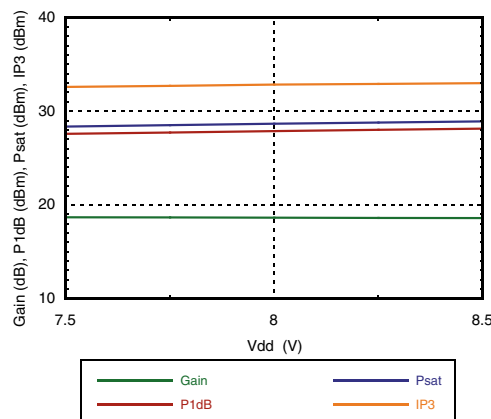
Output IP3 vs. Temperature



Output IP3 vs. Output Power @ 5GHz



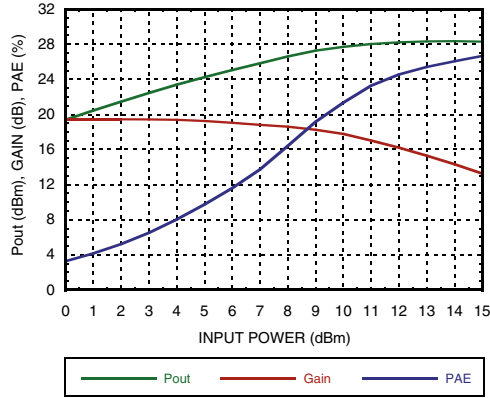
**Gain, Power & Output IP3 vs.
Supply Voltage @ 7 GHz, Fixed Vgg**



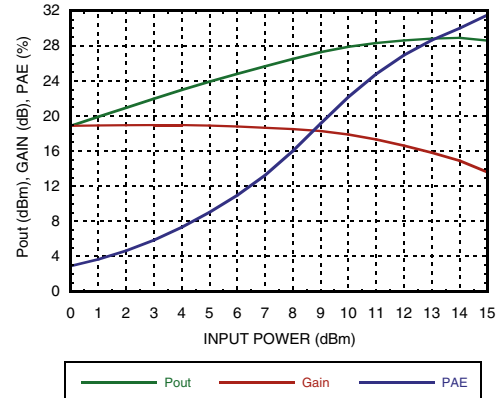


GaAs PHEMT MMIC POWER AMPLIFIER, DC - 15 GHz

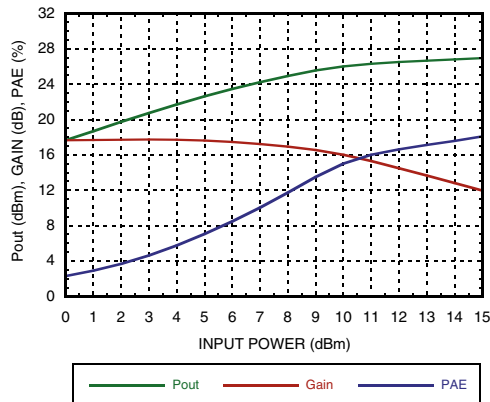
Power Compression @ 2 GHz



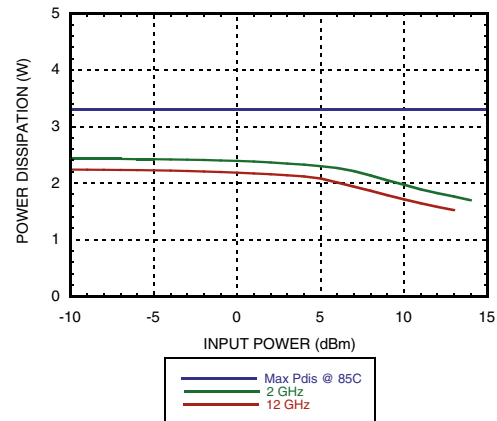
Power Compression @ 7 GHz



Power Compression @ 15 GHz



Power Dissipation



Absolute Maximum Ratings

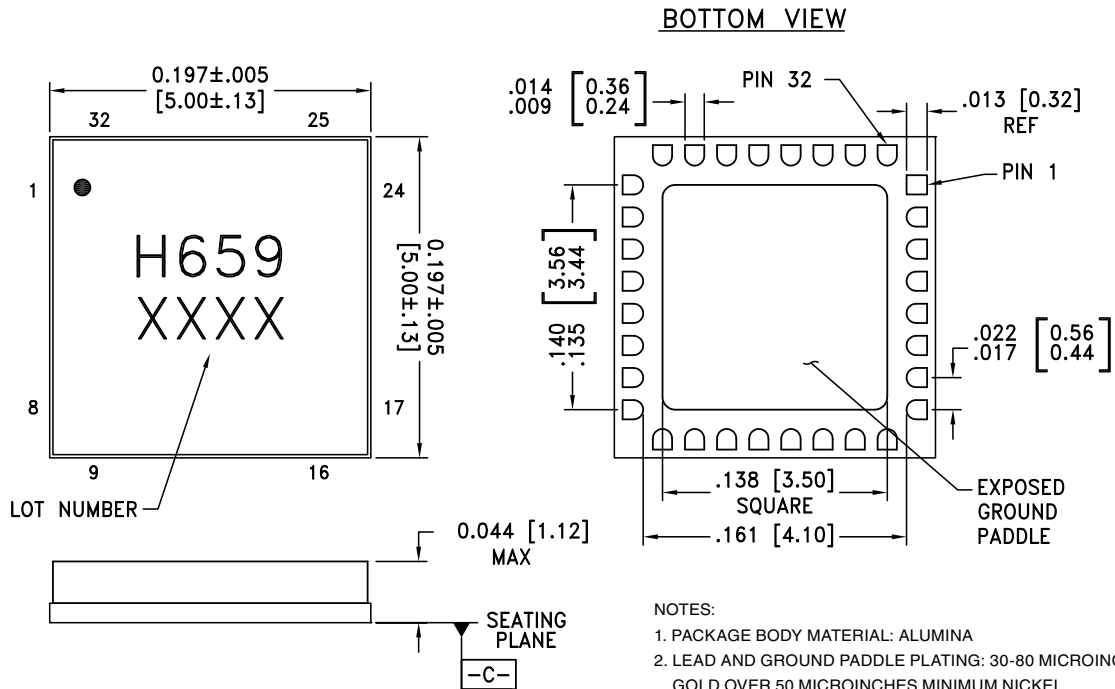
| | |
|--|---------------|
| Drain Bias Voltage (Vdd) | 9 Vdc |
| Gate Bias Voltage (Vgg1) | -2 to 0 Vdc |
| Gate Bias Voltage (Vgg2) | +2V to +4V |
| RF Input Power (RFIN)(Vdd = +8 Vdc) | +20 dBm |
| Channel Temperature | 175 °C |
| Continuous Pdiss (T= 85 °C) (derate 37 mW/°C above 85 °C) | 3.3 W |
| Thermal Resistance (channel to ground paddle) | 27.3 °C/W |
| Storage Temperature | -65 to 150 °C |
| Operating Temperature | -40 to 85 °C |
| ESD Sensitivity (HBM) | Class 1A |

Typical Supply Current vs. Vdd

| Vdd (V) | Idd (mA) |
|---------|----------|
| 7.5 | 299 |
| 8.0 | 300 |
| 8.5 | 301 |



**ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS**

Outline Drawing

NOTES:

1. PACKAGE BODY MATERIAL: ALUMINA
2. LEAD AND GROUND PADDLE PLATING: 30-80 MICROINCHES GOLD OVER 50 MICROINCHES MINIMUM NICKEL.
3. DIMENSIONS ARE IN INCHES [MILLIMETERS].
4. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
5. CHARACTERS TO BE LASER MARKED WITH .018" MIN to .030" MAX HEIGHT REQUIREMENTS. UTILIZE MAXIMUM CHARACTER HEIGHT BASED ON LID DIMENSIONS AND BEST FIT. LOCATE APPROX. AS SHOWN.
6. PACKAGE WARP SHALL NOT EXCEED 0.05 mm DATUM -C-
7. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.

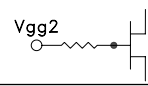
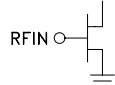
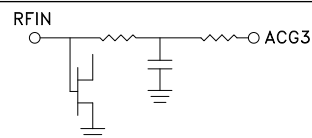
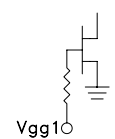
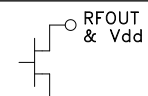
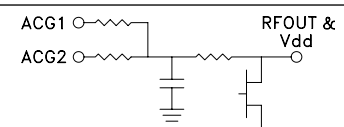

Package Information

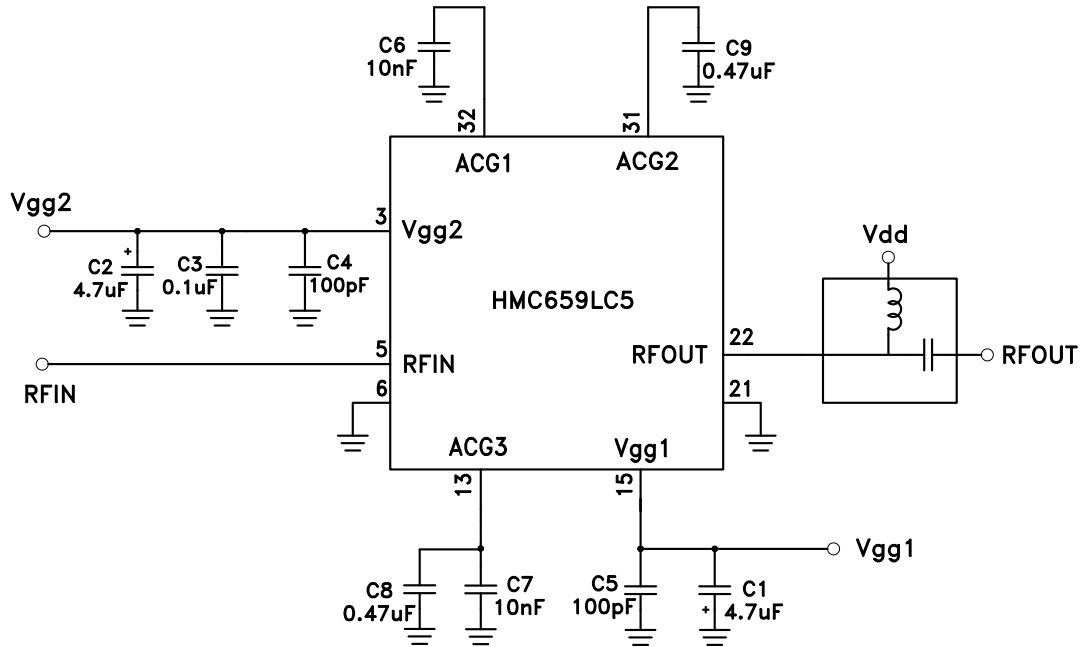
| Part Number | Package Body Material | Lead Finish | MSL Rating | Package Marking ^[2] |
|-------------|-----------------------|------------------|---------------------|--------------------------------|
| HMC659LC5 | Alumina, White | Gold over Nickel | MSL3 ^[1] | H659 XXXX |

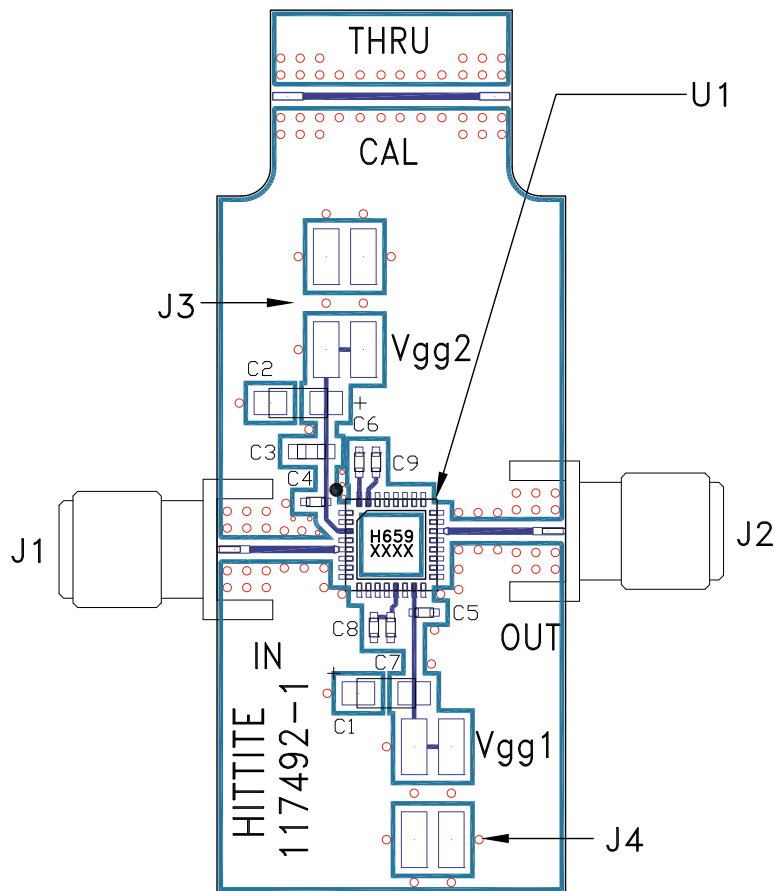
[1] Max peak reflow temperature of 260 °C

[2] 4-Digit lot number XXXX


Pin Descriptions

| Pin Number | Function | Description | Interface Schematic |
|---------------------------------------|-------------|--|---|
| 1, 2, 4, 7 - 12, 14, 16 - 20, 23 - 30 | N/C | No connection. These pins may be connected to RF ground. Performance will not be affected. | |
| 3 | Vgg2 | Gate Control 2 for amplifier. +3V should be applied to Vgg2 for nominal operation. |  |
| 5 | RFIN | This pad is DC coupled and matched to 50 Ohms. |  |
| 13 | ACG3 | Low frequency termination. Attach bypass capacitor per application circuit herein. |  |
| 15 | Vgg1 | Gate Control 1 for amplifier. |  |
| 22 | RFOUT & Vdd | RF output for amplifier. Connect the DC bias (Vdd) network to provide drain current (Idd). See application circuit herein. |  |
| 31 | ACG2 | Low frequency termination. Attach bypass capacitor per application circuit herein. |  |
| 32 | ACG1 | | |
| 6, 21 Ground Paddle | GND | Ground paddle must be connected to RF/DC ground. |  |

Application Circuit


Evaluation PCB

List of Materials for Evaluation PCB 117494 [1]

| Item | Description |
|---------|----------------------------------|
| J1, J2 | SMA-SRI-NS |
| J3, J4 | 2 mm Molex Header |
| C1, C2 | 4.7 μ F Capacitor |
| C3 | 0.1 μ F Capacitor, 0603 Pkg. |
| C4, C5 | 100 pF Capacitor, 0402 Pkg. |
| C6, C7 | 10k pF Capacitor, 0402 Pkg. |
| C8, C9 | 0.47 μ F Capacitor, 0402 Pkg |
| U1 | HMC659LC5 |
| PCB [2] | 117492 Evaluation PCB |

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350

The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads and package bottom should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation board should be mounted to an appropriate heat sink. The evaluation circuit board shown is available from Hittite upon request.



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