PRELIMINARY

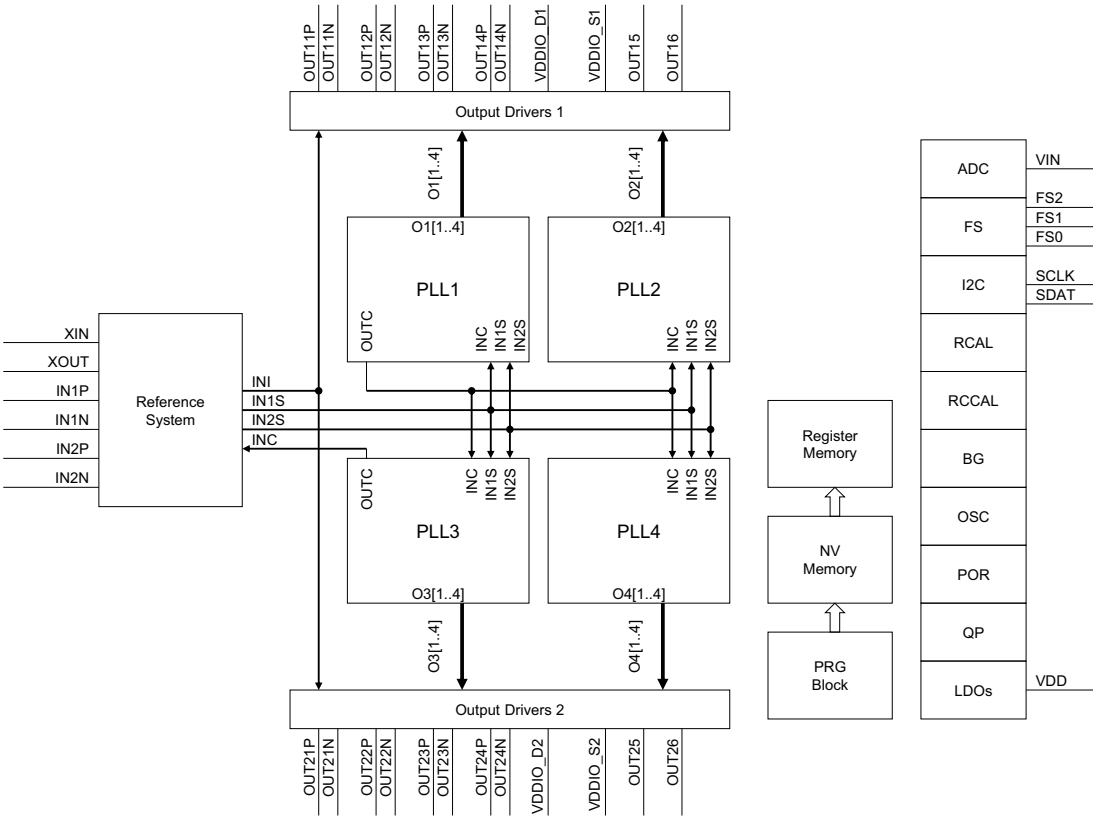
CY27410

4-PLL Spread-Spectrum Clock Generator

Features

- Input frequencies
  - Crystal input: 8 MHz to 48 MHz
  - Reference clock: 8 MHz to 250 MHz LVCMOS
  - Reference clock: 8 MHz to 700 MHz differential
- Output frequencies
  - 25 MHz to 700 MHz LVDS, LVPECL, HCSL, CML
  - 3 MHz to 250 MHz LVCMOS
  - 1 kHz to 8 MHz for one LVCMOS output
- RMS phase jitter: 1-ps max at 12-kHz to 20-MHz offset
- PCIe 1.0/2.0/3.0 compliant
- SATA 2.0, USB 2.0/3.0, 1/10-GbE compliant
- Maximum 12 outputs split in two banks of six outputs each.
  - Up to eight differential output pairs (HCSL, LVPECL, CML, or LVDS)
  - Up to 12 LVCMOS outputs
- Up to 75-ps skew for differential outputs within a bank
- Four fractional N-type phase-locked loops (PLLs) with
  - VCXO (±120 ppm with steps of 0.23 ppm)
  - Spread-spectrum capability (Logic SS and Lexmark profile 0.1% to 5% in 0.1% steps, down or center spread)
- Supply voltage: 1.8 V, 2.5 V, and 3.3 V
- Zero-delay buffer (ZDB) and non-zero delay buffer (NZDB) configurations
- I^2C configurable with onboard programming
- Industrial-grade device, offered in 48-pin QFN (7 × 7 × 1.0 mm) package

Logic Block Diagram



Contents

Functional Description

The CY27410 is a standard-performance programmable clock generator with four independent fractional PLLs, which generates any frequency with a zero-ppm synthesis error. Each PLL is followed by a set of four independent dividers to generate four different frequencies from a single PLL. All four dividers are synchronized to generate phase-aligned clock outputs with minimal skew. The PLLs also support the spread-spectrum feature to reduce EMI. All four PLLs are equipped with VCXO functionality to achieve ppm granularity of output frequency.

CY27410 is the master device with 12 outputs compared to CY27430 with 7, but the feature sets of the two devices are identical.

The CY27410 accepts a crystal clock or a single-ended/differential reference clock. The device supports up to 12 outputs, divided into two banks of six outputs each. Four outputs of PLL1 and PLL2 are multiplexed to output Bank1, and four clock outputs of PLL3 and PLL4 are multiplexed to output Bank2. The 12 outputs of the two banks are configurable as eight differential outputs, 12 single-ended outputs, or a combination of differential and single-ended outputs.

The CY27410 has an on-chip volatile and nonvolatile memory, composed of eight registers, which store the device configuration settings. These registers can be accessed and programmed onboard through the I^2C interface. You can also configure the device on-the-fly to completely reprogram the device on the application board. Besides the I^2C interface, external signals can be applied to multifunction pins for different functions such as the following:

- Dynamically change the output frequency
- Output enable/disable
- Power down
- Spread ON/OFF

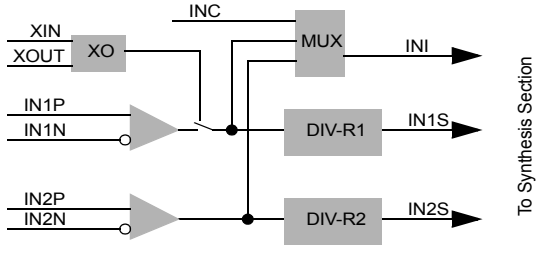
One low-frequency clock output, in kilohertz, is provided to meet the need of widely used reference frequencies, such as 32.768 kHz. The jitter specs of CY27410 make it an ideal choice for the following communication protocols: PCIe 1.0/2.0/3.0, USB 2.0/3.0, SATA 1.0/2.0, and 1/10GbE.

Input System

The input system supports the following (see Figure 1):

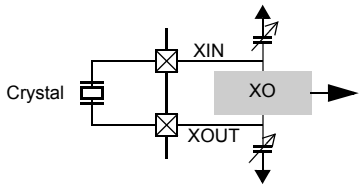
- XIN/XOUT supports crystal input.
- IN1 supports differential and single-ended clock inputs.
- IN2 supports differential and single-ended clock inputs.

Figure 1. Oscillator/Clock Input Block Diagram



If a crystal is used, XIN and XOUT are connected to a crystal oscillator to generate the required internal frequency, as shown in Figure 2. The supported differential tuning capacitor range is 8 pF to 12 pF. To do this, there are two banks of capacitors – one coarse and the other fine.

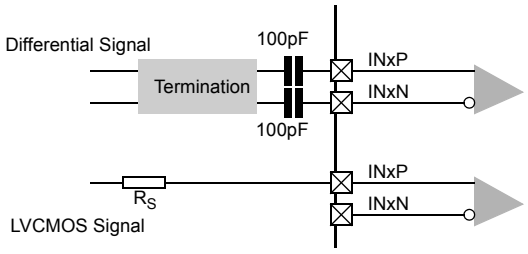
Figure 2. Connecting a Crystal



IN1 and IN2 are designed to accept either a single-ended or differential reference input. IN2 can be used to accept the feedback signal to implement the ZDB functionality of the device.

The differential inputs are capable of interfacing with multiple standards, such as LVPECL, LVDS, CML, and HCSL. The differential signals must be of AC-coupling, as shown in Figure 3.

Figure 3. Interfacing Differential and Single-Ended Signals



VCXO Input Block

The VIN input is used for the VCXO functionality of the device. In this functionality, the output can change with respect to an input voltage required for audio-visual applications. The output frequency can vary up to ±120 ppm. This input voltage directly controls the PLL1 fractional divider to provide the VCXO functionality.

Frequency Select Input

CY27410 supports frequency-select features with which the customer can change output frequencies on-the-fly. The device has eight configuration register sets, which can be preprogrammed or written through I^2C. Changing the signal level of the FS pins (high and low) selects the appropriate configuration registers and changes the output frequency accordingly.

I²C Block (SCLK, SDAT)

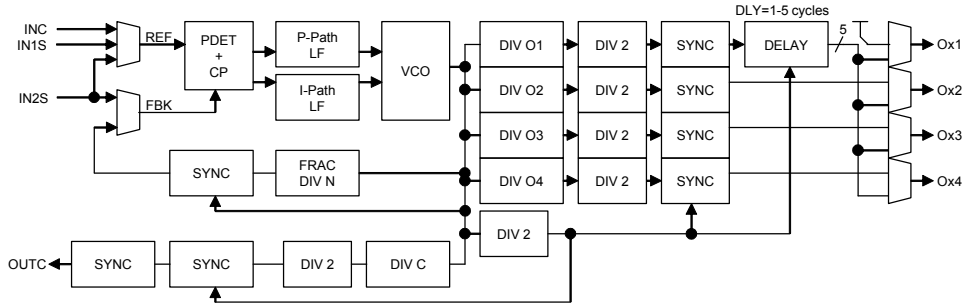
CY27410 supports I²C programming of internal registers, using which you can configure the device. CY27410 also supports user-profile programming to flash memory and allows partial updates. Read, Write, or Read/Write protection is also available. The device is compliant with the I²C-bus Specification, version 2.1 or later. The critical I²C specifications are as follows:

- 400 kb/s (Fast mode)
- 7-bit addressing support
- Selectable device address (programmable), default = 69 hex (7 bits)

Synthesis Section

CY27410 consists of four PLLs, which are the core synthesis blocks of the chip. Each PLL has a fractional N capability, which supports output frequency generation based on an input reference frequency to an accuracy of 100 ppb. The output of the PLL is fed into four dividers and then moves to synchronizers to generate glitch-free clock transition features, variable delay generation circuits to support the programmable delay feature, and so on. The output dividers and multiplexers are also included as part of this subsystem. All the four PLLs have the same architecture, as shown in Figure 4.

Figure 4. PLL Architecture



Output Section

CY27410 consists of two banks of outputs, which are located at the top and bottom of the device. Each bank consists of six outputs with OUT11–OUT14 and OUT21–OUT24 supporting both differential and single-ended outputs and OUT15–OUT16 and OUT25–OUT26 supporting only single-ended outputs.

Each output is fed from a PLL through a divider and then to a MUX, which helps in selecting the source for the output, as shown in Figure 5 and Figure 6.

Figure 5. Bank1 Outputs

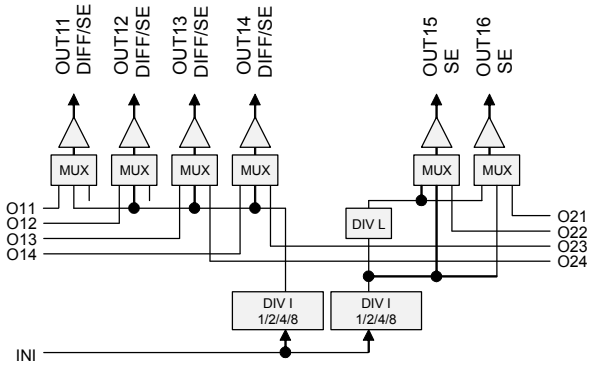
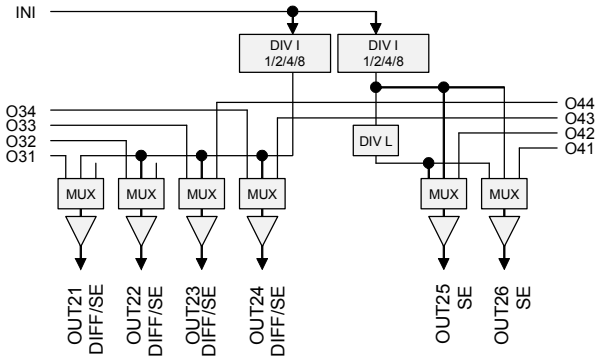


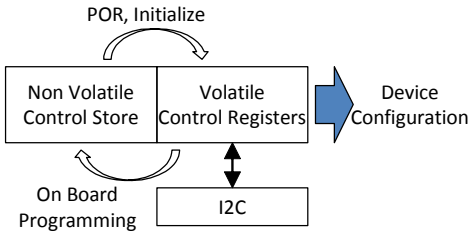
Figure 6. Bank2 Outputs



Onboard Programming

You can write the device memory on the customer board, enabling the use of a blank device that is not preprogrammed. This helps you to use the same device across multiple projects and lets you program the device based on individual projects. Conceptual onboard programming is shown in Figure 7.

Figure 7. Onboard Programming



Functional Features and Application Considerations

CY27410 is a 4-PLL spread-spectrum clock generator targeted at consumer, industrial, and low-end networking applications. The key specifications of the part are differential inputs (2) and outputs (12), supporting frequencies up to 700 MHz. The device has a low RMS phase jitter of 1-ps max and value-added features, such as VCXO, Frequency Select, and PLL Bypass modes. This part is designed to support key standards, such as PCIe 1.0/2.0/3.0, USB 2.0/3.0, and 10GbE.

The product supports LVDS, LVPECL, CML, HCSL, and LVCMOS logic levels.

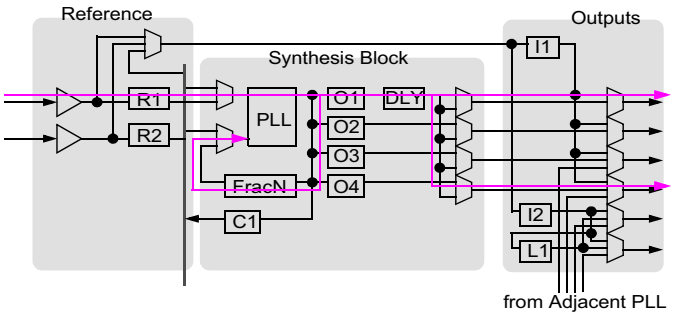
Clock Generator

The main feature of CY27410 is frequency generation from an external reference (IN1) or a crystal. There are four variables to determine the final output frequency. They are input REF, the DIV-R (R1), FracN (DIV-N) dividers, and the post dividers (DIV-O). The basic formula for determining the final output frequency is:

- Clock Generator mode
  - f_{OUT} = ((REF x DIV-N) / DIV-R) / DIV-O
- PLL Bypass mode
  - f_{OUT} = REF / DIV-I or REF / DIV-I / DIV-L

The basic PLL block diagram is shown in Figure 8. Each of the outputs from the PLL is fed to the output MUX through a Delay circuit that provides a certain delay to the individual clock, if needed.

Figure 8. PLL Block Diagram, Clock Generation



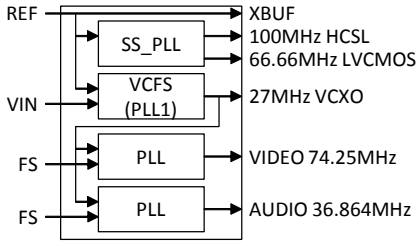
PCIE (HCSL) Clock Generation

For PCIe applications, CY27410 provides eight differential outputs that have the same spread on it at any particular point of time.

VCXO and Related Frequencies

CY27410 provides VCXO functionality and a cascading PLL option to generate critical frequencies with a fixed reference. Digital televisions have a requirement for the audio and video clocks to follow a 27-MHz VCXO signal so that they are synchronized. The architecture of the chip must ensure that this is met by cascading, as shown in Figure 9.

Figure 9. Cascading PLLs



Apart from having the audio and video clocks following the 27-MHz VCXO input, they also need complex divider ratios to generate the output frequencies. Commonly used divider ratios for audio and video signals are listed in Table 1.

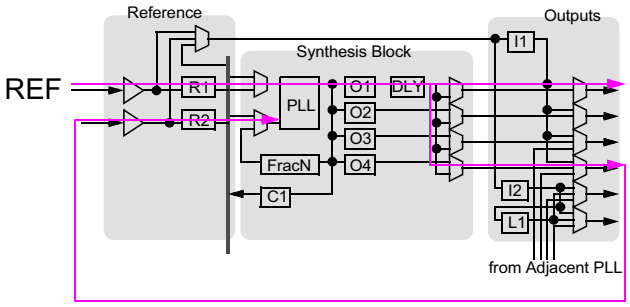
Table 1. Audio and Video Frequencies

Output Frequency	Ratios
74.17582418	91:250
33.8688	625:784
22.5792	1875:1568
16.9344	1250:784
11.2896	1875:784
5.6448	1875:392
36.864	375:512

Zero-Delay Buffer Functionality

CY27410 acts as a zero-delay buffer (ZDB) for one output from a single PLL block. To implement this feature, take one of the outputs and send it back as a feedback reference to the PLL. By providing a divider in the feedback loop, the device can also act as a frequency-multiplying ZDB (see Figure 10). This functionality is supported only when the PLL is in the integer N mode.

Figure 10. ZDB Configuration



CY27410 provides the frequency-multiplying ZDB by modulating the R1 and R2 values in the integer ratio. If both the values are identical, CY27410 acts as a simple ZDB.

Early/Late Output Phase

CY27410 supports a delay circuit in the divider to provide 0 to 5 × VCO/2 cycles. Therefore, an output has a certain lag phase or lead phase to other outputs when this feature is used. This functionality is also available in the ZDB mode and provides “early” phase or “delayed” phase to the Reference input. Refer to Figure 11 and Figure 12.

Figure 11. Early/Delayed Phase Output

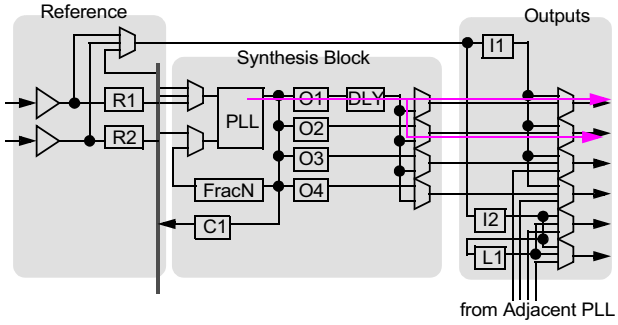
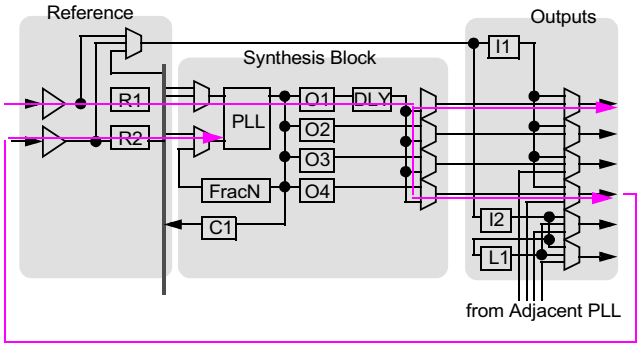


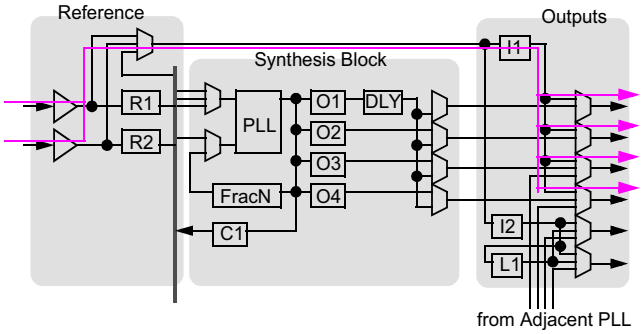
Figure 12. Early/Late Phase in ZDB Configuration



Non-Zero Delay Buffer

CY27410 supports the PLL-bypass mode, which bypasses the entire synthesis block to act as a configurable non-zero delay buffer (NZDB) with level translation and selectable inputs, as shown in Figure 13.

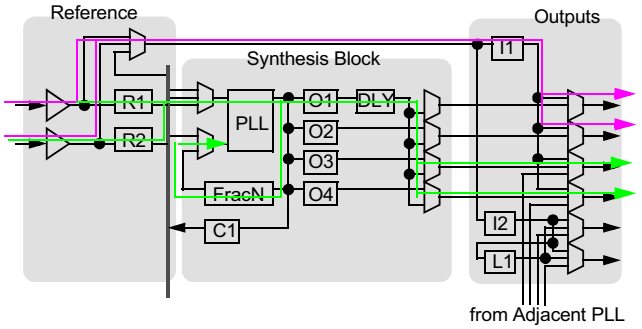
Figure 13. NZDB Configuration



Combination Clock Generator and Buffer

CY27410 provides a combination of a clock generator and a buffer in one device. This is achieved by configuring the input and output selectors for the desired split configuration. An example of such an application is shown in Figure 14.

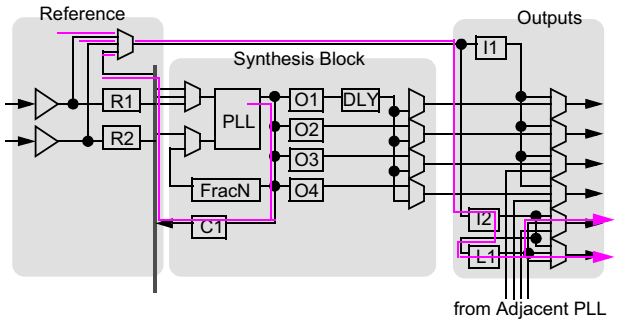
Figure 14. Clock Generator and NZDB



Low-Frequency Output

CY27410 integrates low-frequency generator counters for LVCMOS outputs that may be used for watchdog-time and/or kHz-order clocks for application, as shown in Figure 15.

Figure 15. Low-frequency Output Option



Spread Spectrum

To help reduce electromagnetic interference (EMI), CY27410 supports spread-spectrum modulation. The output clock frequencies can be modulated to spread energy across a broader range of frequencies and lower system EMI. CY27410 implements two types of spread profiles for modulation: linear and nonlinear.

The spread spectrum can be applied to any output clock, any frequency, and any spread amount ranging from 0.1% to 5% in 0.1% step. Center or down spread can be programmable.

The spread modulation rate is limited from 30 kHz to 60 kHz.

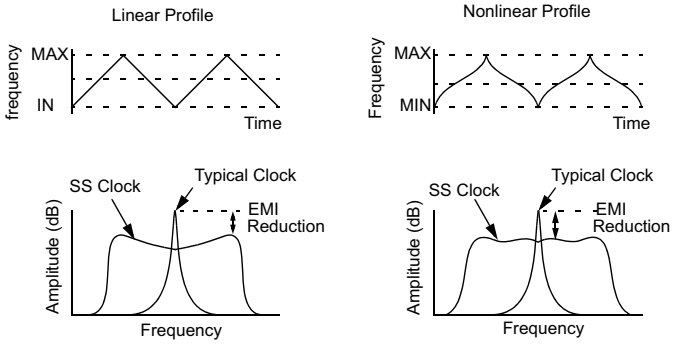
The spread spectrum is generated digitally in the FracN modulation, which means all the parameters are independent of process, voltage, and temperature variations. All the frequencies generating the same PLL have the same amount of modulation.

As shown in Figure 16, a harmonic of a modulated clock has a much lower amplitude than that of an unmodulated signal. The reduction in amplitude is dependent on the harmonic number and the frequency deviation or spread. The equation for the reduction in the nonlinear profile is:

$dB = 6.5 + 9 * \log_{10}(P) + 9 * \log_{10}(F)$

where P is the percentage of deviation and F is the frequency in megahertz where the reduction is measured.

Figure 16. Spread-Spectrum Profile



VCXO (VCFS) Functionality

CY27410 supports VCXO functionality without pulling the crystal frequency. This function is implemented by modulating the FracN counter according to the VIN level, as shown in Figure 17. Therefore, this is called voltage-controlled frequency shift (VCFS).

The VCFS function is implemented by modulating the FracN divider, which means all the parameters are independent of the process, voltage, and temperature variations.

It is not possible to combine the VCFS operation with spread spectrum (see Figure 18).

Figure 17. VCFS Profile

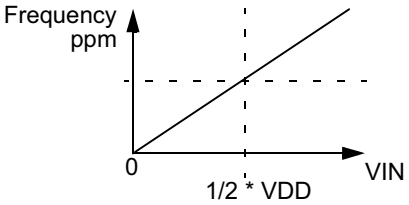
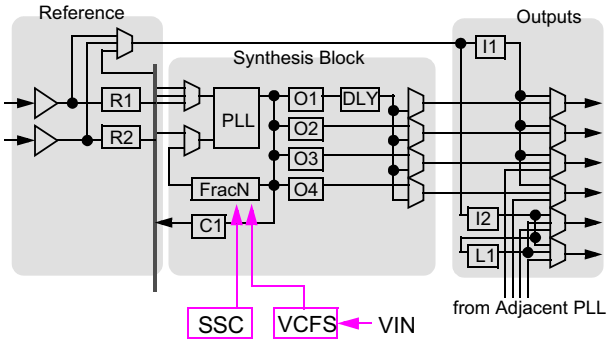


Figure 18. VCFS and Spread Spectrum



Crystal Oscillator

CY27410 supports various low-cost crystals as a reference oscillator at IN1 (XIN/XOUT) to generate multiple frequencies in a single chip. CY27410 supports a crystal with a nominal load capacitance specification from 8 pF to 12 pF. As shown in Figure 2 on page 3, CY27410 integrates all the components, such as a feedback resistor and tuning capacitor, to oscillate the clock with a particular crystal for the following specifications.

To enable proper operation, the crystal specification is divided into three ranges:

- Low range (F_{NOM}) = 8 to 12 MHz
- Midrange = 12 to 20 MHz
- High range = 20 to 48 MHz

The corresponding crystal parameters are listed in Table 2.

Table 2. Crystal Specifications

Range	Min Frequency (MHz)	Max Frequency (MHz)	Max R1 (ohms)	Max DL (uW)
Low	8	12	150	100
Mid	12	20	70	100
High	20	48	50	100

C_L (pF) for all Ranges	Associated Max C_0 (pF)
8	2
9	2
10	2
12	3

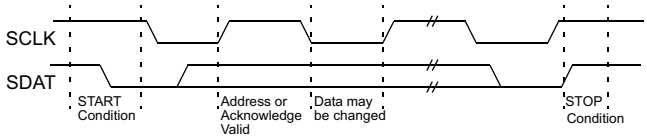
Serial Programming Interface Protocol

The CY27410 uses the SDAT and SCLK pins for a 2-wire serial interface that operates up to 400 Kb/s in Read and Write modes. It complies with the I^2C bus standard. The basic Write protocol is:

Start Bit; 7-bit Device Address; R/W Bit; Slave Clock Acknowledge (ACK); 8-bit Memory Address (MA); ACK; 8-bit Data; ACK; 8-bit Data in MA+1 if desired; ACK; 8-bit Data in MA+2; ACK; and more until STOP Bit.

The basic serial format is shown in Figure 19.

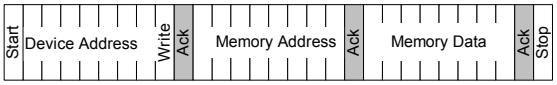
Figure 19. Data Transfer Sequence on the Serial Bus



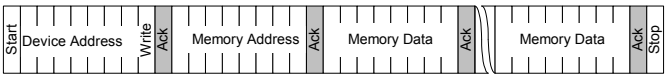
A valid write operation must have a full 8-bit register address after the device address word from the master, which is followed by an acknowledge bit from the slave (SDAT = 0/LOW). The next eight bits must contain the data word intended for storage. After the data word is received, the slave responds with another acknowledge bit (SDAT = 0/LOW), and the master must end the write sequence with a STOP condition (see Figure 20).

Figure 20. Data Frame Architecture (Write)

Random Write

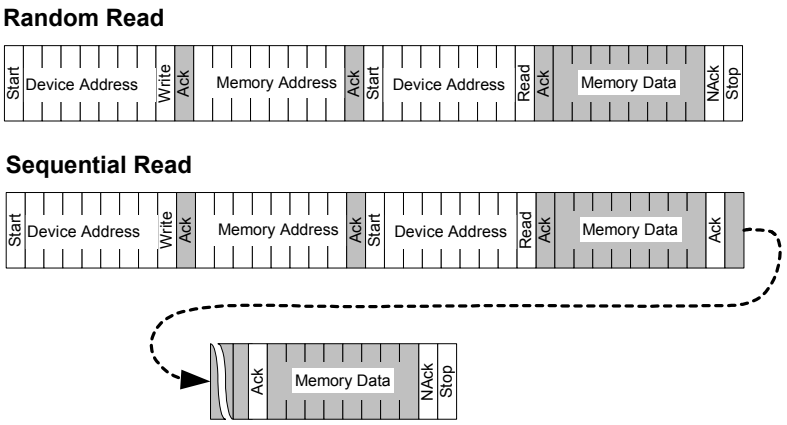


Sequential Write



Read operations are initiated the same way as write operations, except that the R/W bit of the slave address is set to '1' (HIGH). There are two basic read operations: random read and sequential read. Figure 21 illustrates these operations.

Figure 21. Data Frame Architecture (Read)



Through random read operations, the master may access any memory location. To perform this type of read operation, first set the word address. Send the address to CY27410 as part of a write operation. After the word address is sent, the master generates a START condition following the acknowledge. This terminates the write operation before any data is stored in the address, but not before the internal address pointer is set. Next, the master reissues the control byte with the R/W byte set to '1'.

Then, the CY27410 issues an acknowledge and transmits the 8-bit word. The master device does not acknowledge the transfer, but does generate a STOP condition, which causes the CY27410 to stop transmission.

Sequential read operations follow the same process as random reads, except that the master issues an acknowledge instead of a STOP condition after transmission of the first 8-bit data word. This action results in an incrementing of the internal address pointer, and subsequently output of the next 8-bit data word. By continuing to issue acknowledges instead of STOP conditions, the master may serially read the entire contents of the slave device memory.

Pinouts

The CY27410 devices are available in the 48-pin QFN package.

CY27410 Pinout

The CY27410 is the master product that has the maximum number of outputs (12) with all the features including VCXO, I^2C, and Frequency Select options.

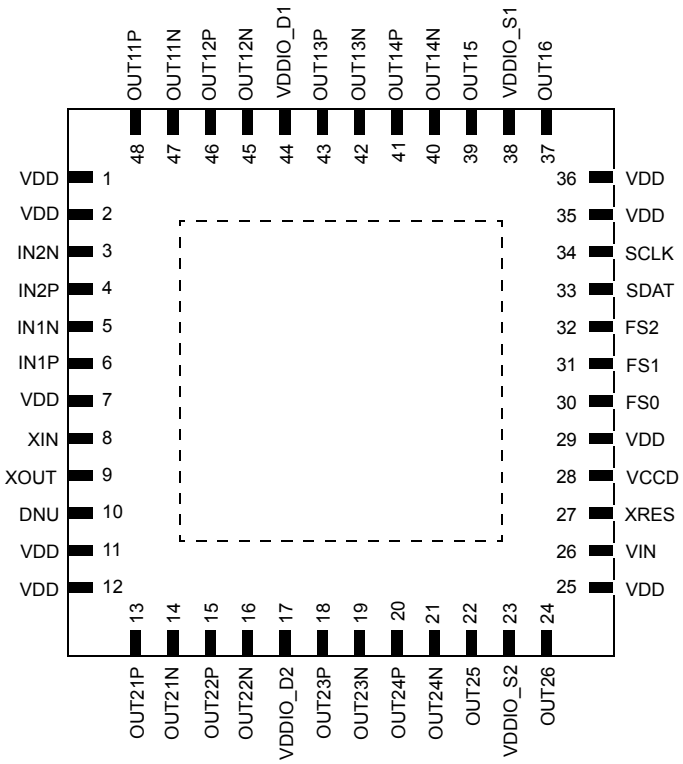
Table 3. 48-Pin QFN (CY27410) Pin Definitions

Name	I/O	Type	# of Pins	Pin #	Function
XIN	I	Crystal	1	8	XIN for crystal
XOUT	O	Crystal	1	9	XOUT for crystal
IN1P	I	LVCMOS/ Differential	1	6	True input for IN1 differential pair. IN1 for LVCMOS input. Need external series capacitor for differential input.
IN1N	I	Differential	1	5	Complement input for IN1 differential pair. None for LVCMOS input. Need external series capacitor for differential input.
IN2P	I	LVCMOS / Differential	1	4	Feedback input for ZDB mode. True input for IN2 differential pair. IN2 for LVCMOS input Need external series CAPS for differential input.
IN2N	I	Differential	1	3	Feedback input for ZDB mode. Complement input for IN2 differential pair. None for LVCMOS input. Need external series CAPS for differential input.
OUT15	O	LVCMOS	1	39	LVCMOS clock output 15
OUT16	O	LVCMOS	1	37	LVCMOS clock output 16
OUT11P	O	LVCMOS / Differential	1	48	Output 11 true output (differential) or Output 11 LVCMOS
OUT11N	O	Differential	1	47	Output 11 complement output (differential) connect to OUT11P for LVCMOS
OUT12P	O	LVCMOS / Differential	1	46	Output 12 true output (differential) or LVCMOS clock output 12
OUT12N	O	Differential	1	45	Output 12 complement output (differential) connect to OUT12P for LVCMOS
OUT13P	O	LVCMOS / Differential	1	43	Output 13 complement output (differential) or Output 13 LVCMOS
OUT13N	O	Differential	1	42	Output 13 complement output (differential) connect to OUT13P for LVCMOS
OUT14P	O	LVCMOS / Differential	1	41	Output 14 true output (differential) or Output 14 LVCMOS output
OUT14N	O	Differential	1	40	Output 14 complement output (differential) connect to OUT14P for LVCMOS
OUT21P	O	LVCMOS / Differential	1	13	Output 21 true output (differential) or Output 21 LVCMOS output
OUT21N	O	Differential	1	14	Output 21 complement output (differential) connect to OUT21P for LVCMOS
OUT22P	O	LVCMOS / Differential	1	15	Output 22 true output (differential) or Output 22 LVCMOS output
OUT22N	O	Differential	1	16	Output 22 complement output (differential) connect to OUT22P for LVCMOS
OUT23P	O	LVCMOS / Differential	1	18	Output 23 true output (differential) or Output 23 LVCMOS output

Table 3. 48-Pin QFN (CY27410) Pin Definitions *(continued)*

Name	I/O	Type	# of Pins	Pin #	Function
OUT23N	O	Differential	1	19	Output 23 complement output (differential) connect to OUT23P for LVCMOS
OUT24P	O	LVCMOS/ Differential	1	20	Output 24 true output (differential) or Output 24 LVCMOS output
OUT24N	O	Differential	1	21	Output 24 complement output (differential) connect to OUT24P for LVCMOS
OUT25	O	LVCMOS	1	22	LVCMOS clock output 25
OUT26	O	LVCMOS	1	24	LVCMOS clock output 26
DNU			1	10	Pin for test purpose
SDAT	I/O	LVCMOS/ Open Drain	1	33	I^2C serial data pin
SCLK	I	LVCMOS	1	34	I^2C clock pin
FS0	I	LVCMOS	1	30	Frequency Select pin
FS1	I	LVCMOS	1	31	Frequency Select pin
FS2	I	LVCMOS	1	32	Frequency Select pin
VIN	I	Analog	1	26	Voltage input for ADC
VDDIO_D1	PWR	PWR	1	44	Output power supply for Bank1 differential outputs
VDDIO_S1	PWR	PWR	1	38	Output power supply for Bank1 LVCMOS outputs
VDDIO_D2	PWR	PWR	1	17	Output power supply for Bank2 Differential outputs
VDDIO_S2	PWR	PWR	1	23	Output power supply for Bank2 LVCMOS outputs
VDD	PWR	PWR	9	1,2,7,11,12, 25,29,35,36	Core power supply
XRES	I	LVCMOS	1	27	Active low RESET SIGNAL
GND	GND	GND	E-PAD		Supply ground
VCCD	Analog	Analog	1	28	For 1.8-V operation, connect to VDD. For 2.5-V or 3.3-V operation, do not connect to VDD; connect a 100-nF capacitor between this pin and GND.

Figure 22. 48-Pin QFN Pinout



Electrical Specifications

Exceeding maximum ratings may shorten the useful life of the device.

Absolute Maximum Ratings

Table 4. Absolute Maximum Ratings

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{DD}	Core supply voltage		–0.5	–	4.6	V
V_{DDIOX}	Output bank supply voltage		–0.5	–	4.6	V
V_{IN}	Input voltage	Relative to V_{SS}	–0.5	–	V_{DD} + 0.4	V
V_{INI2C}	I2C Bus input voltage	SCLK, SDAT pins	–0.5	–	6	V
T_S	Storage temperature	Non functional	–55	–	+150	°C
ESD_{HBM}	ESD (human body model)	JEDEC JS-001-2012	2000	–	–	V
ESD_{CDM}	ESD (charged device model)	JEDEC JESD22-C101E	500	–	–	V
ESD_{MM}	ESD (machine model)	JEDEC JESD22-A115B	200	–	–	V
LU	Latchup	JEDEC JESD78D	–	–	140	mA
UL-94	Flammability rating	V-0 at 1/8 in	–	–	10	ppm
MSL	Moisture sensitivity level		–	3	–	
θ_{JA}	Package Thermal Resistance	PCB dimensions 76x114x1.6mm, 4 Layers, 0 air flow		13		°C/W

Operating Temperature

Table 5. Operating Temperature

Symbol	Description	Conditions	Min	Typ	Max	Units
T_A	Ambient temperature		–40	–	+85	°C
T_J	Junction temperature		–40	–	+100	°C

Operating Power Supply

Table 6. Operating Power Supply

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{DD}	Core supply voltage	1.8-V range: ±5%	1.71	1.80	1.89	V
		2.5-V range: ±10%	2.25	2.50	2.75	V
		3.3-V range: 5%	3.13	3.3	3.46	V
V_{DDIO}	Output supply voltage	1.8-V range: ±5%	1.71	1.80	1.89	V
		2.5-V range: ±10%	2.25	2.50	2.75	V
		3.3-V range: 5%	3.13	3.30	3.46	V
I_{DDO}	Power supply current per pair	LVPECL, output pair terminated 50 Ω to V_{TT} (V_{DD}-2 V)	–	–	38.0	mA
		LVPECL, output pair terminated 50 Ω to V_{TT} (V_{DD}-1.7 V)	–	–	27.0	mA
I_{DDO}	Power supply current per pair	LVDS, output pair terminated 100 Ω	–	–	12.0	mA
I_{DDO}	Power supply current per pair	HCSL, output pair terminated 33 Ω to 49.9 Ω to GND	–	–	26.5	mA
I_{DDO}	Power supply current per pair	CML, output pair terminated 50 Ω to V_{DD}	–	–	16.0	mA
I_{DDO}	Power supply current per pair	CMOS, 10-pF load, 33 MHz	–	–	6.0	mA
I_{DDPLL1}	Current consumption per PLL	Includes DIVC	–	–	26.5	mA
I_{DDXO}	XO/Input block current consumption	XO or IN1 input buffer on, IN2 input buffer off	–	–	3.5	mA

Table 6. Operating Power Supply *(continued)*

Symbol	Description	Conditions	Min	Typ	Max	Units
I_{DDPM}	Power management block current consumption		–	–	2.5	mA
$t_{PLLLOCK}$	PLL lock time	Time from PLL enabled to PLL stable (PLL reaches at ±1-ppm accuracy)	–	–	250	µs
t_{LOCK}	Device power-up time	Time from minimum specified V_{DD} to Output Stable in XO-based clock gen mode. In the case of external clock input, t_{LOCK} will reduce by the crystal oscillator startup time ($t_{OSCSTART}$). This specification is valid when the reference is available and stable at startup. For supply ramps slower than the t_{PU_SR} spec where customers use XRES during power up. Power-up time will be calculated from the release of XRES to output stable.	–	–	8.0	ms
t_{PU_SR}	Power supply slew rate during power up	Power-supply ramp rate for V_{DD} to reach minimum specified voltage (power ramp must be monotonic). For supply ramps slower than 1 V/ms, use XRES to externally keep the part in RESET during power-up and release XRES after V_{DD} reaches the minimum specification.	1	–	67	V/ms

DC Chip-Level Specifications

Table 7. DC Electrical Specifications Input

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{IH33}	Input high voltage	LVCMOS and logic inputs, V_{DD} = 3.3 V	2.0	–	–	V
V_{IH25}	Input high voltage	LVCMOS and logic inputs, V_{DD} = 2.5 V	1.7	–	–	V
V_{IH18}	Input high voltage	LVCMOS and logic inputs, V_{DD} = 1.8 V	1.1	–	–	V
V_{IL33}	Input low voltage	LVCMOS and logic inputs, V_{DD} = 3.3 V	–	–	0.8	V
V_{IL25}	Input low voltage	LVCMOS and logic inputs, V_{DD} = 2.5 V	–	–	0.7	V
V_{IL18}	Input low voltage	LVCMOS and logic inputs, V_{DD} = 1.8 V	–	–	0.5	V
V_{DIFF}	Differential input	LVDS, CML, PECL, HCSL. Differential amplitude, pk.	0.30	–	1.45	V
DC_{DIFF}	Duty cycle, differential input	Measured at crossing point	40	50	60	%
DC_{LVCMOS}	Duty cycle, LVCMOS input	Measured at 1/2 V_{DD}	40	50	60	%
I_{IH}	Input high current	Input = V_{DD}	–	–	150	µA
I_{IL}	Input low current	Input = GND	–150	–	–	µA
C_{IN}	Input capacitance, IN1, IN2	Measured at 10 MHz, differential	–	–	3.0	pF
V_{PPSINE}	AC input swing pk	Clipped sine wave, AC coupled through a 1000-pF capacitor.	0.8	1.0	1.2	V
R_P	Input Pull-down resistance	LVCMOS input	75	115	170	kΩ

DC Output Specifications

Table 8. DC Specifications for LVCMOS Output

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{OH}	Output high voltage	4-mA load	V_{DDIO}–0.3	–	–	V
V_{OL}	Output low voltage	4-mA load	–	–	0.3	V

Table 9. DC Specifications for LVDS Output (V_{DDIO} = 2.5-V or 3.3-V range)

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{PP}	LVDS output AC single-ended pk-pk,	8 MHz to 325 MHz	250	–	470	mV
V_{PP}	LVDS output AC single-ended pk-pk	325 MHz to 700 MHz	200	–	470	mV
ΔV_{PP}	Change in V_{PP} between complementary output states		–	–	50	mV
V_{OCM}	Output common-mode voltage	Met only at 2.5 V and 3.3 V. Need AC coupling for 1.8-V operation	1.125	1.200	1.375	V
ΔV_{OCM}	Change in VOCM between complementary output states		–	–	50	mV
I_{OZ}	Output leakage current	Output off, V_{OUT} = 0.75 V to 1.75 V	–20	–	20	µA

Table 10. DC Specifications for LVPECL Output (V_{DDIO} = 2.5-V or 3.3-V range)

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{OH}	Output high voltage	R-term = 50 Ω to V_{TT} (V_{DDIO}–2.0 V)	V_{DDIO} –1.165	–	V_{DDIO} –0.850	V
V_{OL}	Output low voltage	R-term = 50 Ω to V_{TT} (V_{DDIO}–2.0 V)	V_{DDIO} –2.0	–	V_{DDIO} –1.620	V
V_{PP}	LVPECL output AC single ended pk-pk,	f_{OUT} = 8 MHz to 150 MHz	450	–	–	mV
		f_{OUT} = 150 MHz to 700 MHz	320	–	–	mV

Table 11. DC Specifications for CML Output (V_{DDIO} = 2.5-V or 3.3-V range)

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{OH}	Output high voltage	R-term= 50 Ω to V_{DDIO}	V_{DDIO}–0.1	–	–	V
V_{OL}	Output low voltage	R-term= 50 Ω to V_{DDIO}	V_{DDIO}–0.7	–	V_{DDIO} –0.3	V
V_{PP}	CML output AC single-ended pk-pk	f_{OUT} = 8 MHz to150 MHz	250	–	700	mV
V_{PP}	CML output AC single-ended pk-pk	150 < f_{OUT} < 700 MHz	200	–	600	mV

Table 12. DC Specifications for HCSL Output (V_{DDIO} = 2.5-V or 3.3-V range)

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{OCM}	Output common mode voltage	Common mode	350	–	400	mV
V_{OHDIFF}	Differential output high voltage	Measurement taken from differential waveform	150	–	–	mV
V_{OLDIFF}	Differential output low voltage	Measurement taken from differential waveform	–	–	–150	mV
V_{CROSS}	Absolute crossing point voltage	Measurement taken from single-ended waveform	250	–	550	mV
$V_{CROSSDELTA}$	Variation of V_{CROSS} over all rising clock edges	Measurement taken from single-ended waveform	–	–	140	mV

Table 13. Input Frequency Range

Symbol	Description	Conditions	Min	Typ	Max	Units
$F_{CRYSTAL}$	Crystal frequency	Fundamental AT CUT crystal	8	–	48	MHz
$F_{REFERENCE}$	Reference frequency	Internal reference to PLL	8	–	40	MHz
F_{INCMOS}	LVCMOS input frequency	Buffer mode, all PLLs OFF	8	–	250	MHz
F_{INCMOS}	LVCMOS input frequency	Buffer mode, one or more PLL active	8	–	125	MHz
F_{INCMOS}	LVCMOS input frequency	CLKGEN mode	8	–	250	MHz
F_{INCMOS}	LVCMOS input frequency	ZDB mode, PLL in integer N configuration	8	–	250	MHz
F_{INDIFF}	Differential clock input frequency	Buffer mode, all PLLs OFF	8	–	700	MHz
F_{INDIFF}	Differential clock input frequency	Buffer mode, one or more PLL active	8	–	125	MHz
F_{INDIFF}	Differential clock input frequency	CLKGEN mode	8	–	300	MHz
F_{INDIFF}	Differential clock input frequency	ZDB mode, PLL in integer N configuration	8	–	300	MHz
F_{INCAS}	Cascading clock frequency	Internal cascading frequency in the Buffer mode	8	–	125	MHz

AC Input Clock Specifications

Table 14. AC Input Clock Electrical Specification

Symbol	Description	Conditions	Min	Typ	Max	Units
t_{CMOSDC}	LVCMOS input duty cycle	Measured at 1/2 V_{DD} 20-80%, Functional	40	50	60	%
t_{DIFFDC}	Differential input duty cycle	Measured at V_{OCM} 20-80%, Functional	40	50	60	%
t_{RFCMOS}	LVCMOS input rise/fall time	Measured between 20-80% of V_{DD}	–	–	4	ns

AC Output Specifications

Table 15. AC Electrical Specifications LVCMOS Output. Load: 15 pF < 100MHz, 7.5 pF < 200 MHz, 5 pF > 200 MHz

Symbol	Description	Conditions	Min	Typ	Max	Units
Common AC Electrical Specifications						
t_{RFCMOS}	Rise/fall time	f_{OUT} < 100MHz, 20%–80%	–	–	2.0	ns
t_{RFCMOS}	Rise/fall time	f_{OUT} < 200MHz, 20%–80%	–	–	1.5	ns
t_{RFCMOS}	Rise/fall time	f_{OUT} < 250MHz, 20%–80%	–	–	1.3	ns
t_{SKEW}	Output to output skew	Equally loaded, measured at 1/2 V_{IOX}, in a bank, derived from the same PLL,	–	–	100	ps
Buffer Mode						
f_{OUT}	Output frequency	All PLLs off	8		250	MHz
f_{OUT}	Output frequency	With one or more PLL running	8		125	MHz

Table 15. AC Electrical Specifications LVCMOS Output. Load: 15 pF < 100MHz, 7.5 pF < 200 MHz, 5 pF > 200 MHz *(continued)*

Symbol	Description	Conditions	Min	Typ	Max	Units
t_{DC}	Output duty cycle	Measured at 1/2 V_{IOX}. Input DC = 50%	40	50	60	%
t_{JIT_ADD}	Additive RMS phase jitter	f_{OUT} = 156.25 MHz, 12k-20 MHz offset, DIVI=1.Input slew rate 1.8 V/ns 20%–80% V_{DD}	–	0.7	1.0	ps
t_{DELAY}	Propagation delay	Input to output delay	–	–	7.0	ns
ZDB Mode (IN1 = REF, Differential or LVCMOS feedback to IN2)						
f_{OUT}	Output frequency		8	–	250	MHz
t_{DC}	Output duty cycle	Measured at 1/2 V_{IOX}, f_{OUT} > 200 MHz, V_{DDIO} = 2.5 V or 3.3 V. f_{OUT} > 100MHz, V_{DDIO} = 1.8 V	40	50	60	%
t_{DC}	Output duty cycle	Measured at 1/2 V_{IOX}, $f_{OUT} \le$ 200 MHz V_{DDIO} = 2.5 V or 3.3 V. $f_{OUT} \le$ 100 MHz, V_{DDIO} = 1.8 V	45	50	55	%
t_{OCCJ}	Cycle-to-cycle jitter	pk, measured at 1/2 V_{IOX} over 10-k cycle, f_{OUT} = 100 MHz.Input slew rate 1.8V/ns 20%–80% V_{DD}. Configuration dependent	–	–	50	ps
t_{PJ}	Period jitter	pk-pk, measured at 1/2 V_{IOX} over 10-k cycle, f_{OUT} = 100 MHz.Input slew rate 1.8 V/ns 20%–80% V_{DD}. Configuration dependent	–	–	100	ps
t_{PDELAY}	Propagation delay	Measured at 1/2 V_{IOX} ±250 ps excludes any delay added onboard (from output to inputs). Delay onboard (t_{DELAY_BOARD}) must not exceed 2-ns max. Total delay in the ZDB mode is t_{DELAY_BOARD} + t_{PDELAY}	–250	–	250	ps
CLKGEN Mode						
f_{OUT}	Output frequency		3	–	250	MHz
f_{OUTL}	Low frequency output	1 kHz is supported when the max input frequency to DIVL is 48 MHz	0.001	–	50	MHz
t_{DC}	Output duty cycle	Measured at 1/2 V_{IOX}, f_{OUT} > 200 MHz, V_{DDIO} = 2.5 V or 3.3 V. f_{OUT} > 100 MHz, V_{DDIO} = 1.8 V	40	50	60	%
t_{DC}	Output duty cycle	Measured at 1/2 V_{IOX}, $f_{OUT} \le$ 200 MHz V_{DDIO} = 2.5 V or 3.3 V. $f_{OUT} \le$ 100 MHz, V_{DDIO} = 1.8 V	45	–	55	%
t_{CCJ}	Cycle-to-cycle jitter	pk, measured at 1/2 V_{IOX} over 10-k cycle, f_{OUT}=100 MHz. Configuration dependent	–	–	50	ps
t_{PJ}	Period jitter	pk-pk, measured at 1/2 V_{IOX} over 10-k cycle, f_{OUT} = 100 MHz. Input reference 25-MHz crystal. Configuration dependent	–	–	100	ps
SSC Mode						
f_{OUT}	Output frequency		3	–	250	MHz
t_{DC}	Output duty cycle	Measured at 1/2 V_{IOX}, f_{OUT} > 200 MHz, V_{DDIO} = 2.5 V or 3.3 V. f_{OUT} > 100 MHz, V_{DDIO} = 1.8 V	40	50	60	%
t_{DC}	Output duty cycle	Measured at 1/2 V_{IOX}, $f_{OUT} \le$ 200 MHz V_{DDIO} = 2.5 V or 3.3 V. $f_{OUT} \le$ 100 MHz, V_{DDIO} = 1.8 V	45	50	55	%
t_{CCJ}	Cycle-to-cycle jitter	pk, measured at 1/2 V_{IOX} over 10-k cycle, f_{OUT} = 100 MHz, with a spread of 0.5%. Input reference 25-MHz crystal. Configuration dependent	–	–	100	ps

Table 16. AC Electrical Specifications, Differential Output (LVPECL, CML, LVDS) [1]

Symbol	Description	Conditions	Min	Typ	Max	Units
COMMON AC Electrical Specifications						
t_{RF}	PECL output rise/fall time	20%–80% of AC levels, measured at 622.08 MHz	–	–	450	ps
t_{RF}	CML output rise/fall time	20%–80% of AC levels, measured at 622.08 MHz	–	–	450	ps
t_{RF}	LVDS output rise/fall time	20%–80% of AC levels, measured at 622.08 MHz	–	–	450	ps
t_{SK1}	Output skew	Four differential output pairs in a bank, derived from the same PLL, with same standard and load conditions	–	–	75	ps
BUFFER Mode						
t_{ODC}	Output duty cycle	Differential input signal at 50% duty cycle, differential signal, 622.08 MHz	45	50	55	%
t_{ODC}	Output duty cycle	LVCMOS input signal at 50% duty cycle, differential signal, 250 MHz	40	50	60	%
t_{PD}	Propagation delay	Measured at differential signal, 156.25 MHz	–	–	4	ns
t_{JIT_ADD}	Additive RMS phase jitter	f_{OUT} = 156.25 MHz, 12-k to 20-MHz offset, DIV1 = 1. Input slew rate 4 V/ns differential 400-mV amplitude.	–	–	400	fs
ZDB Mode (REF=IN1, 1 pair of output is feedback to IN2)						
t_{ODC}	Output duty cycle	Measured at differential signal, 100 MHz	45	50	55	%
t_{CCJ}	Cycle-to-cycle jitter	pk, measured differential signal over 10-k cycle, f_{OUT} =156.25 MHz. Input slew rate 4 V/ns differential 400-mV amplitude. (all differential outputs on)	–	–	50	ps
t_{PJ}	Period jitter	pk-pk, measured differential signal over 10-k cycle, f_{OUT} = 156.25 MHz. Input slew rate 4 V/ns differential 400-mV amplitude. (all differential outputs on)	–	–	50	ps
t_{PD}	Propagation delay	Measured differential signal, f_{OUT} = 156.25 MHz, ±250 ps is excluding any delay added onboard (from output to inputs). Delay onboard (t_{DELAY_BOARD}) must not exceed 2-ns max. Total delay in the ZDB mode is t_{DELAY_BOARD} + t_{PDELAY}	–200		200	ps
t_{JRMS}	RMS phase jitter	f_{IN} = f_{OUT} = 156.25 MHz, 12-k to 20-MHz offset. Input slew rate 4 V/ns differential 400-mV amplitude	–	0.7	1.0	ps
PNg10k	Phase noise, offset10 kHz	f_{IN} = f_{OUT} = 156.25 MHz. Input slew rate 4 V/ns differential 400-mV amplitude.	–	–	–110	dBc/Hz
PNg100k	Phase noise, offset = 100 kHz	f_{IN} = f_{OUT} = 156.25 MHz. Input slew rate 4 V/ns differential 400-mV amplitude.	–	–	–119	dBc/Hz
PNg1M	Phase noise, offset = 1 MHz	f_{IN} = f_{OUT} = 156.25 MHz. Input slew rate 4 V/ns differential 400-mV amplitude.	–	–	–131	dBc/Hz
PNg10M	Phase noise, offset = 10 MHz	f_{IN} = f_{OUT} = 156.25 MHz. Input slew rate 4 V/ns differential 400-mV amplitude.	–	–	–147	dBc/Hz

Note
1. AC parameters for differential outputs are guaranteed for only differential outputs. LVCMOS is Off.

Table 16. AC Electrical Specifications, Differential Output (LVPECL, CML, LVDS) [1] *(continued)*

Symbol	Description	Conditions	Min	Typ	Max	Units
PN-SPUR	Spur	At frequency offsets equal to and greater than the update rate of the PLL. Input slew rate 4 V/ns differential 400-mV amplitude.	–	–	–65	dBc/ Hz
CLKGEN Mode						
t_{ODC}	Output duty cycle	Measured at differential signal, 622.08 MHz	45	50	55	%
t_{CCJ}	Cycle-to-cycle jitter	pk, measured at differential signal, 156.25 MHz, over 10-k cycles. Input frequency (24 MHz to 40 MHz) crystal. (all differential outputs on)	–	–	50	ps
t_{PJ}	Period jitter	pk-pk, measured at differential signal 156.25 MHz, over 10-k cycles. Input frequency (24 MHz to 40 MHz) crystal. (all differential outputs on)	–	–	50	ps
t_{JRMS}	RMS phase jitter	f_{OUT} = 156.25 MHz, 12-k to 20-MHz offset	–	0.7	1.0	ps
PNg10k	Phase noise, offset10 kHz	f_{OUT}=156.25 MHz. Input reference 25-MHz crystal	–	–	–110	dBc/ Hz
PNg100k	Phase noise, offset = 100 kHz	f_{OUT}=156.25 MHz. Input reference 25-MHz crystal	–	–	–119	dBc/ Hz
PNg1M	Phase noise, offset = 1 MHz	f_{OUT} = 156.25 MHz. Input reference 25-MHz crystal	–	–	–131	dBc/ Hz
PNg10M	Phase noise, offset = 10 MHz	f_{OUT} = 156.25 MHz. Input reference 25-MHz crystal	–	–	–147	dBc/ Hz
PN-SPUR	Spur	At frequency offsets equal to and greater than the update rate of the PLL	–	–	–65	dBc/ Hz
SSC Mode						
t_{CCJ}	Cycle-to-cycle jitter	pk, measured at differential signal, 156.25 MHz, over 10-k cycles. Input frequency (24 MHz to 40 MHz) crystal, with a spread of 0.5% (all differential outputs on).	–	–	70	ps

Table 17. AC Electrical Specification HSCL Output [2, 3]

Symbol	Description	Conditions	Min	Typ	Max	Units
Common AC Electrical Specifications						
f_{OC}	Output frequency	HCSL	96	–	400	MHz
E_R	Rising edge rate	Measurement taken from differential waveform, –150 mV to +150 mV	0.6	–	4	V/ns
E_F	Falling edge rate	Measurement taken from differential waveform, –150 mV to +150 mV	0.6	–	4	V/ns
T_{STABLE}	Time before V_{RB} is allowed	Measurement taken from differential waveform, –150 mV to +150 mV	500	–	–	ps
T_{PERIOD_AVG}	Average clock period accuracy, 100 MHz	Measurement taken from differential waveform, Spread Spectrum On, 0.5% down spread	–300	–	2800	ppm
T_{PERIOD_ABS}	Absolute period	Measurement taken from differential waveform, Spread Spectrum On, 0.5% down spread	9.874	–	10.203	ns

Notes
2. AC parameters for differential outputs are guaranteed for only differential outputs. LVCMOS is Off.
3. All output clocks 100MHz HCSL format. Jitter is from PCIE jitter filter combination that produces the highest jitter.

Table 17. AC Electrical Specification HSCL Output [2, 3] *(continued)*

Symbol	Description	Conditions	Min	Typ	Max	Units
$R\text{-}F_{MATCHING}$	Rise-fall matching	Measurement taken from single-ended waveform. Rising edge rate to falling edge rate matching 100 MHz	–20	–	+20	%
BUFFER Mode						
T_{DC}	Duty cycle	Measurement taken from differential waveform	45	50	55	%
t_{RMS_ADD}	Additive phase noise	Input slew rate 4 V/ns differential 400-mV amplitude.	–	–	0.4	ps (RMS)
ZDB Mode (REF=IN1, 1 output pair fed back to IN2)						
T_{DC}	Duty cycle	Measurement taken from differential waveform	45	50	55	%
$T_{CCJITTER}$	Cycle-to-cycle jitter	pk, measured at differential signal 100 MHz, over 10-k cycles. Input slew rate 4 V/ns differential 400-mV amplitude (all differential outputs on).	–	–	50	ps
J_{RMS}	Random jitter PCIe 3.0 Common clocked	PCIe Gen3 filters. Input slew rate 4 V/ns differential 400-mV amplitude.	–	0.7	1.0	ps (RMS)
t_{PD}	Propagation delay	Early/Late option is OFF	–200	–	200	ps
CLKGEN Mode						
T_{DC}	Duty cycle	Measurement taken from differential waveform	45	50	55	%
$T_{CCJITTER}$	Cycle-to-cycle jitter	pk, measured at differential signal, 100 MHz, over 10-k cycles. Input frequency (24 MHz–40 MHz) crystal (all differential outputs on).	–	–	50	ps
J_{RMS}	Random jitter PCIe 3.0 Common clocked	REF = 25-MHz crystal, f_{OUT} = 100 MHz, PCIe Gen3 filters	–	0.7	1.0	ps

Table 18. AC I^2C Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
f_{SCK}	SCK clock frequency		0	–	400	kHz
$t_{HD:STA}$	Hold time START condition		0.6	–	–	µs
t_{LOW}	Low period of the SCK clock		1.3	–	–	µs
t_{HIGH}	High period of the SCK clock		0.6	–	–	µs
$t_{SU:STA}$	Setup time for a repeated START condition		0.6	–	–	µs
$t_{HD:DAT}$	Data hold time		0	–	–	µs
$t_{SU:DAT}$	Data setup time		100	–	–	ns
t_R	Rise time		–	–	300	ns
t_F	Fall time		–	–	300	ns
$t_{SU:STO}$	Setup time for STOP condition		0.6	–	–	µs
t_{BUF}	Bus-free time between STOP and START conditions		1.3	–	–	µs

Table 19. Spread-Spectrum Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{MOD}	Modulation rate		30	–	60	kHz
SSper	Spread spectrum amount	Total %	0.1	–	5.0	%
SSStep	Spread spectrum% step		–	0.1	–	%

Table 20. Output Selection Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
t_{FS}	Frequency switching time	Frequency switching time for OUT13,14, 23, 24. Both PLLs are active (change MUX selection Bit).	–	–	500	µs
t_{FS}	Frequency switching time	Frequency switching time for all outputs, DIVO value change	–	–	500	µs
t_{FS}	Frequency switching time	Frequency switching time for all outputs. PLL value change.	–	–	1000	µs
t_{FS}	Output turn-on time	Output turn-on time from FS. PLL is active, change OE or MUX.	–	–	500	µs
t_{FS}	Output turn-on time	Output turn-on time from FS. Resume PLL from Power Down.	–	–	1000	µs
t_{OFF}	Output turn-off time	Output turn-off time from FS. PLL is active, change OE or MUX.	–	–	500	µs

Table 21. NV Memory Specification

Symbol	Description	Conditions	Min	Typ	Max	Units
DRET	NV memory data retention		10	–	–	Years
$PROG_{CYCLE}$	Programming cycle	Programming cycle for NV memory	100 K	–	–	Cycle

Table 22. Miscellaneous Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
t_{XRES}	XRES Low time		10			µs
T_{PROG}	Flash programming temperature		5		55	°C
C_{INADC}	Input Capacitance VIN pin				10	pF

Test and Measurement Circuits

Figure 23. LVPECL Output Load and Test Circuit

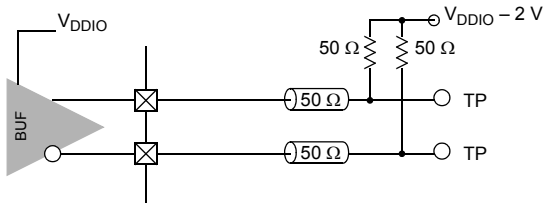


Figure 24. LVDS Output Load and Test Circuit

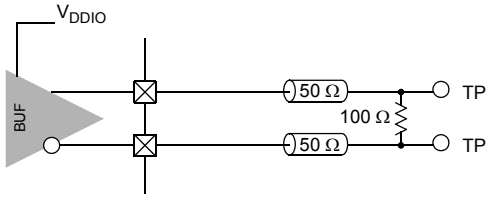


Figure 25. CML Output Load and Test Circuit

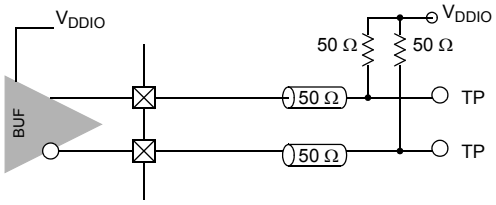


Figure 26. HCSL Output Load and Test Circuit

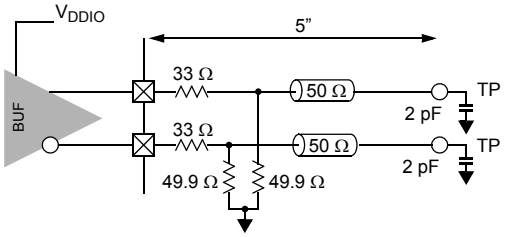
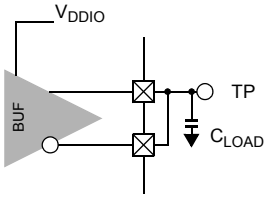


Figure 27. LVCMOS Output Load and Test Circuit



Voltage and Timing Definitions

Figure 28. LVCMOS Input Definitions

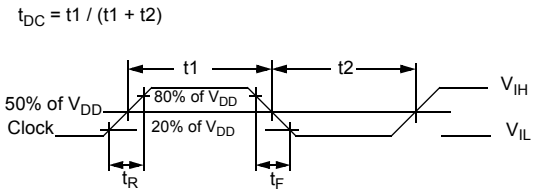


Figure 29. LVCMOS Output Definitions

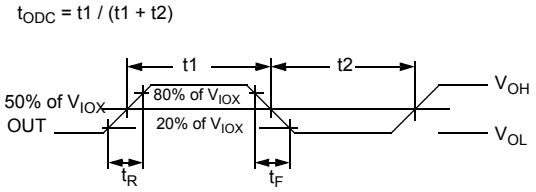


Figure 30. Differential Input Definitions

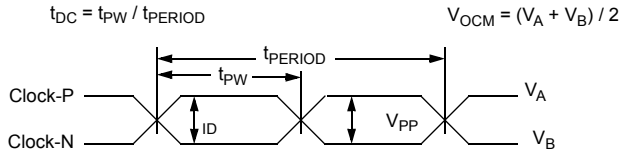


Figure 31. Differential Output Definitions

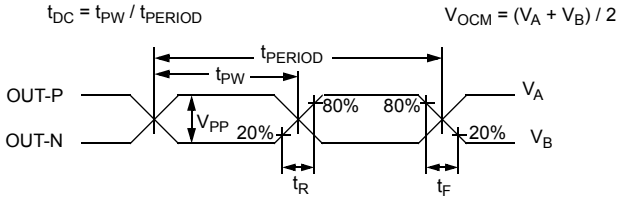


Figure 32. Skew Definition

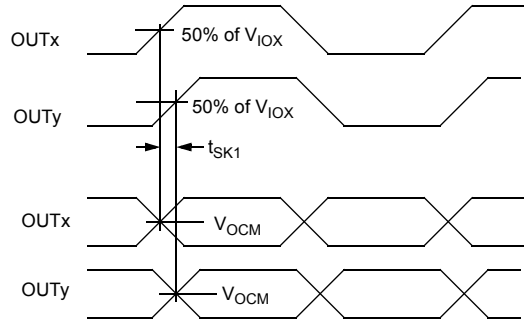


Figure 33. Propagation Delay Definition

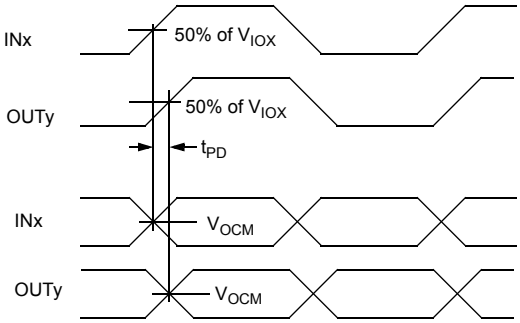


Figure 34. Output Enable/Disable/Frequency Select Timing

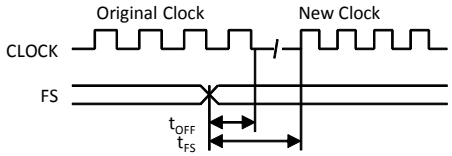


Figure 35. HCSL Single-ended Measurement Point-2

Rise and Fall Time Matching

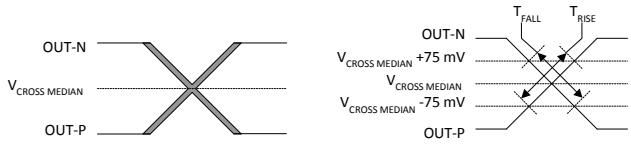


Figure 36. HCSL Differential Measurement Point

Duty Cycle and Period

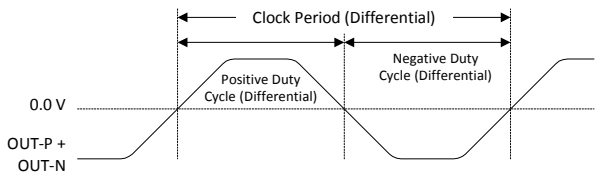


Figure 37. HCSL Differential Measurement for Ringback

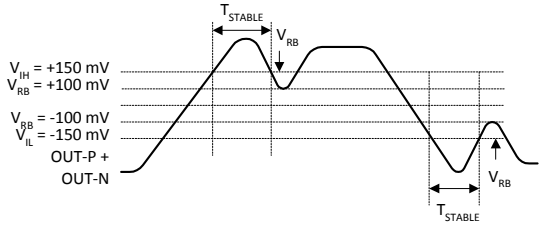


Figure 38. HCSL Rise and Fall Time

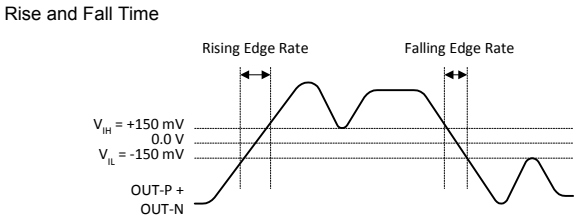


Figure 39. Power Ramp and PLL Lock Time

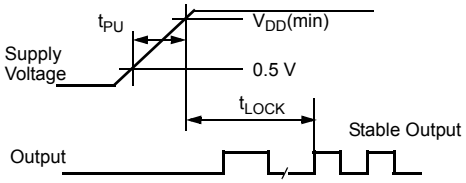
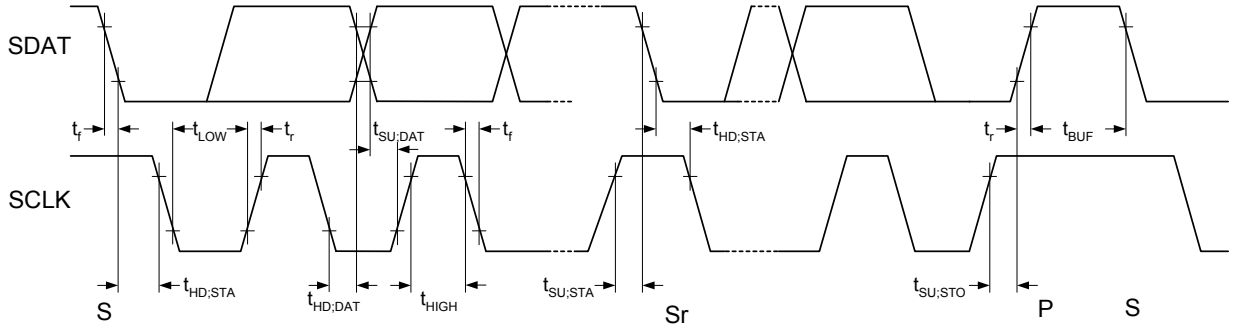


Figure 40. Definition for Timing for Fast/Standard Mode on the I²C Bus

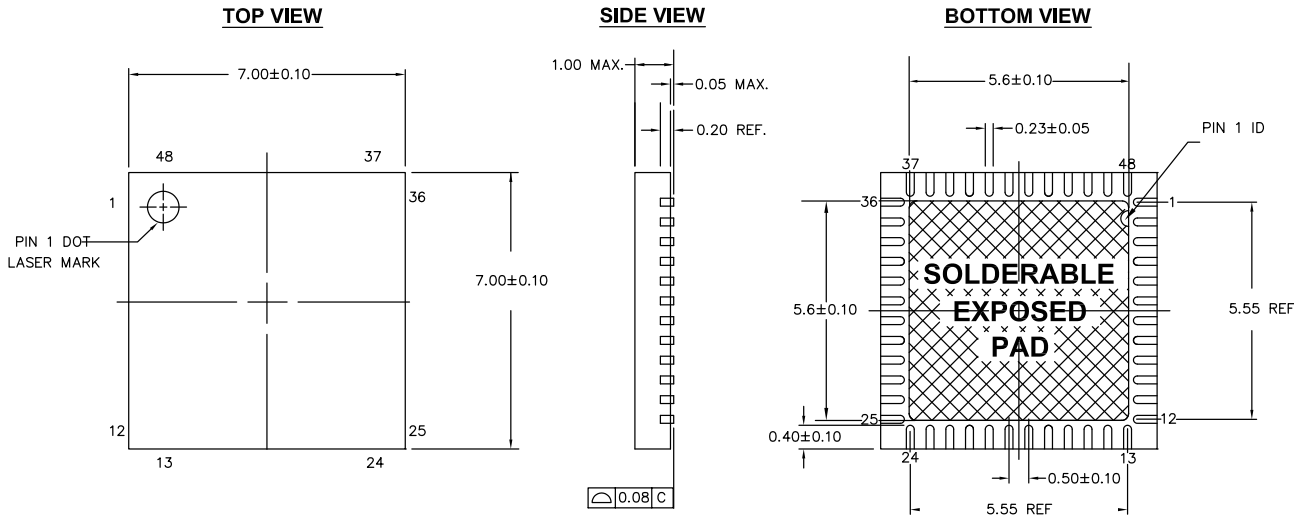


Packaging Information

This section illustrates the packaging specifications for the CY27410 device, along with the thermal impedances for each package.

Important Note The EPAD must be connected to ground to reduce the thermal resistance and for signaling ground.

Figure 41. 48-Pin QFN (7 × 7 × 1.00 mm) LT48D 5.5 x 5.5 EPAD (Sawn) Package Outline



NOTES:

1. ▨ HATCH AREA IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO−220
3. PACKAGE WEIGHT: REFER TO PMDD SPEC.
4. ALL DIMENSIONS ARE IN MM [MIN/MAX]
5. PACKAGE CODE

PART #	DESCRIPTION
LT48D	LEAD FREE

001-45616 *D

For information on the preferred dimensions for mounting QFN packages, refer to the Cypress application note AN72845 - Design Guidelines for Cypress Quad Flat No Extended Lead (QFN) Packaged Devices.

Solder Reflow Specifications

Table 23 shows the solder reflow temperature limits that must not be exceeded.

Table 23. Solder Reflow Specifications

Package	Maximum Peak Temperature (T_C)	Maximum Time above T_C –5 °C
48-pin QFN	260 °C	30 seconds

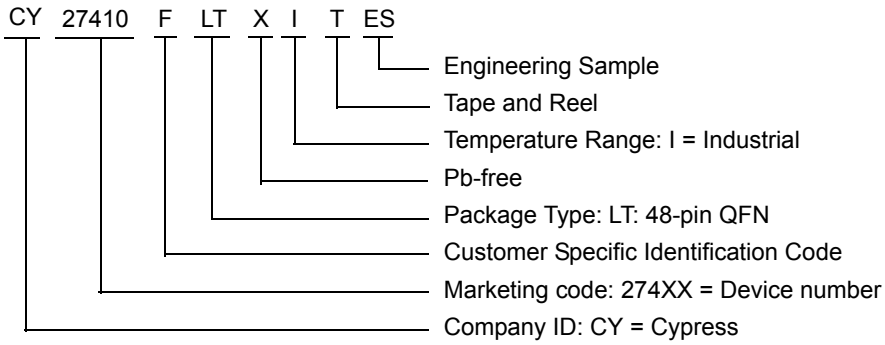
Ordering Information

The following table lists the CY27410 device's key package features and ordering codes.

Table 24. Ordering Information

Part Number	Package	Type
CY27410FLTXIES	48-pin QFN	Industrial, Engineering Sample
CY27410FLTXI	48-pin QFN	Industrial
CY27410FLTXIT	48-pin QFN tape and reel	Industrial

Ordering Code Definitions



Acronyms

Table 25. Acronyms Used in this Document

Acronym	Description
AC	alternating current
ADC	analog-to-digital converter
API	application programming interface
CML	current-mode logic
CMOS	complementary metal oxide semiconductor
DC	direct current
ESD	electrostatic discharge
FS	frequency select
GUI	graphical user interface
HCSL	high-speed current steering logic
I^2C	inter-integrated circuit
I/O	input/output
ISSP	in-system serial programming
JEDEC	Joint Electron Devices Engineering Council
LDO	low dropout (regulator)
LSB	least-significant bit
LVCMOS	low voltage complementary metal oxide semiconductor
LVDS	low-voltage differential signals
LVPECL	low-voltage positive emitter-coupled logic
MSB	most-significant byte
NV	non-volatile
NZDB	non-zero delay buffer
OE	output enable
PCIe	PCI express
POR	power-on reset
PSoC®	Programmable System-on-Chip
QFN	quad flat no-lead
RMS	root mean square
SCLK	serial I^2C clock
SDAT	serial I^2C data
TSSOP	thin shrunk small outline package
USB	universal serial bus
XTAL	crystal
ZDB	zero delay buffer

Document Conventions

Units of Measure

Table 26. Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
dBc	decibels relative to the carrier
fF	femtofarad
fs	femtosecond
g	gram
GHz	gigahertz
Hz	hertz
KHz	kilohertz
Ksps	kilo samples per second
kΩ	kilohm
MHz	megahertz
MΩ	megaohm
µA	microampere
µF	microfarad
µH	microhenry
µs	microsecond
µW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
nF	nanofarad
ns	nanosecond
nV	nanovolt
Ω	ohm
pA	picoampere
pF	picofarad
pp	peak-to-peak
ppm	parts per million
ppb	parts per billion
ps	picosecond
sps	samples per second
σ	sigma: one standard deviation
V	volt
W	watt

Document History Page

Document Title: CY27410, 4-PLL Spread-Spectrum Clock Generator Document Number: 001-89074				
Rev.	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	4116274	XHT	01/20/2014	New document
*A	4355590	XHT	04/21/2014	Removed CY27420 and related description. Changed description for I^2C functionality, Read, Write, or Read/Write protection, partial profile update Corrected (swap) IDDO (LVPECL) parameters 38.0 mA and 27.0 mA. Changed $I_{DDO(LVDS)}$ from 10.5 to 12 mA. Changed V_{DIFF} from 0.4-1.2 V to 0.3-1.45 V Removed V_{IH} Max, V_{IL} Min from Differential Input Specifications Removed V_{IH} Max, V_{IL} Min from LVCMOS Input Specifications Added Internal Pull-Down resistance parameter Changed t_{DELAY} from 6ns to 7 ns in LVCMOS buffer mode Added t_{DC} of 40-60% for (f_{OUT} > 200 MHz) in LVCMOS output Added description ($f_{OUT} \leq 200$ MHz) for t_{DC} in LVCMOS output Changed LVDS output rise/fall time from 300 ps to 350 ps Changed t_{SK1} for differential output from 30 ps to 40 ps Changed t_{JIT_ADD} for Differential Buffer mode output from 300 fs to 400 fs Changed conditions t_{ODC} for differential output from 622.08 MHz to 100 MHz Removed REF = 25 MHz crystal from conditions of RMS Phase Jitter, and modified $f_{IN} = f_{OUT}$ = 156.25 MHz Added conditions for 100 MHz for R-$F_{\_MISMATCH}$ Changed t_{RMS_ADD} from 0.3 ps (RMS) to 0.4 ps (RMS) Add conditions for HCSL CLKGEN Mode T_{DC}, f_{OUT} = 100 MHz. Input frequency [24 MHz - 40 MHz] crystal Remove 40-pin QFN package and soldering information fro 40-pin QFN. Changed 48-pin QFN package from LT48A to LT48D. Changed Pinout for CY27410. Added Automotive device CY27430 pinout. Added Automotive device (CY27430FLXAT) in ordering information. Removed PNg1k specification. Added Conditions: Input slew rate 4 V/ns differential 400-mV amplitude, to Differential (LVPECL, LVDS, CML, and HCSL) output jitter and Phase noise specifications in BUFFER and ZDB Modes. Added Conditions: Input slew rate 1.8 V/ns 20-80% V_{DD}, to LVCMOS output jitter specification in BUFFER and ZDB Modes.
*B	4467362	AJU	08/06/2014	Changed status from Advance to Preliminary. Updated Ordering Information (Updated part numbers).

Document History Page *(continued)*

Document Title: CY27410, 4-PLL Spread-Spectrum Clock Generator Document Number: 001-89074				
Rev.	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*C	4581405	XHT	12/01/2014	Removed 27430 from the entire document. Page 1: Changed skew parameter from 40 ps to 75 ps. Page 1: Removed duplicate description of SATA,USB, and GbE. Page 3: Added "clock" for IN1 description in Input System, Page 3: Specified IN2 for feedback signal. Page 3: Indicated PLL1 for VCXO functionality. Page 4: Modified Figure 4, Figure 5, and Figure 6. Page 5: Changed description in Clock Generator, "(IN1 or IN2)" to "(IN1) or a Crystal". Page 5: Changed "DIV-R (R1 or R2)" to "DIV-R (R1)". Page 5: Modified Figure 9. Page 6: Corrected description of Early/Late "0 to 4" to "0 to 5". Page 8: Added "Random Write" in Figure 20. Page 9: Modified Figure 21. Page 10: Changed CY27410 Pinout. Page 12: Changed 48-Pin QFN Pinout. Table 3: Added active low for XRES functions. Table 4: Changed ESD-HBM condition from JEDEC-JESD22-A-114F to JS-001-2012. Table 4: Changed ESD-MM condition from JESD22-A115C to JESD22-A115B. Table 4: Added V_{INI2C}: I2C bus input voltage Max 6 V. Table 6: Changed HCSL power supply current per pair from 25 mA to 26.5 mA. Table 6: Changed current consumption per PLL (including DivC) from 23.5 mA to 26.5 mA. Table 6: Added the following description: “This specification is valid when the reference is available and stable at startup”. Table 7: Added "IN1, IN2" for CIN input capacitance description. Table 7: Modified to “Measured at 10MHz, differential” Table 9: LVDS output VPP: changed description from AC pk-pk to AC single-ended pk-pk. Table 9: Added conditions 8 MHz to 325 MHz. Table 9: LVDS output VPP: Added 200 (min)–470 (max) for conditions: 325-700MHz Table 9: Changed I_{OZ} for +/-15 to 20 µA. Table 10: Changed L_{VPECL} output high voltage from V_{DD}-1.025 to V_{DD}-0.880 V to V_{DD}-1.165 to V_{DD}-0.85 Table 10: Changed description of $V_{PP}(L_{VPECL})$ from AC pk-pk to AC single-ended pk-pk, min 600 mV to 450 mV (f_{OUT} 8 to 150 MHz) Table 10: Changed description of $V_{PP}(L_{VPECL})$ from AC pk-pk to AC single-ended pk-pk, min 400 mV to 320 mV (f_{OUT} 150 MHz to 700 MHz) Table 10 and Table 11: Changed V_{DD} to V_{DDIO} Table 11: V_{PP}(CML): Changed description from AC pk-pk to AC Single-ended pk-pk Table 11: V_{PP}(CML): Changed description from AC pk-pk to AC single-ended pk-pk Table 11: V_{PP}(CML): Changed V_{PP} from 250 mV to 200 mV in f_{OUT}>150-MHz condition Table 12: Removed 0.7 V from Table 12 caption. Table 15: Changed loading condition for LVCMOS output, 15 pF <100MHz, 7.5 pF <200 MHz Table 15: Changed output to output skew: LVCMOS from 50 ps to 100 ps. Table 15: Changed parameter names form $T_{RF18,25,33}$ to T_{RFCMOS}, and max parameters are 2 ns < 100 MHz, 1.5 ns < 200 MHz and 1.2 ns < 250 MHz Table 15: LVCMOS t_{CCJ} and t_{PJ}: added condition: "Configuration dependent" Table 15: Added description for tSK, in a bank, derived from the same PLL.

Document History Page *(continued)*

Document Title: CY27410, 4-PLL Spread-Spectrum Clock Generator Document Number: 001-89074				
Rev.	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*C (contd.)	4581405	XHT	12/01/2014	Table 16: Changed PECL output rise/fall time from 300 ps to 450 ps. Table 16: Changed CML output rise/fall time from 250 ps to 450 ps. Table 16: Changed LVDS output rise/fall time from 350 ps to 450 ps. Table 16: Changed output skew between differential outputs from 40 ps to 75 ps. Table 16: t_{CCJ}, t_{PJ}: Added condition "All differential outputs on". Table 16: t_{CCJ}, t_{PJ}: Changed Max from 30 ps to 50 ps. Table 16: t_{CCJ} in SSC mode: Changed Max from 50 ps to 70 ps. Table 16: Added description for tSK1: derived from the same PLL. Table 17: HCSL $T_{CCJITTER}$: Added condition of "All differential outputs on" and changed Max from 30 ps to 50 ps. Table 20: t_{FS}: Changed conditions for all outputs and changed DIVO max value from 1000 µs to 500 µs Table 22: Updated memory programming and XRES specifications. Table 22: Added t_{XRES} minimum low time 10 µs. Table 22: Added T_{PROG} programming temperature 5 to 55 °C. Table 22: Added C_{INADC} Input capacitance for V_{IN} pin. Table 3: Added "Feedback input for ZDB mode" in IN2P and IN2N Function. Table 15: Added condition t_{DC}: f_{OUT} > 200 MHz, V_{DDIO} = 2.5 V or 3.3 V. f_{OUT} > 100 MHz, V_{DDIO} = 1.8 V. Table 15: Added condition t_{DC}: f_{OUT}≤200 MHz, V_{DDIO} = 2.5 V or 3.3 V. f_{OUT} ≤ 100 MHz, V_{DDIO} = 1.8 V.
*D	4665617	XHT	2/19/2015	Updated Functional Description: Updated Input System: Updated Figure 3: Changed input series capacitance value from 100 nF to 100 pF. Updated Electrical Specifications: Updated Absolute Maximum Ratings: Added θ_{JA} parameter and its details. Updated DC Chip-Level Specifications: Updated Table 7: Removed “Output Pull-down resistance” parameter and its details. Updated AC Output Specifications: Updated Table 16: Added Note 1 and referred the same note in Table 16. Updated Table 17: Added Note 2, 3 and referred the same note in Table 17. Updated details in “Condition” column of t_{RMS_ADD} parameter in Buffer mode. Updated details in “Description” and “Condition” columns of J_{RMS} parameter in ZDB mode. Updated details in “Description” and “Condition” columns of J_{RMS} parameter in CLKGEN Mode. Updated Packaging Information: Removed Note “$T_J = T_A$ + Power × θ_{JA}.” Removed Note “To achieve the thermal impedance specified for the QFN package, the center thermal pad must be soldered to the PCB ground plane.” Updated Ordering Information: Updated part numbers. Changed part number suffix from FLXIT to FLTXIT.

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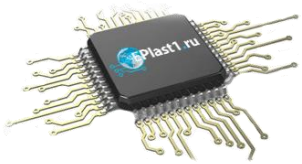
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

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